5.4 MC34161, MC33161 SPICE MODELING

5.4.1 Scope

The purpose of this analysis is to model MC34161, MC33161 Universal Voltage Monitors

Analysis:	**Universal Voltage Monitor modeling**
Performed by:	
Last Rev Date:	**September 14, 2006**
Publication Number:	**MC34161/D**
Revision	**April, 2001-Rev.4**
SPICE File	**MC33161\test1.cir**

5.4.2 Functional Description

The MC34161, MC33161 Universal Voltage Monitors are used as signal conditional. The device has two inputs and outputs. The two output channels can be programmed, from a mode select input (pin 7), as both non-inverting or inverting, or output 1 is non inverting and output 2 is inverting.

5.4.3 Assumptions

1. The temperature for this model is 25 degrees centigrade.
2. Under voltage lockout circuit for the output drivers are not shown in figure1 block diagram of the Publication Order Number MC34161/D; therefore, the circuits were not included in the model. The model is valid for VCC greater than 4.5V.
3. No propagation delays in the model.
4. No Comparator input bias current in the model.

5.4.4 Methods of modeling

IsSpice4 was used to model the device. The model Spice net list is as follows:

```
*SYM=MC33161
.SUBCKT MC33161 23   5   24  7   22   15   1    3
*               VREF IN1 IN2 GND OUT2 OUT1 MODE VCC
.MODEL COMP SW (VT=1.27 VH=0.025 RON=1K ROFF=10MEG)
.MODEL DMOD D (IS=1E-16)
.MODEL QN1 NPN (BF=200 RC=8.5)
.MODEL QN2 NPN (BF=500)
.MODEL M1 NMOS VTO=2.3 KP=100
Bicc 3 7 i=v(3) > 1.6 ? 380u : 0
R1 2 3 1MEG
BCOND 4 7 V=V(2) > 2.5 ? 5 : 0
R3 9 7 250K
V3 11 10 2
R4 10 6 12K
I1 6 7 24U
D2 7 6 DMOD
```

D5 1 9 DMOD

D6 9 11 DMOD

BCOMP1 12 7 V=2.8 < V(1) ? 5 : 0 ; It was 2.8 > V(1)

BXOR1 13 7 V=ABS(V(12,4)) < 2.5 ? 5 : 0

R5 26 13 44K

Q1 15 26 7 QN1

S2 17 7 24 7 COMP

R8 17 3 1MEG

B2 16 7 V=V(17) > 2.5 ? 5 : 0

BCOM2B 20 7 V=0.6 < V(1) ? 5 : 0 ; It was 0.6 > V(1)

BXOR2 19 7 V=ABS(V(20,16)) < 2.5 ? 5 : 0

R9 18 19 44K

Q3 22 18 7 QN1

Q4 3 21 25 QN2

R12 3 21 250K

R13 25 23 0.3

R15 23 27 10K

R16 27 7 100K

M1 21 27 7 7 M1

S1 2 7 5 7 COMP

.ENDS

The model was simulated and the results were correlated to the actual data points. The Spice test circuit for mode select Vref is shown in figure 5.4.1, and the Spice net List is shown in figure 5.4.2. In addition, the model Comparator Input threshold Voltage, Output Saturation voltage, and Supply Current in figures 5.4.6 to 5.4.9 were compared to the published electrical characteristic data.

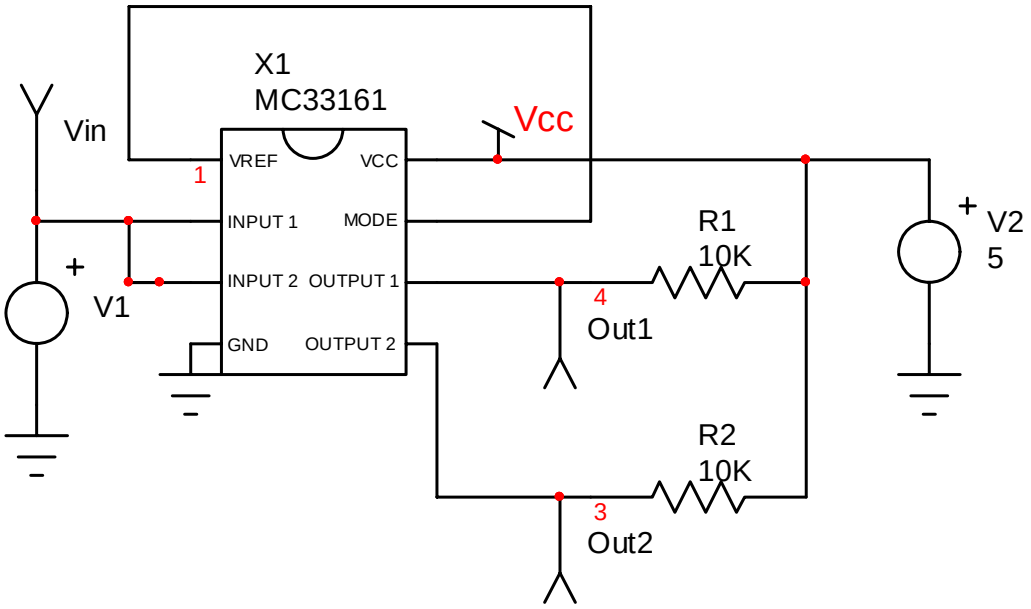

Figure 5.4.1. Spice test circuit for mode-select (Vref). For mode-select Vcc and ground, the mode pin should be connected to Vcc pin or ground respectively.

Figure 5.4.2. SPICE test fixture Net List

```
*INCLUDE ON.LIB
.TRAN 1M 4 0 0.1
.OP
.DC V2 4.5 40 0.5
*ALIAS  V(4)=OUT1
*ALIAS  V(3)=OUT2
.PRINT DC  V(1)
.PRINT TRAN  V(4)  V(3)  V(6)
V1 6 0 PULSE 0 5 100U 1M 1M 1 2
V2 2 0 5
R1 4 2 10MEG
R2 3 2 10MEG
H1 1 0 V2 -1
X1 5 6 6 0 3 4 2 2 MC33161
.END
```

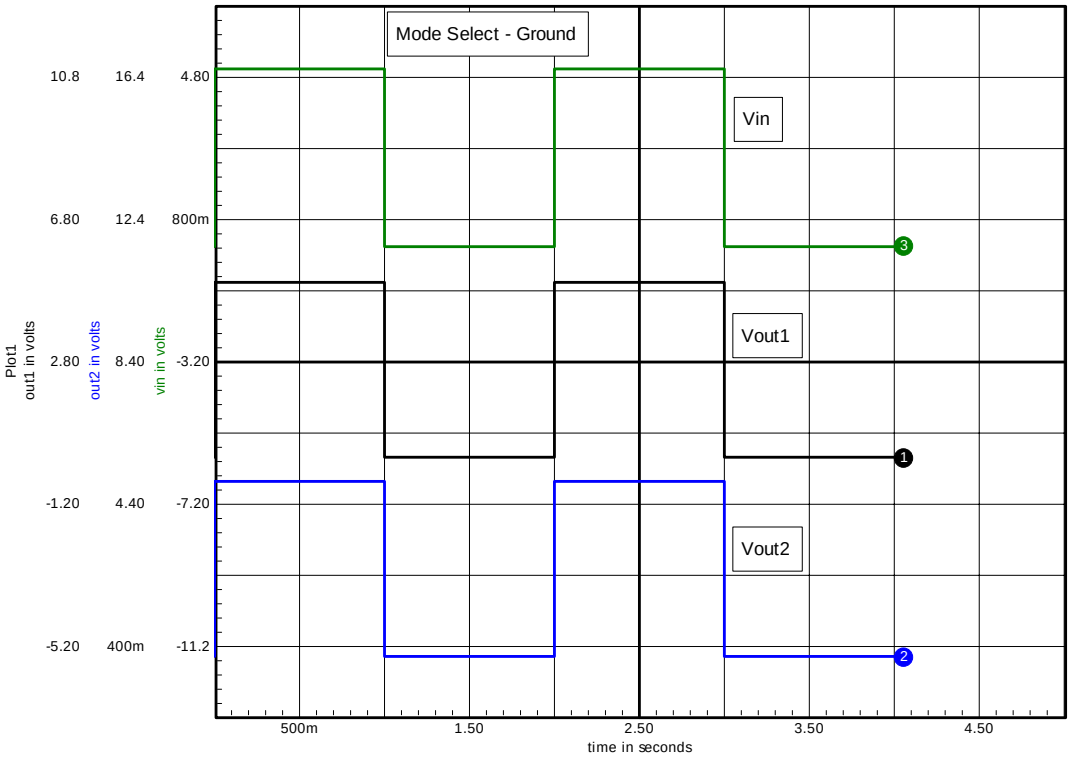

Figure 5.4.3. SPICE Waveforms of mode-select ground configuration

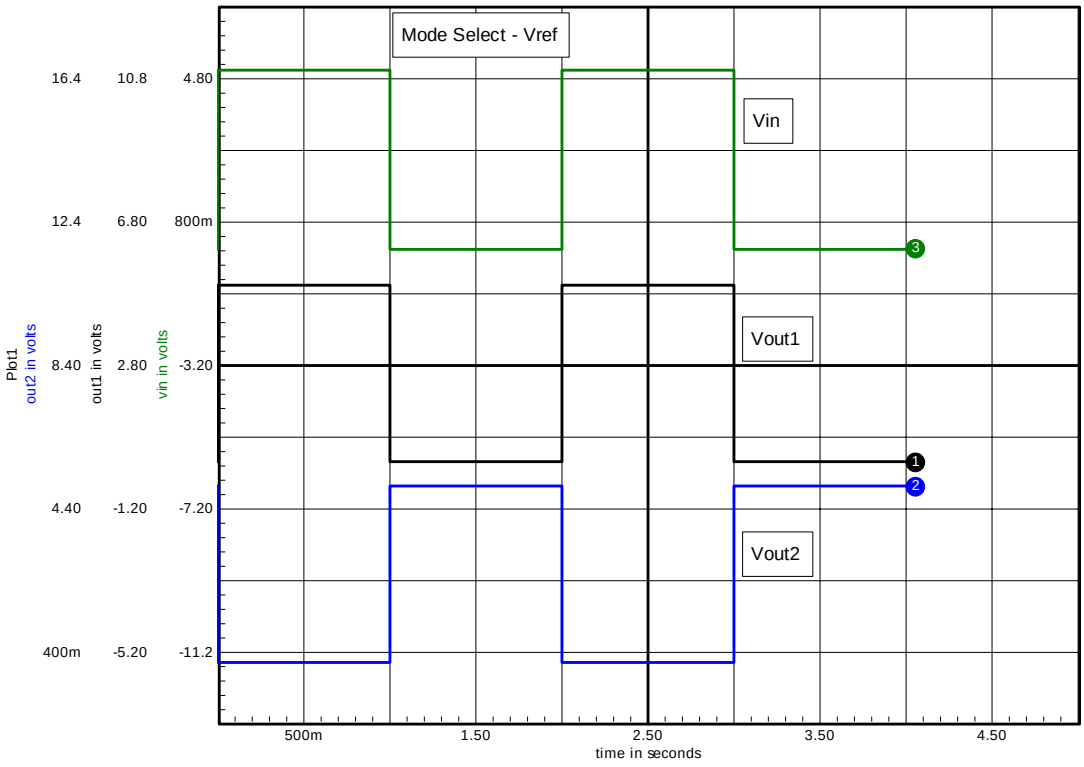

Figure 5.4.4 SPICE Waveforms of mode-select Vref configuration

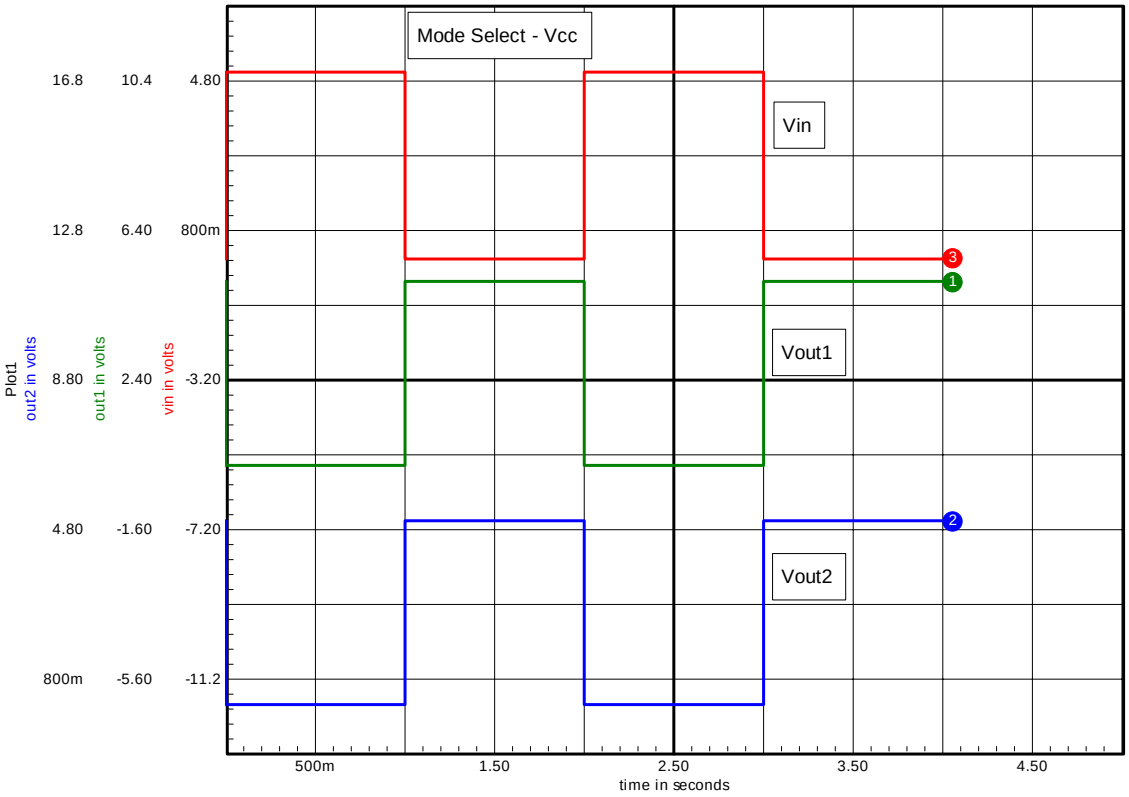

Figure 5.4.5. SPICE Waveforms of mode-select Vcc configuration

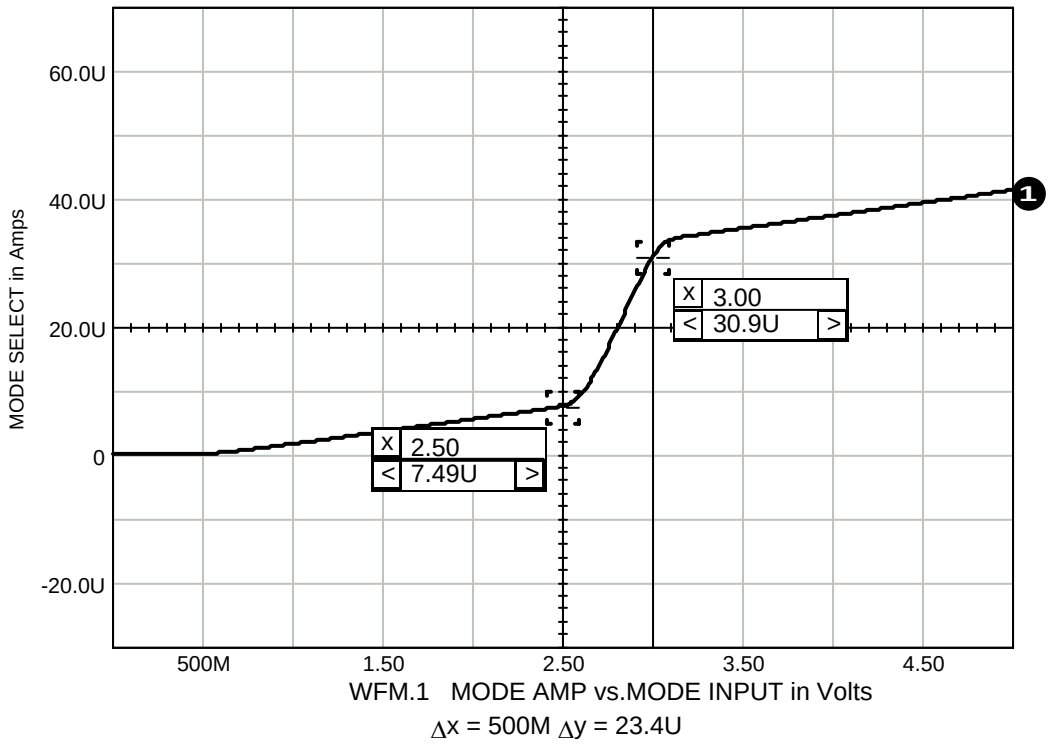

Figure 5.4.6 SPICE Waveform of mode select input current Vs Voltage

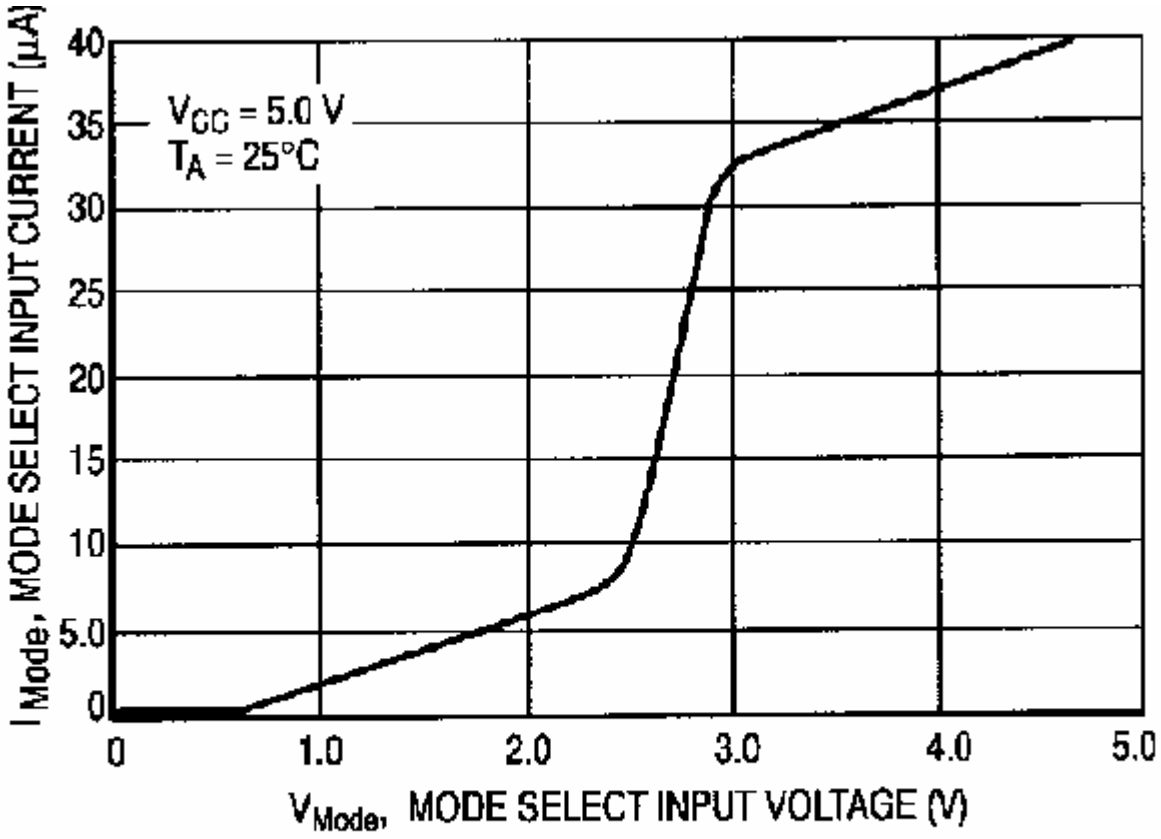

Figure 7. Mode Select Input Current versus Input Voltage

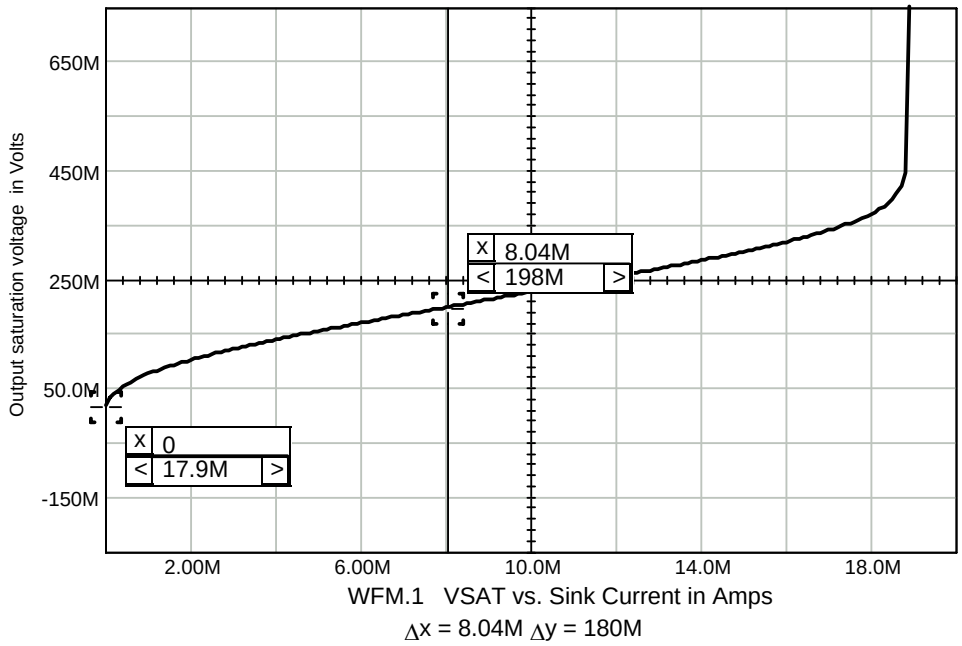

Figure 5.4.7 SPICE Waveform of output saturation voltage Vs Sink Current

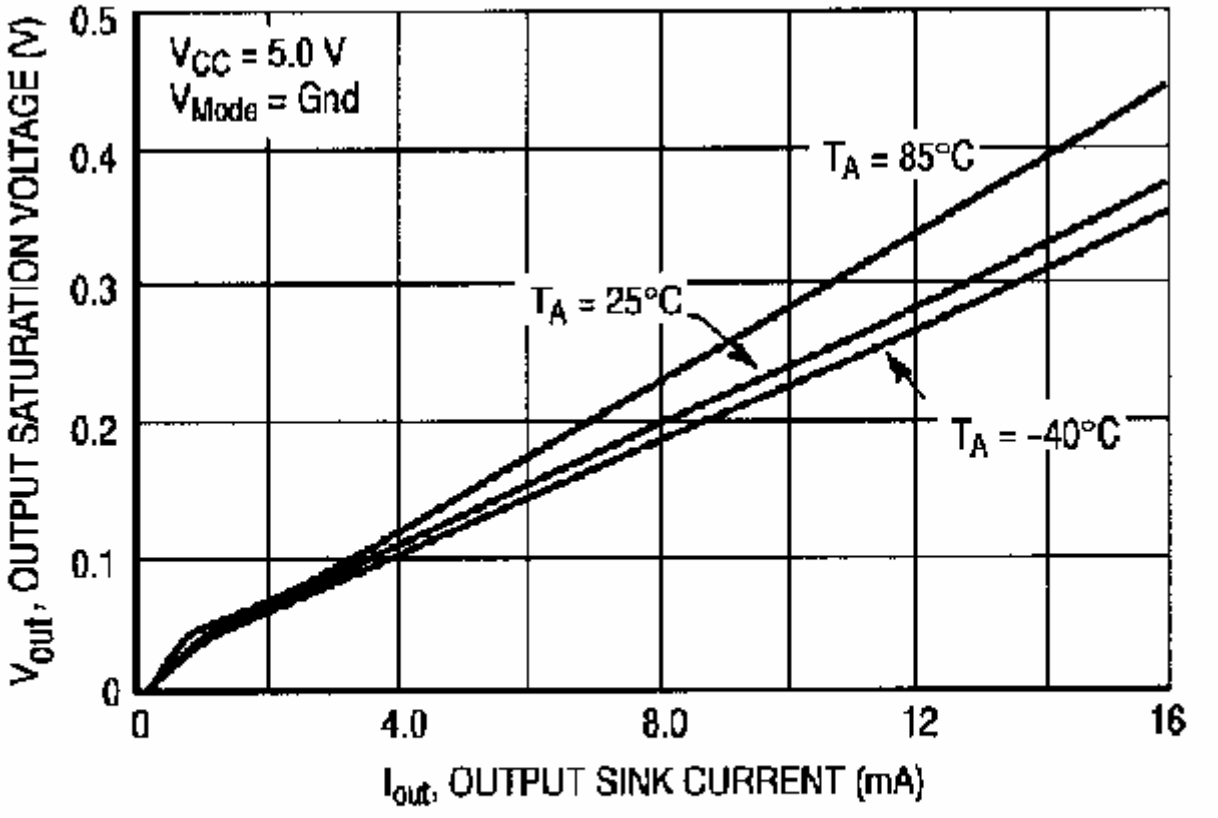

Figure 11. Output Saturation Voltage versus Output Sink Current

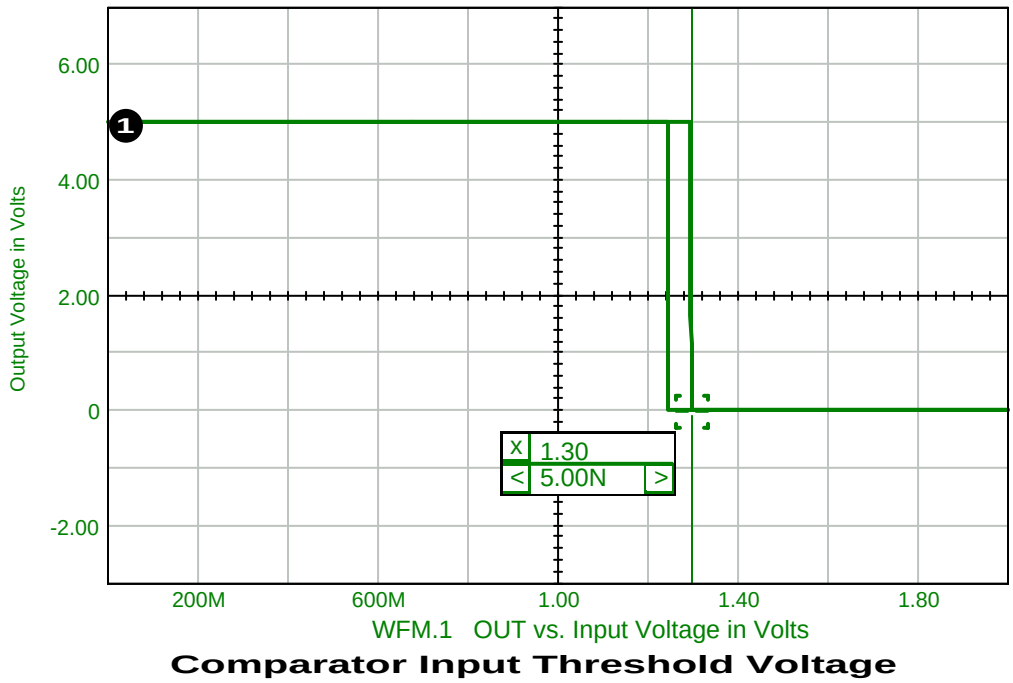

Figure 5.4.8 SPICE Waveform of input 1 voltage Vs Output 1 Voltage

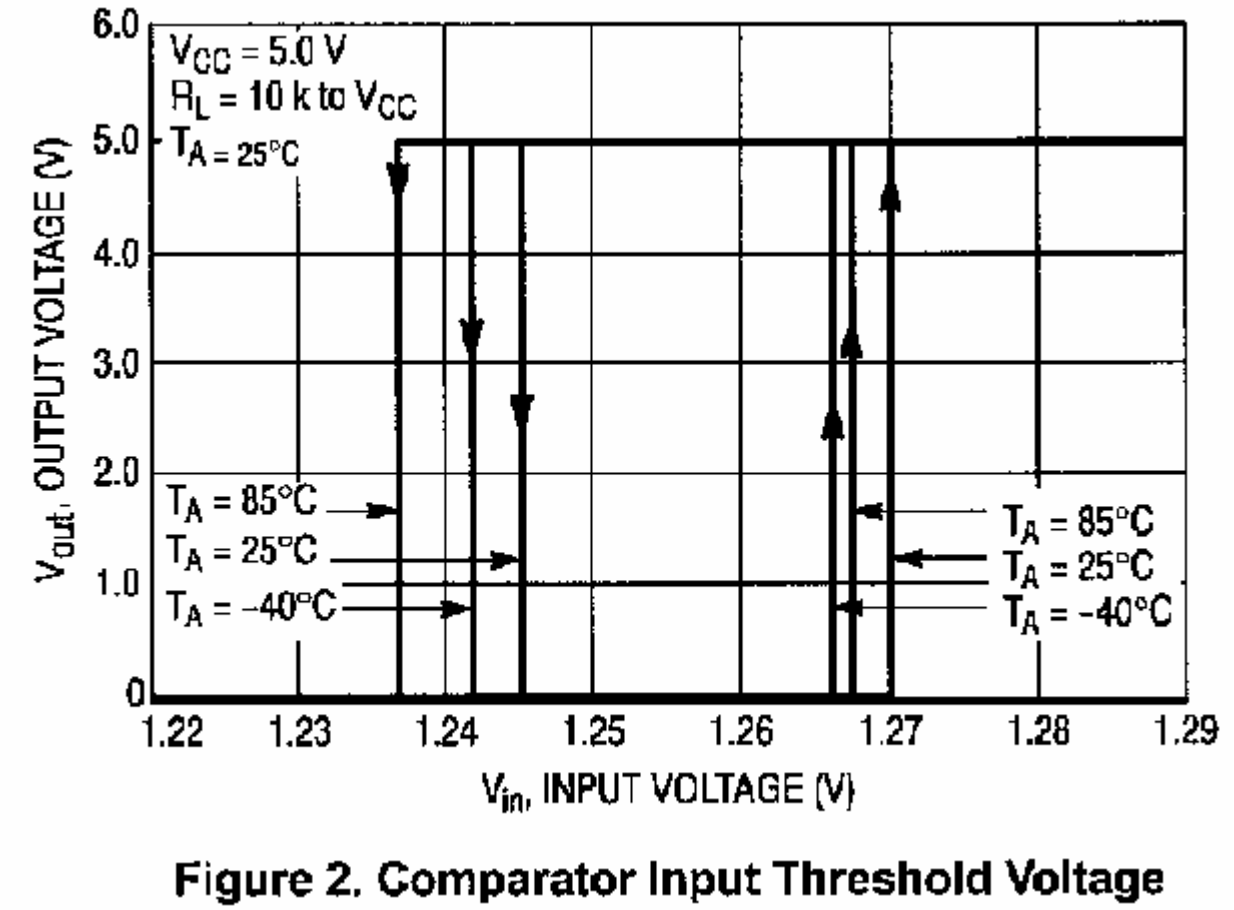

Figure 2. Comparator Input Threshold Voltage

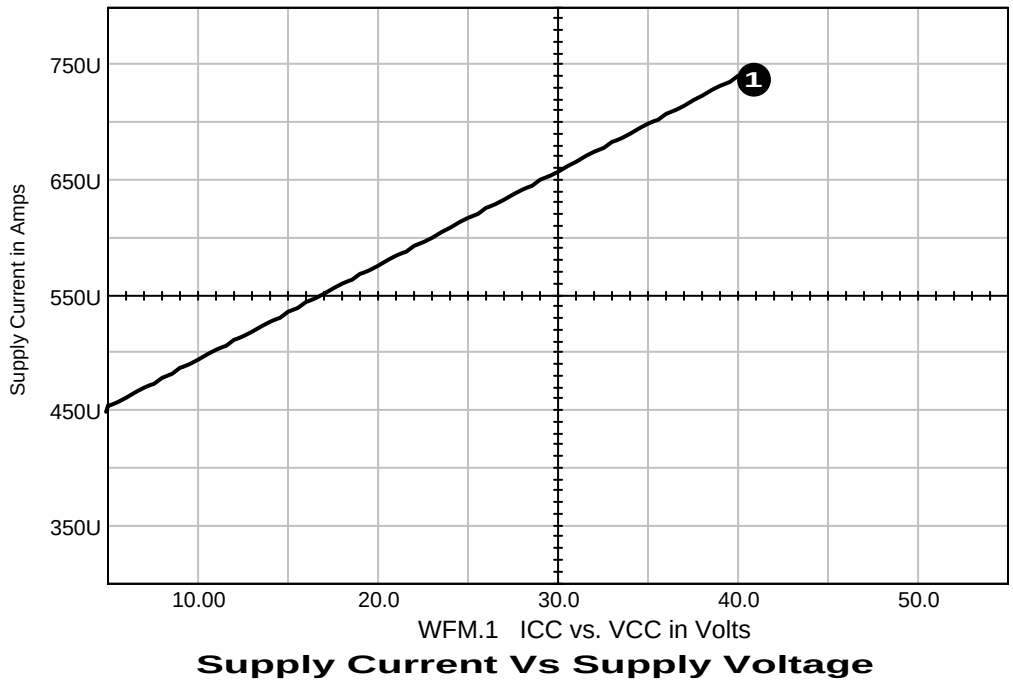

Figure 5.4.9 SPICE Waveform of supply current Vs Voltage

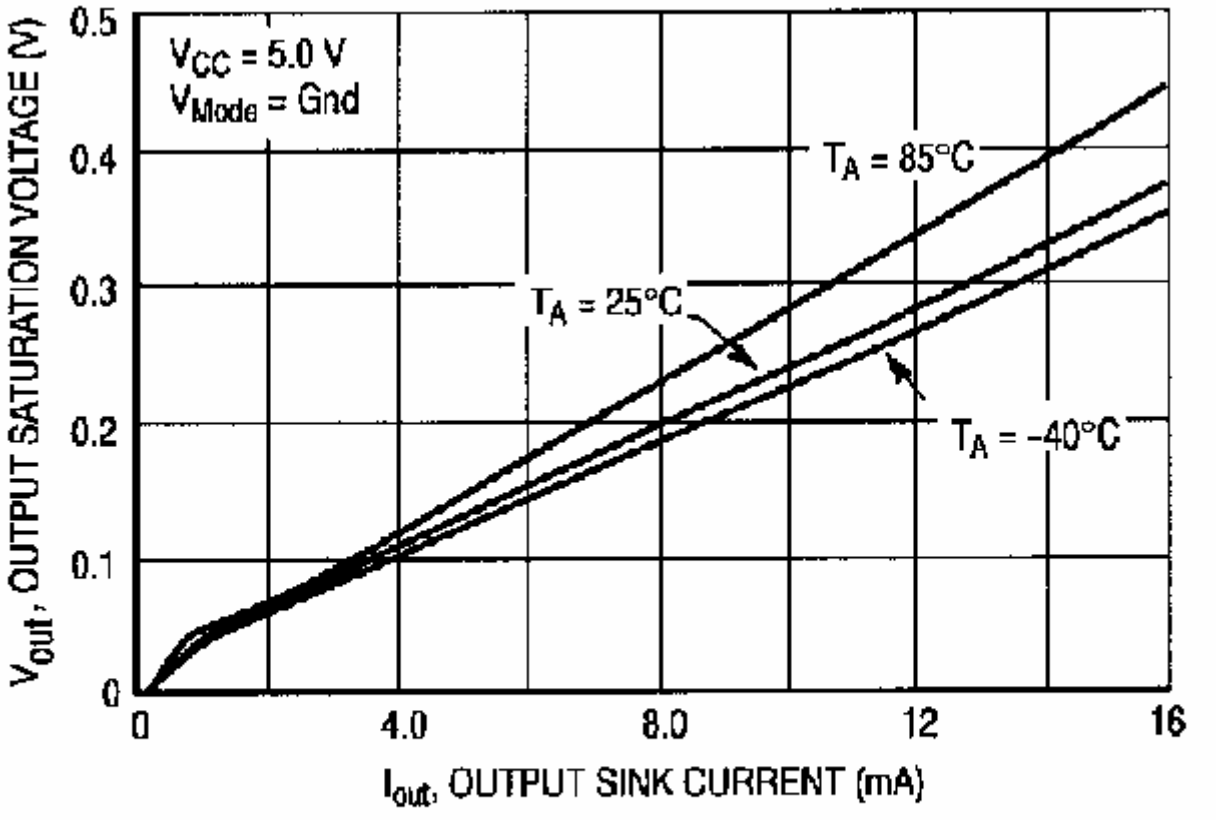

Figure 11. Output Saturation Voltage versus Output Sink Current

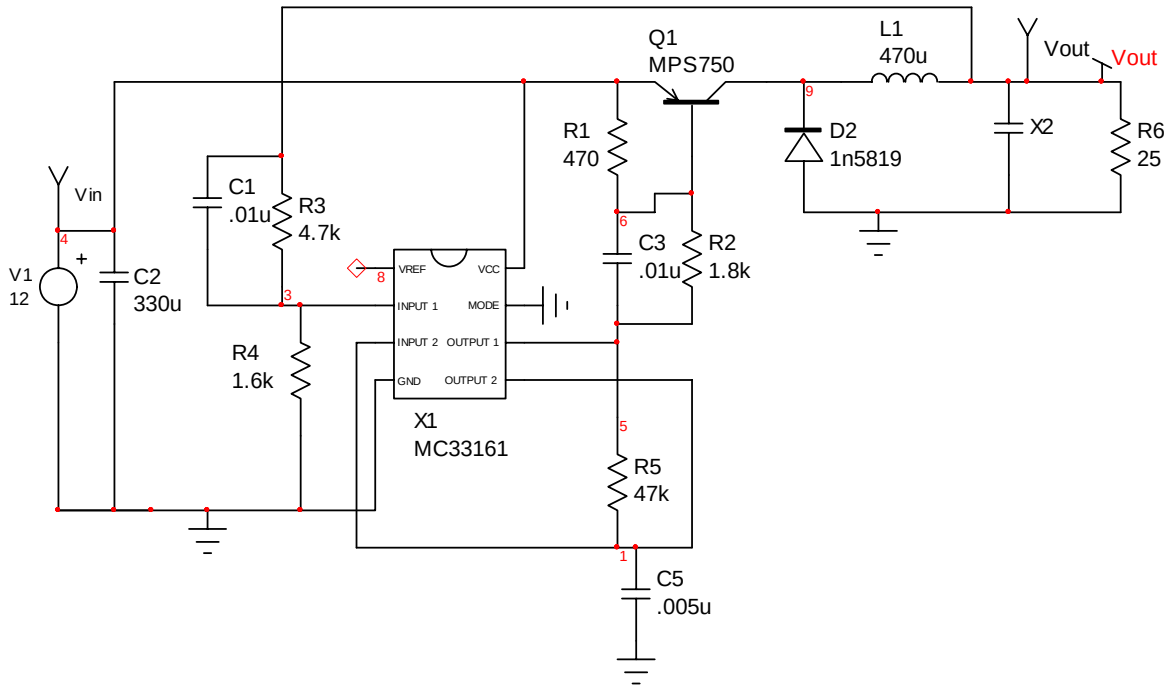

Figure 5.4.10 5V regulated output application circuit using MC33161.

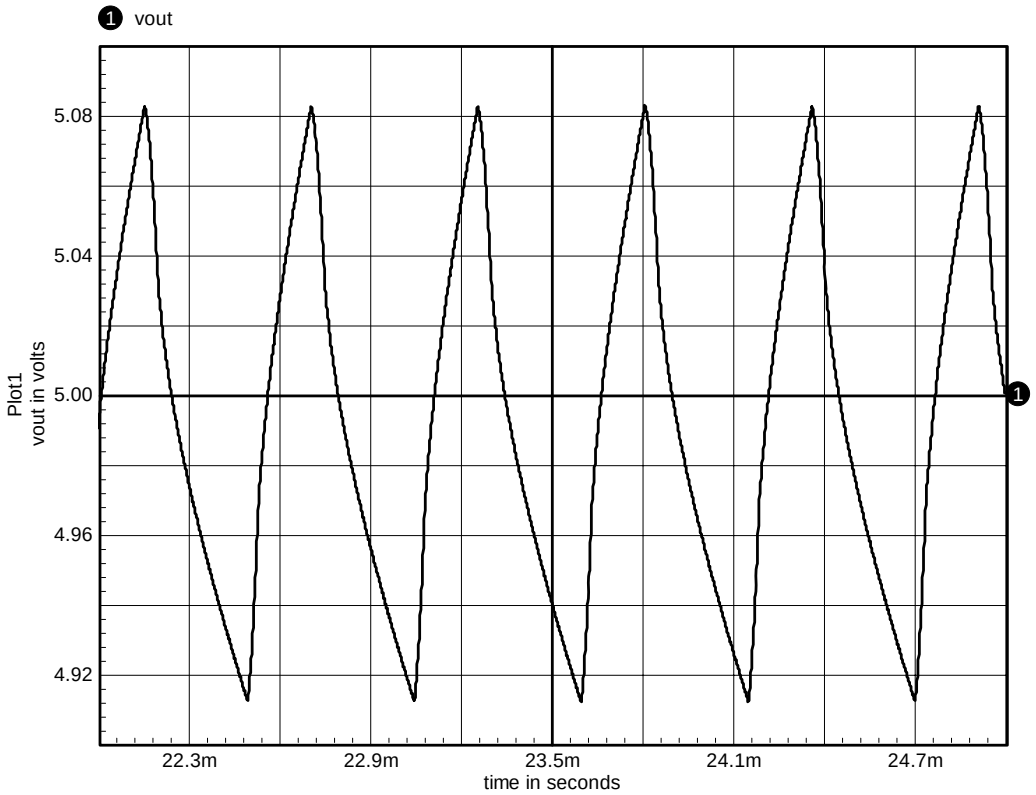

Figure 5.4.11 Simulation voltage output response.

5.4.5 Conclusions and Recommendations

The Spice simulation result of the reference output voltage was 2.532Vdc, and the short circuit current was 8.33mA. Figure 5.4.3 to 5.4.5 are in agreement with the device truth table configurations and all the simulation results are within the electrical characteristic specifications.