NCN26010XMNEVB 10Base-T1S MACPHY Evaluation Board User's Manual

EVBUM2832/D

Figure 1. Evaluation Board Photograph (Revision 1)

Figure 2. Evaluation Board Photograph (Revision 2)

Introduction

NCN26010XMNEVB is a printed circuit board (PCB) designed to allow customers to evaluate **onsemi**'s NCN26010 SPI-enabled 10Base-T1S transceiver. The NCN26010 integrates both the physical-layer transceiver (PHY) and media access controller (MAC) into a "MACPHY" device.

Features

The NCN26010XMNEVB evaluation board (EVB) includes all circuitry to act as a 10Base-T1S node, when connected to a host computer / MCU via SPI.

The evaluation board has two RJ45 connectors that allow attaching a twisted single pair data cable. For ease of use, standard CAT 5 Ethernet cables can be connected to the RJ45 connectors. Note that only one pair (connected to pin 1 and 2) of the RJ45 connector is used. Alternatively, terminal blocks or pin headers may be used.

The serial peripheral interface (SPI) of the NCN26010 is routed to a PMOD connector on the evaluation board, allowing the connection to micro-controller demonstration and evaluation boards of various vendors. One example of such a board is **onsemi**'s RSL10 BDK-GEVK.

When pairing the NCN26010XMNEVB with the NCN26010BMNEVB bridge board, users can connect the eval board to a Raspberry Pi single board computer (SBC). For details on how this is done, please refer to the NCN26010XMNEVK eval kit users guide.

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To allow monitoring of the SPI traffic, the EVB features a 0.1" pitch pin header that is easily accessible. This header could also be used to connect a logic analyser, allowing tracing of the SPI signals while in full operation together with a Raspberry Pi (not supplied) or any other suitable host micro-controller or SBC. Users can also use this connector for connecting to host PCBs (3rd party MCU evaluation boards) that do not offer a PMOD connector.

The evaluation board was revised in 2024. Refer to section "Revision information" for detailed information.

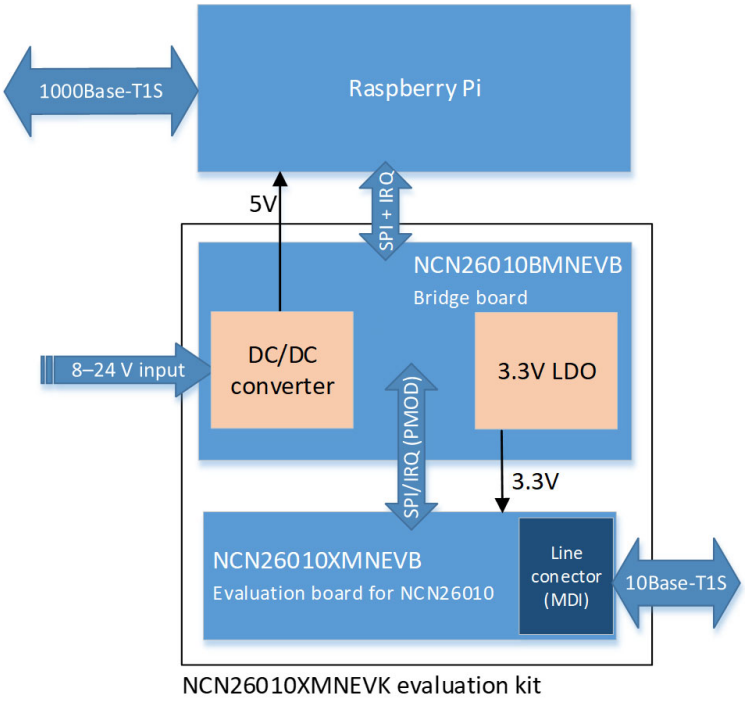

Figure 3. Simplified Block Diagram of the Complete Evaluation Kit

APPLICATION INFORMATION

To act as a communication node, the evaluation board needs a host computer to perform any network communication. The NCN26010XMNEVB performs the functions of a MAC (media access controller) and a PHY (physical layer) device.

The upper layer protocols need to be provided by software running on the host. The host will also have to handle the SPI communication between the MACPHY and the host, since the MACPHY operates as an SPI slave device.

In addition, the MACPHY provides an IRQn signal that signals data is available and other events that need to be handled by the host.

Connectors and Jumper Locations

The top view of the EVB is shown in Figure 4 (revision 1) and Figure 5 (revision 2):

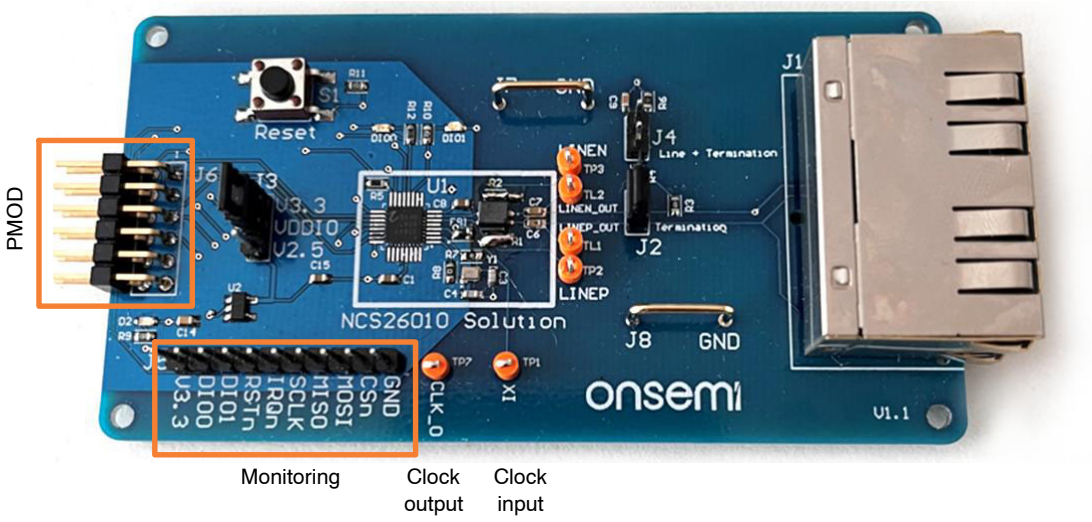

Figure 4. Evaluation Board, Revision 1

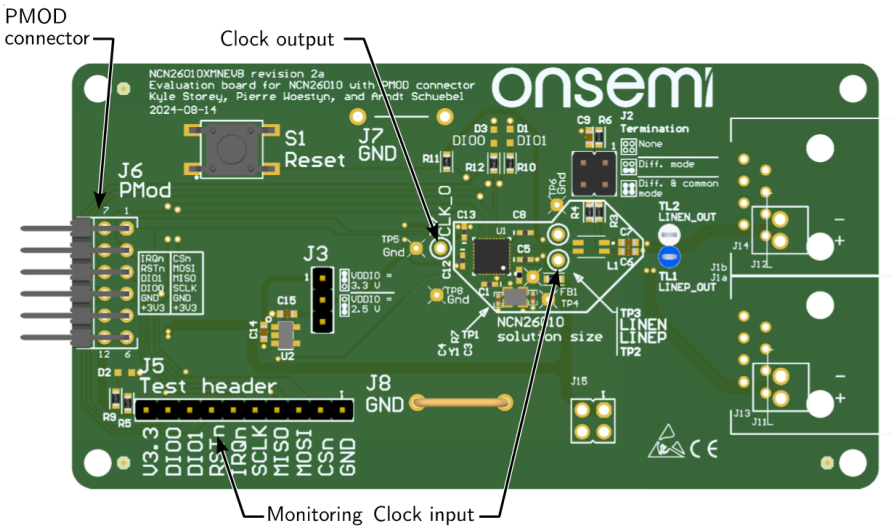

Figure 5. Evaluation Board, Revision 2

Power Supply, Test Points and Connectors

NCN26010XMNEVB needs a single 3.3 V power supply that can provide a peak current of at least 100 mA. Note that at full operation the board draws approximately 45 mA of current but has an inrush current of up to 100 mA at power on.

Power can be fed through the PMOD connector J6 or the edge connector J5.

Table 1 lists all connectors and test points on the NCN26010XMNEVB evaluation board.

Table 1. CONNECTORS AND JUMPERS

Name on Board	Function	Comment
J1 (revision 1 boards)	Single-pair Ethernet, dual RJ45	These connectors are used to connect standard Cat5 ethernet cables. Only the twisted pair connecting to pins 1 and 2 of the RJ45 connectors is used. Users can crimp their own cables by utilizing pins 1 and 2 of the RJ45 connectors. The two sockets are electrically connected to connecting multiple NCN26010 boards to build a larger network. Refer to “SPE connectors”.
J1a, J1b (revision 2 boards)	Single-pair Ethernet, alternative 1: Single RJ45	As J1, with separate connectors.
J2	Jumper to set termination	Refer to “Termination”.
J3	Digital IO voltage selection	Use this jumper to select between a 3.3 V and 2.5 V VDDIO voltage. The eval board has a 2.5 V Voltage regulator to allow interfacing with MCUs that use 2.5 V IOs; set the jumper accordingly. Note that in any case, the Eval boards power supply will have to be 3.3 V.
J4	Jumper to set Opt-BIN termination	Refer to “Termination”.
J5	SPI and IRQ debug/Monitoring	This port can be used to connect a logic analyzer, allowing to monitor the OA−Protocol on the SPI interface. It can also be used to interface to MCU boards that do not have a PMOD connector. The board can also be powered though this port. **When connecting the board via the PMOD (J6) connector, do not use J5 to power the board.** The pinout of J5 is detailed on the eval board.
J6	PMOD connector	This is the primary connector allowing to power the Eval board and bring the SPI, DIO and IRQ signals to a host MCU. The pinout mostly follows the Digilent PMOD interface Type 2A
J7, J8	GND	Ground connection bar. Allows easy ground connection for oscillo-scope probes or similar.
J11, J12 (revision 2 boards)	Single-pair Ethernet, alternative 2: 2.54 mm headers	Alternative to J1. Populate with TE 5-103634-1 or comparable.
J13, J14 (revision 2 boards)	Single-pair Ethernet, alternative 3: 2.54 mm terminal blocks	Alternative to J1. Populate with Würth 691210910002 or comparable.

Besides connectors and jumpers, the board features several test points that allow monitoring of various signals. Refer to Table 2.

Table 2. TEST POINTS

Name on Board	Function	Comments
TP1	Clock input.	In case the board should be clocked by an external clock, TP1 can be used to inject a 25 MHz LVCMOS external clock signal. For this to work, the on−board crystal circuit needs to be disconnected from the NCN26010 device. This is done by removing the 0 Ω resistor R7.
TP2, TP3	LineP and LineN Test Points	TP2 and TP3 can be used to monitor the 10BASE-T1S signal at the NCN26010 pins (behind the decoupling network). **onsemi** recommends the use of a differential probe with low capacitance, when monitoring the LINEN/P differential 10BASE−T1S signals
TL1, TL2	MDI L+ and L− Test Point (LINEP/N_OUT)	Same as TP2 and T3, these test points can be used to monitor the activity on the SPE Ethernet line (or cable). In contrast to TP2 and TP3, TL1 and TL2 are test points that allow monitoring the SPE signal before the AC coupling capacitors and the common mode choke (at the MDI)
TP7	Clock output	This test pin can be used to monitor the 25MHz system clock of the device. See datasheet for details on how to enable or disable this output.

Connector Pinouts

PMOD connector J6

The PMOD connector J6 is used to connect the eval board to the host CPU. Its pinout follows the Digilent recommendations for an SPI PMOD 2A connector pinout. Figure 6 shows the numbering scheme when looking directly at the connector from the left edge of the board.

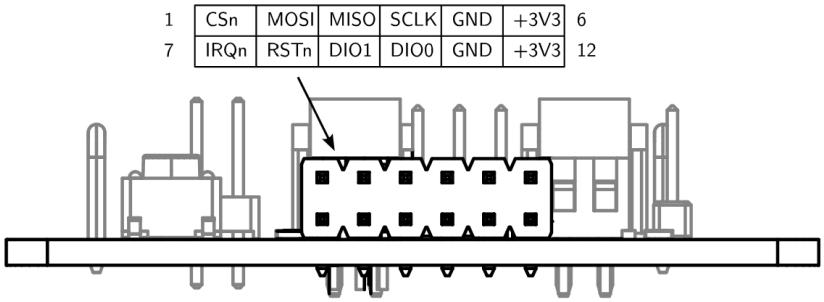

Figure 6. J6 PMOD Connector Pinout

Refer to Table 3 for the pin-out and pin description of the J6 PMOD connector.

Table 3. J6 PMOD CONNECTOR PINOUT

Pin	Signal	Comment
1	CSn	SPI active-low chip select. Driven by the host, input to the eval board. This pin is used to select the device for an SPI transaction. When low, the NCN26010 will accept SPI data from the host.
2	MOSI	Master Out Slave In Output from the host micro-controller, input to NCN26010. MOSI is part of the SPI interface.
3	MISO	Master In Slave Out Input to the host, output from NCN26010. MISO is part of the SPI interface.

Table 3. J6 PMOD CONNECTOR PINOUT

Pin	Signal	Comment
4	SCK	SPI clock, driven by host. The SPI clock needs to be in the range between 15—25 MHz to comply with the requirements of the Open Alliance specification.
5	GND	Ground connection
6	VDD	3.3 V power supply. Used to power the Evaluation Board.
7	IRQn	Interrupt request signal, driven by NCN26010. Output from NCN26010, input to the host computer / MCU. Used by NCN26010 to signal that data was received and other events.
8	RSTn	To reset the device, this pin needs to be driven low by the host. As this pin is an open drain bidirectional pin on NCN26010, it should never be driven to VDD to prevent damage to both the host and the NCN26010. The board provides a 3.3 kΩ pull-up resistor on this pin.
9	DIO1	Digital GPIO from NCN26010, see datasheet for details.
10	DIO0	Digital GPIO from NCN26010, see datasheet for details.
11	GND	Ground connection
12	VDD	3.3 V power supply for the evaluation board.

Side connector J5

The side connector J5 can be used to monitor the SPI traffic as well as the DIO0/1 and IRQn pins of NCN26010.

As it provides all necessary pins to connect the NCN26010XMNEVB to a host MCU, it can also be used instead of the PMOD (J6) connector for 3rd party SBC or MCU boards that do not offer a PMOD port.

The pinout of the J5 connector is shown in Table 4. For a brief functional description please consult Table 3.

Table 4. J5 SIDE CONNECTOR PINOUT

Pin number	Function
1	GND
2	CSn
3	MOSI
4	MISO
5	SCK
6	IRQn
7	RSTn
8	DIO1
9	DIO0
10	3.3V VDD

SPE Connectors

The evaluation provides two SPE connection points, allowing it to be used as an end node or as a multi-drop node (see however “Termination” for end nodes).

Revision-1 boards have a single connector: the dual-port RJ45 connector J1.

To increase flexibility, revision-2 boards are delivered without populated SPE connectors. Instead, they have 3 footprint types allowing the user to select the connector best suited for his application:

- J1a and J1b are single RJ45 connectors (Figure 7). These may be populated with Adam Tech MTJ-881X1 or compatible.
- J12 and J13 are terminal blocks with a 2.54 mm pitch (Figure 8). Würth 691210910002 is used by default, but most other blocks with 2.54 mm pitch will fit.
- J12 and J14 are 2.54 mm pitch headers, as designed TE 5-103634-1 (Figure 9). This header is specifically designed to mate with TE 487526-1, but most female 2.54 mm receptacles will fit.

Two terminal blocks and two RJ45 connectors are delivered with each board.

Figure 7. SPE Connector on Revision-2 Boards: Alternative 1, RJ45

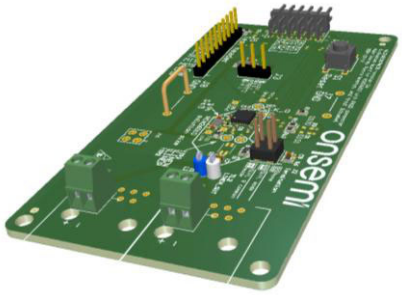

Figure 8. SPE Connector on Revision-2 Boards: Alternative 2, Terminal Blocks

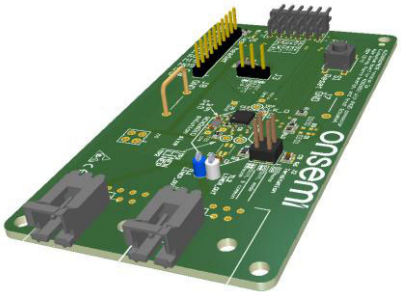

Figure 9. SPE Connector on Revision-2 Boards: Alternative 3, 2.54 mm Pin Headers

Termination

Each end of the bus must have a 100 Ω termination. The termination network on the evaluation board may be used for this. Of course, only the first and last board in a segment should have the termination resistor enabled.

On revision-1 boards, close jumper J2 to terminate the differential mode (i.e. across the MDI wires; see Figure 10). Optionally, close jumper J4 to also add a common-mode termination with a resistor and capacitor. This jumper should only be set when J2 is set.

Note the termination is placed before the capacitors. Do not use the on-board termination in combination with PoDL; use capacitively-coupled off-board termination instead.

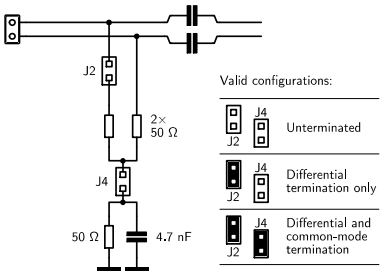

Figure 10. Termination on Revision-1 Boards

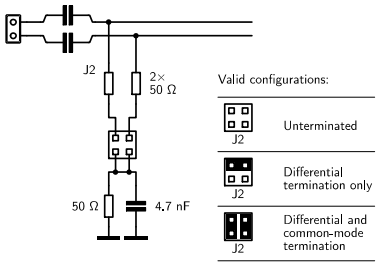

Figure 11. Termination on Revision-2 Boards

On revision-2 boards, the termination network is behind the capacitors and can be safety used together with PoDL (Figure 11). The jumpers are now arranged differently. First, the equivalent of J2 is placed behind the 50 Ω resistor to lower the capacitive loading on the bus. Secondly, a 2x2 pin header is used to allow for complete symmetry. Place the jumpers as indicated in Figure 11 or as shown on the silkscreen (Figure 5).

Using an External Clock

If the NCN26010 must be clocked from an external 25 MHz clock instead of the on-board crystal oscillator, this clock can be feed into the board via the XI (TP1) test point after removing the R7 resistor (Figure 12).

On revision-2 boards, TP1 (XIN) and TP7 (clock-out) were made smaller to reduce electromagnetic emission. When feeding in an external clock, it is recommended to solder twisted wires to these test points and the dedicated ground test points TP4 and TP5, as shown in Figure 13. The wires should be kept as short as possible.

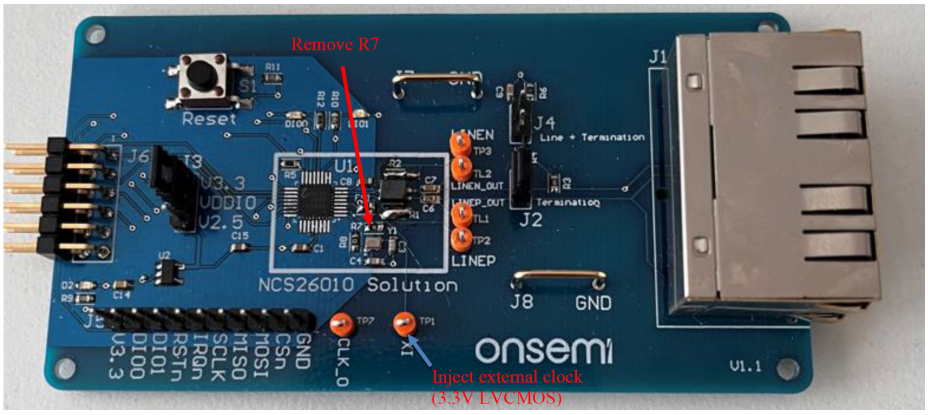

Figure 12. Using an External Clock (Revision-1 Boards)

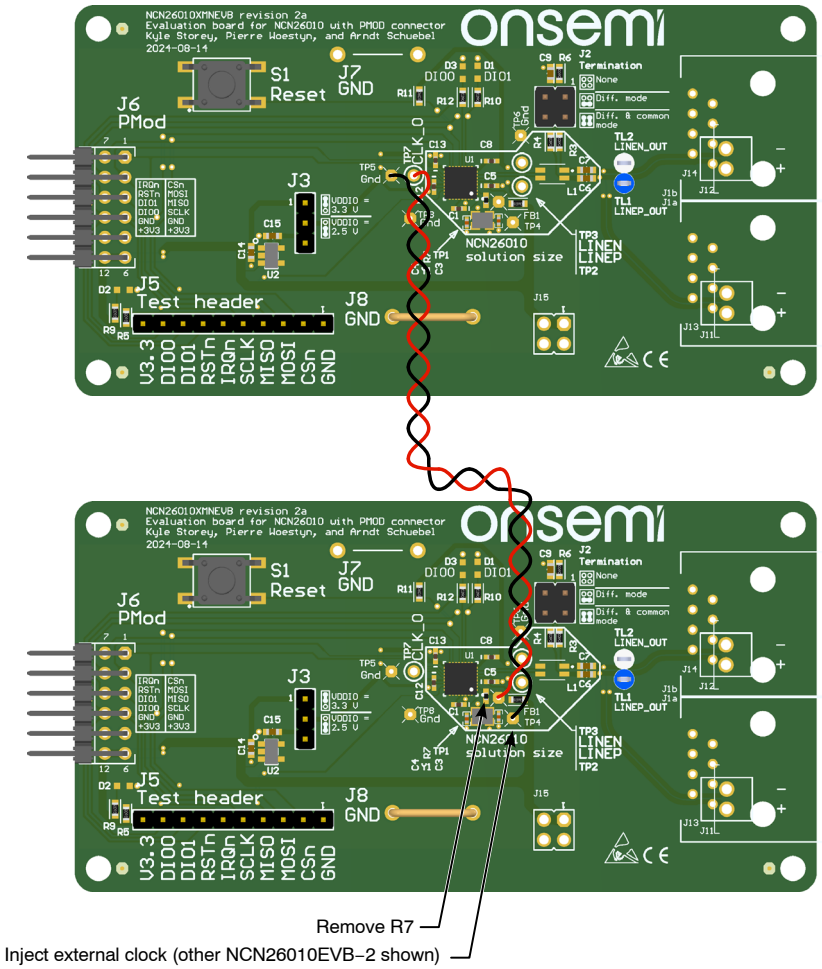

Figure 13. Using an External Clock (Revision-2 Boards)

Bypassing the Common Mode Choke

In some cases, users may wish to test the performance without a common mode choke.

To bypass the common mode choke, two 0 Ω resistors (R1 and R2) need to be populated by the user.

In addition, users can also remove the common mode choke from the boards when R1 and R2 are populated.

DESIGN NOTES

The Ethernet net pairs require careful attention during printed circuit board (PCB) layout.

For intermediate (dropped-off) nodes on a multiple-drop bus, the stub should be kept as short as possible (Figure 14).

The second revision of the evaluation board is significantly better in this regard (Figure 15).

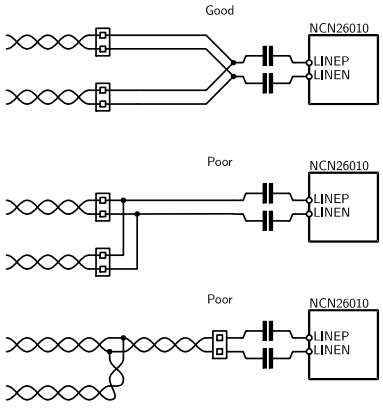

Figure 14. Stubs in Intermediate Nodes should be Kept as Short as Possible

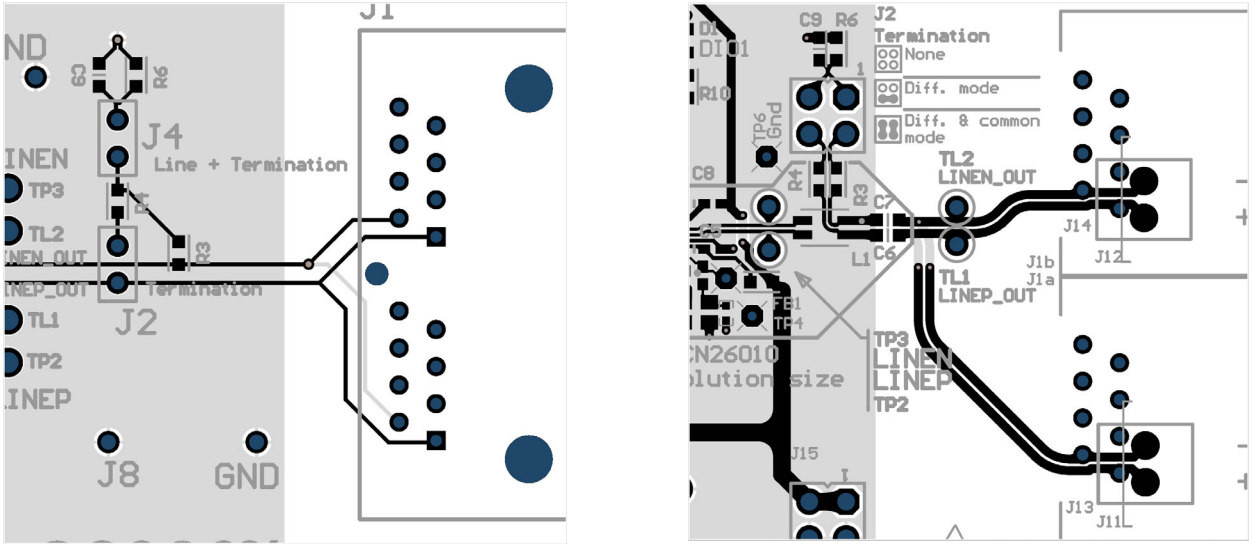

Figure 15. Layout of the SPE Pairs in the First (left) and Second (right) Revision of the EVB

To optimize the signal quality, the wiring and connectors should have a differential impedance of 100 Ω. The same impedance should be used on the board, for end nodes certainly up to the termination (Figure 16). For intermediate nodes, 100 Ω impedance should be maintained until the branch point (Figure 17), For the stub to the transceiver, **onsemi** recommend a slightly higher impedance.

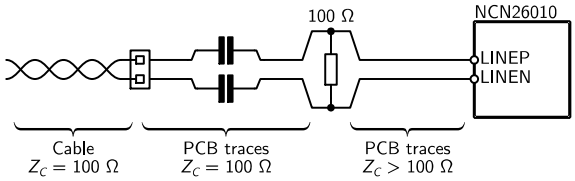

Figure 16. In an End Node, an Impedance of 100 Ω should be Maintained up to Termination

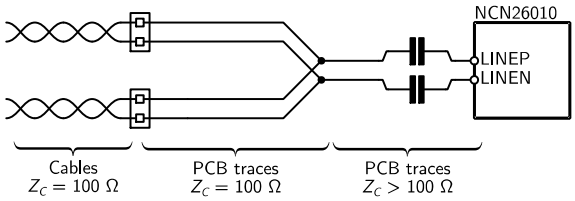

Figure 17. In an Intermediate Node, an Impedance of 100 Ω should be Maintained to the Branch Point

The trace pair may be routed over a ground plane (Figure 18). If unshielded connectors are used, **onsemi** recommend omitting the ground plane until the common-mode choke. This minimizes capacitive common-mode coupling from the bus to the node (Figure 19).

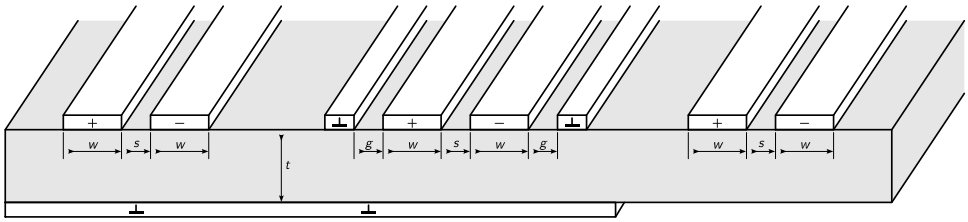

Figure 18. Differential Traces With (left, centre) and Without a Ground Plane (right)

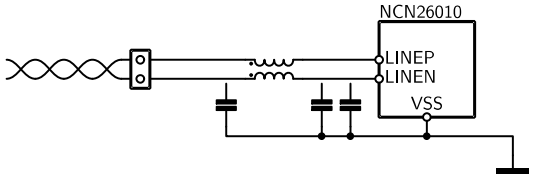

Figure 19. The Ground Plane should be Omitted Until the Common-mode Choke (left) to Avoid Capacitive Coupling (right)

For traces routed over a ground plane (Figure 18), the differential impedance can be calculated using approximative formulas. Refer to [1, 12.2] for more information on a few approximations and their limitations. Software or online calculators must be used with care: very few describe the underlying formula and its applicability. A numerical simulator using the boundary element method (BEM) may be used to verify the geometry. A free BEM simulator may be found in QucsStudio or on-line on the website of Sierra Circuits.

If power over data line (PoDL) is used, the gap is constrained by the DC voltage between the traces: functional isolation requirements will impose a minimum gap. For the evaluation board, the application, and therefore the applicable safety standard and the DC working voltage, is indeterminate. Strictly speaking, IEEE 802.3cg does not standardize PoDL for 10Base-T1S; we may however refer to 10Base-T1L. For illustration only, the design is based on the maximum allowed DC voltage of 10Base-T1L: 58 V [2, 104.3]. Again for illustration only, the design used IEC 60950, where table 2G shows that functional insulation is sufficient regardless of the circuit class of the SPE pairs. Assuming pollution degree 1, a clearance and creepage distance of 0.2 mm is required (table 2K). This is higher than the 150 μm typically allowed by PCB manufacturers, but choosing this minimum value this is often not beneficial, as it increases the effect of manufacturing tolerances.

For the evaluation board, the board thickness h is 1.55 mm; the end copper thickness t is 35 µm. The typical relative permittivity is $\varepsilon_R = 4.6$.

With these values, the trace width w should be about 0.55 mm without close coplanar ground traces (Figure 18, left) or 0.35 mm with those traces (Figure 18, centre; $g = s = 0.20$ mm).

For the pairs not over a ground plane, the trace width should be about 0.6 mm.

Manufacturing Test Procedure

The EVBs are tested after production. This procedure may also be used to verify correct operation afterwards. An oscilloscope with three channels and a bandwidth of at least 100 MHz is required.

Use the dedicated test board (Figure 21) to simplify the connections. Note the test board is not quite optimised; for instance, the 3 LEDs on the EVB are poorly visible. It is also not quite robust; handle it with great care.

To build the set-up, follow these steps:

1. Compensate the three channels of the oscilloscope.
2. Connect the three oscilloscope probes as shown in Figure 22.
3. Set the oscilloscope screen to a time base of about 40 ns/division.

Revision Information

The board was revised in 2024. Refer to Figure 1 and Figure 2 for the visual appearance and to Figure 25 and Figure 26 for the schematics.

The second revision can be identified from the silkscreen. The relevant changes are:

1. The routing of the SPE pairs was improved (Figure 15).

4. Connect a power supply capable of delivering at least 5 W.
5. Connect the test board to two 5½ -digit or better multimeters as shown in Figure 22.
   Connect a current-sensing multimeter between the blue banana connectors to measure the 3.3 V current consumed by the evaluation board under test.
   Connect a voltage-sensing multimeter between the black and green banana connectors to measure the output of the 2.5 V LDO on the EVB.
6. Verify that with no evaluation board present, the yellow activity LED on the test board blinks rapidly (10 Hz).

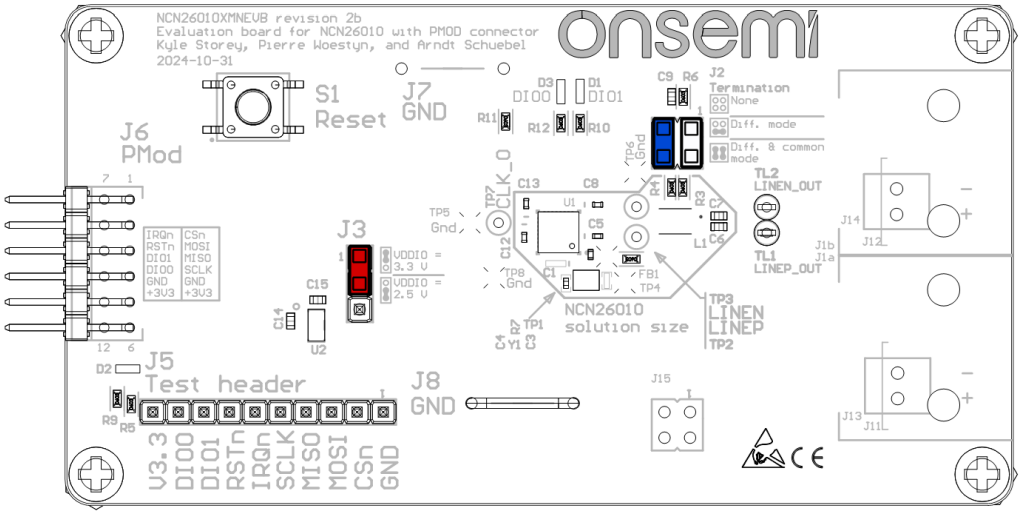

Figure 20. Placement of Jumpers after Manufacturing (Revision-2 Board Shown)

For each evaluation board to be tested, follow these steps:

7. Place two jumpers on J2 for differential and common-mode termination. For revision-2 boards, refer to Figure 20 (see also Figure 11).
8. Place one jumper on J3 for 3.3 V operation, as shown in Figure 20.
9. Place the EVB upside-down on the test board, taking care to keep it horizontally.
10. For the first 2–3 seconds, the yellow activity LED should blink rapidly (10 Hz) while the controller on the test board identifies the EVB and runs tests. When the yellow activity LED starts to blink slowly (2 Hz), all automatic tests have been completed successfully. If so, proceed to the next. If the LED continues to blink quickly for more than about 10 s, reject the board.
11. Verify the DIO0 LED (yellow) and DIO1 LED (green) on the EVB blink alternatingly at about 2 Hz. Unfortunately these LEDs are only visible in their reflection on the test board (Figure 22).
12. Verify the blue power LED on the EVB is constantly on. This LED, too, is only visible in reflection (Figure 22).

13. Verify a 25 MHz clock is present on CLKO as shown in Figure 23 (channel 3, red). The signal quality is limited by the pogo spring-contact pin; what is important is that the frequency is 25 MHz and the amplitude is roughly 3.3 V_{PP}.
    If a high-bandwidth oscilloscope is not available, an oscilloscope with a bandwidth of about 10 MHz can still be used, as long as the frequency and amplitude can still be meaningfully compared to a reference EVB (as in Figure 24).
14. Verify signals on the SPE outputs Line+ and Line− are present as shown in Figure 23 (channels 1 and 2, black and blue). As with the clock output, the exact signal quality is not important; the frequency must however be exact (25 MHz) and the amplitude roughly 1 V_{PP}. Line+ and Line− must both be present as differential signals. If either is missing or they are not the opposite of each other, reject the board.
    Again, a low-bandwidth oscilloscope can be used as long as the amplitude can be compared to a reference EVB (Figure 24).
15. Observe the current drawn by the EVB on the first multimeter. The current will be somewhat unstable due to the LED toggling; use the highest current. Write down the current in the results spreadsheet. Reject the board if it does not fall in the range 32—48 mA.
16. Observe the voltage on the second multimeter (output of the 2.5 V LDO). Reject the board if it does not fall in the range 2.45—2.55 V.
    Please see NOTE at the end of these instructions.
17. Remove the EVB from the test board.
18. Mount the screws and spacers P1–P8.
19. If applicable to the assembly variant, solder the connectors J1a—J1b or J11—J14.

After all boards have been tested, follow these steps:

20. Power down the Raspberry Pi safely by pressing the power button (Figure 21, centre top). Do *not* remove power until 10 s after the yellow activity LED stops blinking.

NOTE: The accuracy of the NCP730 LDO is ±1% from −40 °C to +85 °C. Some additional margin is added to account for measurement uncertainty. The uncertainty is *added*, i.e. opposite to normal parametric-testing practice, because this is a pass-fail test for soldering quality, not a parametric test of the LDO. The LDO leaves the factory fully tested.

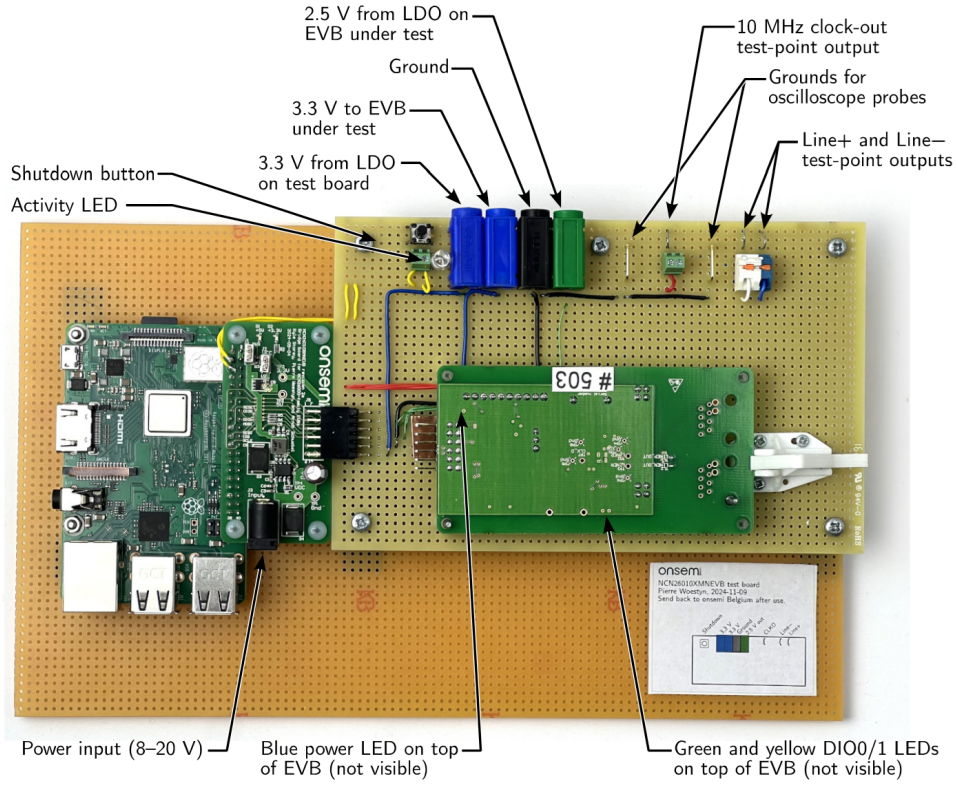

Figure 21. Test Board

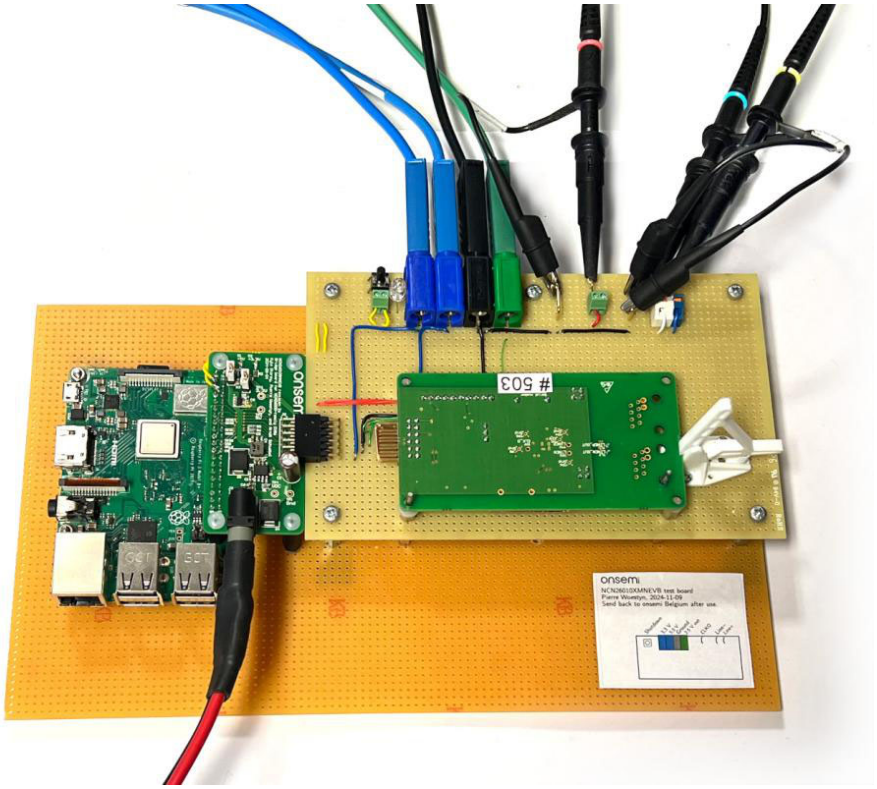

Figure 22. Test Board Connected to the Measurement Instruments

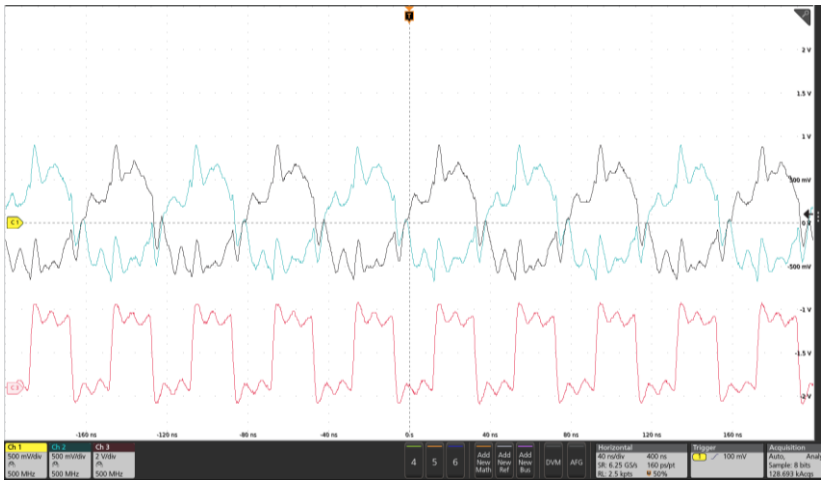

Figure 23. Oscilloscope Screen Showing the Correct Waveforms (High Bandwidth)

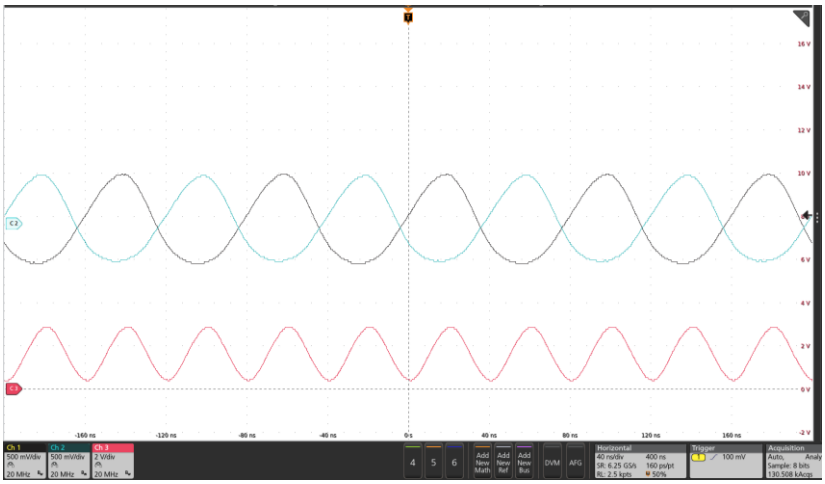

Figure 24. Oscilloscope Screen Showing the Correct Waveforms (Low Bandwidth)

SCHEMATICS

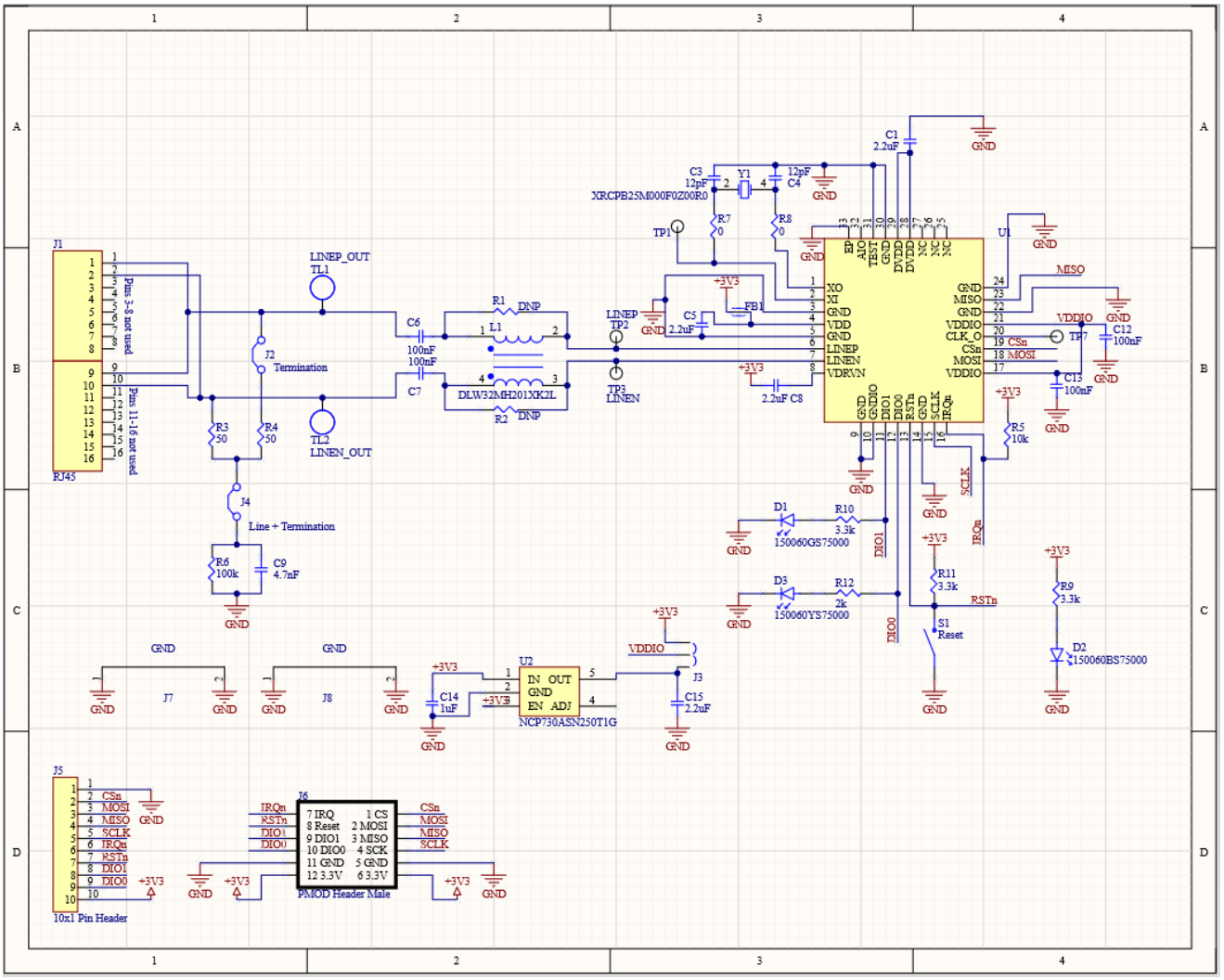

Figure 25. NCN26010XMNEBV Schematic (Revision 1)

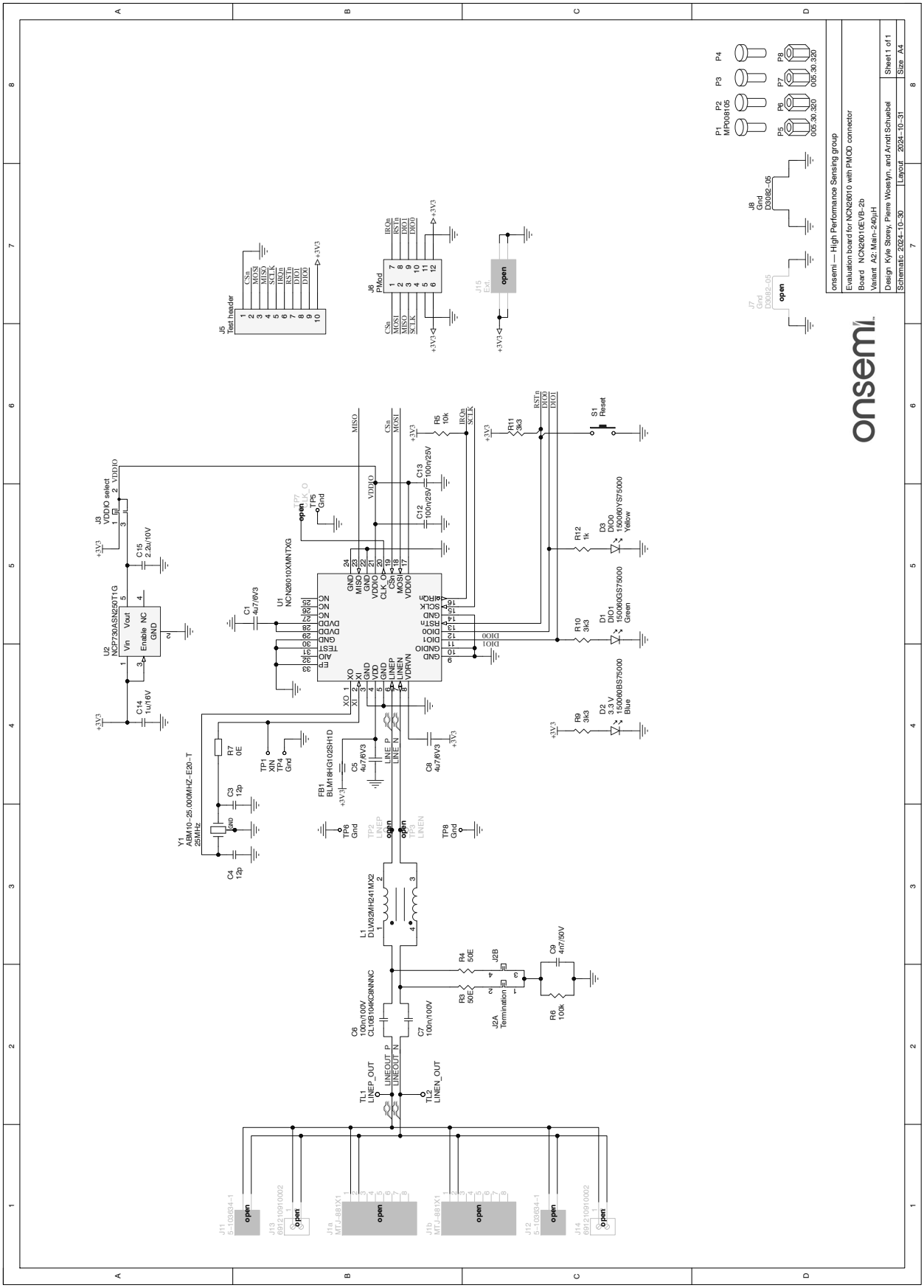

Figure 26. NCN26010XMNEBV Schematic (Revision 2)

References

[1] Michael Margraf, Stefan Jahn, and Vincent Habchi. *QucsStudio Technical Documentation.* 2018.

[2] IEEE Computer Society. *IEEE Standard for Ethernet —Amendment 5: Physical Layers Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors.* 2019.

[3] **onsemi**. *NCN26010BMNEVB 10BASE-T1S Power Supply and Adapter Board User's Manual (EVBUM2834/D).* 2024.

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