

# Isolated Dual Channel Gate Driver Evaluation Board User's Manual

## NCP51563 EVBUM

### Introduction

This user manual supports the evaluation board for the NCP51563. It should be used in conjunction with the NCP51563 datasheets as well as onsemi's application notes and technical support team. Please visit onsemi's website at [www.onsemi.com](http://www.onsemi.com).

This document describes the proposed solution for 5 kV<sub>RMS</sub> isolated dual channel gate driver using the NCP51563. This user's guide also includes information regarding operating procedures, input/output connections, an electrical schematic, printed circuit board (PCB) layout, and a bill of material (BOM) for each evaluation board.

These evaluation boards can be used both with NCP51563 and NCV51563.

### Description

The NCP51563 are isolated dual-channel gate drivers with 4.5 A / 9 A source and sink peak current respectively. They are designed for fast switching to drive power MOSFETs, and SiC MOSFET power switches. The NCP51563 offers short and matched propagation delays.

Two independent and 5 kV<sub>RMS</sub> internal galvanic isolation from input to each output and internal functional isolation between the two output drivers allows a working voltage of up to 1850 V<sub>DC</sub>. This driver can be used in any possible configurations of two low side, two high-side switches or a half-bridge driver with programmable dead time. An ENA/DIS pin enable or disable both outputs simultaneously when set high or low for ENABLE or DISABLE mode respectively.

The NCP51563 offers other important protection functions such as independent under-voltage lockout for both gate drivers and a Dead Time adjustment function.

### Key Features

- Flexible: Dual Low-Side, Dual High-Side or Half-Bridge Gate Driver
- Independent UVLO Protections for Both Output Drivers
- Output Supply Voltage from 6.5 V to 30 V with 5 V, 8 V for MOSFET, 13 V and 17 V UVLO for SiC, Thresholds
- 4.5 A Peak Source, 9 A Peak Sink Output
- Common Mode Transient Immunity CMTI >200 V/ns
- Propagation Delay Typical 36 ns with
  - ♦ 5 ns Max Delay Matching per Channel
  - ♦ 5 ns Max Pulse-Width Distortion
- User Programmable Input Logic
  - ♦ Single or Dual-Input Modes via ANB
  - ♦ ENABLE or DISASBLE Mode
- User Programmable Dead-Time

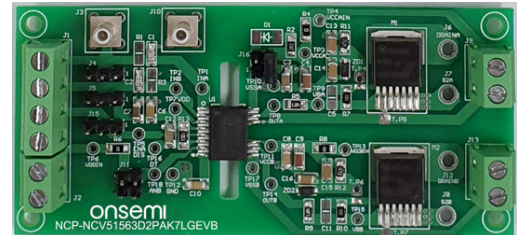
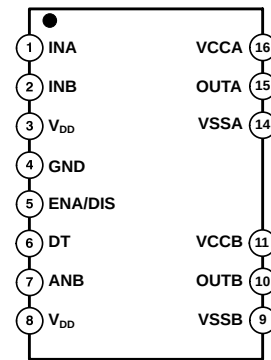
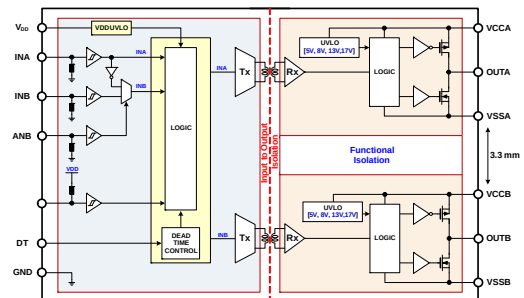


Figure 1. Evaluation Board Picture

### PIN CONNECTIONS



### FUNCTIONAL BLOCK DIAGRAM



## EVALUATION BOARD OPERATION

This section describes how to operate the NCP51563 evaluation board (EVB). Make external connections to the NCP51563 EVB using either the installed test-points or by installing wires into the connectors. The main connections that must be made to the EVB are the analog supply voltage, input signal, and output load and monitoring equipment.

### Features

- Evaluation board for the NCP51563 product family in a wide body SOIC-16 package
- 3 V to 5.0 V  $V_{DD}$  power supply range, and up to 30 V  $V_{CCA}/V_{CCB}$  power supply range
- 4.5 A and 9 A source/sink current driving capability.
- TTL –compatible inputs
- Allowable input voltage up to 18 V with for INA, INB, and ANB pins
- Onboard trimmer potentiometer for dead-time programming
- 3-position header with for INA, INB, and ENA/DIS pins
- 2-position header with for ANB pin
- Support for half-bridge test with MOSFETs, and SiC MOSFETs with connection to external power stage

### Power and Ground

NOTE: Connecting the all power supplies in reverse polarity (backwards) will instantly device when power is turned on and device damage can result.

The primary side of the EVM ( $V_{DD}$ ) operates from a single 3 V to 5.0 V power supply and connected via J2. Test

point (TP6 and TP7) is available for monitoring the primary power supply.

The EVM provides connections for evaluating the output side ( $V_{CCA}$ ,  $V_{SSA}$ ,  $V_{CCB}$ , and  $V_{SSB}$ ) power supplies for the channel A and B, from a minimum 6.5 V to maximum 30 V for 5 V UVLO version as shown in Figure 4.  $V_{CCA}$  and  $V_{CCB}$  can be monitored via TP3 and TP11, respectively.

The  $V_{CCA}$  and  $V_{CCB}$  pin should be bypassed with a capacitor with a value of at least ten times the gate capacitance, and over 100 nF and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. We had recommends using 2 capacitors; a over 100 nF ceramic surface-mount capacitor, and another a tantalum or electrolytic capacitor of few microfarads added in parallel.

### Input and Output

1. Connection of primary-side power supply to the  $V_{DD}$  connector [J2].
2. Connection of secondary-side power supply to the  $V_{CCA}$  and  $V_{CCB}$  connector [J9, and J13].
3. Connection of INA signal to the SIGNAL connector [J1-1, and J4].
4. Connection of INB signal to the SIGNAL connector [J1-2, and J5].
5. Connection of ENABLE or DISABLE signal to the ENA/DIS connector [J1-3, and J15].
6. Connection of ANB signal to the ANB jumper [J11].

# NCP51563 EVBUM

## Evaluation Board Jumper Setting

**Table 1. EVB JUMPER SETTING**

| Jumper       | Jumper Setting Options |                                                                                                           | Default Setting |
|--------------|------------------------|-----------------------------------------------------------------------------------------------------------|-----------------|
| J4-INA       | Option1                | Jumper not installed, INA/PWM signal provided by external signal and this pin is default low if left open | Option1         |
|              | Option2                | Jumper on J4-INA-2 and J4-INA-3 set INA low                                                               |                 |
|              | Option3                | Jumper on J4-INA-2 and J4-INA-1 set INA high                                                              |                 |
| J5-INB       | Option1                | Jumper not installed, INB signal provided by external signal and this pin is default low if left open     | Option1         |
|              | Option2                | Jumper on J5-INB-2 and J5-INB-3 set INB low                                                               |                 |
|              | Option3                | Jumper on J5-INB-2 and J5-INB-1 set INB high                                                              |                 |
| J11-ANB      | Option1                | Jumper on J11-ANB-2 and J11-ANB-4 set ANB low for dual input mode                                         | Option1         |
|              | Option2                | Jumper on J11-ANB-1 and J11-ANB-3 set ANB high for single input (PWM) mode                                |                 |
| J15-ENA/DIS  | Option1                | Jumper not installed, DISABLE signal provided by external signal and this pin is default low if left open | Option2         |
|              | Option2                | Jumper on J15-ENA/DIS-2 and J15-ENA/DIS-3 set DISABLE low (Or ENABLE low)                                 |                 |
|              | Option3                | Jumper on J15-ENA/DIS-2 and J15-ENA/DIS-1 set DISABLE high (Or ENABLE high)                               |                 |
| T.P1         | Option1                | Jumper on T.P1-1 and T.P1-2 for half-bridge application                                                   | Option2         |
|              | Option2                | Jumper off T.P1-1 and T.P1-2 for bench test.                                                              |                 |
| T.P2         | Option1                | Jumper on T.P2-1 and T.P2-2 and jumper on J16-2 and J16-4 for single power supply (VCCA = VCCB)           | Option1         |
|              | Option2                | Jumper on T.P2-1 and T.P2-2 and and jumper on J16-1 and J16-3 for VCCA bootstrap supply                   |                 |
| T.P3         | Option1                | Jumper on T.P3-1 and T.P3-2 for single power supply (e.g. VSSA = VSSB)                                    | Option1         |
|              | Option2                | Jumper off T.P3-1 and T.P3-2 for dual power supply                                                        |                 |
| T.P4<br>T.P5 | Option1                | Jumper on T.P4-1 and T.P4-2 for negative gate drive bias.                                                 | Option2         |
|              | Option2                | Jumper on T.P5-1 and T.P5-2 for unipolar gate drive.                                                      |                 |
| T.P6<br>T.P7 | Option1                | Jumper on T.P6-1 and T.P6-2 for negative gate drive bias.                                                 | Option2         |
|              | Option2                | Jumper on T.P7-1 and T.P7-2 for unipolar gate drive.                                                      |                 |

### Evaluation Board Setting before Power Up

1. If the ENABLE mode is used (e.g. NCP51563xA version), ENA/DIS pin (PIN5) should be connected to  $V_{DD}$  (PIN3 or PIN8) through a wire-bridge between pin 1 and pin 2 of J15 or this pin is default HIGH if left open.  
On the other hand, if using the DISABLE mode (e.g. NCP51563xB version), should be connect ENA/DIS pin to GND pin through a wire-bridge between pin 2 and pin 3 of J15.
2. If using the dual input mode, should be ANB pin (PIN7) connected to GND (PIN4) through a

wire-bridge between pin 2 and pin 4 of J11.

On the other hand, if using the single input mode, should be connect ANB pin to  $V_{DD}$  pin through a wire-bridge between pin 1 and pin 3 of J11.

3. Should be connect to the resistance between DT pin (pin6) and GND (pin4) for dead-time control mode. In addition, Cross-conduction between both driver outputs (OUTA, and OUTB) is not allowed with minimum dead time ( $t_{DTMIN}$ ) typically 10 ns when the DT pin is floating (Open).

## NCP51563 EVBUM

### Bench Setup

The bench setup diagram includes the function generator, power supplies and oscilloscope connections.

Follow the connection procedure below and use Figure 2 as a reference.

- Make sure all the output of the function generator, power supplies are disabled before connection.
- Function generator channel-A channel applied on INA (J4 or J1 pin-1) ↔ TP1 as seen in Figure 2.
- Function generator channel-B channel applied on INB (J5 or J1 pin-2) ↔ TP2 as seen in Figure 2.
- If the ENABLE mode is used, ENA/DIS pin (PIN5) should be connected to  $V_{DD}$  (PIN3 or PIN8) through a wire-bridge between pin 1 and pin 2 of J15. On the other hand, if using the DISABLE mode, should be connect ENA/DIS pin (PIN5) to GND pin (PIN4) through a wire-bridge between pin 2 and pin 3 of J15.
- If using the dual input signals (INA and INB) with same polarity, should be DT pin (PIN6) connected to  $V_{DD}$  (PIN3 or 8). On the other hand, if using the dual input signals with opposite polarity, should be connect to the resistance

(R13) between DT pin (pin6) and GND (pin4) or DT pin is floating (Open).

- If using the dual input mode, should be ANB pin (PIN7) connected to GND (PIN4) through a wire-bridge between pin 2 and pin 4 of J11.
- On the other hand, if using the single input mode, should be connect ANB pin (PIN7) to  $V_{DD}$  pin (PIN3 or 8) through a wire-bridge between pin 1 and pin 3 of J11.
- Power supply #1: positive node applied on J2 pin-1 (or TP6), and negative node applied on J2 pin-2.
- Power supply #2: positive node applied on J9 pin-1 (or TP4), negative node connected directly to J9 pin-2 (or TP10) and should be connected to VAIN and  $V_{CCA}$  through a wire-bridge between pin 2 and pin 4 of J16.
- Power supply #3: positive node applied on J13 pin-1 (or TP13), negative node connected directly to J13 pin-2 (or TP17).
- Oscilloscope channel-A probes TP8 ↔ TP10, smaller measurement loop is preferred.
- Oscilloscope channel-B probes TP14 ↔ TP17, smaller measurement loop is preferred.

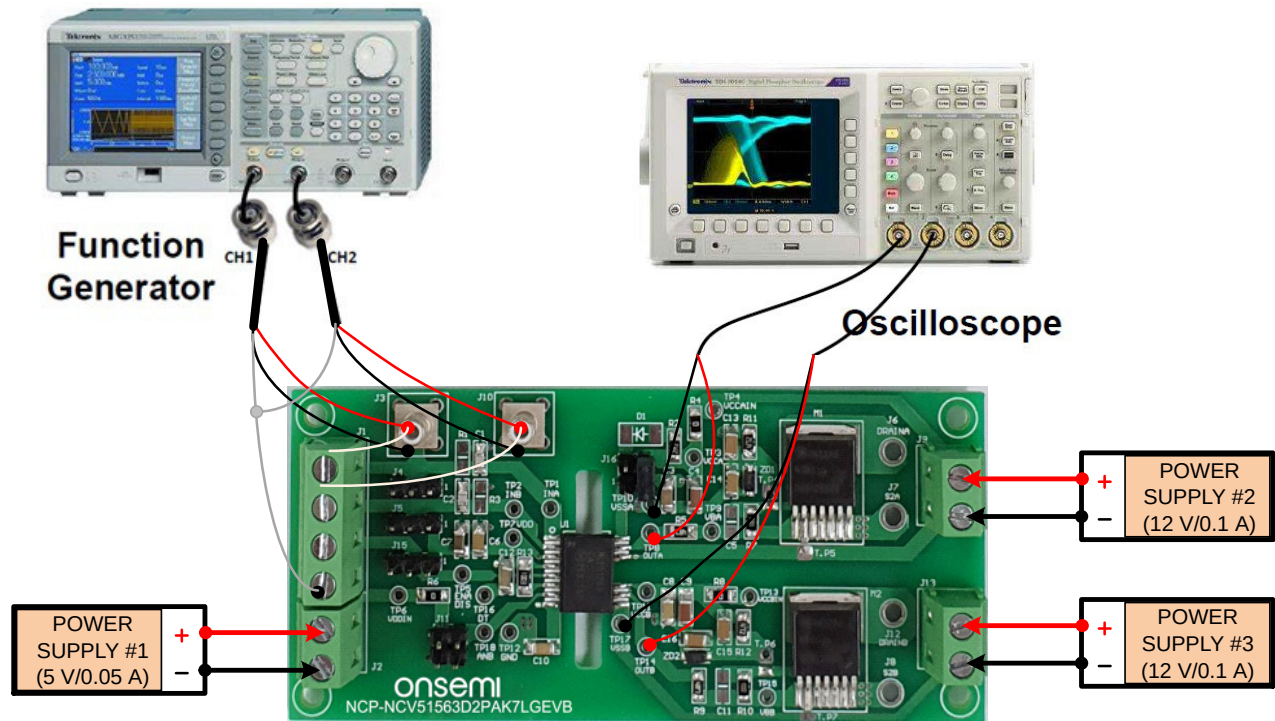


Figure 2. Bench Setup Diagram and Configuration

## Power-Up and Power Down Procedure

### Power Up

1. Could be connect VSSA pin to VSSB pin through a wire-bridge between pin 1 and pin 2 of T.P3, if the Half-Bridge application is not used.
2. Enable power supply through pin1 of J2  $V_{DD}$  connector in primary-side.
3. Enable power supply through pin1 of J9  $V_{CCA}$  connector and through pin1 of J13  $V_{CCB}$  connector in secondary-side. Measure the quiescent current of  $V_{CCA}$ , and  $V_{CCB}$  on DMM1 and DMM2 ranges from 0.5 mA to approximately 1.0 mA if everything is set correctly.
4. Examples of implementing negative gate drive bias:
  - A Should be connect switches source pins (S2A, and S2B) to ZD1 and ZD2 pin through a wire-bridge between pin 1 and pin 2 of T.P4 and T.P6 , if the use the negative gate drive bias. The negative bias is set by the Zener diode voltage.
  - B Should be connect switches source pins (S2A, and S2B) to VSSA and VSSB pins through a wire-bridge between pin 1 and pin 2 of T.P5 and T.P5, if the use the unipolar gate driving. **(Default)**
5. Enable the function generator, two-channel outputs: channel-A and channel-B;
6. There will be:
  - A Stable pulse output on the channel-A and channel-B in the oscilloscope.
  - B Scope frequency measurement is the same with function generator output;
  - C DMM #1 and #2 read measurement results should be around 3 mA  $\pm$  1 mA under no load conditions. For more information about operating current, refer to the NCP51563 data sheet.

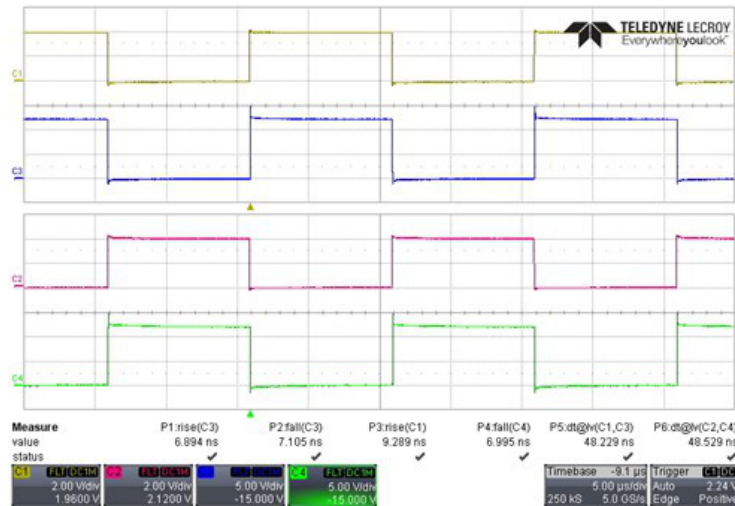


Figure 3. Experimental Waveforms of Input to Output

### Power Down

1. Disable function generator.
2. Disable power supply of  $V_{CCA}$ , and  $V_{CCB}$  in secondary-side.
3. Disable power supply of  $V_{DD}$  in primary-side.
4. Disconnect cables and probes.

## NCP51563 EVBUM

Figure 4 shows an application schematic of the NCP51563 evaluation board. This EVB allows for

evaluation of the device with an MOSFET and SiC MOSFET load in the standard D2PAK-7L footprint.

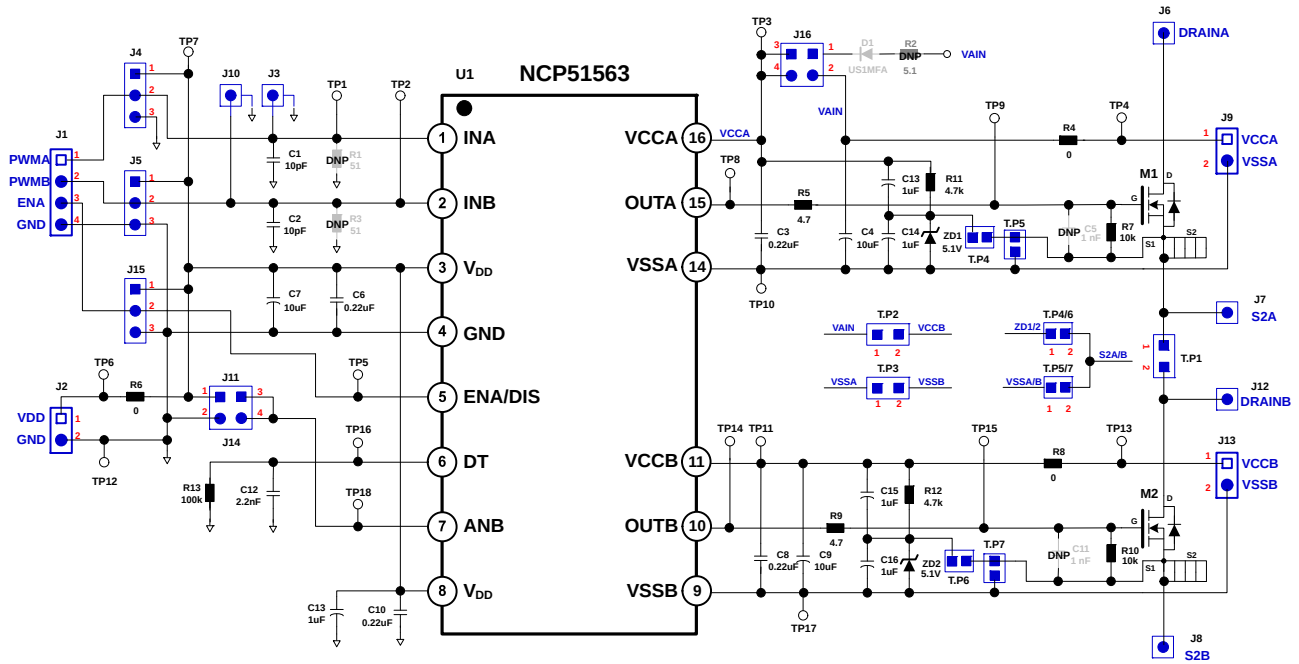


Figure 4. Typical Application Schematic of NCP51563 EVB

## NCP51563 EVBUM

### List of Test Point

Table 2 shows the test point list of NCP51563 for an evaluation board.

**Table 2. LIST OF TEST POINT**

| TP   | Reference | Description                                                                                                                                                                                                                                                                     |
|------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TP1  | INA       | Logic input for Channel A with internal pull-down resistor to GND.                                                                                                                                                                                                              |
| TP2  | INB       | Logic input for Channel B with internal pull-down resistor to GND.                                                                                                                                                                                                              |
| TP3  | VCCA      | Supply voltage for output Channel A.                                                                                                                                                                                                                                            |
| TP4  | VCCAIN    | It is recommended to place a bypass capacitor from VCCA to VSSA.                                                                                                                                                                                                                |
| TP5  | ENA/DIS   | Logic input High enables both output channels with Internal pull-up resistor for an ENABLE version. Conversely, Logic input High disables both output channels with internal pull-down resistor for the DISABLE version.                                                        |
| TP6  | VDDIN     | Input-side supply voltage.                                                                                                                                                                                                                                                      |
| TP7  | VDD       | It is recommended to place a bypass capacitor from VDD to GND.                                                                                                                                                                                                                  |
| TP8  | OUTA      | Output for Chanel A                                                                                                                                                                                                                                                             |
| TP9  | VGA       |                                                                                                                                                                                                                                                                                 |
| TP10 | VSSA      | Ground for Channel A                                                                                                                                                                                                                                                            |
| TP11 | VCCB      | Supply voltage for output Channel B.<br>It is recommended to place a bypass capacitor from VCCB to VSSB.                                                                                                                                                                        |
| TP12 | GND       | Ground Input-side. (all signals on input-side are referenced to this pin)                                                                                                                                                                                                       |
| TP13 | VCCBIN    | Supply voltage for output Channel B.                                                                                                                                                                                                                                            |
| TP14 | OUTB      | Output for Channel B                                                                                                                                                                                                                                                            |
| TP15 | VGB       |                                                                                                                                                                                                                                                                                 |
| TP16 | DT        | Input for programmable Dead-Time                                                                                                                                                                                                                                                |
| TP17 | VSSB      | Ground for Channel B                                                                                                                                                                                                                                                            |
| TP18 | ANB       | It is recommended to tie this pin to GND or floating (not recommended) if the ANB pin is not used to achieve better noise immunity. The ANB pin has a typical 3.3 $\mu$ s internal filter to improve noise immunity but we recommend to tie to GND, if the ANB pin is not used. |



# NCP51563 EVBUM

## Electrical Specifications

Table 3 show the recommended operating conditions of NCP51563 for an evaluation board.

**Table 3. ELECTRICAL SPECIFICATIONS**

| Rating                                        |                   | Symbol             | Min  | Max  | Unit |
|-----------------------------------------------|-------------------|--------------------|------|------|------|
| Power Supply Voltage – Input side             |                   | $V_{DD}$           | 3.0  | 5.0  | V    |
| Power Supply Voltage – Driver side            | 5 V UVLO Version  | $V_{CCA}, V_{CCB}$ | 6.5  | 30   | V    |
|                                               | 8 V UVLO Version  |                    | 9.5  | 30   | V    |
|                                               | 13 V UVLO Version |                    | 14.5 | 30   | V    |
|                                               | 17 V UVLO Version |                    | 18.5 | 30   | V    |
| Logic Input Voltage at pins INA, INB, and ANB |                   | $V_{IN}$           | 0    | 18   | V    |
| Logic Input Voltage at pin ENA/DIS            |                   | $V_{EN}$           | 0    | 5.0  | V    |
| Operating Junction Temperature                |                   | $T_J$              | -40  | +125 | °C   |

## Bill of Material (BOM)

Table 4 shows the bill of material (BOM) of NCP51563 for an evaluation board.

**Table 4. BILL OF MATERIAL**

| Reference          | Qty | Description        | Value              | Footprint   | Manufacturer |
|--------------------|-----|--------------------|--------------------|-------------|--------------|
| U1                 | 1   | Gate Driver        | NCP51563           | 16 SOIC-WB  | onsemi       |
| D1                 | 0   | Diode              | US1MFA (DNP)       | SMB/DO214AA | onsemi       |
| ZD1, ZD2           | 2   | Zenner Diode       | 5.1 V              | SOD-123     |              |
| R1, R3             | 0   | Resistor           | 51 $\Omega$ (DNP)  | SMD 0805W   |              |
| R2                 | 1   | Resistor           | 5.1 $\Omega$       | SMD 0805W   |              |
| R4, R6, R8         | 3   | Resistor           | 0 $\Omega$         | SMD 0805W   |              |
| R5, R9             | 2   | Resistor           | 4.7 $\Omega$       | SMD 0805W   |              |
| R7, R10            | 2   | Resistor           | 10 k $\Omega$      | SMD 0805W   |              |
| R11, R12           | 2   | Resistor           | 4.7 k $\Omega$     | SMD 0805W   |              |
| R13                | 1   | Resistor           | 100 k $\Omega$     | SMD 1206W   |              |
| C1, C2             | 2   | Capacitor, Ceramic | 10 pF, 50 V        | SMD 0805W   |              |
| C3, C6, C8, C10    | 4   | Capacitor, Ceramic | 0.22 $\mu$ F, 50 V | SMD 3216    |              |
| C4, C7, C9         | 3   | Capacitor, Ceramic | 10 $\mu$ F, 50 V   | SMD 3216    |              |
| C5, C11            | 0   | Capacitor, Ceramic | 1 nF, 50 V (DNP)   | SMD 0805W   |              |
| C12                | 1   | Capacitor, Ceramic | 2.2 nF, 50 V       | SMD 3216    |              |
| C13, C14, C15, C16 | 4   | Capacitor, Ceramic | 1 $\mu$ F, 50 V    | SMD 3216    |              |
| M1, M2             | 2   | Switch             |                    | D2PAK-7L    |              |
| J1                 | 1   | Connector          |                    | EB21A-04-D  |              |
| J2, J9, J13        | 3   | Connector          |                    | EB21A-02-D  |              |
| J3, J10            | 2   | BNC Connector      |                    | SMB         |              |
| J4, J5, J15        | 3   | Header 3           |                    |             |              |
| J11, J16           | 2   | Header 2 x 2       |                    |             |              |
| J6, J7, J8, J12    | 4   | Connector          |                    |             |              |



## Input Stage

The input pins of NCP51563 is based on a TTL compatible input-threshold logic that is independent of the  $V_{DD}$  supply voltage for INA, INB, ANB, and ENA/DIS pins.

The logic level compatible input provides a typically high threshold of 1.6 V and a typically low threshold of 1.1 V. The input impedance of the NCP51563 is 200 k $\Omega$  typically, as shown in Figure 5.

And we recommend an RC network is to be added on the PWM input pins, INA and INB, for reducing the impact of system noise and ground bounce, for example, 51  $\Omega$  (R1, and R3) with 10 pF (C1, and C2) is an acceptable choice as shown in Figure 5.

INA, INB, ENA/DIS and ANB signal can be monitored via TP1, TP2, TP5 and TP18, respectively.

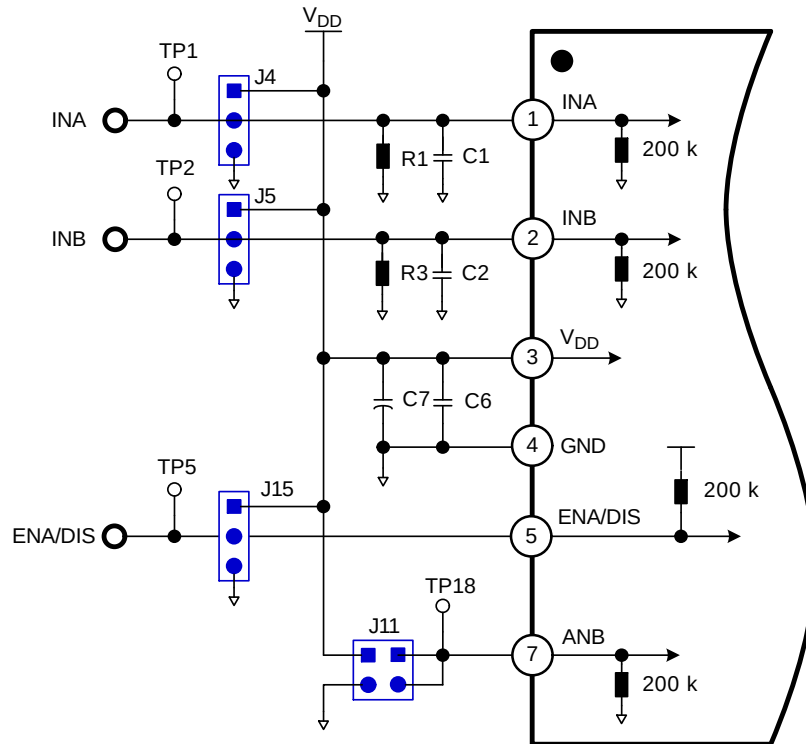


Figure 5. Recommended Input Circuit for an ENABLE Version

## Output Stage

The output stage is able to sink/source typically around 4.5 A/9.0 A at 25°C for the NCP51563.

The EVB comes populated with a 1 nF load (C5, and C11) on the output side. The OUTA and OUTB can be monitored directly via TP8 and TP14, respectively.

The EVB provides an additional connection (J6) for applying an external power supply to the MOSFET Drain. The EVB is not intended for high voltage testing and the voltage applied to J6 should be limited to 50 V<sub>DC</sub>.

# NCP51563 EVBUM

## PERFORMANCE OF EVALUATION BOARD

This section describes application guidance and operation of the NCP51563 for an evaluation board (EVB) include key functions.

### Input Signal Configuration

The NCP51563 allows changing the input signal pin configuration by the ANB pin for user convenience. (e.g. single input – dual output, or dual input – dual output).

### ANB Function

The NCP51563 allows changing the input signal pin configuration by the ANB pin for user convenience. There are two operating modes that allow changing the configuration of the input to output channels (e.g. single input – dual output, or dual input – dual output).

Figure 6 and Figure 7 shows the experimental result of ANB function with and without dead-time control.

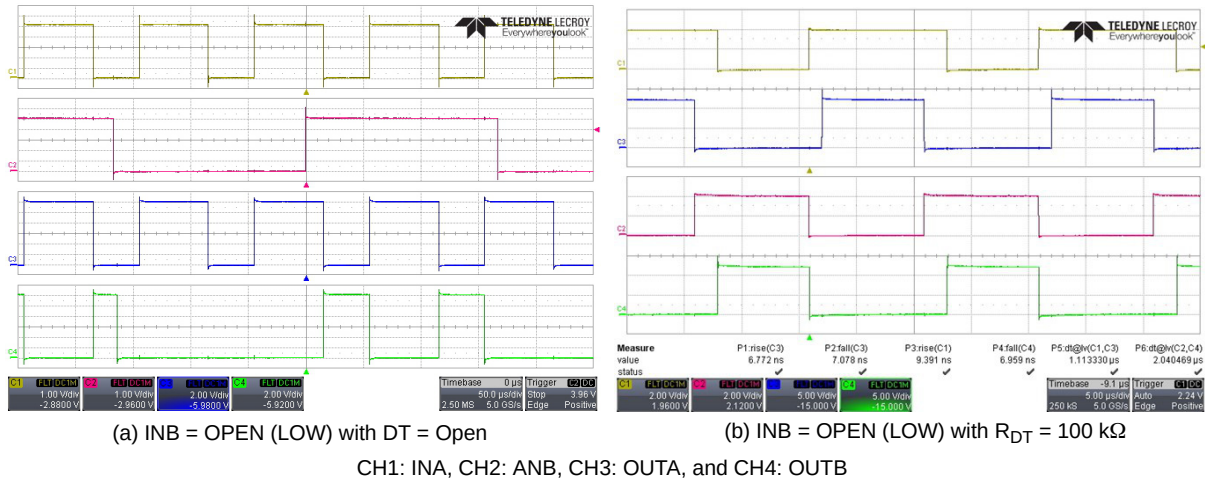


Figure 6. Experimental Waveforms of ANB Function with Dead-Time

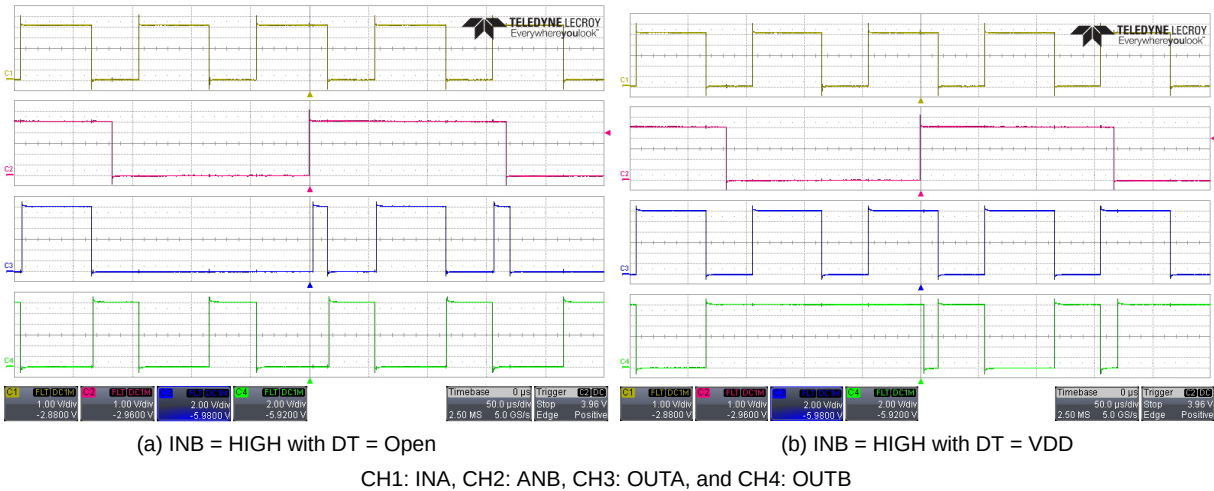


Figure 7. Experimental Waveforms of ANB Function

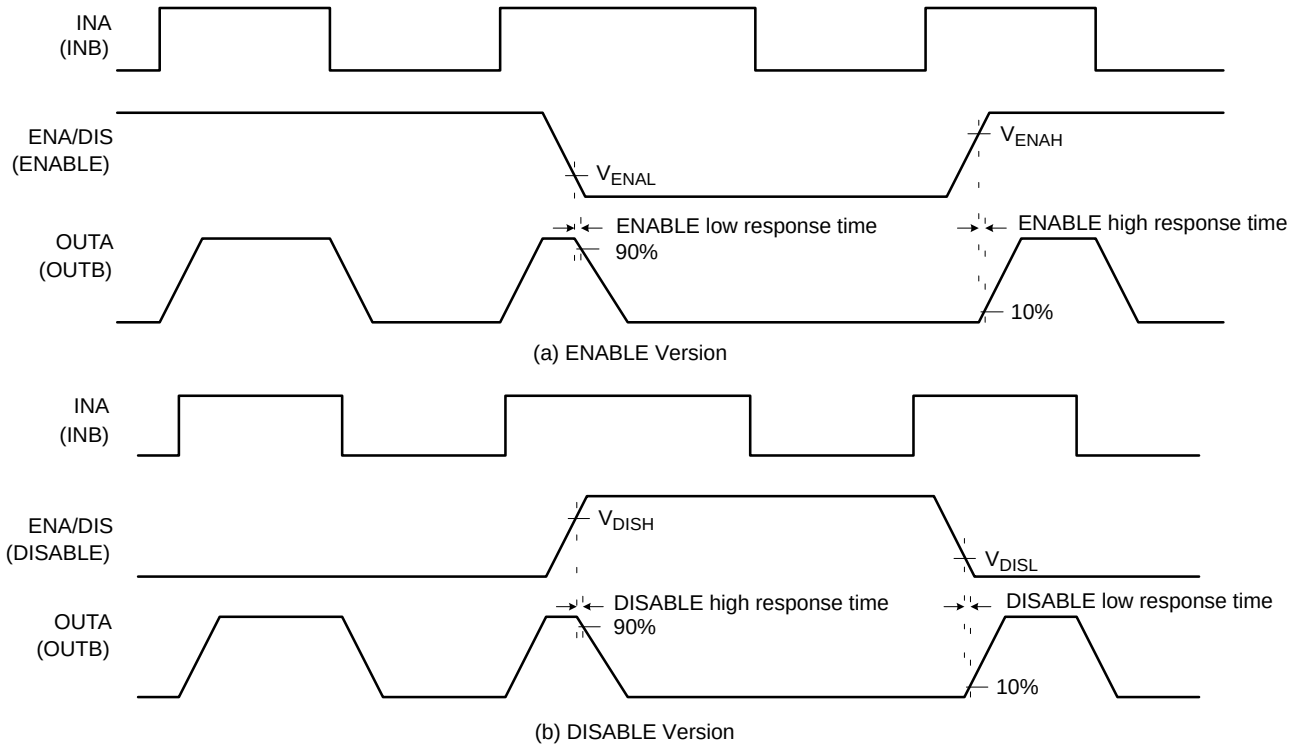
## NCP51563 EVBUM

### Protection Function

NCP51563 provide the protection features include Enable or Disable function, and Under-Voltage Lockout (UVLO) of power supplies in primary-side ( $V_{DD}$ ), and secondary-side both channels ( $V_{CCA}$ , and  $V_{CCB}$ ).

### ENABLE and DISABLE Function

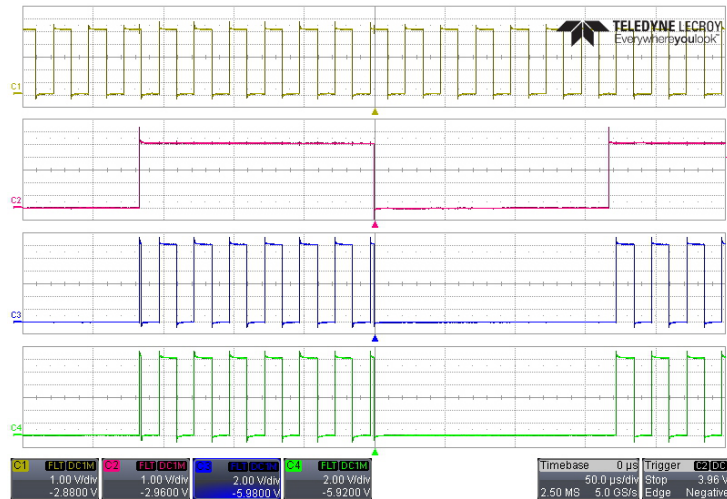
Figure 8 shows the timing chart of ENABLE and DISABLE function. (e.g. NCP51563xA or NCP51563xB version).



**Figure 8. Timing Chart of ENABLE and DISABLE**

Figure 9 shows an experimental result of enable function that the ENA/DIS pin voltage goes to LOW state in normal

operation, the both driver output is turned-off immediately even though input signals, INA and INB, are HIGH state.



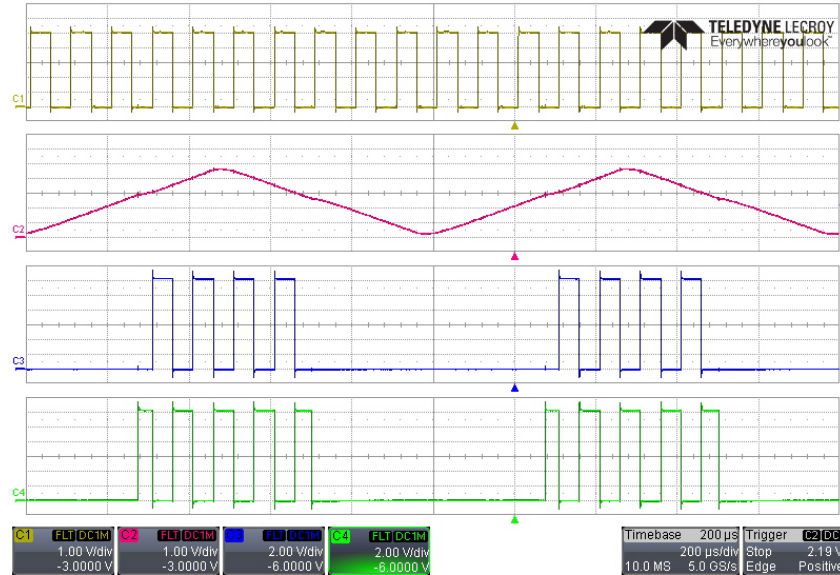
**Figure 9. Experimental Waveforms of Enable Function**

## NCP51563 EVBUM

### Under-Voltage Lockout Protection $V_{DD}$

The NCP51563 provides the Under-Voltage Lockout (UVLO) protection function for  $V_{DD}$  in primary-side as shown in Figure 10. The OUTA and OUTB as

complementary outputs from one PWM input signal on the INA pin regardless the INB signal when the ANB pin is high. As test result, the  $V_{DD}$  UVLO turn-on and off threshold voltages are around 2.8 V and 2.7 V respectively.



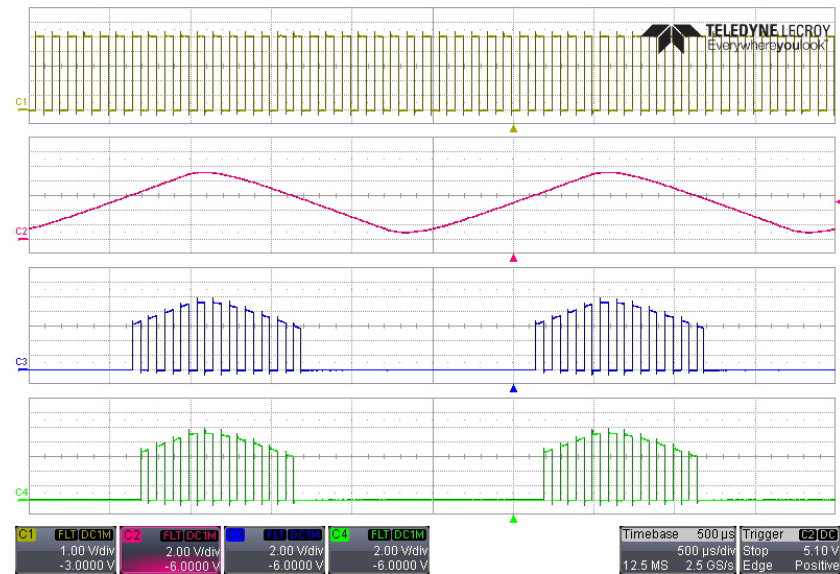
CH1: INA, CH2: VDD, CH3: OUTA, and CH4: OUTB

Figure 10. Experimental Waveforms of VDD Under-Voltage Lockout Protection

### Under-Voltage Lockout Protection $V_{CCx}$ ( $V_{CCA}$ and $V_{CCB}$ )

The NCP51563 provides the Under-Voltage Lockout (UVLO) protection function for both gate drive output for  $V_{CCA}$  and  $V_{CCB}$  for 5 V version in secondary-side as shown

in Figure 11. The OUTA and OUTB as complementary outputs from one PWM input signal on the INA pin regardless the INB signal when the ANB pin is high. As test result, the  $V_{CCx}$  UVLO turn-on and off threshold voltages are around 6.0 V and 5.7 V respectively.



CH1: INA, CH2: VCCA, and VCCB, CH3: OUTA, and CH4: OUTB

Figure 11. Experimental Waveforms of VCC Under-Voltage Lockout Protection

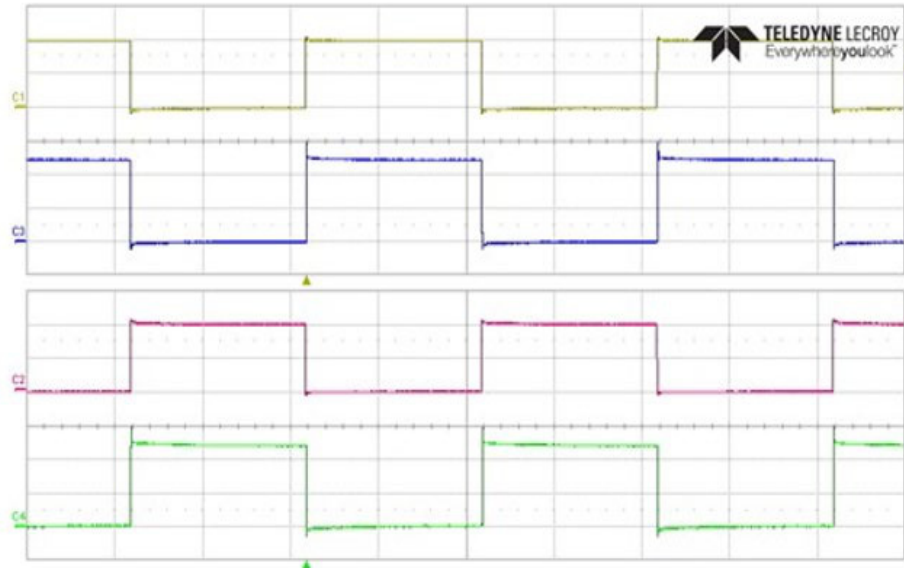
## NCP51563 EVBUM

### Experimental Waveforms with Different Dead-Time Configurations

This section shows experimental test results of dead-time control with different dead-time (DT) configuration.

### DT Pin Floating or Left Open (R13 and C12 are Open)

The dead-time(DT) between the outputs (OUTA and OUTB) of the two channels is typically around 10 ns, which is preset for shoot-through prevention as shown in Figure 12.

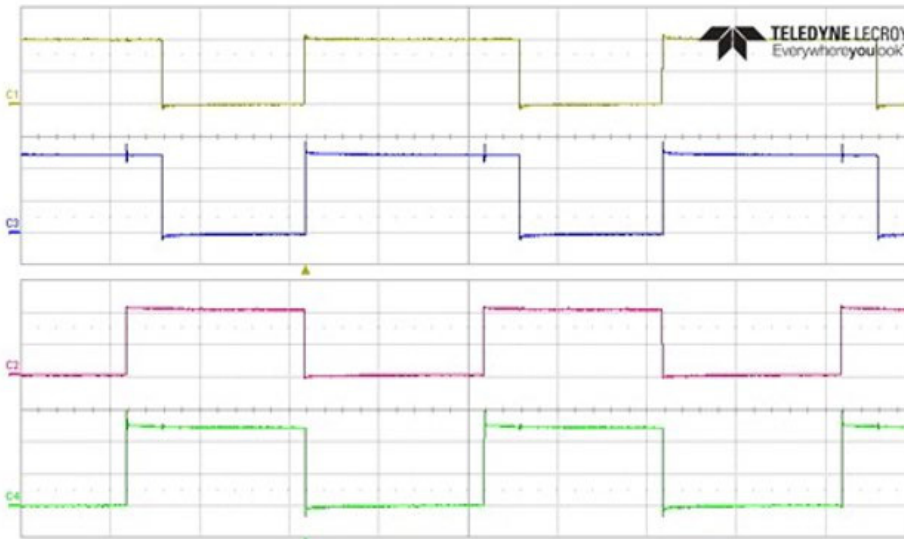


CH1: INA, CH2: INB, CH3: OUTA, and CH4: OUTB

**Figure 12. Experimental Waveforms if DT is Left Open**

### DT Pin Connected to $V_{DD}$

Overlap is allowed both switches from conducting even though at the same time when the DT pin pulled to  $V_{DD}$  as shown in Figure 13.



CH1: INA, CH2: INB, CH3: OUTA, and CH4: OUTB

**Figure 13. Overlap is Allowed when DT Connected to VDD**

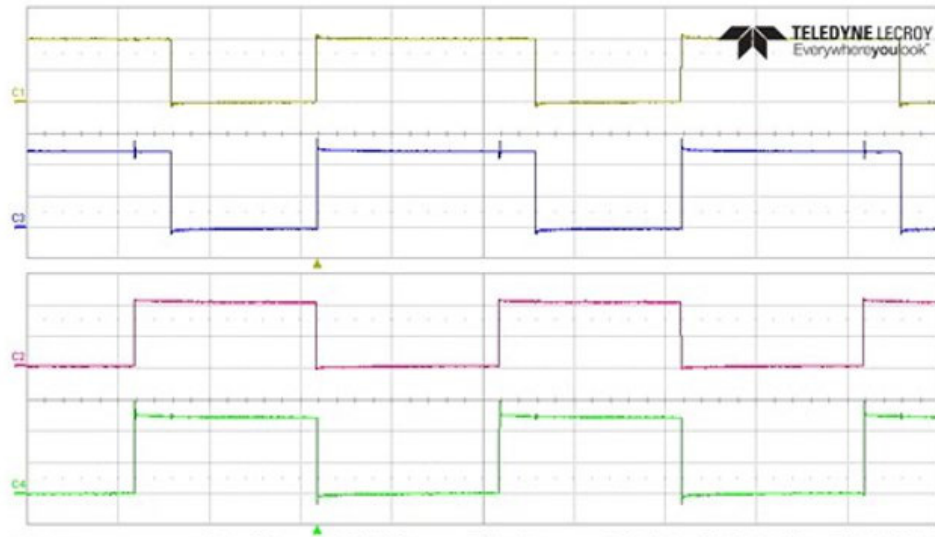
## NCP51563 EVBUM

### DT Pin Connected to $R_{DT}$

Overlap is not allowed both switches at the same time when the dead time (DT) control mode. The dead-time (DT) between both outputs is set according to:

$$DT \text{ (in ns)} = 10 \times R_{DT} \text{ (in k}\Omega\text{)}.$$

Figure 14 shown the experimental results when the dead-time control resistance for 100 k $\Omega$ .



CH1: INA, CH2: INB, CH3: OUTA, and CH4: OUTB

Figure 14. Experimental Waveforms if DT Connected to  $R_{DT}$

### Dead Time Characteristics

Figure 15 shows the dead time characteristics and operating modes according to the dead-time resistance values of the NCP51563.

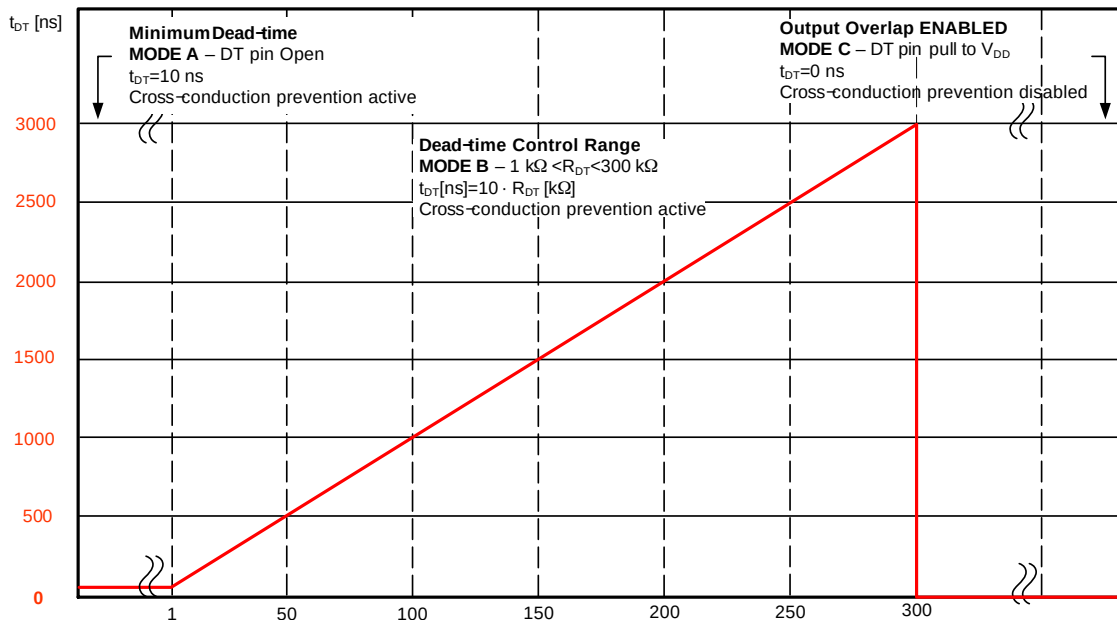


Figure 15. Dead Time (DT vs.  $R_{DT}$ )



## Select the Type of Output Drive

There are many similarities between SiC MOSFETs and Si MOSFETs. However, some of the challenges faced by the designers of SiC MOSFETs is the control of the gate threshold voltage. The SiC MOSFETs require a higher positive gate drive voltage (+20 V) and, depending on the application, a negative OFF gate voltage in the -2 V to -6 V range because it exhibits lower  $V_{gs}$  threshold that could lead to unwanted Turn-ON of the SiC MOSFET. Below are examples of implementing negative gate drive bias with negative bias turn-off on the gate driver using a Zener diode on an isolated power supply (e.g. ZD1 and ZD2) as shown in Figure 16.

Can be selected the type of output drive for the unipolar or negative bias as follows:

**A** Should be connect switches (M1 and M2) source pins (S2A, and S2B) to ZD1 and ZD2 pin through a wire-bridge between pin 1 and pin 2 of T.P4 and T.P6 respectively, if the use the negative gate drive bias.

**B** Should be connect switches (M1 and M2) source pins (S2A, and S2B) to VSSA and VSSB pins through a wire-bridge between pin 1 and pin 2 of T.P5 and T.P7 respectively, if the use the unipolar gate driving. **(Default)**

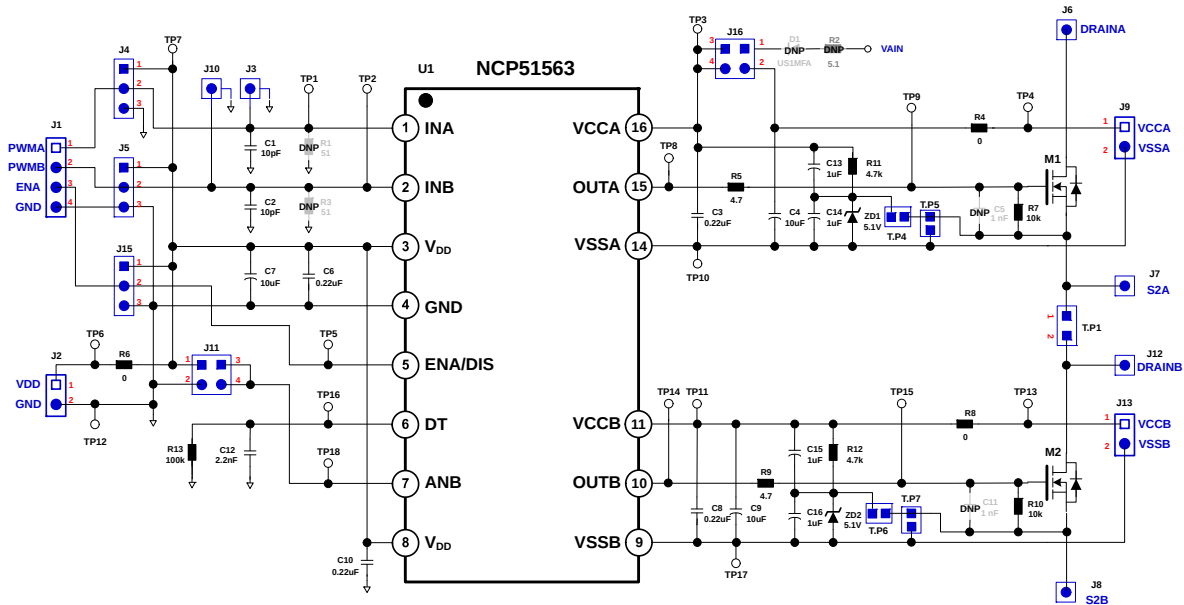
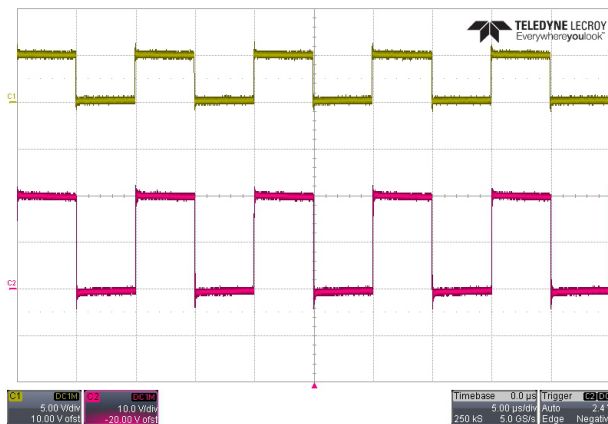


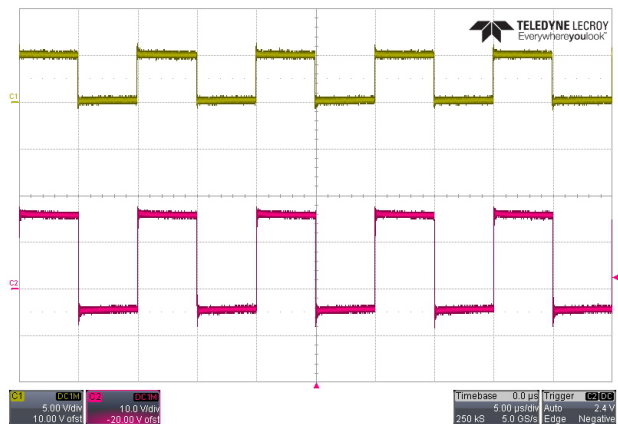
Figure 16. Application Schematic of Negative Bias with Zener Diode on Iso-Bias Power Supply Output

Figure 17 shows the experimental result of unipolar and bipolar driving output with negative bias gate driving respectively. The examples were design to have a +15 V and

-5.1 V drive power supply referenced to the device source by using the 20 V isolated power supply.



(a) Unipolar Gate Driving Output



(b) Negative Bias Gate Driving Output

CH1: INPUT Signal, and CH2: OUTPUT

Figure 17. Experimental Waveforms of Output Driving Voltage

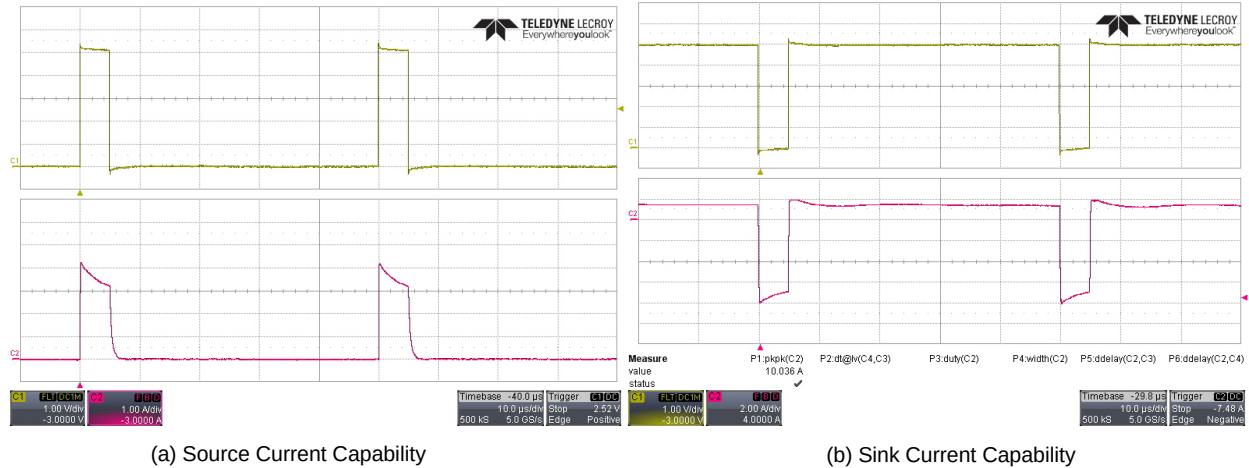


# NCP51563 EVBUM

## Output Driving Current Capability

Figure 18 shows the experimental result of source and sink peak currents driving capability around 4.0 A and 10 A

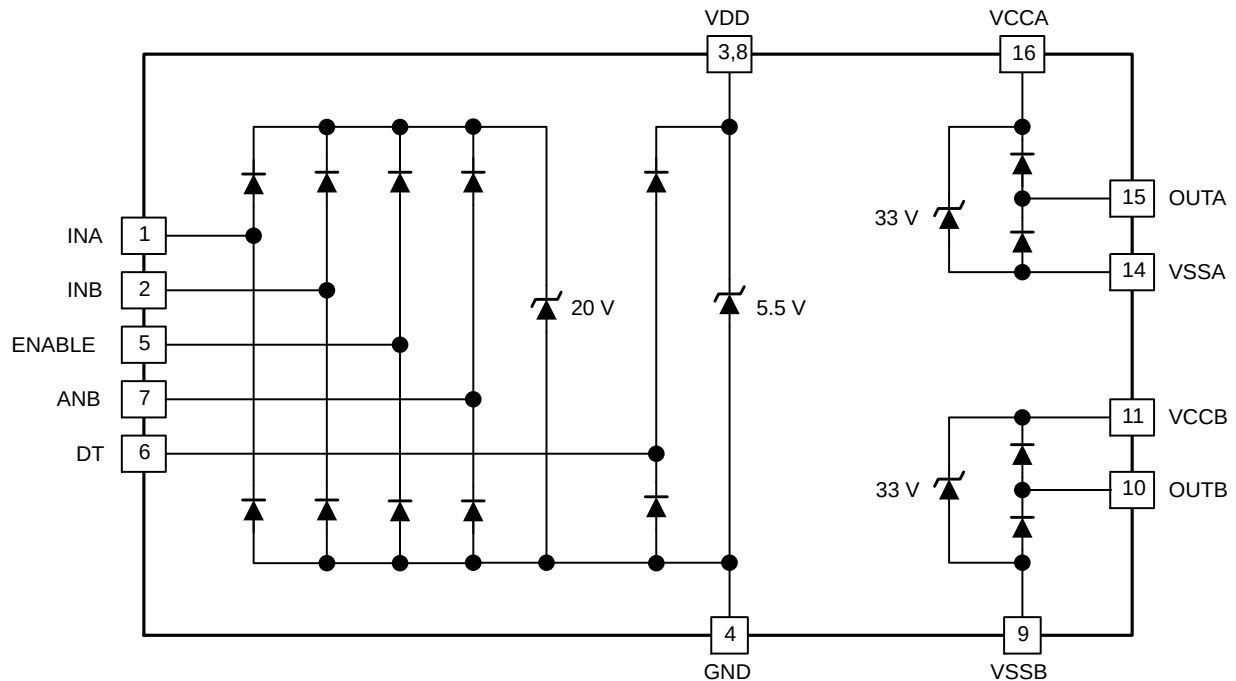
respectively at 25°C when the supply voltage ( $V_{CCA}$  and  $V_{CCB}$ ) is applied 12 V.



**Figure 18. Experimental Waveforms of Current Driving Capability**

## ESD Structure

Figure 19 shows the multiple diodes related to an ESD protection components of NCP51563. This illustrates the absolute maximum rating for the device.



**Figure 19. ESD Structure**

## NCP51563 EVBUM

### Printed Circuit Board

Figure 20 shows the photograph of the NCP51563 evaluation board. This EVB allows for evaluation of

the device with an MOSFET and SiC MOSFET load in the standard D2PAK-7L footprint.

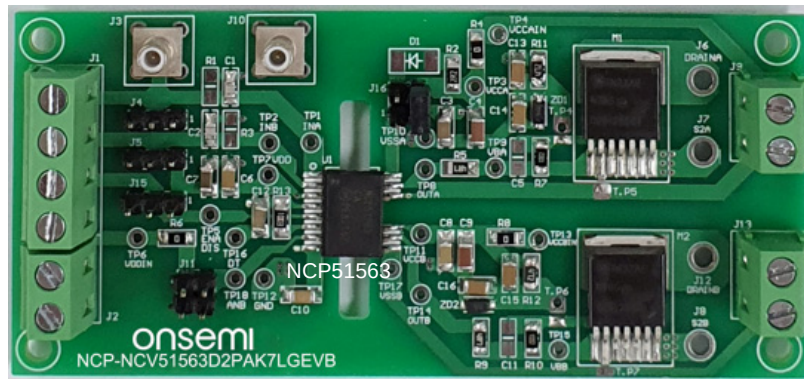
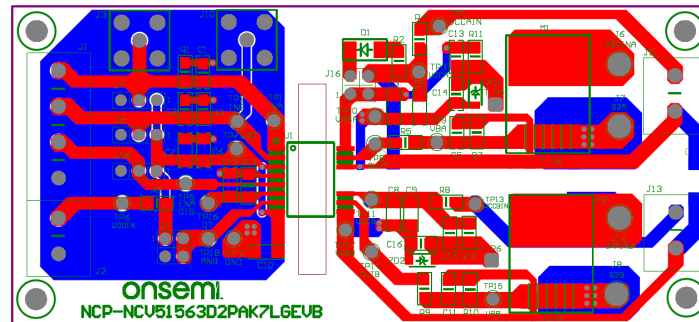
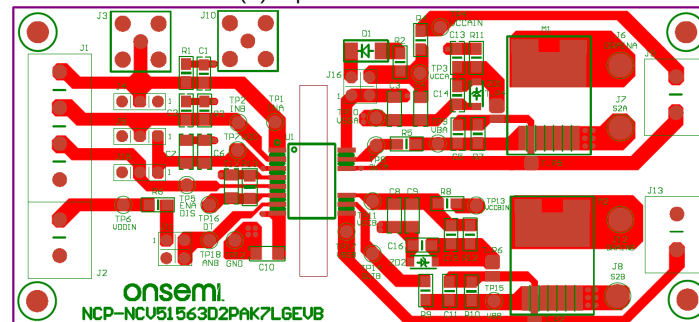


Figure 20. Evaluation Board Picture (Top View)

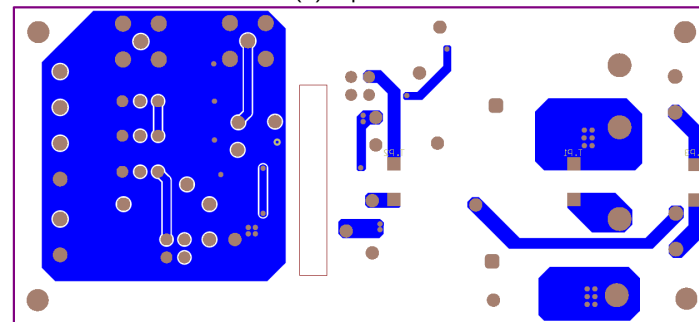
Figure 21 shows the printed circuit board layout of NCP51563 evaluation board.



(A) Top & Bottom View



(B) Top View



(C) Bottom View

Figure 21. Printed Circuit Board

## NCP51563 EVBUM

### Related Product Information

- [1] Datasheet of [NCP51563/D](#) available on **onsemi** website
- [2] Datasheet of [NCV51563/D](#) available on **onsemi** website

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