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Design Note – DN05110/D

The NCP156 - Design hints

Device	Application	Input Voltage	Topology	I/O Isolation
NCP156	Consumer	5.5 V max.	Linear regulator	No

Other Specification

	Output 1	Output 2
Output Voltage	0.8 – 1.8 V	1.8 – 3.6 V
PSRR @1kHz	70 dB	92 dB
Output Noise (10Hz-100kHz)	40 uV_{RMS}	8.5 uV_{RMS}
Nominal Current	0.5 A	0.25 A
Max Voltage	5.5 V	5.5 V

THE POWER REQUIREMENTS

This design note provides better understanding of design constrains that need to be kept in mind in order to achieve the best NCP156 performance. Some additional non-obvious aspects of NCP156 concept are explained.

The NCP156 is a dual linear regulator optimized for camera sensor applications. It provides power supplies for digital sensor core (DVDD) as well as for analog rail (AVDD). General supply requirements for the digital line are high current, low output voltage (typ. 1.2 V) and as low dropout as possible to maximize efficiency and reduce power dissipation in image sensor array vicinity. Analog supply rail requirements are almost opposite. Currents are lower, voltages are higher (typ. 2.8 V) and the output voltage needs to be very stable and clean. Main parameters are high PSRR over wide frequency range, ultra-low noise and excellent transient response (especially load transient). There is also high pressure to reduce size and cost of the power supply solution, because the camera modules are getting smaller and cheaper themselves. NCP156 offers unique combination of N-MOS and P-MOS linear regulators inside small 6-bumbs WLCSP package. It also reduces the number of external components as much as possible. Figure 1 shows typical application schematic.

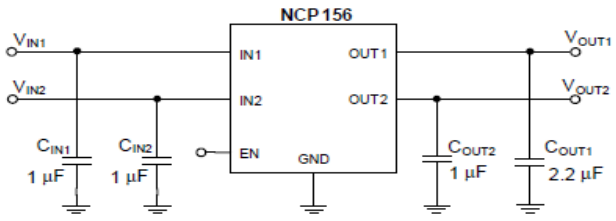

Figure 1. NCP156 Typical application schematic

Picture above shows that only four external capacitors are needed to ensure stable operation. NCP156 provides excellent noise performance (integral noise value as low as 8.5 uV_{rms}) even without additional noise reduction or feedforward capacitors.

As mentioned before NCP156 combines P-MOS and N-MOS regulator which brings certain requirements to supply voltages. N-MOS regulator needs auxiliary voltage to drive the gate of the N-MOS pass transistor well above its output voltage. The auxiliary voltage is generally called “Bias Voltage” or V_{BIAS} for short. Two common topologies are used with N-MOS regulators to deal with the need for V_{BIAS}. First topology uses external bias pin where V_{BIAS} is provided from external source. Second topology relies on internal charge pump for creating bias voltage which is higher enough with respect to output voltage. Both solutions offer certain advantages and disadvantages. In case of NCP156 first option was chosen and bias voltage for N-MOS pass device is provided by V_{IN2} pin. Figure 2 shows internal block diagram of NCP156 with highlighted important power traces.

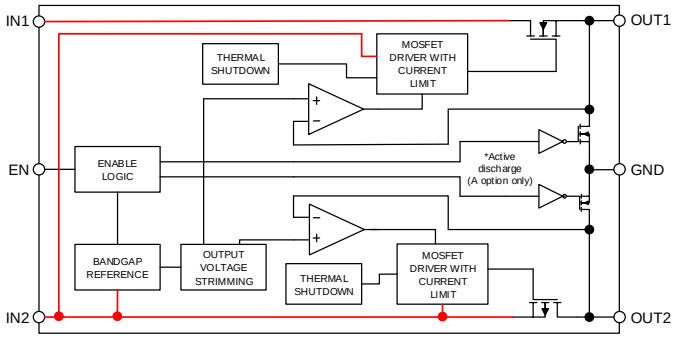

Figure 2. NCP156 internal block diagram

It is obvious from the picture above that pin IN2 is used for powering all internal circuitry such as voltage reference, both pass device drivers etc., while IN1 is connected only to N-MOS pass device drain. That is the key point for selecting IN2 value. Datasheet recommendation for V_{IN2} is following:

V_{IN2} = 2.7 V or (V_{OUT1} + 1.6 V) or ($V_{OUT2(NOM)}$ + 0.3 V) whichever is greater

These conditions are used for device characterization and production testing and guarantee optimal performance of NCP156. Minimum input voltage also specified in datasheet only says that part is working but with no guaranteed parameters. Equation below describes minimal V_{IN2} and it is obvious that part works very close to dropout and some parameters especially PSRR can´t be as good as for higher input voltage.

V_{IN2} = 2.4 V or (V_{OUT1} + 1.5 V) or $V_{OUT2(NOM)}$ + V_{DO} whichever is greater

On the other hand the equation shows first important assumption for designing V_{IN2} power line: **V_{IN2} has to be at least 1.5 V higher than V_{OUT1}** to ensure OUT1 correct function. What this means in reality is that when using NCP156 with output voltages OUT1=1.2 V and OUT2=1.8 V, V_{IN2} needs to be at least 2.7 V to ensure proper function of V_{OUT1}. It can bring some issues with power dissipation for V_{OUT2} and has to be considered before using this part.

Choosing V_{IN2} with respect to V_{OUT2} is much easier and straightforward. There is only one simple condition:

$$V_{IN2} \geq V_{OUT2(NOM)} + V_{DO}$$

To achieve reasonable V_{OUT2} performance, V_{IN2} needs to be at least 0.3V higher than V_{OUT2}.

Suggestions above are relatively clear and obvious but there is one more condition that must be taken into account. It concerns the relation between both output voltages. As shown on internal block diagram on Figure 2 the reference voltages are generated by ***bang-gap reference*** block together with ***output voltage trimming*** blocks. The trimming blocks use standard band-gap voltage 1.25 V to generate two precise reference voltages, which are then translated to the outputs of the device by output drivers in the voltage-follower configuration. Both output voltages are equal to internal reference voltages. Overall process of reference voltages generation can be simplified to figure 3.

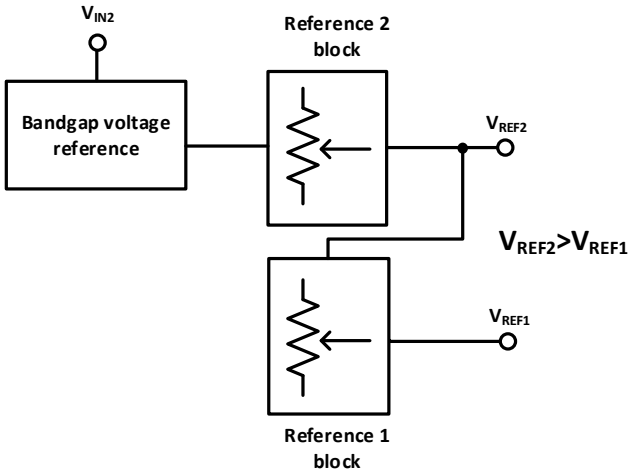

Figure 3. Simplified reference voltage schematic

Reference voltages are generated one after another from the ***Band-gap block***. At first point V_{REF2} is generated directly from band-gap voltage. Then V_{REF1} is derived from V_{REF2}. The main point is that V_{REF2} is always higher than V_{REF1} and any disturbance of V_{REF2} affects V_{REF1} as well. This is the key point to understand what happens with V_{OUT1} if V_{OUT2} goes out of regulation due to low V_{IN2}. When V_{IN2} drops close (approx. 50 mV) to nominal OUT2 voltage then ***Reference 2 block*** doesn't have enough voltage headroom to maintain V_{REF2} and then V_{REF1} drops too and affects V_{OUT1}.

The most important voltage for NCP156 is V_{IN2} which supplies both references and output drivers. V_{IN2} should be held approximately >50 mV above V_{OUT2} to proper function of the whole device.

UNDERSTANDING DROPOUT VOLTAGE

One of the important parameters of linear regulator is the dropout voltage. It defines minimum voltage difference between input and output of the regulator to keep nominal output voltage at specified output current. Generally it is caused by pass device R_{DS_ON} and it is proportional to output current. The N-MOS regulator adds additional dropout parameter V_{DO_BIAS} which determines minimal voltage between regulator output and bias voltage. In case of NCP156 bias voltage for OUT1 is supplied from IN2 pin.

For better understanding, three charts for three dropout parameters are attached to show real NCP156 performance. Data were measured on standard demoboard (Figure 7). For more details about PCB layout and BOM please refer to the appendix.

First chart (Fig. 4) corresponds to dropout voltage of OUT2 at V_{OUT2} = 2.8 V, various temperatures and whole current range. This dropout voltage is a simple difference V_{IN2}-V_{OUT2} when V_{OUT2} drops by 3% below nominal V_{OUT2} (datasheet condition).

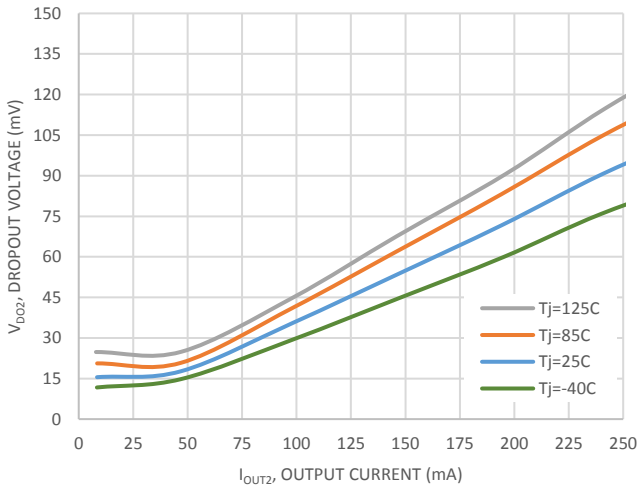

Figure 4. OUT2 Dropout voltage vs. Output current

Next chart covers dropout voltage vs. output current as well, but this time it is measured on OUT1 at V_{OUT1} = 1.2 V, V_{IN2} = 5.5 V, various temperatures and whole current range. The graphs illustrate the biggest advantage of N-MOS regulators which is very low dropout in comparison with P-MOS output transistor. At the same output current the N-MOS provides almost five times lower dropout value with respect to the same die area.

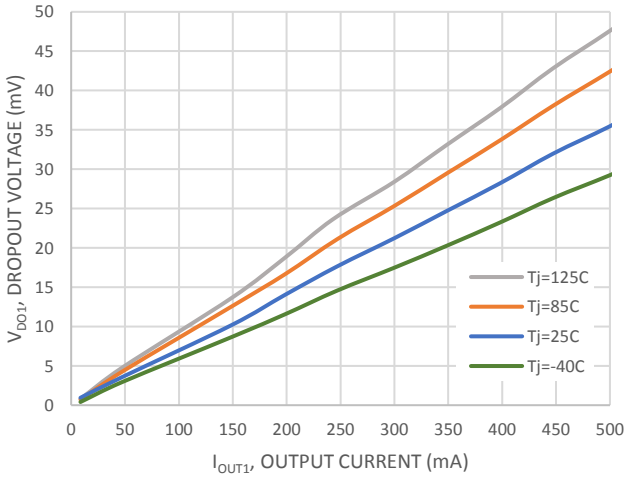

Figure 5. OUT1 Dropout voltage vs. Output current

The last and most difficult to understand is dropout from bias voltage (V_{IN2} in case of NCP156). It means how V_{IN2} affects V_{IN1}-V_{OUT1} dropout. Results are shown in figure 6.

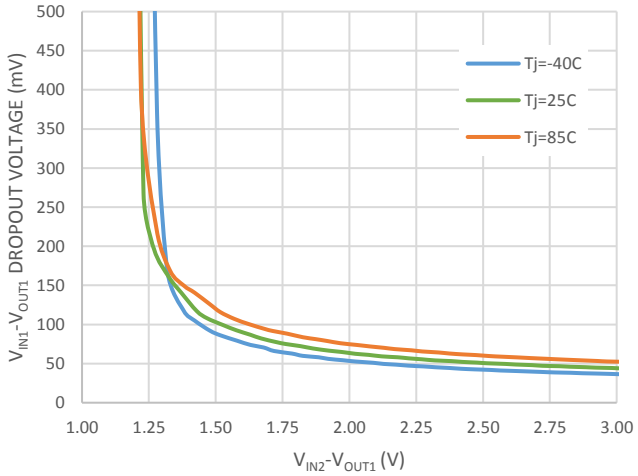

Figure 6. OUT1 Dropout vs. (V_{IN2}-V_{OUT1})

Specification recommends 1.5 V as minimum for V_{IN2}-V_{OUT1} and it is in accordance with figure 6. Decreasing V_{IN2} below this recommended value causes very steep increase in IN1 dropout voltage value (V_{IN1} – V_{OUT1}).

CONCLUSION

Circuit design with NCP156 is simple and when a few basic rules are kept in mind there shouldn't be any issue at all. Above-mentioned recommendations provide basic guide line to achieve good performance and avoid unwanted behavior. Probably the most non obvious thing is that V_{IN2} must be kept high enough with respect to V_{OUT2} to ensure proper V_{OUT1} functionality. This is due to relation between internal reference voltages. The second important thing is considering output voltage combinations. For example combination 1.8 V / 2.0 V is not ideal if V_{OUT2} should supply high steady current (i.e. 250 mA) because minimal V_{IN2} must be at least 3.5 V. Power dissipation only on OUT2 is 400 mW.

The NCP156 is primary designed to power camera module rails where digital DVDD range is 1.0 V-1.2 V and AVDD for pixel array is near to 2.7 V. In such case customer gets high performance and high efficiency of the power solution on small PCB area.

Appendix

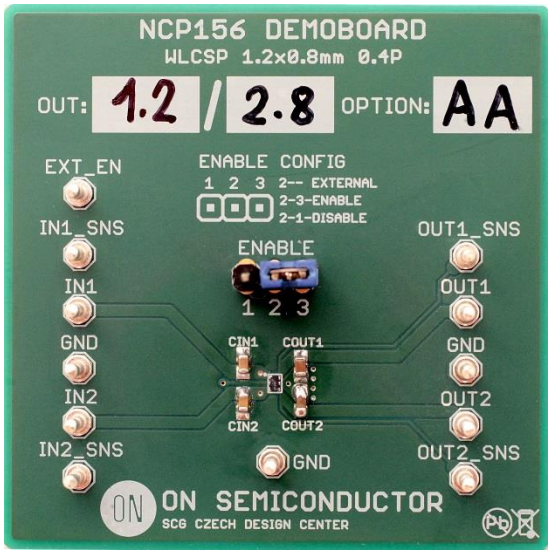

Figure 7. The NCP156 demoboard

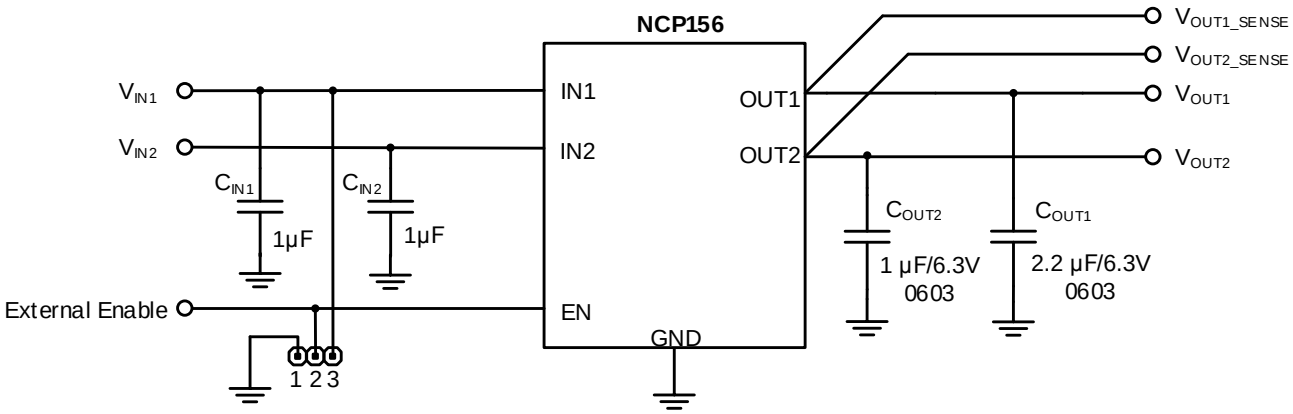

Figure 8. The NCP156 demoboard schematic

Table 1. The NCP156 Demoboard bill of material

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer part no.
C_{IN1}	1	Ceramic capacitor, X7R	1 µF	±10%	0603	Taiyo Yuden	JMK107B7105KA-T
C_{IN2}	1	Ceramic capacitor, X7R	1 µF	±10%	0603	Taiyo Yuden	JMK107B7105KA-T
C_{OUT1}	1	Ceramic capacitor, X7R	2.2 µF	±10%	0603	Taiyo Yuden	JMK227B7105KA-T
C_{OUT2}	1	Ceramic capacitor, X7R	1 µF	±10%	0603	Taiyo Yuden	JMK107B7105KA-T
JP1,2	2	Jumper, 2.54mm	N/A	N/A	2.54 mm	Various	
N/A	1	Dual 300mA LDO	N/A	N/A	WLCSP6 1.2x1.2	ON Semiconductor	NCP156xxFCTxxxxxxT2G
N/A	10	Pin 1.3mm	N/A	N/A	1.3 mm	Various	Various

Design note created by Petr Novobilsky, e-mail: petr.novobilsky@onsemi.com