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DN05041/D

85-115 Vac Buck LED Driver

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DESIGN NOTE

Overview

As LED lighting grows in the general lighting market, cost pressure increases as the volumes grow. Performance is weighted against cost especially for low power applications. LED manufacturers are developing high voltage LEDs whose voltage is more closely matched to the line voltage and thus supports high conversion efficiency with low line ripple.

This makes the CrM buck topology an excellent architecture as an LED driver for the following reasons:

- Low RMS Current Stress on the FET and Output Diode since the Current is Much Lower for the HV LEDs and the Duty Cycle to Relatively High
- Low Current Stress Allows the Use of Smaller FETS and Diodes Leading to Optimum Bill-of-material (BOM) Cost
- Standard Mass Produced Inductors Can also be Used which Further Supports a Cost Effective Design

Key Features

Operation of the NCL30002 CrM controller for buck operation is detailed in AND9094D. While that application note describes how the device can be used to implement a high power factor buck implementation, this design note will describe a low ripple configuration.

Please note the input bulk capacitor was sized to comply with JIS61000−3−2 Class C (Japan), but the same basic design can be used for other lower voltage mains regions like US, Canada, and Latin America for example where that standard does not apply.

The key reason this controller was selected is that it has a very accurate current sense threshold of 485 mV ±2% which is important to achieve good current regulation accuracy.

In addition, in this design the inductor was also the focus of change from the standard implementation to eliminate the need for auxiliary winding for V_{CC} power and ZCD (Zero Current Detector). This allows the designer to use a standard off-the-shelf inductor rather than a custom inductor.

Referencing the schematic, V_{CC} power and ZCD now come from a charge pump driven from the drain of the FET. The charge pump consists of C11, D9, and R12. When the FET turns off, drain current charges C11 providing a pulse of current into the V_{CC} capacitor via D9.

Figure 2 and 3 show some simulations of the charge pump. The 2 noteworthy items from figure 2 are that the current is limited because it is driven by the inductor. Also the drain voltage has well defined rise time which reduces EMI and reduces the trailing edge power losses. At turn on, the FET is fast but turns on into a low current.

Table 1. DEVICE DETAILS

Device	Application	Input Voltage	Output Power	Topology	I/O Isolation
NCL30002	LED Lighting	85 to 115 Vac	3.6 W	CRM Buck	No

Table 2. OTHER SPECIFICATIONS

	Output Specification
Output Voltage	60 V
Nominal Current	60 mA
Harmonic Content	JIS61000−3−2 Class C
Efficiency	86.5% Typical

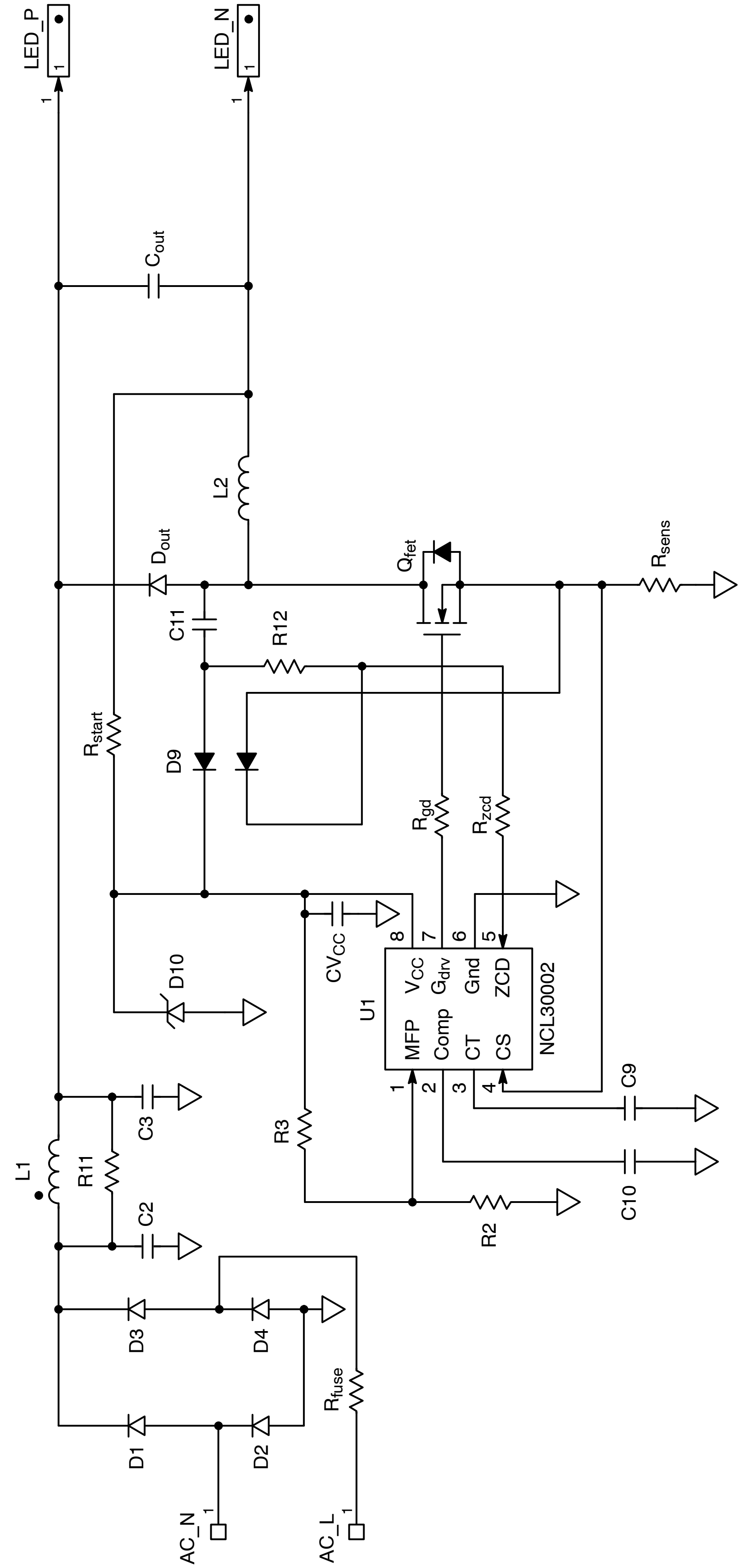


Figure 1. Schematic

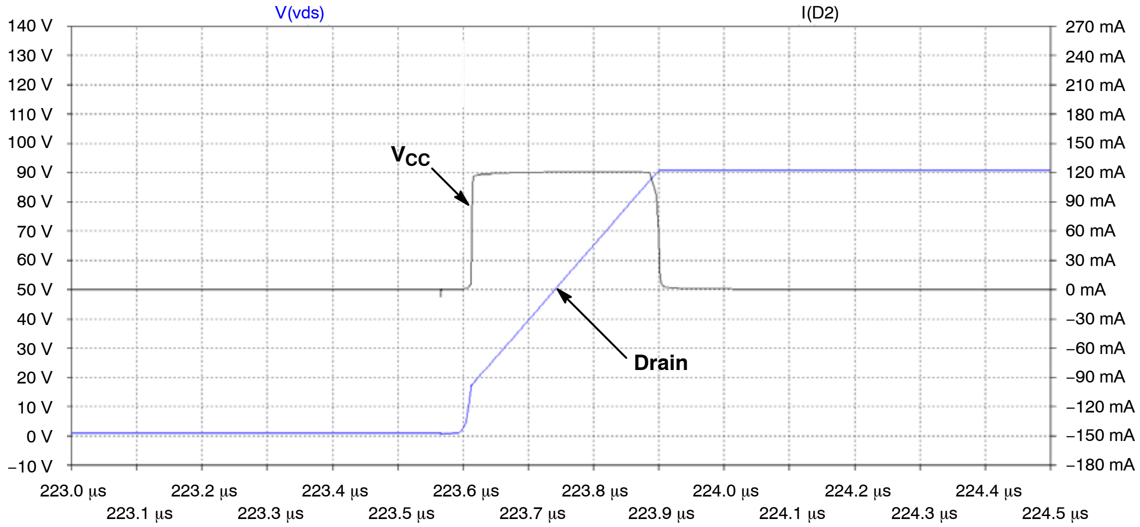


Figure 2. Simulation of Drain Voltage and Charge Current

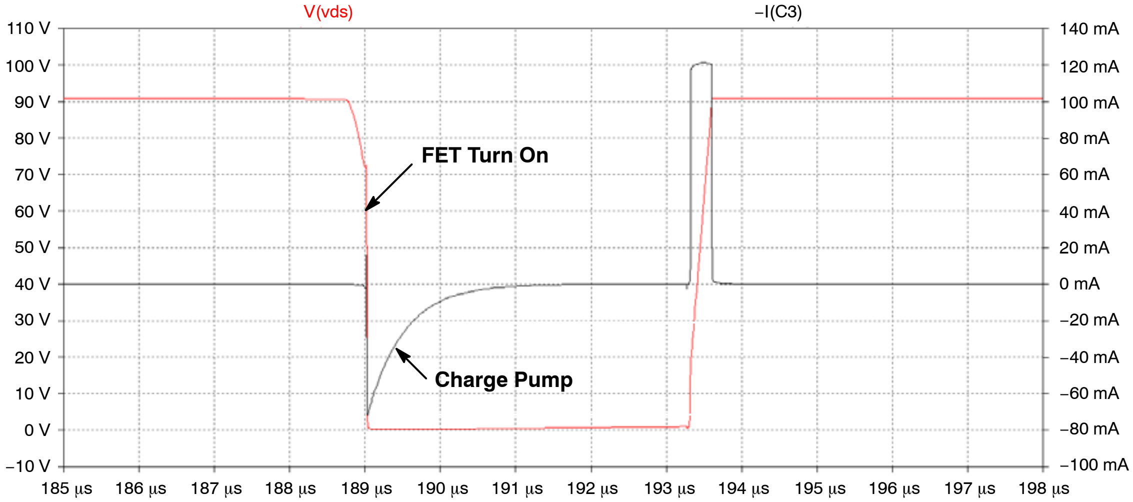


Figure 3. FET Drain Voltage and Charge Pump Capacitor Current

The turn on of the FET discharges the charge pump capacitor through R12. The on time needs to be at least 3RC time constants of C11 and R12 to ensure good discharge. R12 should be chosen to provide the lowest discharge current while still allowing for a complete discharge of C11.

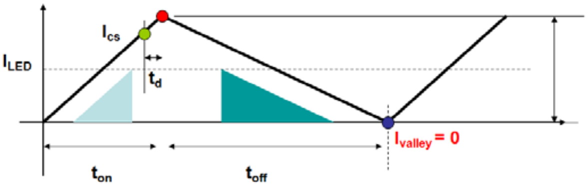
Start-up

The start-up resistor (Rstart) connects to the output. This type of connection has three key advantages:

1. *Fast Start-up:*
   The start-up resistor precharges the output capacitor while also charging the V_{CC} capacitor.
2. *Low dissipation:*
   In operation, the output voltage is much lower than the HVDC bulk voltage.
3. *Inherent open circuit protection:*
   If the load is open, there is no current available to start switching.

Regulation

The NCL30002 controller operates as a peak current limit controller with no feedback. The internal error amplifier is bias by R2 and R3 to saturate the error amplifier output high. The error amplifier input cannot be left open as this is detected as an open feedback divider and the controller will shutdown. The value of the timing capacitor (C9) is chosen to be long enough not to limit the on time.



$$\Delta I = \frac{(V_{in} - V_{LED})}{L} \cdot t_{on} = \frac{V_{LED}}{L} \cdot t_{off} = I_{peak}$$

$$I_{LED} = \frac{I_{peak}}{2}$$

Since this is a CrM control, the peak to average current is 2:1. So by controlling the peak current by choice of R_{sens}, we can control the average current. In any open loop control, there are error sources that show up in the regulation. The two major error sources are:

1. *Propagation Delay in the Sensing and Control:*
   The delays in the current sense cause the current to overshoot the target value resulting in the output current creeping up with the line voltage. This is a relatively linear effect. Higher frequency operation will show this more than low frequency operation.
2. *Charge-pump Operation:*
   The charge pump capacitor causes a delay in rise time of the drain voltage. This effect is more prominent at higher switching frequency which is the case at higher line voltages.

Conclusion

The charge pump buck LED driver is best used in a single line range configuration. The charge pump current increases with frequency and voltage. The nature of CrM operation causes both frequency and voltage to increase together. The charge pump capacitor is sized by the lowest operating voltage (which is also the lowest frequency). As the line voltage increases, excess charge pump current is dissipated in D10. The effect of this is seen in the efficiency curves. The effect on efficiency is most noticed in low power applications. While ±3% regulation is very good over the extremes of a single line range, the addition of feed forward into the current sense node can further improve the line regulation. This requires the addition of 2 resistors R13 and R14 shown in the following schematic.

Table 3. BILL OF MATERIALS

Item	Qty	Reference	Part	Manufacturer	Part Number	Substitution	RoHS
1	1	CV_{CC}	1.0 µF	Panasonic	ECE-A1HKK010	Yes	Yes
2	1	C_{out}	470 nF	TDK	C2012X7S2A474M/SOFT	Yes	Yes
3	2	C2, C3	4.7 µF 200 V	Rubycon	200LLE4R7MEFC6.3X11	Yes	Yes
4	1	C9	10 nF	Kemet	C0402C103K3GACTU	Yes	Yes
5	1	C10	1 nF	Kemet	C0402C102K3GACTU	Yes	Yes
6	1	C11	470 pF	Kemet	C0805C4712GACTU	Yes	Yes
7	1	D_{out}	UFM13PL–TP	MCC	UFM13PL–TP	Yes	Yes
8	1	D4	MB6S	MCC	MB6S	Yes	Yes
9	1	D9	BAS21DW5T1G	ON Semiconductor	BAS21DW5T1G	No	Yes
10	1	D10	NZ9F18VT5G	ON Semiconductor	NZ9F18VT5G	No	Yes
11	1	F1	FUSE	Littelfuse	0263.500WRT1L	Yes	Yes
15	1	L1	100 µH	Wurth	7447462101	Yes	Yes
16	1	L2	2.2 mH	Bourns	RL875S–222K	Yes	Yes
17	1	Q_{fet}	BSS131	Infineon	BSS131 H6327	Yes	Yes
18	1	R_{gd}	10 Ω	Yageo	RC0402FR–0710RL	Yes	Yes
19	1	R_{sens}	2 Ω	Yageo	RC0603JR–072R0L	Yes	Yes
20	1	R_{start}	1.0 MΩ	Yageo	RC0805FR–071ML	Yes	Yes
21	1	R_{zcd}	24.9 kΩ	Yageo	RC0402FR–0724k9L	Yes	Yes
22	1	R2	100 kΩ	Yageo	RC0402FR–07100kL	Yes	Yes
23	1	R3	681 kΩ	Yageo	RC0402FR–07681kL	Yes	Yes
24	1	R12	2 kΩ	Stackpole	RNCP1206FTD2K32	Yes	Yes
25	1	U1	NCL30002	ON Semiconductor	NCL30002	No	Yes

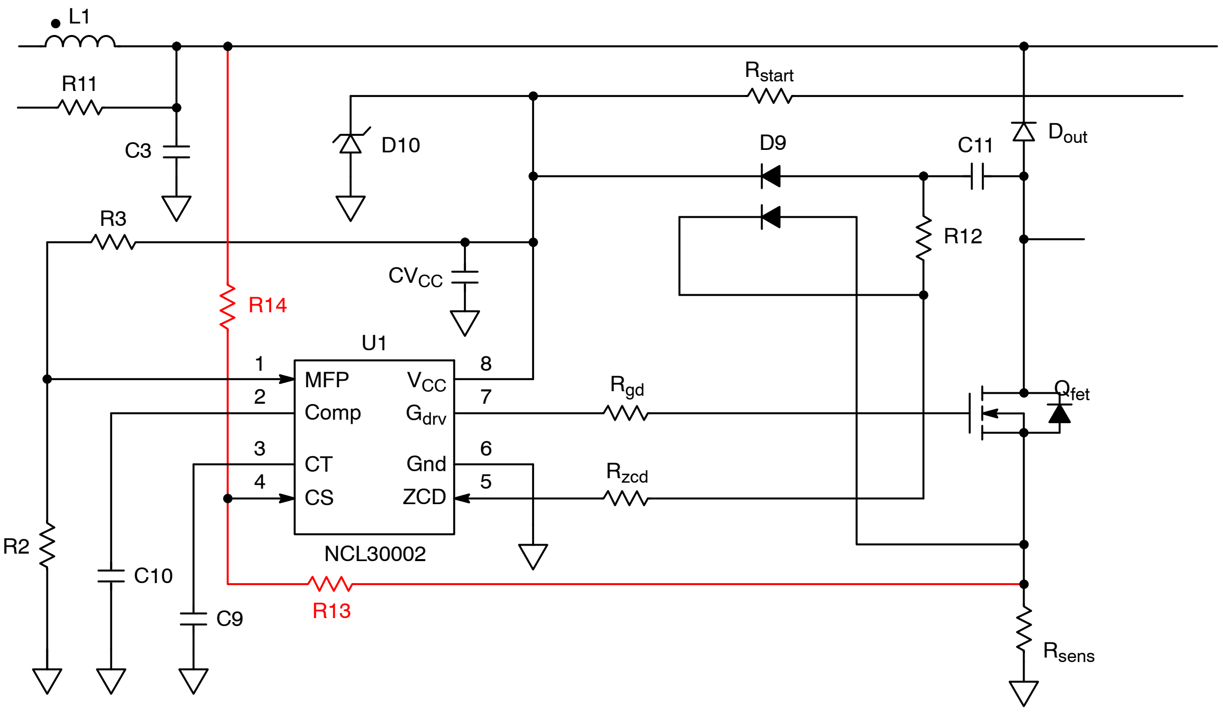


Figure 4. Proposed Line Regulation Feed Forward Improvement

RESULTS

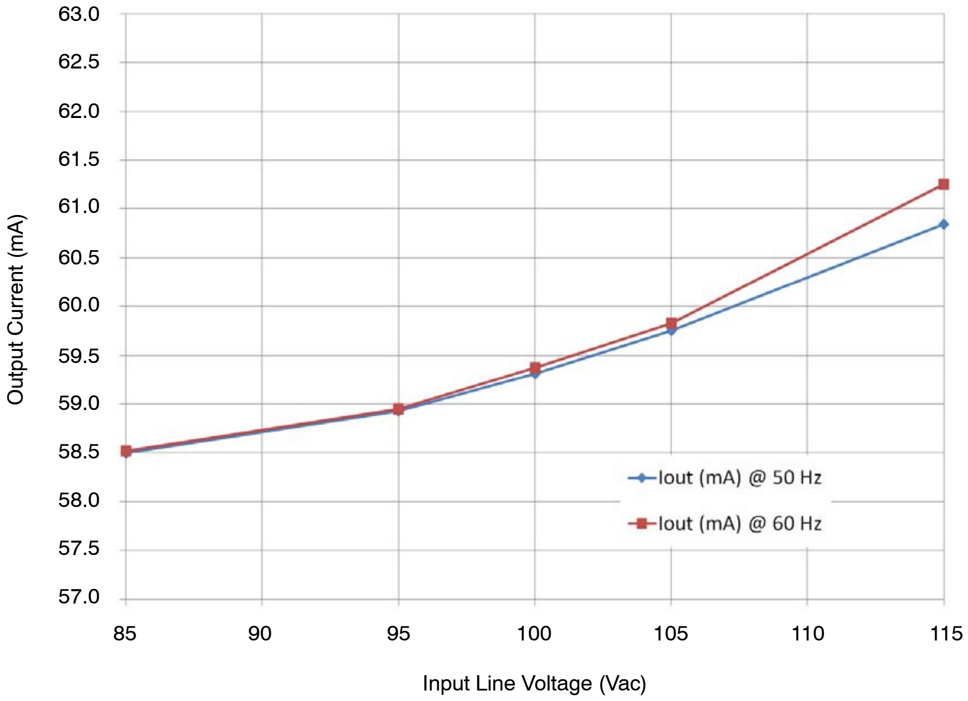


Figure 5. Output Current across Input Line Voltage

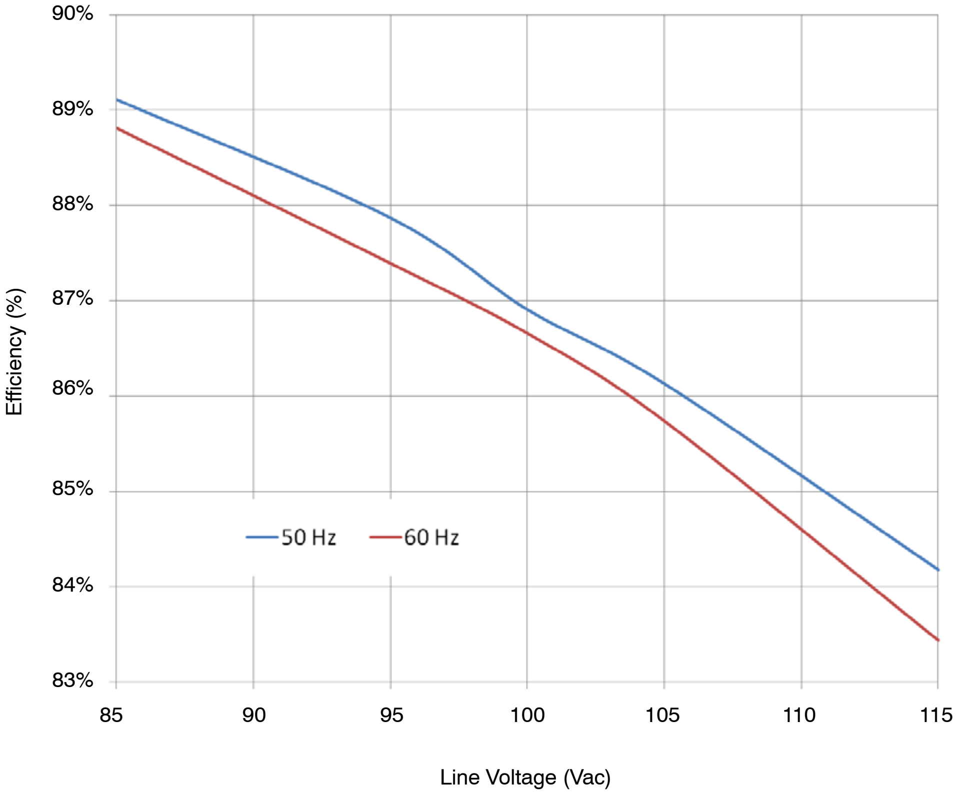


Figure 6. Output Efficiency across Line (V_f = 60 Vdc Nominal)

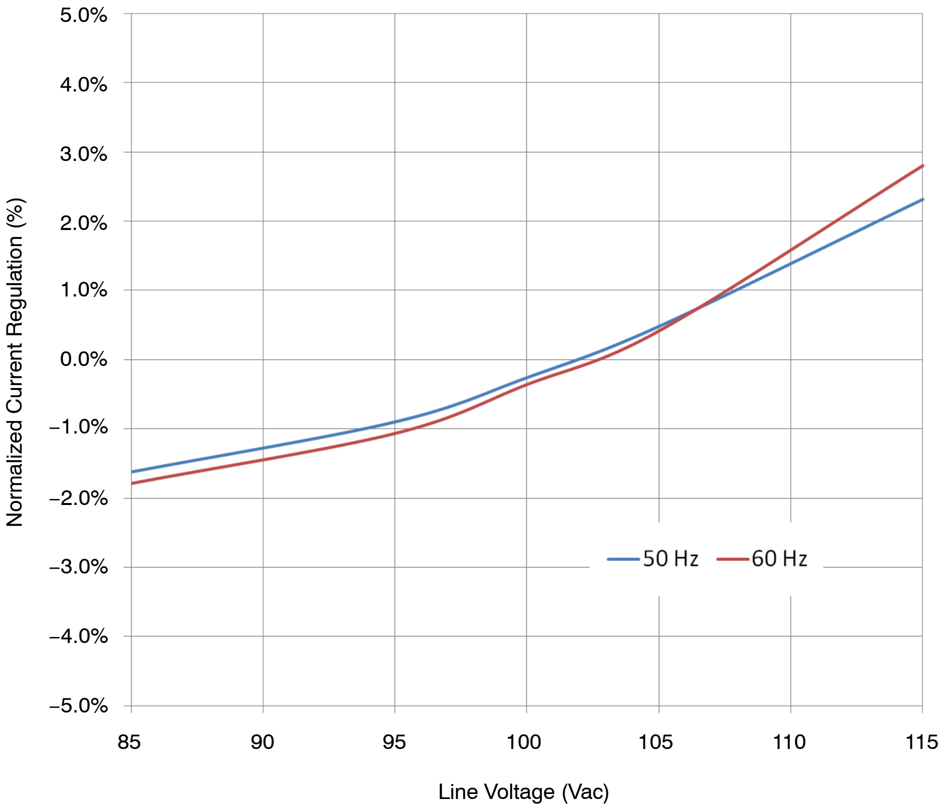


Figure 7. Normalized Output Current across Input Line Voltage (V_f = 60 Vdc Nominal)

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