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Application Note Describing Dual Edge Rails Tuning

ON Semiconductor offers a wide range of voltage regulators for Intel platforms. For multiphase dc-dc solutions dual edge rail architecture is used. This application note discusses the tuning techniques for a dual edge rail.

Dual Edge Rails

The dual edge modulator under discussion in this application note compares the compensated error signal with a number of internally generated interleaved ramps to produce the required PWM duty cycle. The number of ramps is equal to the number of phases per output voltage rail. Dual edge modulation offers advantages such as fast response to load attack and release events, fixed frequency operation allowing for predictable output voltage ripple. The following sections describe tuning of a dual edge voltage rail.

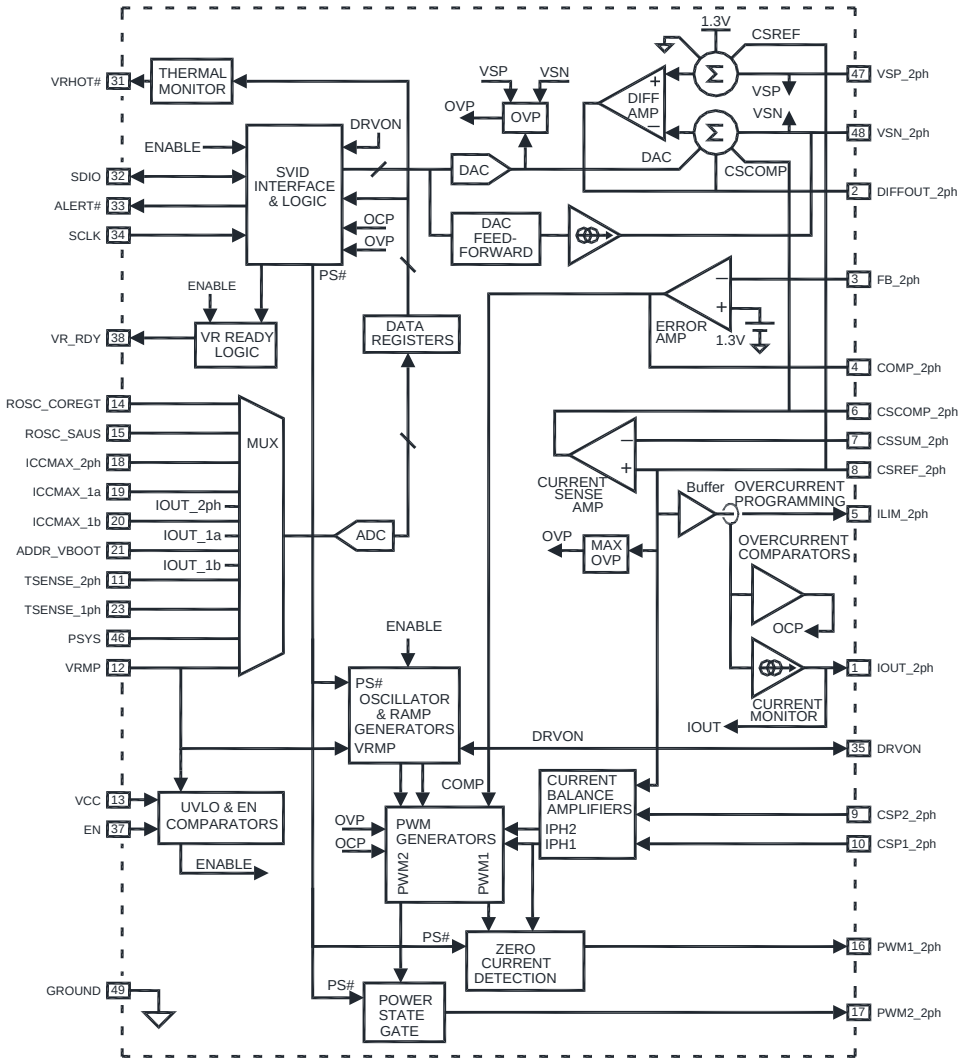

Figure 1: Block Diagram of Dual Edge Architecture

Table 1: Glossary of terms and their values

Name	Description	Value
LL	Loadline	2 mΩ
f_{SW}	Switching Frequency	600kHz
V_{IN}	Maximum input voltage	20V
V_{OUT}	Output voltage	0.9V
V_{ov}	Allowed overshoot	70mV
CCM V_{RIPPLE}	Continuous conduction mode voltage ripple	±10mV
ΔI	Maximum load step	70A
Ilimit	Over current protection trip value	80A
IccMax	Rail maximum current	70A
Np	Number of Phases	3

LC Selection

The selection of output stage components is usually the first step in any VR system design. The inductor and capacitor selection directly influences the maximum output current, output voltage ripple and dynamic performance.

The minimum value for an output inductor required can be estimated by the expression below:

$$L_{\min} \geq \frac{V_0 \times LL}{f_{SW} \times V_{RIPPLE}} \times \left[1 - N_p \times \frac{V_0}{V_{in}}\right] \qquad \text{Eq 1}$$

$$L_{\min} \geq \frac{0.9V \times 2m\Omega}{600kHz \times 20mV} \times \left[1 - 3 \times \frac{0.9V}{20V}\right] = 130nH$$

$L_{selected}$ =220nH

The next step is to estimate the output capacitance required. The selected output capacitance can be a mix of multilayer ceramic capacitors (MLCCs) and electrolytic capacitors.

The value for the required minimum output capacitance can be estimated by the expression below:

$$C_{OUTstarting} = \frac{L_{select} / N_P \times \Delta I}{(LL + \frac{V_{OV}}{\Delta I}) \times V_0} \qquad \text{Eq 2}$$

$$C_{OUTstarting} = \frac{220nH / 3 \times 70A}{(2m\Omega + \frac{70mV}{70A}) \times 0.9V} = 1.9mF$$

Please note C_{OUT} may be higher or lower based on board performance. Dynamic testing needs to be completed to reach the optimum value of C_{OUT}.

Discrete Components Selection for Tuning

Differential Current Balance Amplifier

Inductor DCR current sensing method is used to extract accurate per phase current information. For this purpose RCSN and CCSN is connected in parallel to the inductor as shown in Figure 2 below:

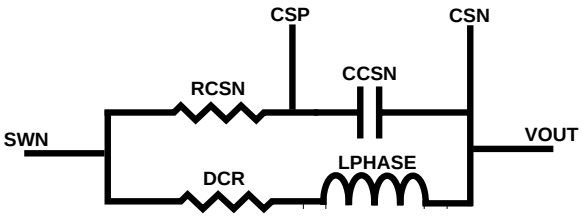

Figure 2: DCR current Sensing

Ensure that the CCSN chosen is in the range of 20nF to 470nF, while keeping the RCSN above 2kΩ. Thus, the expression for RCSN can be written as

$$RCSN = \frac{L_{PHASE}}{CCSN \times DCR} \quad \text{Eq 3}$$

Select C_{CSN}=0.033µF and by using above expression the value of R_{CSN} can be calculated as follows:

$$R_{CSN} = \frac{0.22\mu H}{0.033\mu F \times 2.76m\Omega} = 2.415k\Omega$$

Total Current Sense Amplifier

The currents from all phases are summed together in a single temperature compensated total current signal.

The R_{ref} resistors average the voltages at the output sides of the inductors to create a low impedance reference voltage CSREF. The R_{PH} are use to set the gain of the current sense (CS) amplifier and influence the loadline. Figure 3 below is showing an example of a two phase current sense amplifier.

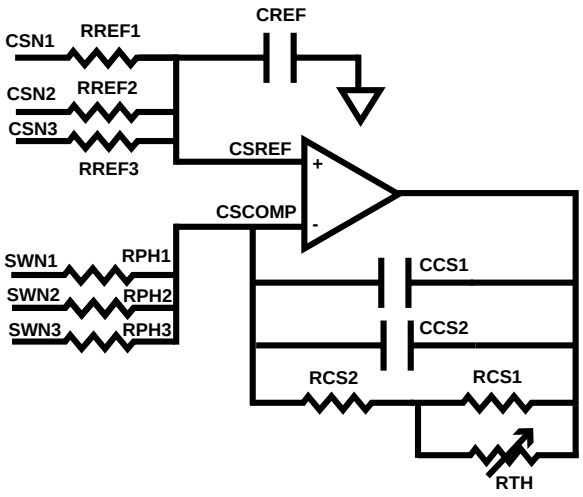

Figure 3: A typical Total Current Sense Amplifier

The DC equation for the current sense is

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1 * Rth}{Rcs1 + Rth}}{Rph} * (Iout_{Total} * DCR) \quad \text{Eq 4}$$

Taking V_{cscomp}-V_{csref} divided by Iout gives the resulting load line of the rail as follows:

$$LL = \frac{R_{CS}}{R_{Ph}} \times DCR \quad \text{Eq 5}$$

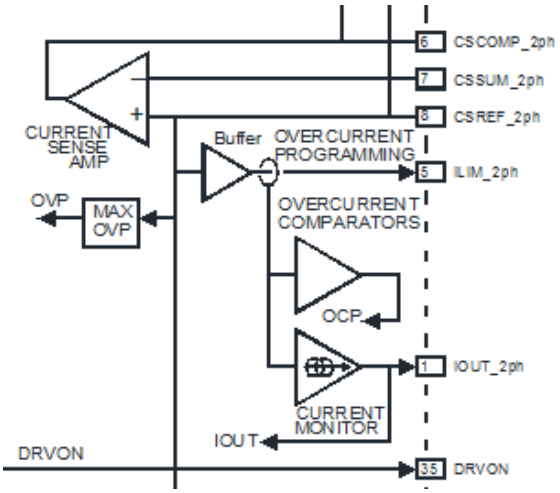

Figure 4: Section of Block Diagram showing CS Amplifier block

It is recommended to choose Rcs = 220kΩ and then calculate R_{CS1}, R_{CS2} and R_{TH} as described in the next section and then solve for Rph(x).

DCR Temperature Compensation

An NTC Thermistor (R_{TH}) is placed in the feedback network of total current sense amplifier. The thermistor must be placed near the phase 1 inductor to sense the inductor temperature and compensate both the DC gain and the filter time constant for the DCR change with temperature. The values of R_{CS1} and R_{CS2} are set based on the effect of temperature on both the thermistor and inductor.

The following procedure and equations will give rise to the values of R_{CS1}, R_{CS2} and R_{TH} (at 25°C)

1) Select an NTC thermistor close to selected R_{CS}. In this case an NTC value of 220kΩ is chosen.

2) The next step is to calculate the relative resistance of the selected thermistor at two temperatures. The temperatures that were chosen in this case are 50°C and 90°C. Calculate the relative resistance ratios A and B as follows:

$$A = \frac{R_{TH(50^0C)}}{R_{TH(25^0C)}} = \frac{68.411}{220} = 0.311$$

$$B = \frac{R_{TH(90^0C)}}{R_{TH(25^0C)}} = \frac{13.962}{220} = 0.0634$$

From the thermistor datasheet that is selected A and B can be calculated as 0.311 and 0.0634 respectively

3) Find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage temperature change needed, which is initially 0.39% /°C. These are called r_1 and r_2 respectively and can be calculated as follows:

$$r_1 = \frac{1}{1 + TC \times (T_1 - 25^0C)} \quad r_2 = \frac{1}{1 + TC \times (T_2 - 25^0C)}$$

Where T_1 =50°C, T_2 =90°C, TC=0.0039°C^{-1}

Substituting above values and the values of r_1 and r_2 can be calculated as 0.9112 and 0.7978 respectively.

The relative values for R_{CS1}, R_{CS2} and R_{TH} are called r_{CS1}, r_{CS2} and r_{TH} respectively. These values are calculated by using the expressions below:

$$r_{CS2} = \frac{(A-B)r_1r_2 - A(1-B)r_2 + B(1-A)r_1}{A(1-B)r_1 - B(1-A)r_2 - (A-B)}$$

$$r_{CS1} = \frac{(1-A)}{\frac{1}{1-r_{cs2}} - \frac{A}{r_1 - r_{cs2}}} \qquad r_{TH} = \frac{1}{\frac{1}{1-r_{cs2}} - \frac{1}{r_{cs1}}}$$

The values of r_{CS1}, r_{CS2} and r_{TH} are calculated 0.738933, 0.340444 and 1.120791

4) Calculate the required value of R_{TH} by using the expression below:

$$R_{TH} = r_{TH} \times R_{CS} = 246.1k\Omega$$

The closest value to 246.574kΩ is 220kΩ. Therefore, we select a NTC Thermistor of value 220kΩ.

5) Compute a scaling factor k based on the ratio of the actual thermistor used relative to the calculated ideal.

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} = 0.894$$

6) The value of R_{CS1} and R_{CS2} can be calculated by using equations below:

$$R_{CS1} = R_{CS} \times k \times r_{cs1}$$
$$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{cs2}))$$

The calculated values of Rcs1 & Rcs2 are 66.81kΩ and 168.3kΩ respectively. Finally we can select the closest standard resistor values for R_{CS1}=75kΩ and R_{CS2}=165kΩ.

Loadline Programming

The gain of the total current sense amplifier is decided by the ratio of R_{CS} and $R_{PH.}$ The value of R_{CS} can be calculated as follows:

$$R_{CS} = R_{CS2} + \frac{R_{CS1} \times R_{TH}}{R_{CS1} + R_{TH}} \qquad \text{Eq 6}$$

Substituting RCS1=75kΩ, R_{CS2}=165kΩ and R_{th}=220kΩ the calculated value of R_{CS} =220.932kΩ. The corresponding value of RPH=304.88kΩ can be calculated by using the expression below:

$$R_{PH} = \frac{R_{CS}}{LL} \times DCR = \frac{220k\Omega}{2m\Omega} \times 2.76m\Omega = 304k\Omega$$

Eq 7

CCS Calculation

The total current signal is proportional to the component of inductor voltage caused by DCR drop and consequently relative to inductor current. Connecting C_{CS2} in parallel with C_{CS1} allows fine tuning of the pole frequency. It is recommended to fine tune this filter frequency during transient testing. The expression for the calculation of CCS is as follows:

$$C_{CS} = \frac{L}{DCR \times R_{CS}} \qquad \text{Eq 8}$$

$$C_{CS} = \frac{220nH}{2.76m\Omega \times 220k\Omega} = 362\,pF$$

Over Current Protection

The current limit of the converter is programmed with a resistor R_{ILIM} between the ILIM and CSCOMP pins. The expression for the setting of Rilim is as follows:

$$R_{ILIM} = \frac{\frac{R_{CS}}{R_{PH}} \times (I_{OUT} \times DCR)}{10\mu A} \qquad \text{Eq 9}$$

The maximum current limit is 80A.

$$R_{ILIM} = \frac{\frac{220k\Omega}{304k\Omega} \times (80A \times 2.76m\Omega)}{10\mu A} = 16k\Omega$$

RIOUT Selection

The IOUT pin sources a current equal to 10 times the ILIM sink current. A resistor to ground on the IOUT pin converts this current to a voltage. R_{IOUT} should be scaled such that a load current equal to the rail max current generates a 2V signal.

$$R_{IOUT} = \frac{2 \times R_{ILIM}}{10 \times (\frac{R_{CS}}{R_{PH}} \times DCR) \times I_{OUT\,max}} \qquad \text{Eq 10}$$

R_{IOUT} is calculated as follow for an IOUT max of 70A:

$$R_{IOUT} = \frac{2V \times 16k\Omega}{10 \times (\frac{220k\Omega}{304k\Omega} \times 2.76m\Omega) \times 70A} = 22.8k\Omega$$

A capacitor (C_{IOUT}) is selected to filter output ripple current information from the Iout reading but must not be so large that it significantly increases the settling time of the IOUT reading. The C_{IOUTSP} chosen for this case is 470pF.

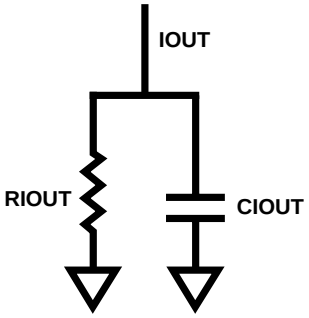

Figure 5: RIOUT Network

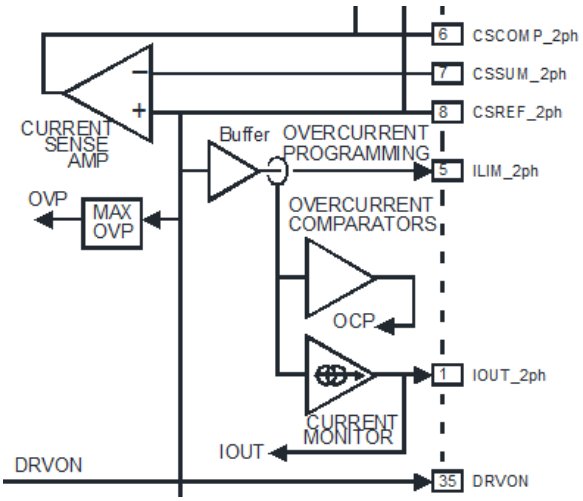

Figure 6: Section of Block Diagram showing ILIM and IOUT block

DAC Feed Forward Programming

DAC feed-forward is used to aid the output voltage in tracking the internal DAC during VID up transitions. The DAC feed-forward implementation is realized by having a filter on the VSN pin. Programming RFF sets the gain of the DAC feed-forward and CFF provides the time constant to cancel the time constant of the system per the following equations.

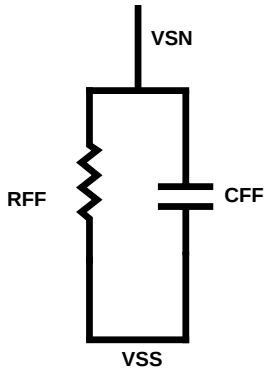

Figure 7: DAC Feed Forward Filter

$$R_{FF} = C_{OUT} * LL * 453.6 \times 10^{6} \quad \text{Eq 11}$$

$$C_{FF} = \frac{LL * Cout}{R_{FF}} \quad \text{Eq 12}$$

Using Eq 11 and Eq 12 to calculate component values:

$$R_{FF} = 1.9mF * 2m\Omega * 453.6 \times 10^{6} = 1.72k\Omega$$

$$C_{FF} = \frac{2m\Omega * 1.9mF}{1.72k\Omega} = 2.2nF$$

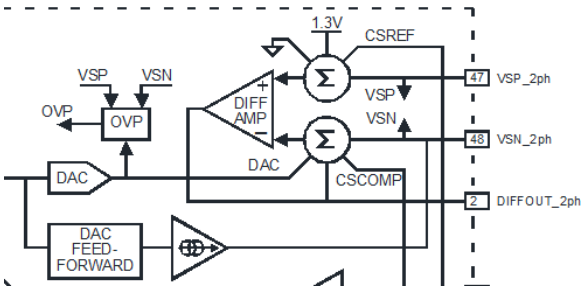

Figure 8: Section of Block Diagram DAC feed forward block

Voltage Compensation

The block diagram of feedback Control Loop for a buck converter is shown below:

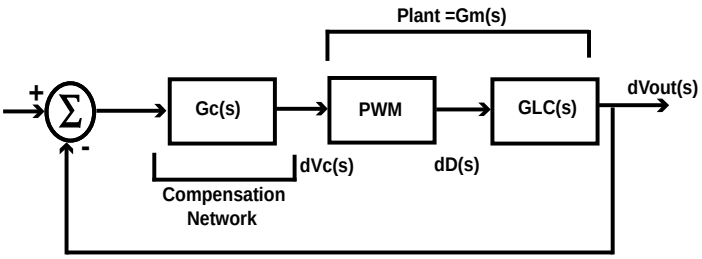

Figure 9: Block Diagram of a Control System

The PWM and output filter stages are grouped together as the plant (modulator) $G_m(s)$. The compensation network transfer function is $G_c(s)$. The open loop transfer functions of the output Vout with respect to duty cycle D(s) can be written as follows:

$$\frac{dV_{out}(s)}{dD(s)} = V_{in} \frac{sR_{ESR}C_{out} + 1}{s^2 LC_{out} + s\left[\frac{L}{R_0} + C_{out}(DCR + R_{ESR})\right] + 1} \quad \text{Eq 13}$$

R_{ESR} = ESR of output capacitor C, L = Inductance of output inductor, C_{OUT}= Output capacitance, R_0=output load

There will be two poles and one zero in the above transfer functions. The poles are created by the resonance of LC output filter while the zero is created by the ESR of the output caps. The double poles are located at

$$f_p = \frac{1}{2\pi\sqrt{L_n C_{OUT}}} \quad \text{Eq 14}$$

Where $L_n = \frac{L}{n}$ and n= number of phases. The zero is located at

$$f_0 = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad \text{Eq 15}$$

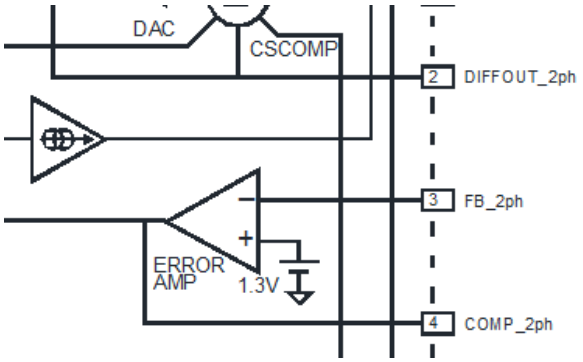

Figure 10: Section of Block Diagram showing voltage compensation block

Type III compensation is used optimize the response of the VR. This network provides a pole at the origin with two poles and two zeros.

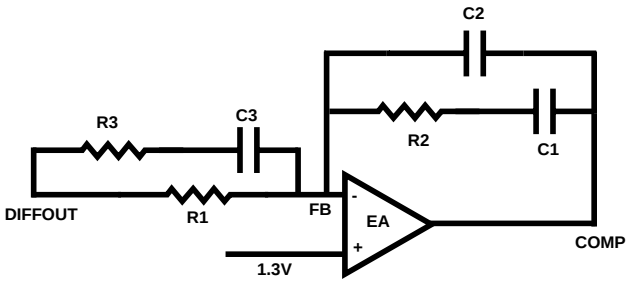

Figure 11: Type III compensator

The open loop transfer functions of the output Vout with respect to compensation network $V_C(s)$ can be written as follows:

$$\frac{dV_{out}(s)}{dV_C(s)} = \frac{V_{IN}}{V_M} \frac{sR_{ESR}C_{OUT}+1}{s^2LC_{out}+s\left[\frac{L}{R_0}+C_{OUT}(DCR+R_{ESR})\right]+1}$$

Substituting $V_M=V_{IN}/10$

$$\frac{dV_{out}(s)}{dV_C(s)} = 10\times\frac{sR_{ESR}C_{OUT}+1}{s^2LC_{OUT}+s\left[\frac{L}{R_0}+C_{OUT}(DCR+R_{ESR})\right]+1} \quad \text{Eq 16}$$

Example: f_C=120 kHz, L=220n H, N_p=3, DCR=2.76mΩ, C_{out}=1.9m F, R_0=10kΩ, R_{ESREQ}= 30μΩ, M=Desired Phase Margin=75°

The basic steps to synthesize a type III compensation network are as follows:

1) Choose a cross over frequency and determine the plant gain G_M at the cross over frequency, f_C

$$G_m = 10\times\frac{2\times\pi\times f_C\times R_{ESREQ}C_{OUT}+1}{(2\times\pi\times f_C)^2L_nC_{OUT}+(2\times\pi\times f_C)\left[\frac{L_n}{R_0}+C_{OUT}(DCR_{EQ}+R_{ESREQ})\right]+1}$$

Substituting the values in the above expression gives

G_m=0.128

2) Determine the LC double pole and ESR zero frequencies f_P and F_Z using Eq14 and Eq15 respectively.

$$f_p = \frac{1}{2\pi\sqrt{L_nC_{out}}} = \frac{1}{2\pi\sqrt{\left[\frac{220nH}{3}*1.9mF\right]}} = 13.5kHz$$

$$f_z = \frac{1}{2\pi R_{ESREQ}C_{out}} = \frac{1}{2\pi\times30\mu\Omega\times1.9mF} = 2.79.MHz$$

3) Determine the plant Phase shift P_m in degrees at f_C using the expression below:

$$P_m = \left[Tan^{-1}\left(\frac{f_C}{f_Z}\right)-2Tan^{-1}\left(\frac{f_C}{f_P}\right)\right] \quad \text{Eq 17}$$

Substituting the values in the above expression to calculate plant phase shift gives:

$$P_m = \left[Tan^{-1}\left(\frac{120kHz}{2.79MHz}\right)-2Tan^{-1}\left(\frac{120kHz}{13.5kJz}\right)\right] = -164.7^0$$

4) Determine the required compensation network gain G. The gain G is the required compensation gain at f_C and must be equal to the plant attenuation. Substituting the value of G_m gives the value of required compensator gain as:

$$G = \frac{1}{0.128} = 7.8125$$

5) Choose the desired phase margin (75°) at f_C. Calculate the required phase boost by using expression below:

$$\theta_{boost} = M - Pm - 90^0 \qquad \text{Eq 18}$$

Substituting the values in the above expression gives phase boost as follows:

$$\theta_{boost} = 75^0 + 165^0 - 90^0 = 149.7^0$$

6) Determine the K value as follows:

$$K = \tan^2\left[\frac{\theta_{boost}}{4} + 45^0\right]$$

Substituting the values in the above expression gives K as follows:

$$K = \tan^2\left[\frac{150^0}{4} + 45^0\right] = 56.6$$

7) Choose a value of R_1 between 500Ω and 1kΩ. Selecting R_1=1kΩ and calculate the values of the components using the K-factor approach expressions below:

$$R_2 = \frac{\sqrt{K}}{K-1} GR1 = 1.06k\Omega$$

$$R_3 = \frac{R_1}{K-1} = 18\Omega$$

$$C_1 = \frac{K-1}{2\pi f_C G R_1} = 9.44nF$$

$$C_2 = \frac{1}{2\pi f_C G R_1} = 170\,pF$$

$$C_3 = \frac{1}{2\pi f_C G R_1} . \frac{K-1}{\sqrt{K}} = 1.26nF$$

IccMax Setting

On startup a resistor to ground on the IccMax pin programs the IccMax register value (for details regarding IccMax please consult the relevant datasheet). The value of the register is 1A per LSB. The exact expression of IccMax can be found in the relevant datasheets

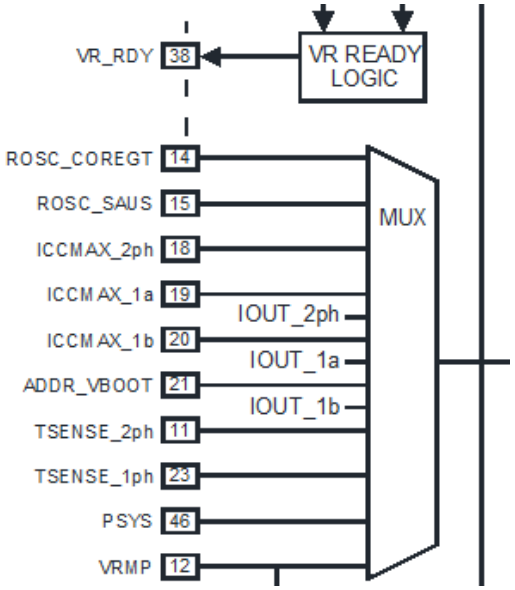

Figure 12: Section of Block showing ICCmax & Tsense block

TSENSE Network Tuning

A temperature monitoring input is provided by the Tsense pin. The voltage on the temperature sense input is sampled by the internal ADC. See the specification table for the thermal sensing voltage thresholds and source current in the corresponding datasheets.

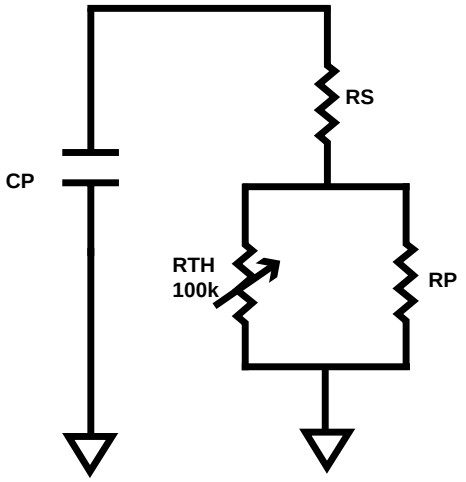

Figure 13: Tsense Network

The steps for the calculation of Tsense network is as follows:

1. Select VR_HOT and ALERT assert threshold voltages form the datasheet.
2. Convert the threshold voltages in the datasheet to resistor values using I_{bias} current from the datasheet as R_1 and R_2.
3. Select two target temperatures T_1 and T_2 and calculate NTC resistance values at those temperatures as R_{n1} and R_{n2} using expression below:

$$R_{nx} = R_{NTC} \times e^{\beta(\frac{1}{T_x} - \frac{1}{T_0})} \quad \text{Eq 19}$$

T_X= Selected temperature in Kelvin

T_0= Room temperature in Kelvin

4. Calculate the value of A,B and C as follows:

$$A = (R_{n1} + R_{n2}) - (R_{n2} + R_1) \quad \text{Eq 20}$$
$$B = (R_2 - R_1) \times (R_{n1} + R_{n2}) \quad \text{Eq 21}$$
$$C = (R_2 - R_1) \times (R_{n1} \times R_{n2}) \quad \text{Eq 22}$$

5. Calculate the value of R_P using the expression below:

$$R_P = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \quad \text{Eq 23}$$

6. Calculate the value of Rs using the expression below:

$$R_S = R_1 - \frac{R_{n1} R_P}{R_{n1} + R_P} \quad \text{Eq 24}$$

Example:

For I_{bias}=120µA, VR_Hot threshold=468m V, Alert threshold=488m V the values of R_1 and R_2 can be calculated as:

R_1=3.9kΩ, R_2=4.066kΩ

For T_1=104˚C, T_2=100˚C, T_0=25˚C, R_{NTC}=100kΩ and ß=4250 the values of R_{n1} and R_{n2} can be calculated as:

R_{n1}=5.049 kΩ, R_{n2}=5.698kΩ

Using Eq 23 R_P can be calculated as:

R_P= 5.52kΩ

Using Eq 24 R_S can be calculated as:

R_S= 1.26kΩ

7. The recommended value of C_P is 0.1µF.

Conclusion

The equations discussed previously are given to aid the platform designer to select the compensation and configuration components for use with ON Semiconductor's multiphase VR controller. An overall example of schematic block diagram is shown in Figure 14 below:

Dual Edge Rails Tuning

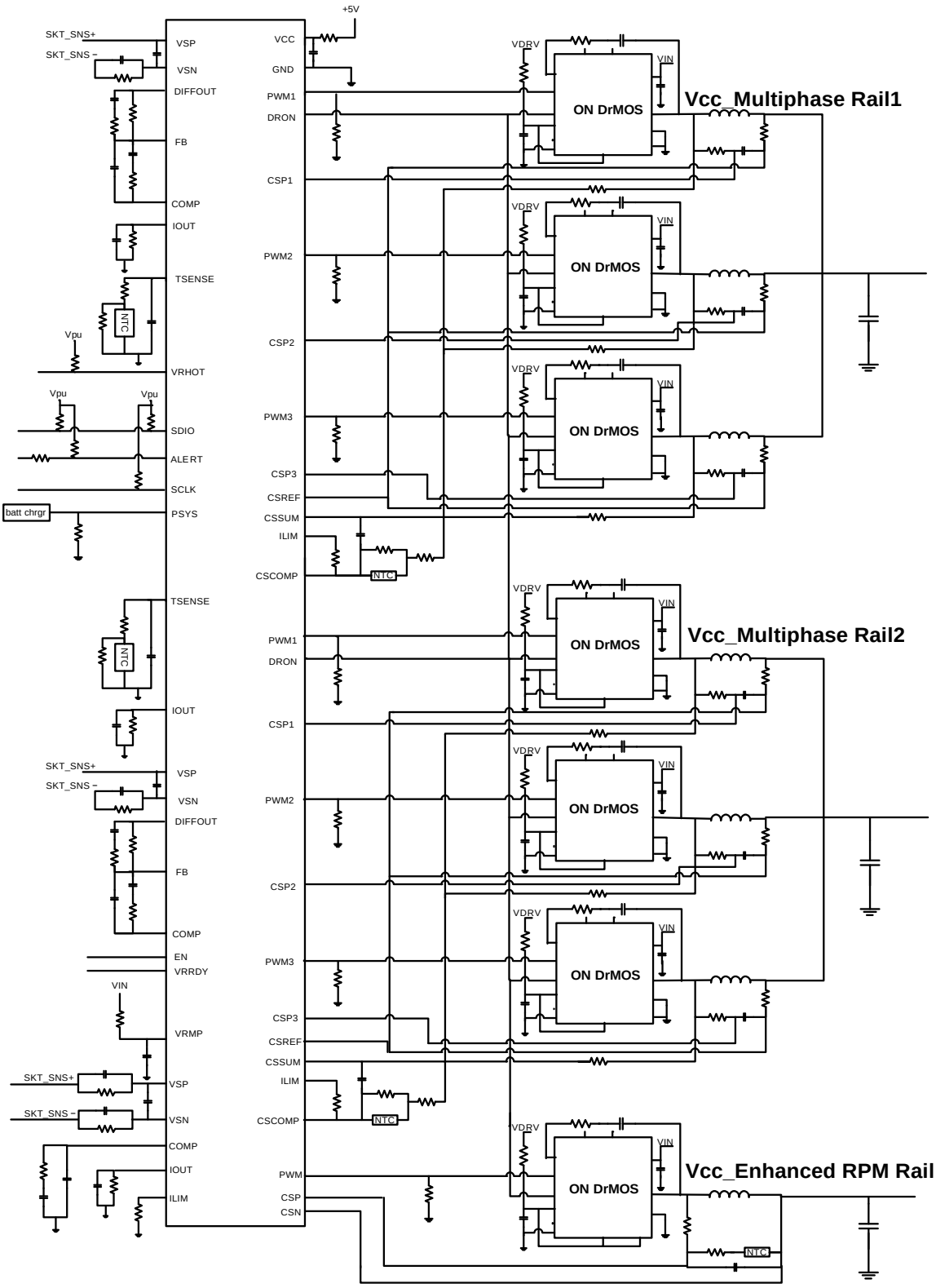

Figure 14: Rails schematic Block Diagram