LV8121V

Three-phase Brushless Motor Driver IC Application Note

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Overview

The LV8121V is a three-phase brushless motor driver that uses a PWM drive technique. The motor speed is controlled by changing the PWM duty that based on an analog voltage input. The motor driver includes an automatic return constraint protection circuit and is optimal for driving fan motors.

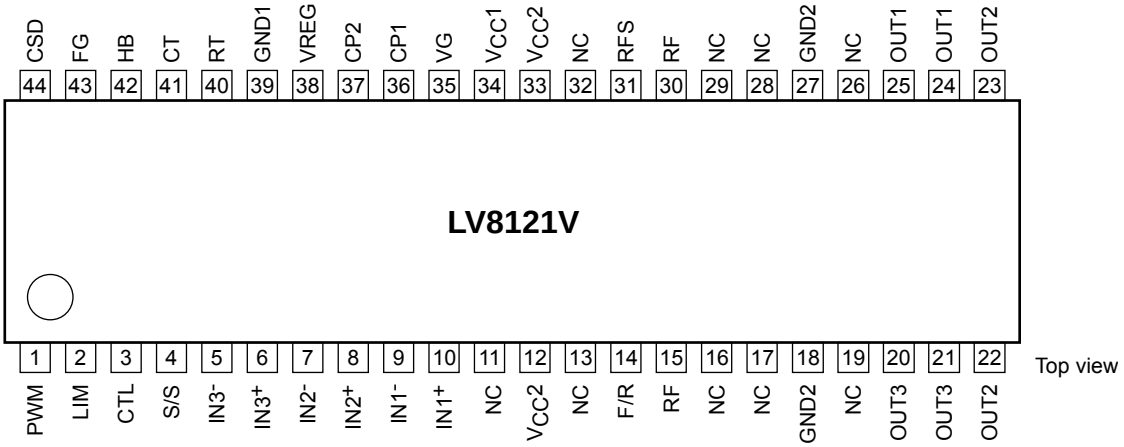
Features

- PWM control based on an analog voltage input (the CTL voltage), synchronous rectification
- One Hall-effect sensor FG output
- Automatic return constraint protection circuit (ON/OFF=1/15)
- Start/Stop switching circuit, Forward/Reverse switching circuit
- Current limiter circuit, Low-voltage shutdown protection circuit, Thermal shutdown protection circuit

Typical Applications

- Fan motors for Consumer electronics
- Pump motors for Hot water heaters

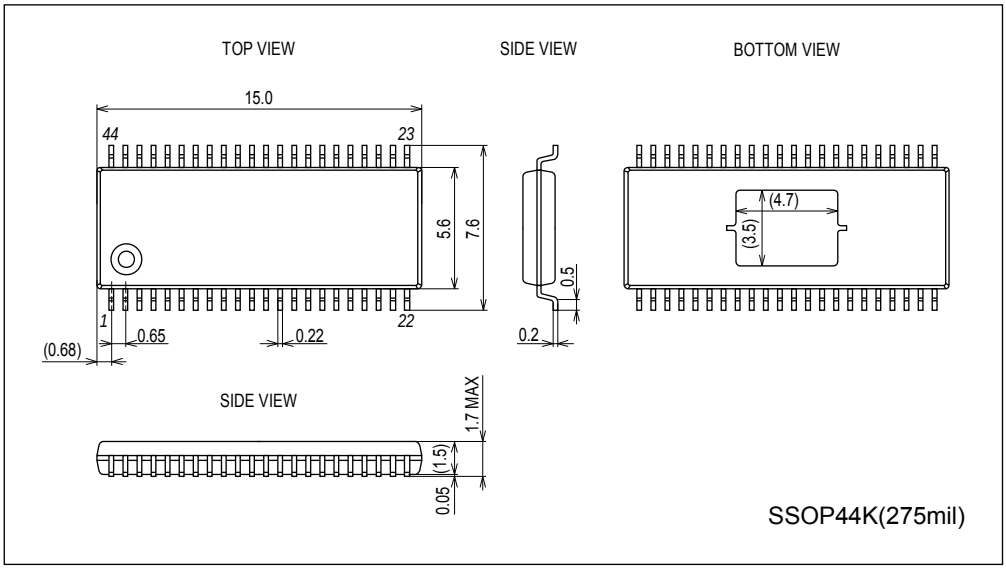
Pin Assignment



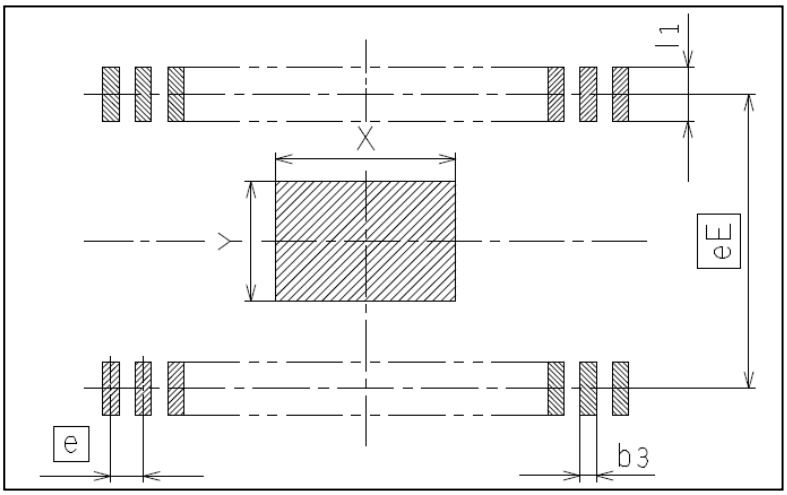
Top view

Package Dimensions

unit : mm (typ)
3333A



Mounting Pad Sketch

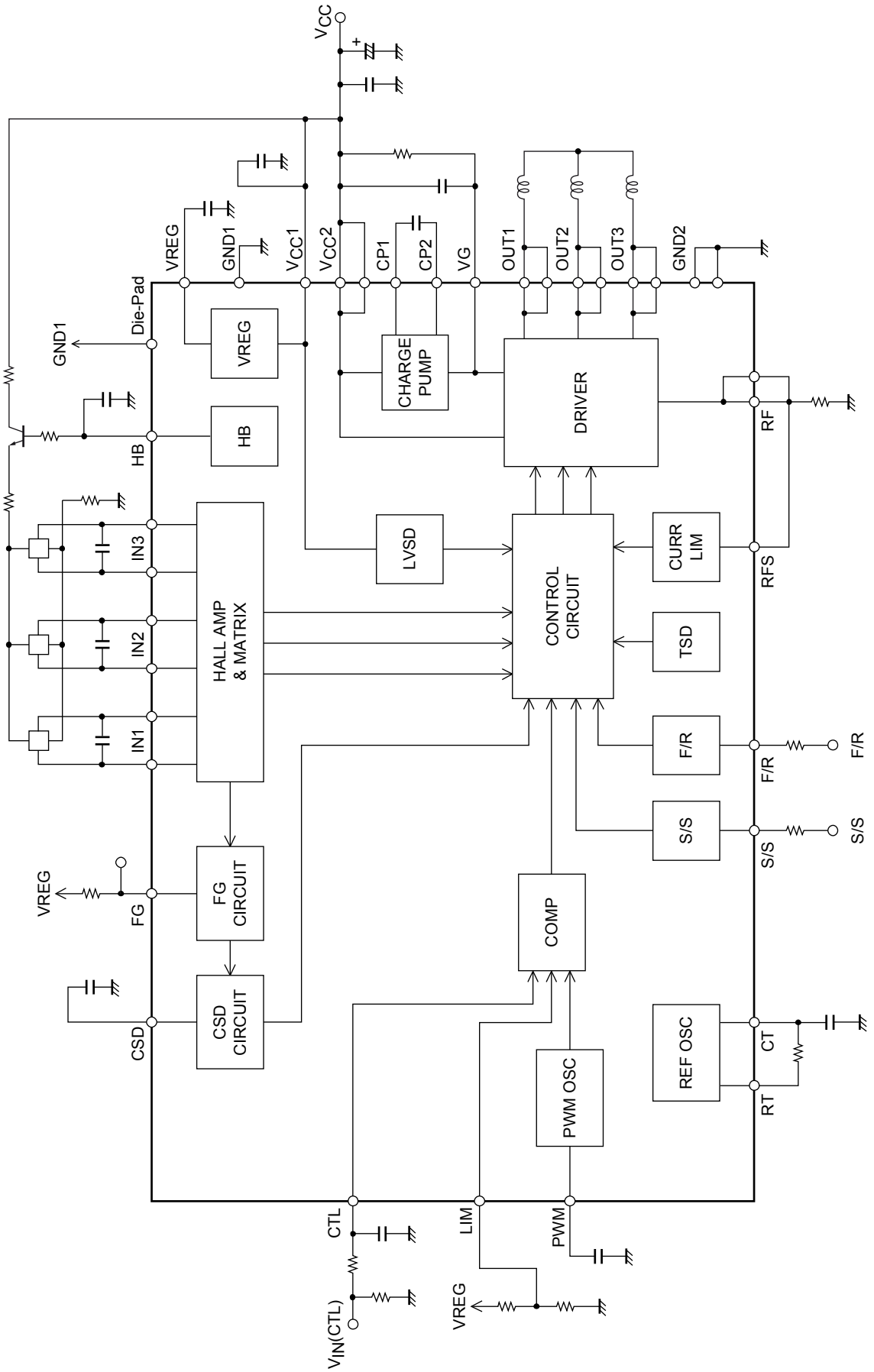


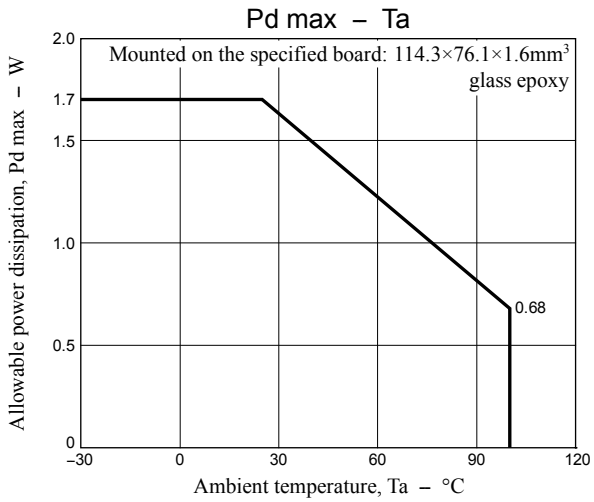
(Unit: mm)

Reference symbol	SSOP44K(275mil)
eE	7.00
e	0.65
b3	0.32
l1	1.00
X	(4.7)
Y	(3.5)

Caution: The package dimension is a reference value, which is not a guaranteed value.

Block Diagram





Three-phase logic truth table (A high level input is the state where $IN^+ > IN^-$)

	F/R = L			F/R = H			Output		
	IN1	IN2	IN3	IN1	IN2	IN3	OUT1	OUT2	OUT3
1	H	L	H	L	H	L	L	H	M
2	H	L	L	L	H	H	L	M	H
3	H	H	L	L	L	H	M	L	H
4	L	H	L	H	L	H	H	L	M
5	L	H	H	H	L	L	H	M	L
6	L	L	H	H	H	L	M	H	L

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	V_{CC} pin	36	V
	V_G max	V_G pin	42	V
Output current	I_O max	t ≤ 500ms	3.5	A
Allowable power dissipation	Pd max	Mounted on the specified board *	1.7	W
Operating temperature	Topr		-30 to +100	°C
Storage temperature	Tstg		-55 to +150	°C
Junction temperature	Tjmax		150	°C

* Specified board : 114.3mm × 76.1mm × 1.6mm, glass epoxy board

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommendation Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		8.0 to 35	V
5V constant voltage output current	I_{REG}		0 to -6	mA
HB output current	I_{HB}		0 to -7	mA
FG applied voltage	V_{FGS}		0 to 6	V
FG output current	I_{FGS}		0 to 5	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	$I_{CC}1$			3.5	4.7	mA
Supply current 2	$I_{CC}2$	At stop		1.1	1.5	mA
Output block						
Lower side output ON resistance	RON(L1)	IO= 1.2A		0.26	0.43	Ω
	RON(L2)	IO= 2.0A		0.26	0.43	Ω
Upper side output ON resistance	RON(H1)	IO= -1.2A		0.27	0.45	Ω
	RON(H2)	IO= -2.0A		0.27	0.45	Ω
Mid output current	IO(M)	VO= 12V		120	170	μA
Lower side diode forward voltage	VD(L1)	ID= -1.2A		0.9	1.20	V
	VD(L2)	ID= -2.0A		1.0	1.35	V
Upper side diode forward voltage	VD(H1)	ID= 1.2A		0.9	1.20	V
	VD(H2)	ID= 2.0A		1.0	1.35	V
5V Constant voltage Output						
Output voltage	VREG		4.6	5.0	5.4	V
Line regulation	ΔV(REG1)	V_{CC}= 8.0 to 35V		20	100	mV
Load regulation	ΔV(REG2)	IO= -1 to -6mA		5	100	mV
Hall Amplifier						
Input bias current	IB(HA)		-2	-0.1		μA
Common mode input voltage range 1	VICM1	When Hall-effect sensors are used	0.3		VREG-1.7	V
Common mode input voltage range 2	VICM2	When one-side inputs are biased (Hall IC application)	0		VREG	V
Hall input sensitivity	VHIN	SIN wave	80			mVp-p
Hysteresis width	ΔVIN(HA)		9	20	35	mV
Input voltage L → H	VSLH		3	8	16	mV
Input voltage H → L	VSHL		-20	-12	-5	mV
HB pin						
Output voltage	VHBO	IHB= -0.5mA	VREG-0.27	VREG-0.18	VREG-0.10	V
Output leakage current	IL(HB)	VO= 0V	-10			μA
Reference Oscillator (CT pin)						
High level voltage	VH(CT)		VREG x 0.54	VREG x 0.56	VREG x 0.58	V
Low level voltage	VL(CT)		VREG x 0.43	VREG x 0.45	VREG x 0.47	V
Amplitude	V(CT)		VREG x 0.10	VREG x 0.11	VREG x 0.12	V
Oscillation frequency	f(REF)	C= 56pF , R= 11kΩ	1.71	2.11	2.51	MHz
RT pin						
High level output voltage	VOH(RT)	IRT= -0.3mA	VREG-0.15	VREG-0.1	VREG-0.05	V
Low level output voltage	VOL(RT)	IRT= 0.3mA	0.05	0.1	0.15	V
Charge Pump Output (VG pin)						
Output voltage	VGOUT		V_{CC} +4.1	V_{CC} +4.7	V_{CC} +5.4	V
CP1 pin						
High level output voltage	VOH(CP1)	ICP1= -2mA	V_{CC} -1.4	V_{CC} -1.1	V_{CC} -0.7	V
Low level output voltage	VOL(CP1)	ICP1= 2mA	0.55	0.75	0.90	V
Charge pump frequency	f(CP1)			f(REF) / 32		MHz

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
PWM Oscillator						
High level voltage	VH(PWM)		2.75	3.05	3.35	V
Low level voltage	VL(PWM)		1.20	1.35	1.50	V
Amplitude	V(PWM)		1.40	1.70	2.00	V
Charge current	ICHG	VPWM= 2.1V	-80	-63	-45	μA
Oscillation frequency	f(PWM)	C= 1800pF	15.1	19.2	24.8	kHz
LIM pin						
Input bias current	IB(LIM)		-2	-0.1		μA
CTL pin						
Input voltage	VCTL1	Output duty: 100%	2.74	3.07	3.40	V
	VCTL2	Output duty: 0%	1.15	1.33	1.51	V
Input bias current	IB(CTL)		-2	-0.2		μA
Current limiter operation						
Limiter voltage	VRF		0.23	0.25	0.275	V
CSD Oscillator						
High level voltage	VH(CSD)		2.75	3.05	3.35	V
Low level voltage	VL(CSD)		1.43	1.68	1.93	V
Amplitude	V(CSD)		1.12	1.37	1.62	V
Charge current	ICSD1		-13.5	-10.5	-7.0	μA
Discharge current	ICSD2		8.0	11.5	14.5	μA
Oscillation frequency	f(CSD)	C= 0.047μ F	62	83	104	Hz
Thermal shutdown operation						
Thermal shutdown operation temperature	TSD	Design target value * (Junction temperature)	150	180		℃
Hysteresis width	ΔTSD	Design target value * (Junction temperature)		40		℃
FG pin						
Low level output voltage	VOL(FG)	IFG= 2mA		0.1	0.3	V
Output leakage current	IL(FG)	VFG= 6V			10	μA
Low-voltage shutdown protection circuit						
Operating voltage	VSDL		6.52	7.03	7.54	V
Release voltage	VSDH		6.98	7.49	8.00	V
Hysteresis width	ΔVSD		0.36	0.46	0.56	V
F/R pin						
High level input voltage range	VIH(FR)		2.0		VREG	V
Low level input voltage range	VIL(FR)		0		1.0	V
Input open voltage	VIO(FR)		VREG-0.5		VREG	V
Hysteresis width	VIS(FR)		0.15	0.35	0.5	V
High level input current	IIH(FR)	VF/R= VREG	-10	0	10	μA
Low level input current	IIL(FR)	VF/R= 0V	-80	-50	-35	μA
S/S pin						
High level input voltage range	VIH(SS)		2.0		VREG	V
Low level input voltage range	VIL(SS)		0		1.0	V
Input open voltage	VIO(SS)		VREG-0.5		VREG	V
Hysteresis width	VIS(SS)		0.15	0.35	0.5	V
High level input current	IIH(SS)	VS/S= VREG	-10	0	10	μA
Low level input current	IIL(SS)	VS/S= 0V	-80	-50	-35	μA

* : These items are design target value and are not tested.

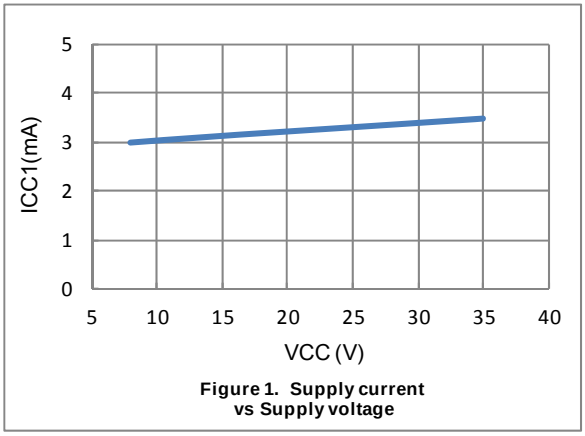


Figure 1. Supply current vs Supply voltage

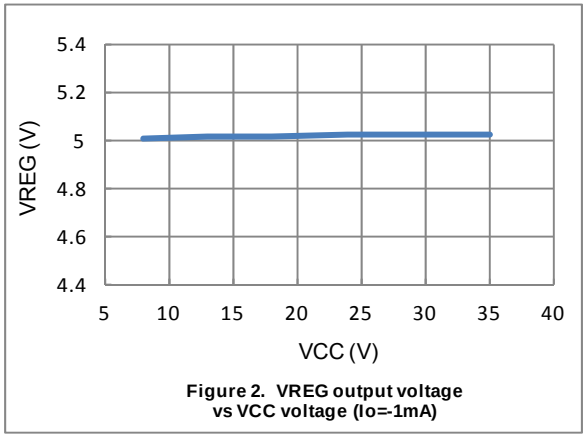


Figure 2. VREG output voltage vs VCC voltage (Io=-1mA)

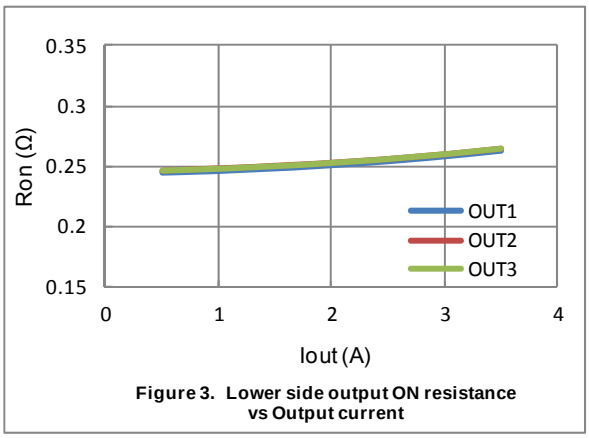


Figure 3. Lower side output ON resistance vs Output current

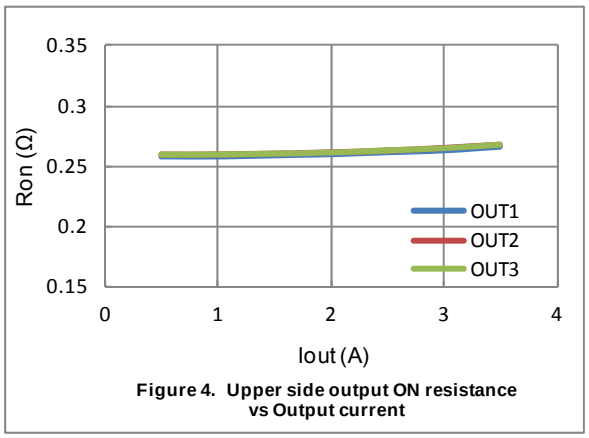


Figure 4. Upper side output ON resistance vs Output current

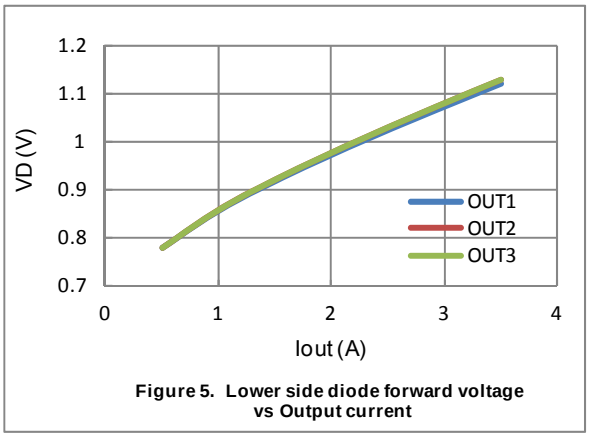


Figure 5. Lower side diode forward voltage vs Output current

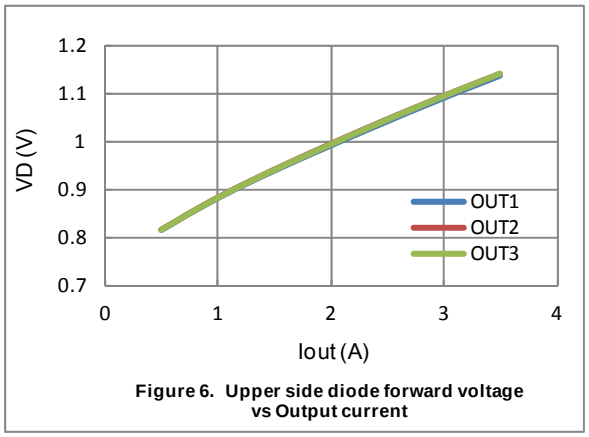


Figure 6. Upper side diode forward voltage vs Output current

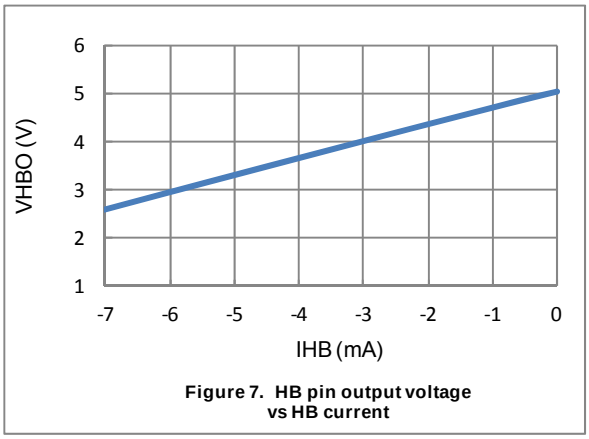


Figure 7. HB pin output voltage vs HB current

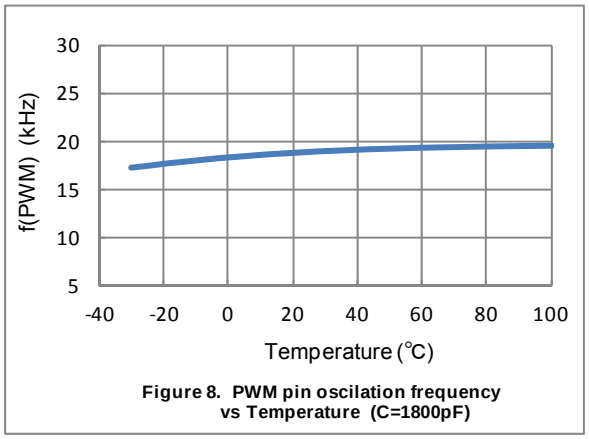


Figure 8. PWM pin oscilation frequency vs Temperature (C=1800pF)

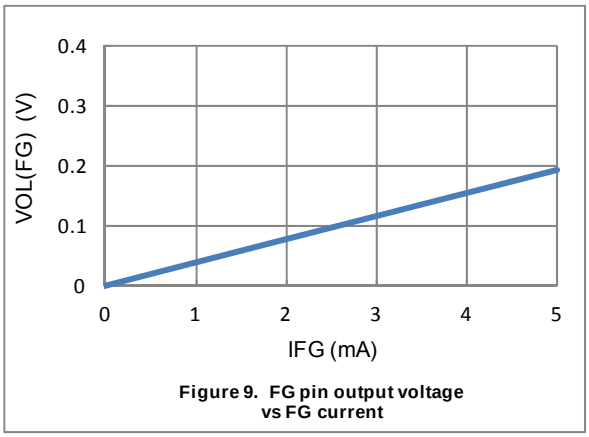
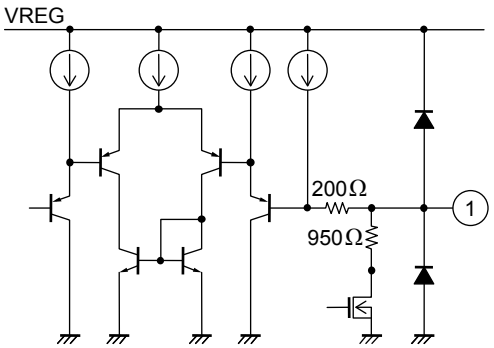
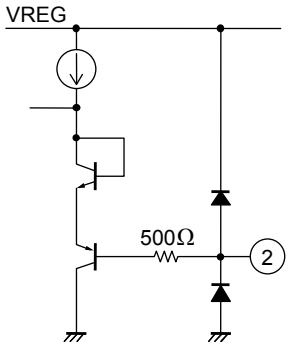
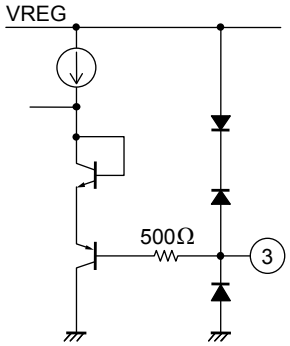
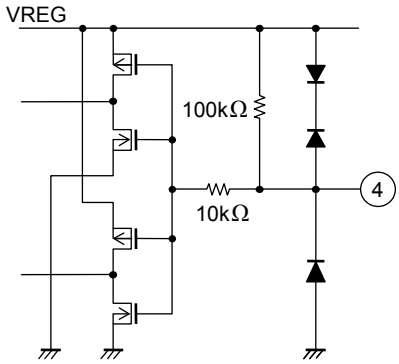


Figure 9. FG pin output voltage vs FG current

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	PWM	Pin to set the PWM oscillation frequency. Connect a capacitor between this pin and GND1. A frequency of about 19kHz can be set by using a 1800pF capacitor.	
2	LIM	Pin to set the minimum output duty. A minimum output duty can be set by inputting a fixed voltage to the LIM pin through resistor division of VREG. Connect the LIM pin to GND1 if this pin is not used, then the minimum output duty becomes 0 %.	
3	CTL	Pin to control the output duty. The output duty is determined by the result of comparing the CTL pin voltage with the PWM oscillation waveform. When the CTL pin is open, the output duty becomes 100%. Therefore, connect a pull-down resistor to prevent open.	
4	S/S	Start / Stop control pin. Low : 0V to 1.0V High : 2.0V to VREG Goes high when left open. Low for start. The hysteresis width is about 0.35V.	

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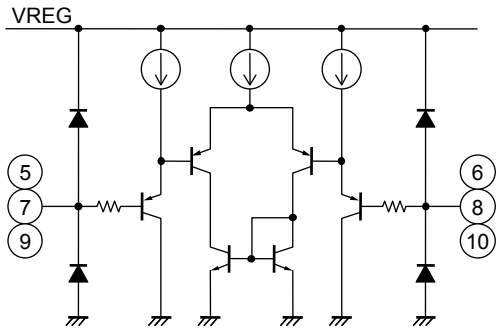
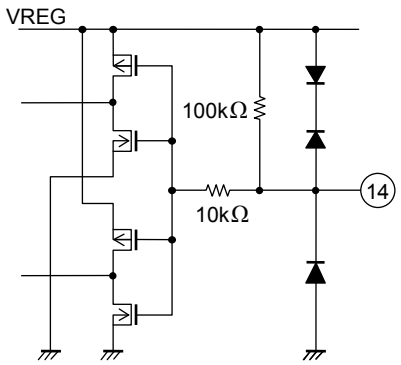
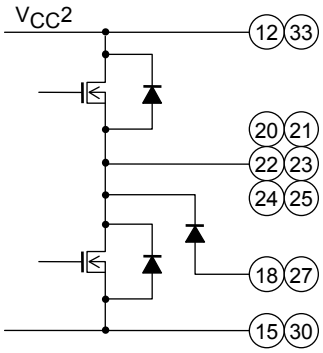
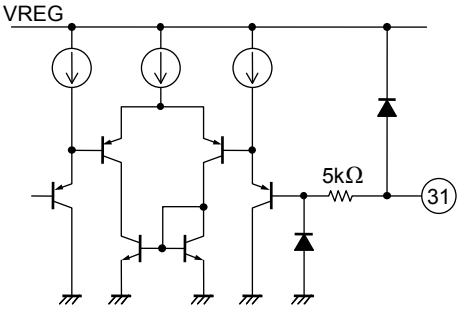
Pin No.	Pin name	Function	Equivalent circuit
5 6 7 8 9 10	$IN3^-$ $IN3^+$ $IN2^-$ $IN2^+$ $IN1^-$ $IN1^+$	Hall input pins. The input is seen as the high level input when $IN^+ > IN^-$, and as the low level input for the opposite state. If noise on the Hall signals is a problem, connect a capacitor between the corresponding IN^+ and IN^- inputs.	
14	F/R	Forward / Reverse control pin. Low : 0V to 1.0V High : 2.0V to VREG Goes high when left open. Low for forward. The hysteresis width is about 0.35V.	
34	VCC1	Power supply pin. (For systems other than the motor drive output.) Connect a capacitor between this pin and GND1 for stabilization.	
12,33	VCC2	Motor drive output power supply pins.	
20,21 22,23 24,25	OUT3 OUT2 OUT1	Motor drive output pins.	
15,30	RF	Source pins of the lower side output FET. Connect a resistor (Rf) between these pins and GND.	
18,27	GND2	Motor drive output circuit GND pins.	
31	RFS	Output current detection pin. Connect the RFS pin to the RF pin.	

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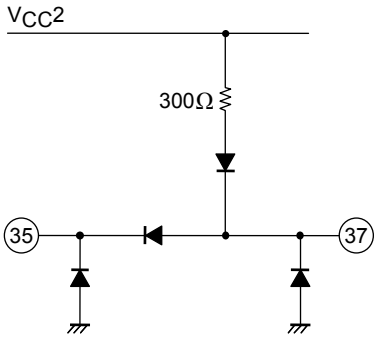
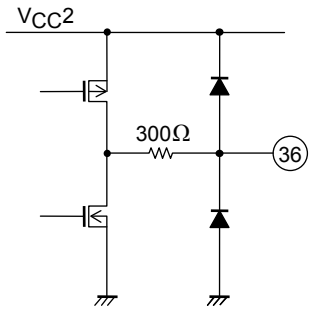
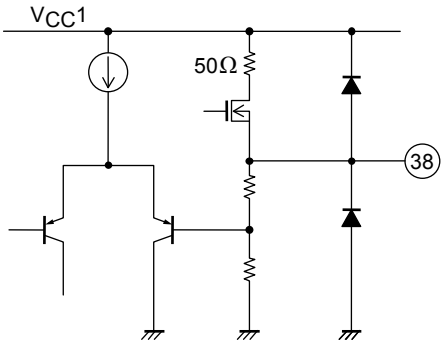
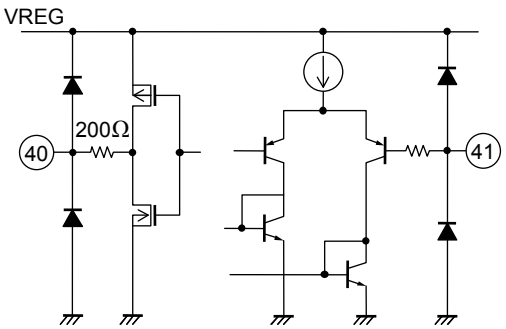
Pin No.	Pin name	Function	Equivalent circuit
35	VG	Charge pump output pin. Connect a capacitor between this pin and VCC2.	
37	CP2	Pin to connect the capacitor for charge pump. Connect a capacitor between this pin and CP1.	
36	CP1	Pin to connect the capacitor for charge pump. Connect a capacitor between this pin and CP2.	
38	VREG	5V constant voltage output pin. (Power supply pin for the control circuits.) Connect a capacitor between this pin and GND1 for stabilization.	
39	GND1	GND pin for the control circuits.	
40	RT	Pin to set the reference oscillation frequency. Connect a resistor to charge / discharge the capacitor of CT between this pin and CT.	
41	CT	Pin to set the reference oscillation frequency. Connect a capacitor between this pin and GND1.	

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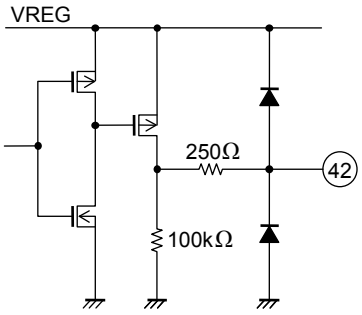
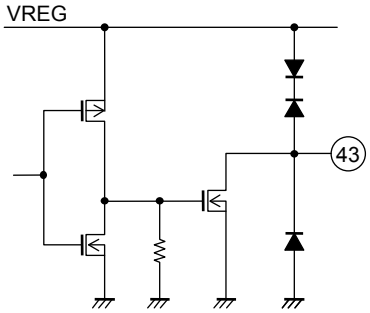
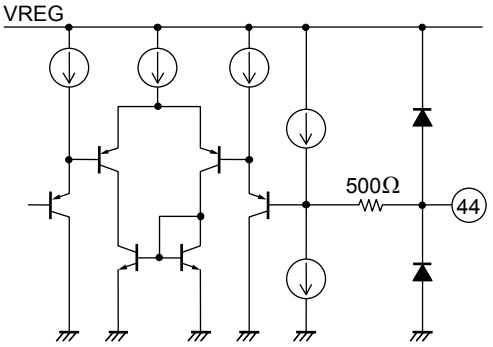
Pin No.	Pin name	Function	Equivalent circuit
42	HB	Hall bias switch pin. Goes off when the S/S input is the stop mode.	
43	FG	One hall-effect sensor FG output pin. (This is an open-drain output.)	
44	CSD	Pin to set the operating time of the constraint protection. Connect a capacitor between this pin and GND1.	
11,13 16,17 19,26 28,29 32	NC	No connection pins.	
Backside metal	Die-Pad	Exposed Die-Pad. The metal of the IC's backside is the Exposed Die-pad and is internally connected to GND1, GND2. For stabilization, connect the Exposed Die-pad to GND1 externally.	

Description of LV8121V

1. Motor Drive Output Circuit

   The LV8121V provides a charge pump circuit and implements both upper side and lower side N-channel power FET drive circuit. This IC employs the direct PWM drive technique. The motor speed is controlled by changing the output duty according to an analog voltage input (CTL). The upper side N-channel power FET is switched so that the output duty tracks the CTL voltage.

   The PWM frequency is determined by the capacitor connected between the PWM pin and GND1.

   When the PWM switching of the upper side N-channel power FET is off, the lower side N-channel power FET is turned on (synchronous rectification). Therefore, it is possible to reduce the temperature increase of the lower side N-channel power FET.

2. PWM Oscillator

   The PWM frequency is set by the oscillation frequency of the PWM pin. When a capacitor C [F] is connected between the PWM pin and GND1, the PWM frequency (f_{PWM}) is calculated as follows.

   $f_{PWM} = 1 / (28900 \times C)$

   When a 1800pF capacitor is connected, this frequency becomes about 19kHz.

   By the variance of the IC, “28900” of the above formula has varied from 22400 to 36800.

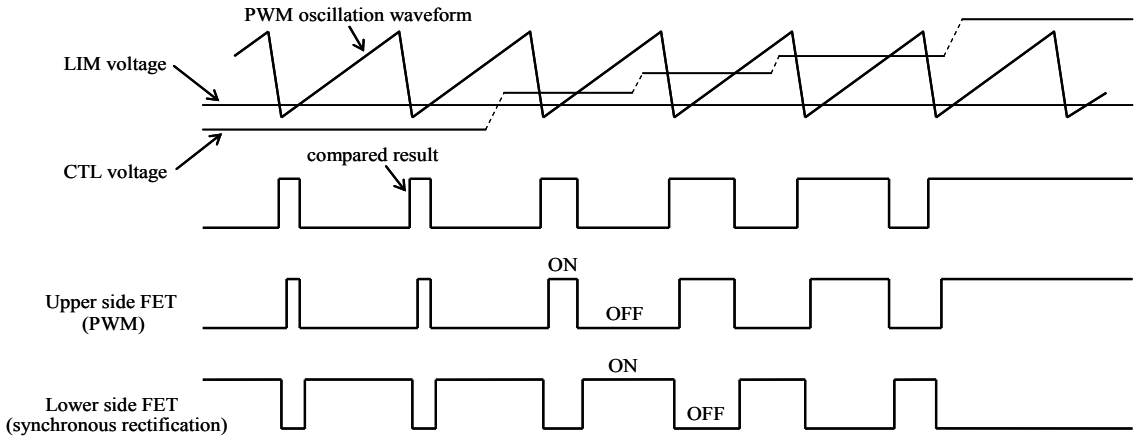
   If the PWM frequency is too high, since the switching power loss will be large, the IC temperature increase will be excessive. The PWM frequency therefore should be normally kept below 50kHz, which is achieved with a capacitor C of 1000pF or higher. The GND lead of the connected capacitor to the PWM pin should be connected as close as possible to the GND1 pin.

3. Output Duty

   The CTL voltage and the PWM oscillation waveform are compared to determine the output duty of the upper side N-channel power FET.

   If the LIM pin is not used (LIM=GND), the output duty becomes 0% when the CTL voltage is lower than about 1.3V and 100% when it exceeds about 3.1V.

   For the application that inputs a fixed voltage to the LIM pin, the LIM voltage and the PWM oscillation waveform are compared to determine the minimum output duty. Accordingly, even if the CTL voltage is lower than the LIM voltage, the output duty does not decrease below the minimum output duty.



   If a minus voltage is applied to the CTL pin, this pin current must be limited within 2mA by inserting the resistor of about 200Ω.

   When the CTL pin is open, the output duty becomes 100%. Therefore, connect a pull-down resistor to prevent open.

   If the output duty is fast reduced by dropping the CTL voltage quickly when the motor speed is changed from high to low, since this IC employs the synchronous rectification, the lower side N-channel power FET can be the short brake condition that turns on two phases. If the lower side N-channel power FET (synchronous rectification) is switched from on to off while this condition, the motor current may flow on the power supply side, and the power supply voltage may bounce. The bounce of the power supply voltage is different on the motor speed, the varied range of the CTL voltage and the capacitance of the power supply line. Therefore, check sufficiently that the bounce of the power supply voltage does not exceed the maximum rating when the CTL voltage is changed.

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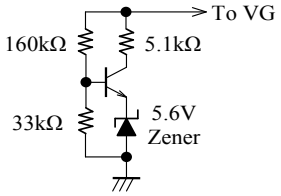


In case of limiting the bounce of the power supply voltage, the maximum voltage of the VCC can be limited according to the following method. The maximum voltage of the VG is limited by using Zener diode, NPN transistor and some resistors. Normally, the relation between VG and VCC becomes "VG = VCC + 4.7V". If VCC rises above "VGmax - 4.7V" when VG is limited to VGmax, this relation does not keep. Because the sufficient gate voltage cannot be applied to the upper side N-channel power FET when this relation does not keep, this IC includes the protective function that turns off the upper side N-channel power FET.
Accordingly, if VCC rises above "VGmax - 4.7V" when VG is limited to VGmax, the upper side N-channel power FET is turned off, and the VCC bounce caused by dropping the CTL voltage can be limited to "VCC = VGmax - 4.7V". When the above reference circuit is used, VG is limited to about 36.7V, and VCC is limited to about 32.0V. But this function does not guarantee that any VCC bounce can be limited. If VCC is steeply bounced by dropping the CTL voltage, this function may not limit the VCC bounce.

4. Current Limiter Circuit

The current limiter circuit limits the output current peak to the value determined by "I = VRF / Rf" (VRF = 0.25V typ., Rf: current detection resistor). When the current limiter is operating, the upper side N-channel power FET is switched, and the output current is suppressed by reducing the output duty.

5. Reference Oscillator

Connect a 56pF capacitor between CT and GND1, and a 11kΩ resistor between RT and CT. Then, the reference oscillation frequency becomes about 2.1MHz. The reference oscillation frequency functions as a reference clock for the internal logic circuit. The charge pump circuit boosts the voltage using a frequency that is 1/32 of the reference oscillation frequency.

6. Start / Stop Switching Circuit

When the S/S pin is set to the low level, start/stop switching circuit is the start mode. Inversely, when the S/S pin is set to the high level or open, start/stop switching circuit is the stop mode. This IC goes into a power saving state that reduces the supply current at the stop mode. In the power saving state, the bias current is removed from most of the circuits in the IC.
The operating circuits in the power saving state are limited to the start/stop switching circuit and the 5V constant voltage output. The other circuits do not operate. Both upper side and lower side N-channel power FET are turned off in the power saving state.
If a minus voltage is applied to the S/S pin, this pin current must be limited within 2mA by inserting the resistor of about 200Ω.

7. Forward / Reverse Switching Circuit

The motor rotation direction can be switched by using the F/R pin. However, the following notes must be observed if the F/R pin is switched while the motor is rotating.

- This IC is designed to avoid the through current when the direction is switched. However, the bounce of the VCC voltage (due to the motor current that flows instantly on the power supply side) may be caused during the direction switching. If this bounce is a problem, the capacitance inserted between VCC and GND must be increased.
- If the motor current after the direction switching exceeds the current limiter value, the upper side N-channel power FET will be turned off, but the lower side N-channel power FET will be the short brake condition. On the short brake condition, the current determined by the motor back EMF voltage and the coil resistance will flow. Because the current limiter circuit of this IC cannot limit this current, applications must be designed so that this current does not exceed the maximum rating (3.5A). When the motor speed is higher, the direction switching is dangerous.

If a minus voltage is applied to the F/R pin, this pin current must be limited within 2mA by inserting the resistor of about 200Ω.

8. Hall Input Signal

The input amplitude of 100mVp-p or more (differential) is desirable in the Hall inputs. The closer the input wave-form is to a square wave, the required input amplitude is lower. Inversely, the closer the input wave-form is to a triangular wave, the higher input amplitude is required. Also, note that the input DC voltage must be set within the common mode input voltage range.

For the Hall IC application, one side (either the + or – side) of the Hall inputs must be fixed at a voltage within the common mode input voltage range that applies when the Hall-effect sensors are used, and the input voltage range for the other side becomes 0V to VREG.

If noise on the Hall signals is a problem, that noise must be excluded by inserting capacitor between the Hall inputs as close as possible to these pins.

When the Hall inputs for all three phases are in the same state, all the outputs (the both upper side and lower side N-channel power FET) are turned off.

9. FG Output

The FG pin is the pulse output that has the same frequency as Hall input IN1 (one Hall-effect sensor FG output).

10. HB Pin

The HB pin is the 5V constant voltage output that combines the switch function. This pin is connected to the base of external NPN transistor that supplies the bias of the Hall-effect sensors. If the HB output is turned off, this external NPN transistor is too turned off, and the bias of the Hall-effect sensors is cut (Hall bias switch).

The HB output is turned off and is made pull-down by a 100kΩ internal resistor when the S/S pin is the stop mode. Therefore, the bias of the Hall-effect sensors can be cut when the S/S pin is the stop mode.

In case the LIM pin is not used (LIM=GND), if the CTL voltage falls below 0.7V, the HB output is turned off, and the bias of the Hall-effect sensors is cut.

In case the minimum output duty is determined by the LIM pin, even if the CTL voltage falls below 0.7V, the HB output is not turned off.

If the HB pin is not used, keep open.

11. Constraint Protection Circuit

The constraint protection circuit operates to turn the motor drive (the upper side N-channel power FET) on or off repeatedly in the motor constrained state. Therefore, the IC and the motor are protected. The drive on/off time can be set by adjusting the oscillation frequency of the CSD pin with external capacitor. When a capacitor C [μF] is connected between the CSD pin and GND1, the drive on/off time is calculated as follows.

TCSD1 (drive on time) = 8.21 x C

TCSD2 (drive off time) = TCSD1 x 15

When a 0.047μF capacitor is connected, this protection function will iterate an on/off period in which drive is on for about 0.39sec and off for about 5.8sec.

By the variance of the IC, “8.21” of the above formula has varied from 5.41 to 11.01.

If the switching from L to H of the Hall input IN1 (the rising edge on the FG output) is not caused during the drive on time, this protection function turns the motor drive off, and returns the motor drive on after the drive off time.

If the drive on time to be set is too short, this protection function operates at a normal motor start-up, and the motor may not speed up since this protection function iterates an on/off period. Also, if the motor speed is too low, this protection function operates when one cycle of the Hall input IN1 is longer than the drive on time. The drive on time must be set to a sufficient time so that this protection function does not operate except the motor constrained state.

The oscillation waveform of the CSD pin is used for some circuits in addition to the constraint protection circuit. Therefore, it is desirable to oscillate the CSD pin even if the constraint protection function is unnecessary.

The CSD pin combines the function as the initial reset pin. The time that the CSD voltage is charged to about 1.25V is determined as the initial reset. At the initial reset, all the outputs (the both upper side and lower side N-channel power FET) are turned off.

If the constraint protection function is not used, the oscillation of the CSD pin must be stopped by connecting a 220kΩ resistor and a 0.01μF capacitor in parallel between the CSD pin and GND1. However, when the oscillation of the CSD pin is stopped, note that some functions do not operate in the following cases.

- If the motor does not rotate at the motor start-up because the motor is constrained, the upper side N-channel power FET may be switched by the current limiter. But, the synchronous rectification does not operate when the oscillation of the CSD pin is stopped.
- In case the LIM pin is not used (LIM=GND), even if the CTL voltage falls below 0.7V, the HB output is not turned off when the oscillation of the CSD pin is stopped.

12. Low-voltage Shutdown Protection Circuit

The IC includes a low-voltage shutdown protection circuit to protect against incorrect operation when the VCC power supply is switched on or if the VCC voltage falls below the allowable operating range. When the VCC voltage falls below the specified voltage (VSDL), this protection function operates, and all the outputs (the both upper side and lower side N-channel power FET) are turned off. When the VCC voltage rises above the release voltage (VSDH), this protection function is released.

13. Thermal Shutdown Protection Circuit

If the junction temperature rises to the specified temperature (TSD), this protection function operates, and the upper side N-channel power FET is turned off. If the temperature decrease falls to more than the hysteresis width (ΔTSD), this protection function is released.

14. Power Supply Stabilization

Because a large switching current flows in the VCC line, the line inductance and other factors can lead to VCC voltage fluctuations. Sufficient capacitance should be provided between VCC and GND for stabilization. When long wiring routes are used, choose a capacitor with even larger capacitance.
Ceramic capacitors of about 0.2μF must be connected between the VCC1 pin and the GND1 pin as close as possible to these pins for excluding noise.

15. VREG Pin

The VREG pin is the power supply for the control circuits. Therefore, a capacitor of about 0.1μF must be connected between the VREG pin and the GND1 pin as close as possible to these pins for stabilization.

16. VG Pin

When the S/S pin is the stop mode, the VG pin is the high-impedance condition in the IC. If the ambient temperature of the capacitor inserted between VG and VCC2 becomes high when the VG pin is the high-impedance condition, since the voltage charged in this capacitor may rise due to the temperature characteristic of the capacitor, the VG voltage may rise. Therefore, prevent the VG voltage from rising by inserting the resistor of about 200 kΩ between VG and VCC2 or VG and GND1 so that the VG pin is not the high-impedance condition.

17. Notes on wiring of a Printed Circuit Board

Two pins are provided for each of pins (VCC2, RF, OUT1, OUT2, OUT3, GND2) where large current flows. Both of these pins should be externally connected.

18. The Metal of the IC's Backside

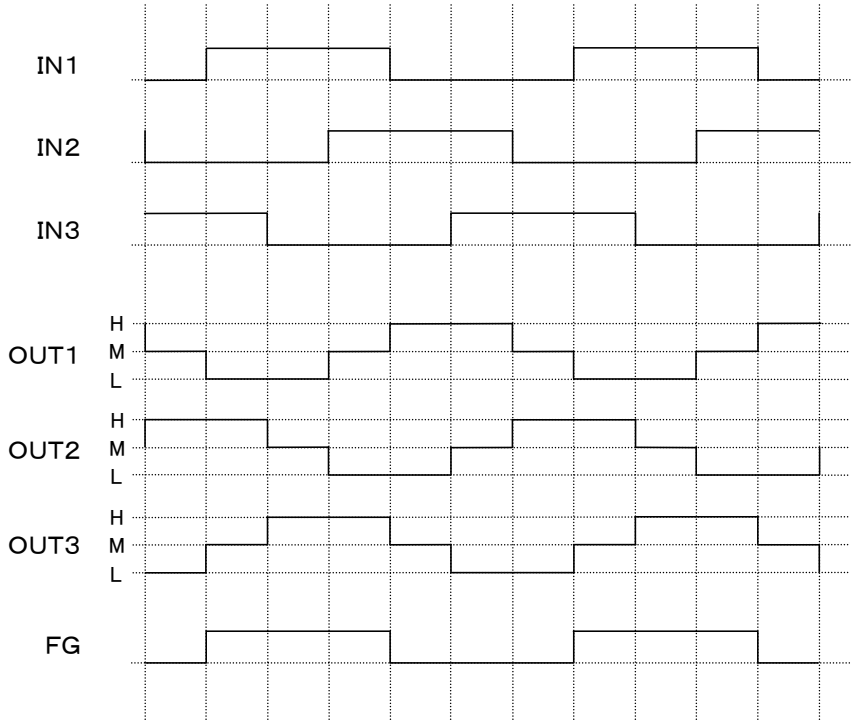
The metal of the IC's backside is the Exposed Die-pad and is internally connected to GND1, GND2. For stabilization, connect the Exposed Die-pad to GND1 externally. The IC's generation of heat can be efficiently diffused to a printed circuit board by soldering the Exposed Die-pad to the copper of the printed circuit board.

19. NC Pins

The NC pins are electrically open. These pins may be used for wiring routes.

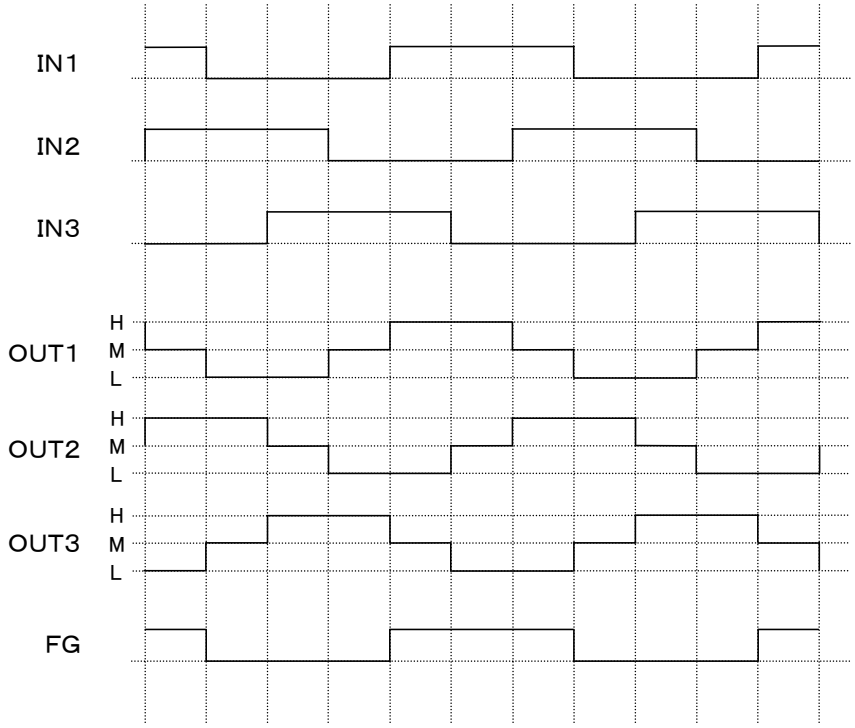
Three-phase logic timing chart (example of forward rotation)

When F/R＝”L”



H : The upper FET is turned ON. The lower FET is turned OFF.
M : The upper FET is turned OFF. The lower FET is turned OFF.
L : The upper FET is turned OFF. The lower FET is turned ON.

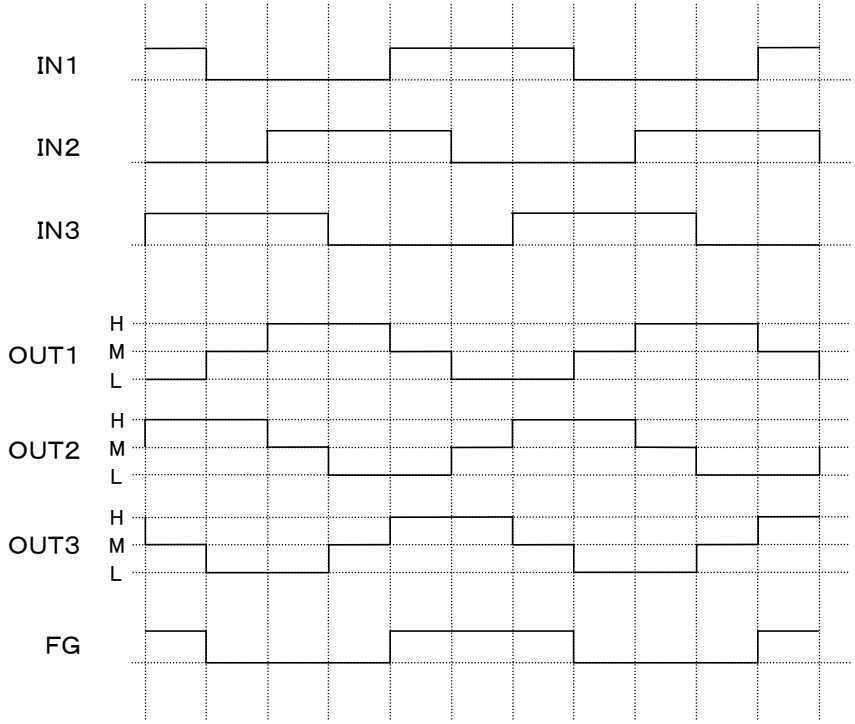
When F/R＝”H”



H : The upper FET is turned ON. The lower FET is turned OFF.
M : The upper FET is turned OFF. The lower FET is turned OFF.
L : The upper FET is turned OFF. The lower FET is turned ON.

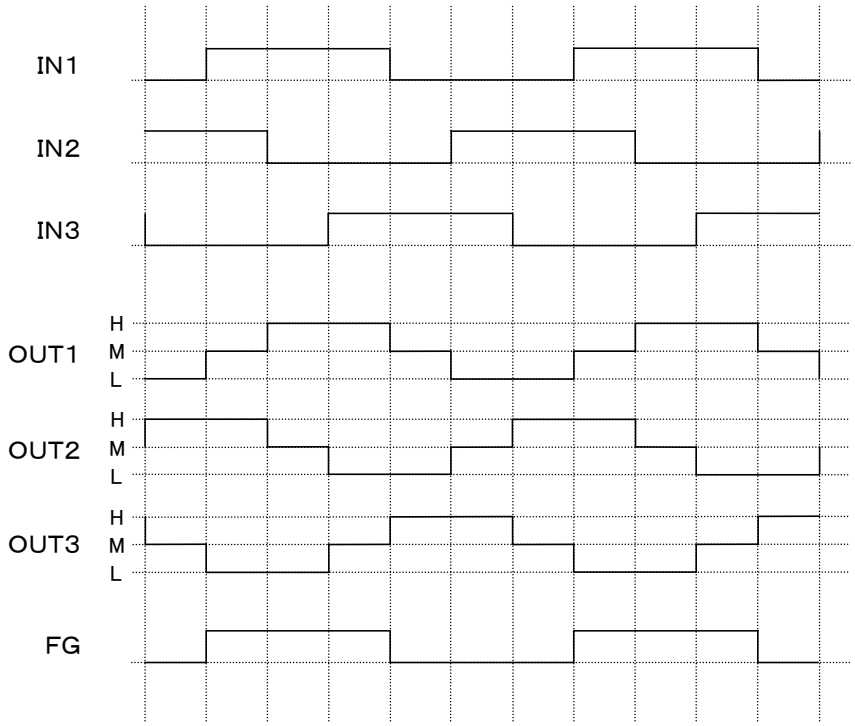
Three-phase logic timing chart (example of reverse rotation)

When F/R＝”L”



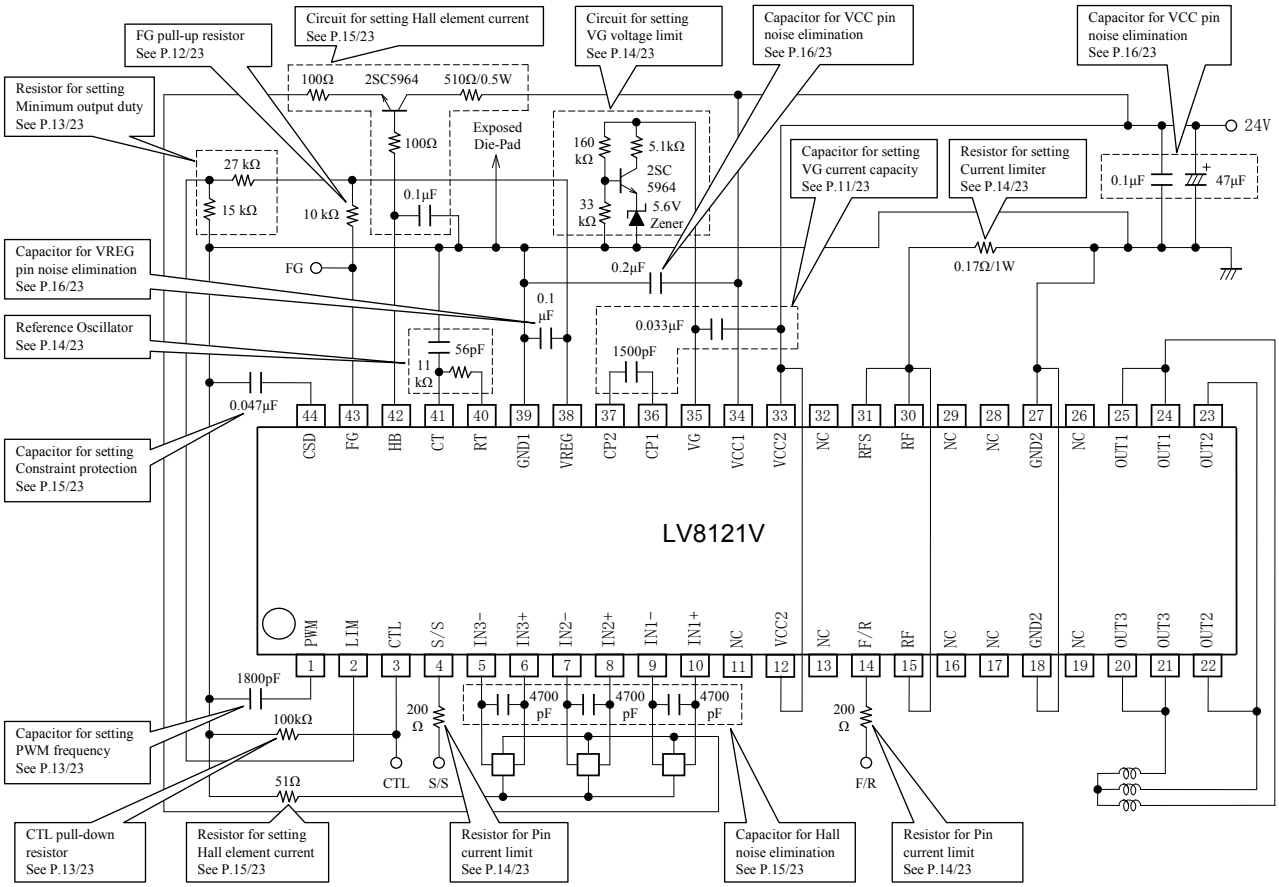
H : The upper FET is turned ON. The lower FET is turned OFF.
M : The upper FET is turned OFF. The lower FET is turned OFF.
L : The upper FET is turned OFF. The lower FET is turned ON.

When F/R＝”H”

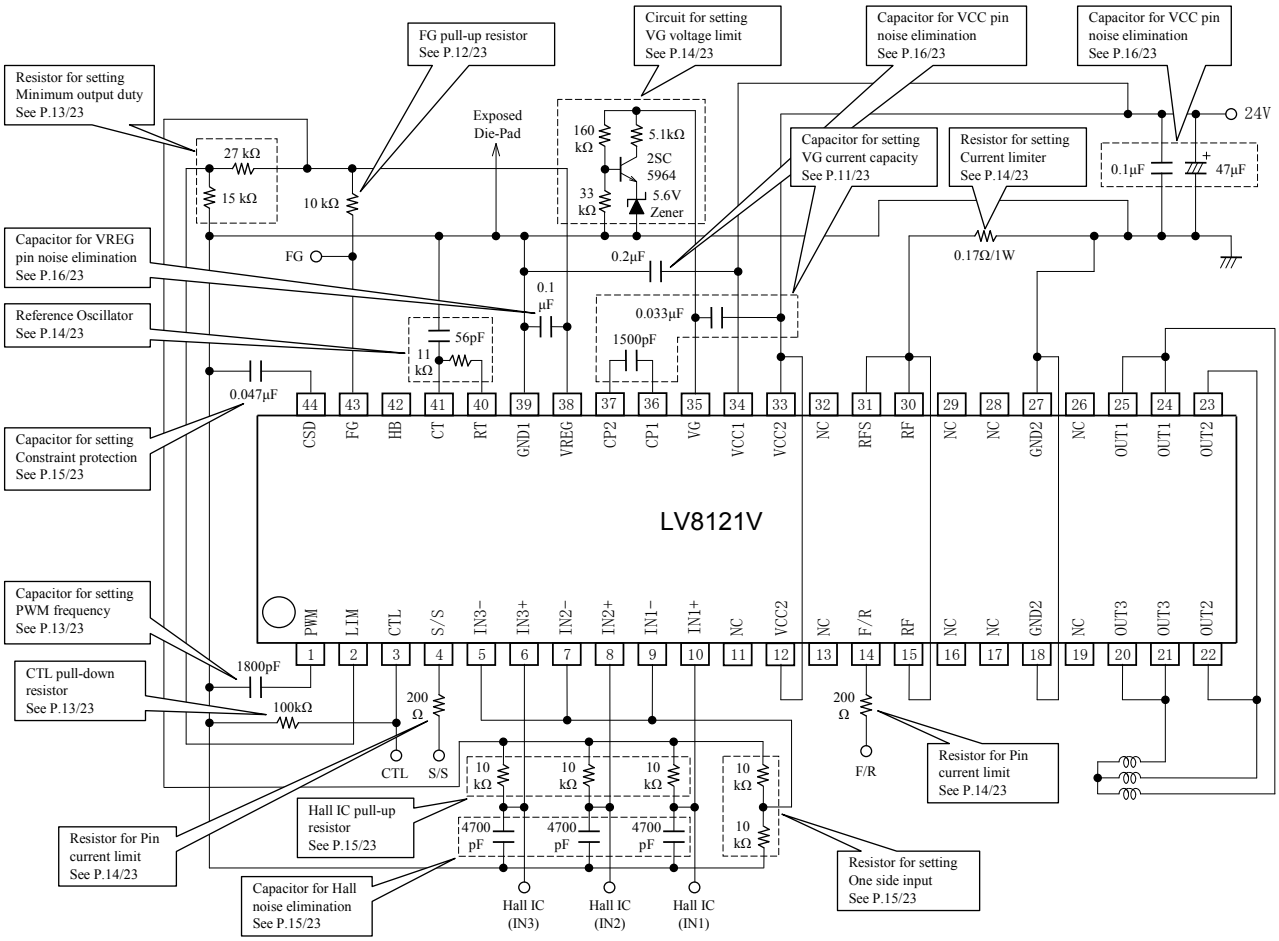


H : The upper FET is turned ON. The lower FET is turned OFF.
M : The upper FET is turned OFF. The lower FET is turned OFF.
L : The upper FET is turned OFF. The lower FET is turned ON.

Application Circuit for Hall elements (Reference value)



Application Circuit for Hall ICs (Reference value)



Evaluation Board (“M-DrAGON means Motor-Driver And GUI produced by ON semiconductor)

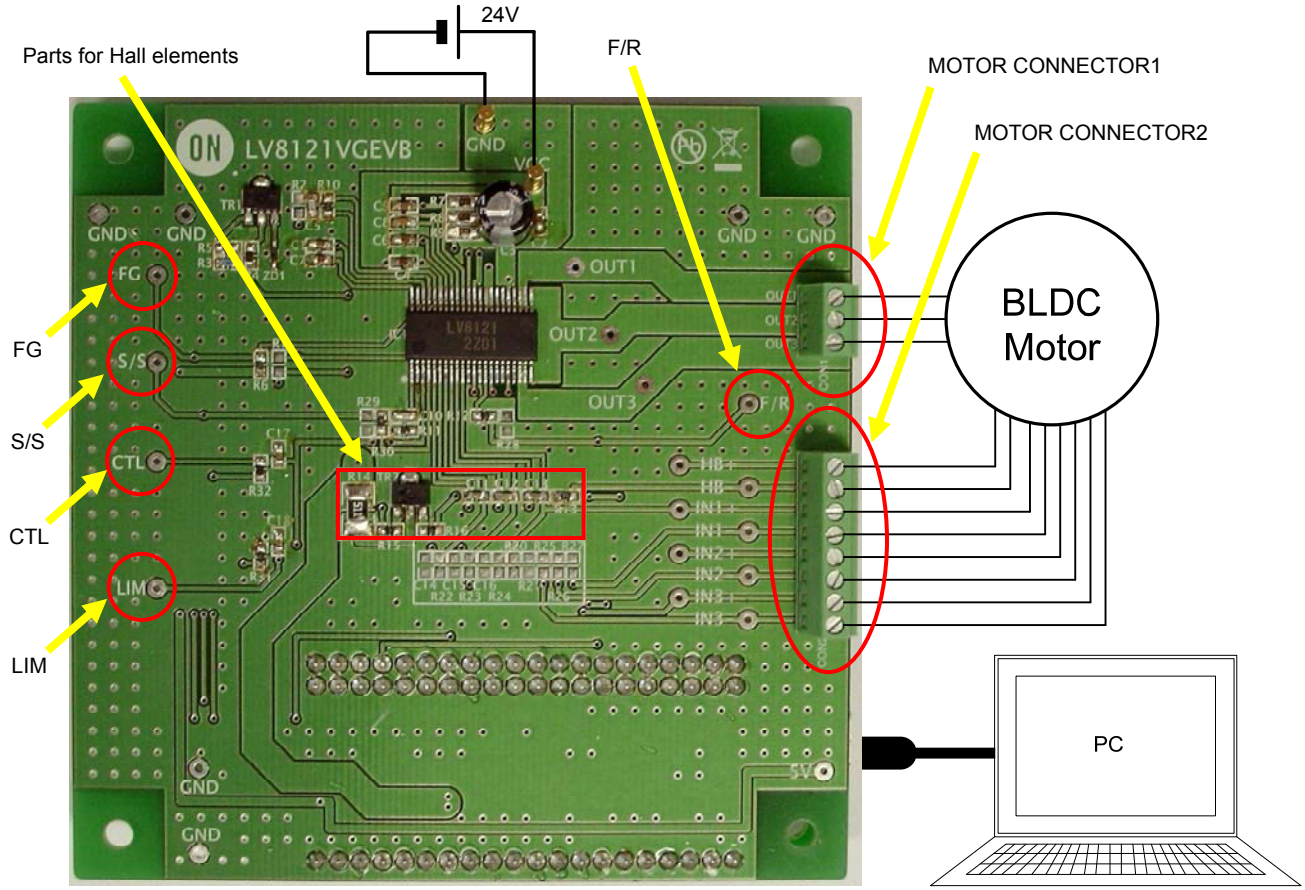


Figure10. “M-DrAGON” overview (Top view)

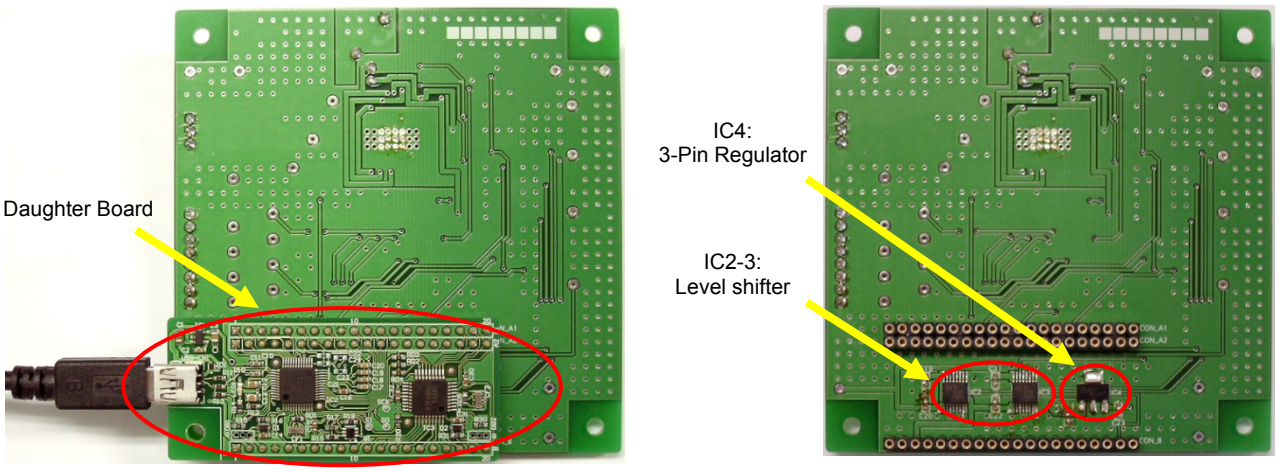


Figure11. “M-DrAGON” overview (Bottom view)

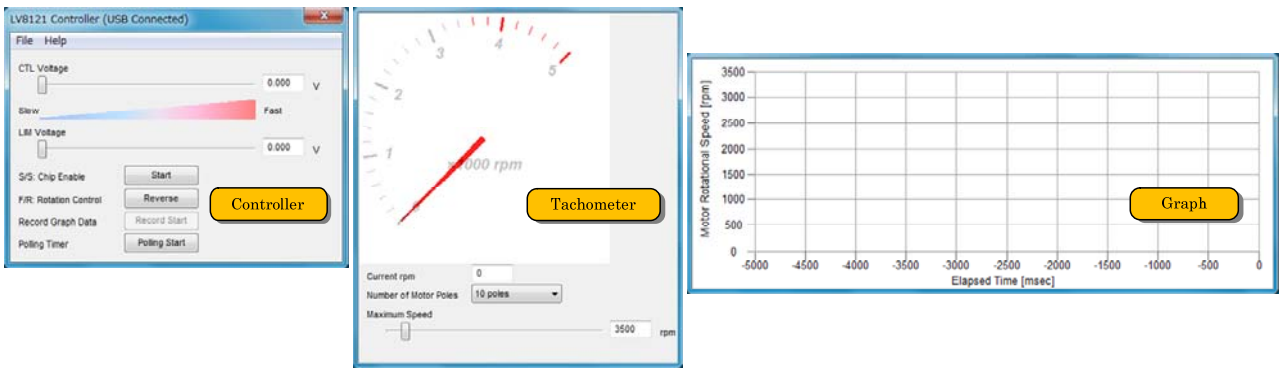
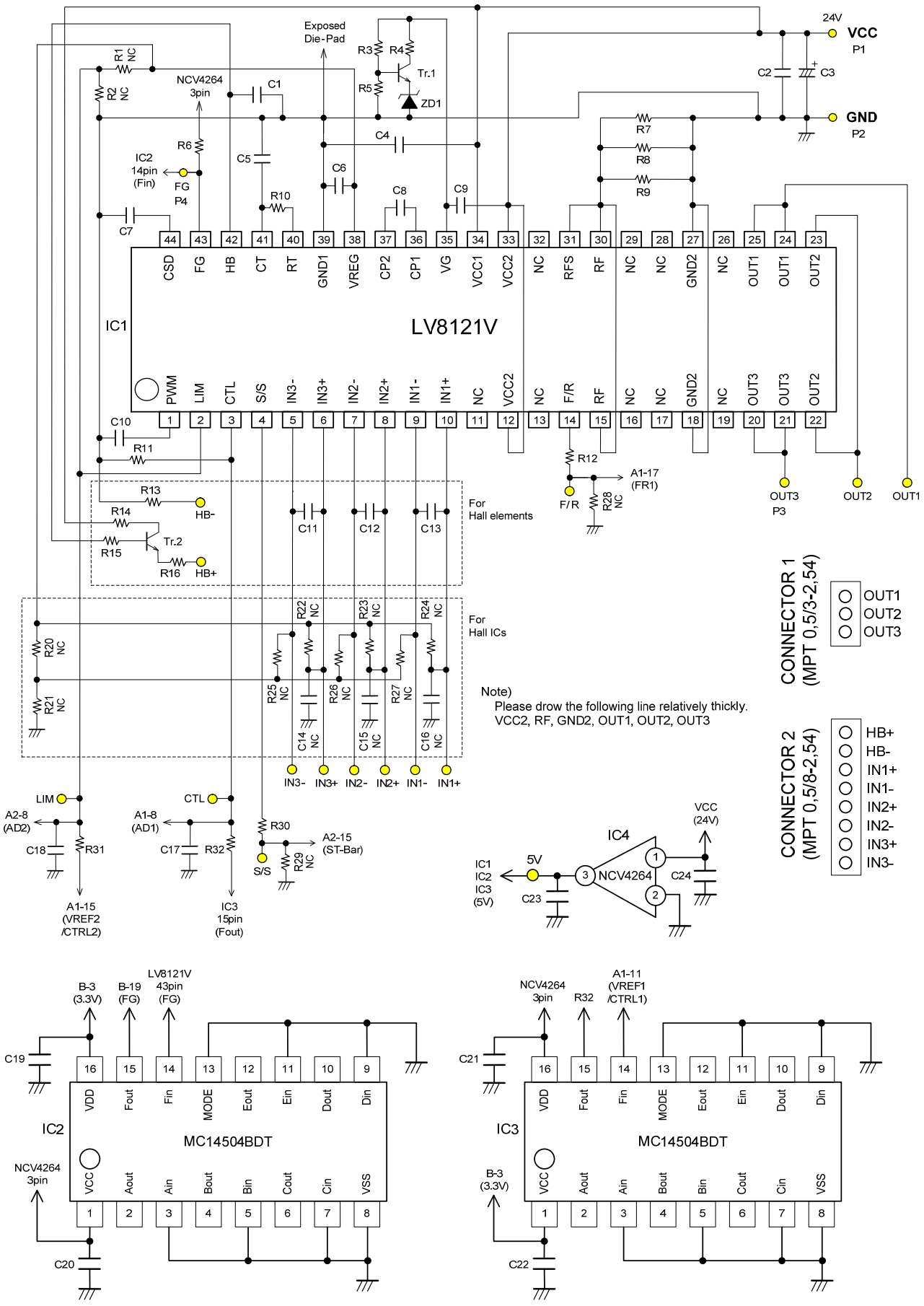


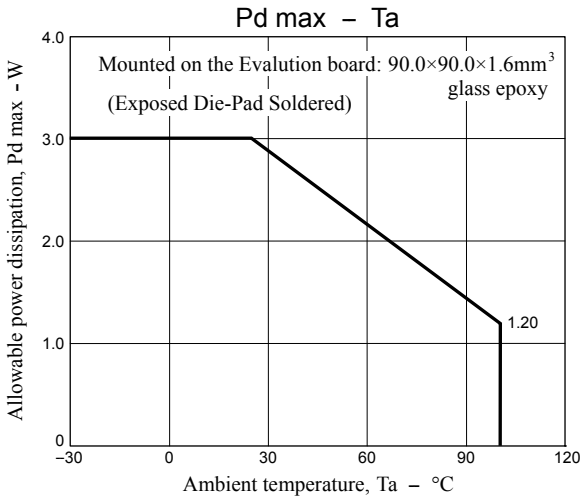
Figure12. Images of GUI

Bill of Materials for LV8121V Evaluation Board

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
IC1	1	Motor Driver			SSOP44K	ON semiconductor	LV8121V	No	Yes
IC2-3	2	Level Shifter			TSSOP16	ON semiconductor	MC14504BDT	No	Yes
IC4	1	3-Pin Regulator			SOT-223	ON semiconductor	NCV4264-2ST50T3G	Yes	Yes
Tr.1	1	Clamping Circuit			PCP	ON semiconductor	2SC5964	Yes	Yes
Tr.2	1	Bias of Hall sensors			PCP	ON semiconductor	2SC5964	Yes	Yes
ZD1	1	5.6V Zener Diode			SOD-523	ON semiconductor	MM5Z5V6ST1G	Yes	Yes
CONNECTOR1	1	Motor connection socket			2.54mm pitch	Phoenix Contact	MPT 0,5/3-2,54	Yes	Yes
CONNECTOR2	1	Motor connection socket			2.54mm pitch	Phoenix Contact	MPT 0,5/8-2,54	Yes	Yes
R1	1	LIM(pull up)	NC		1608 (0603Inch)			Yes	Yes
R2	1	LIM(pull down)	NC		1608 (0603Inch)			Yes	Yes
R3	1	Tr.1(pull up)	160kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD164J	Yes	Yes
R4	1	Tr.1(pull up)	5.1kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD512J	Yes	Yes
R5	1	Tr.1(pull down)	33kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD333J	Yes	Yes
R6	1	FG(pull up)	10kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	Yes	Yes
R7-9	3	RF	0.51Ω (0.25W)	±5%	2012 (0805Inch)	ROHM	MCR10EZHJLR51	Yes	Yes
R10	1	CT	11kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD113J	Yes	Yes
R11	1	CTL (pull down)	100kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD104J	Yes	Yes
R12	1	F/R	200Ω (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD201J	Yes	Yes
R13	1	Hall bias	51Ω (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD510J	Yes	Yes
R14	1	Hall bias	510Ω (0.5W)	±5%	3225 (1210Inch)	Panasonic	ERJP14J511U	Yes	Yes
R15	1	Hall bias	100Ω (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD101J	Yes	Yes
R16	1	Hall bias	100Ω (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD101J	Yes	Yes
R20-24	5	Hall IC application	NC		1608 (0603Inch)			Yes	Yes
R25-27	3	Jumper	NC		1608 (0603Inch)			Yes	Yes
R28-29	2	Jumper	NC		1608 (0603Inch)			Yes	Yes
R30	1	S/S	200Ω (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD201J	Yes	Yes
R31	1	LIM	100kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD104J	Yes	Yes
R32	1	CTL	27kΩ (0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD273J	Yes	Yes
C1	1	HB Bypass Capacitor	0.1uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188R11H104KA93	Yes	Yes
C2	1	VCC Bypass Capacitor	0.1uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188R11H104KA93	Yes	Yes
C3	1	VCC Bypass Capacitor	47uF /50V	±20%		SUN Electronic	50ME47HC	Yes	Yes
C4	1	VCC Bypass Capacitor	0.22uF /50V	±10%	1608 (0603Inch)	MURATA	GCM188R71H224KA49	Yes	Yes
C5	1	CT	56pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H560JA01	Yes	Yes
C6	1	VREG Bypass Capacitor	0.1uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188R11H104KA93	Yes	Yes
C7	1	CSD	0.047uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188B11H473KA61	Yes	Yes
C8	1	CP	1500pF /50V	±10%	1608 (0603Inch)	MURATA	GRM188B11H152KA01	Yes	Yes
C9	1	VG	0.033uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188B11H333KA61	Yes	Yes
C10	1	PWM	1800pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H182JA01	Yes	Yes
C11-13	3	IN+ / -	4700pF /50V	±10%	1608 (0603Inch)	MURATA	GRM188B11H472KA01	Yes	Yes
C14-16	3	IN+ / GND	NC		1608 (0603Inch)			Yes	Yes
C17	1	CTL	0.1uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188R11H104KA93	Yes	Yes
C18	1	LIM	0.1uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188R11H104KA93	Yes	Yes
C19-22	4	VCC, VDD of MC14504BDT	0.1uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188R11H104KA93	Yes	Yes
C23-24	2	IN, OUT of NCV4264-2ST50T3G	0.1uF /50V	±10%	1608 (0603Inch)	MURATA	GRM188R11H104KA93	Yes	Yes
Daughter Board	1	Interface board				ON semiconductor		No	Yes
CON_A1, A2, B	3	Female Socket				MAC8	PM-61	Yes	Yes
P1-4	4	Terminal Pin				MAC8	ST-1-3	Yes	Yes

Evaluation board circuit





Operation Guide

- Connect a Three-phase Brushless DC motor with MOTOR CONNECTOR1 and MOTOR CONNECTOR2.
  When we provide the Evaluation Board, it is mounted peripheral parts for Hall elements. If you drive the Brushless DC motor with Hall ICs, please remove Tr.2, R13-16, C11-13 and mount R20-27, C14-16. Refer to 19 page for details. When you control LV8121V by DSP, remove the Daughter Board and R32. Then, apply each signal to CTL, LIM, S/S, F/R terminal pads.
- Please start up the system along the following procedures.
  1. Plug the USB cable into the Daughter Board.
  2. Start GUI for LV8121.
  3. Switch on the VCC power supply.
     Don't apply the voltage before plugging the USB cable and starting GUI.
  4. Input the drive signals of the motor with GUI.
- After switching off the VCC power supply, unplug the USB cable from the Daughter Board.
- Don't exceed the absolute maximum ratings under no circumstances.
- When the motor speed is higher, the direction switching is dangerous. If the motor current after the direction switching exceeds the current limiter value, the upper side N-channel power FET will be turned off, but the lower side N-channel power FET will be the short brake condition. On the short brake condition, the current determined by the motor back EMF voltage and the coil resistance will flow. The current limiter of the IC cannot limit this current.

Notes in design

- VCC2, RF, GND2 and each OUT are the large current lines. These lines should be layouted thick and short as possible.
- VCC bypass capacitor between VCC1 and GND1 should be mounted as near as possible to the IC.
- VREG bypass capacitor between VREG and GND1 should be mounted as near as possible to the IC.
- The metal of the IC's backside is the Exposed Die-pad. The IC's generation of heat can be efficiently diffused to a printed circuit board by soldering the Exposed Die-pad to the copper of the printed circuit board. The Exposed Die-pad should be connected to GND1 pin of the IC.