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LC89091JA

Digital Audio Interface Receiver
Application Note

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This document is an application note for the LC89091JA which is a digital audio interface receiver.
It describes the following items. Please refer along with the data sheet of the LC89091JA.

Table of Contents

Modification History

Ver.	Date	Description
0.00	2013. 02. 19	First edition

1. Preparation

• First of all, please read the following items before using LC89091JA.

1-1. Notes on Implementation

• Attach a small-capacity ceramic capacitor (chip capacitor) between each power supply pin.
• Attach the ceramic capacitor so as to be nearest to the LC89091JA.
• A standard capacity of a ceramic capacitor is 0.1μF. Please connect a ceramic capacitor of 0.01μF and an electrolytic capacitor parallel as required.
• Connect all GND pins with a ground-plane set right under the LC89091JA.
• The capacitance value of the electrolytic capacitor depends on a distance from the power supply circuit or a quality of the power supply. An electrolytic capacitor of around 10μ to 47μF is usually used.

1-2. Oscillation Amplifier Module Connection (XIN, XOUT)

• LC89091JA must supply a 24.576MHz clock to XIN pin for an operation of a demodulation function, computation of sampling frequencies, or clock supply when PLL is unlocked, etc.

[How to Supply Clock]
• Configure an oscillation circuit with a crystal oscillator by using a built-in oscillation amplifier.
• Supply from other oscillation circuit.
(Connect to an oscillation circuit such as a commercial oscillation module).

[Notes]
• It uses an oscillator with a fundamental wave.
• Feed back with 1MΩ resistor between XIN and XOUT when the oscillator is connected.
• A limiting resistor is required when the oscillator is connected. A resistor value depends on characteristics of the oscillator.
• It uses 0.001% as a guide of accuracy of an oscillator and an oscillation module.
• When using the oscillation module, the output connectes to XIN. (XOUT open)
• No feedback resistor is required when using the oscillation module.
• XIN absolute maximum rating is VDD+0.3V. (VDD=3.0 to 3.6V)
• The resistor value and the capacitance value of the example reference circuit do not provide any guarantees against the operation in the mass-production design.
• It consults with the oscillator manufacturer about values of limiting resistor and load capacitance.

[Reference Information on Application]
• Usually, the oscillation amplifier is set to be stopped automatically, when PLL locks. This intends to avoid the oscillation amplifier clock from interfering with PLL clock in order to obtain the maximum jitter performance.
• AMPOPR register always sets oscillation amplifier as continuous action regardless of PLL state. This setting can read the calculation result of the input sampling frequency which followed input data, even if a sampling frequency changes the input data from which the sampling information on channel status does not change within PLL capture range. However, since oscillation amplifier will be in an operating state also during PLL locks, the clock jitter performance gets worse.

1-3. PLL Loop Filter Setting (LPF)

• LC89091JA incorporates a PLL. LPF is a setting pin for PLL loop filter.

[Notes]

• It uses a film capacitor and resistor of J-level (±5%) error for filter elements.
• It notes that some types of capacitors have extremely poor temperature characteristics and voltage-dependent characteristics; although a ceramic capacitor can be used.
• As shown in the figure below, 0.022µF capacitor for eliminating high frequency is allocated closer to the LC89091JA than 0.1µF and 100Ω.

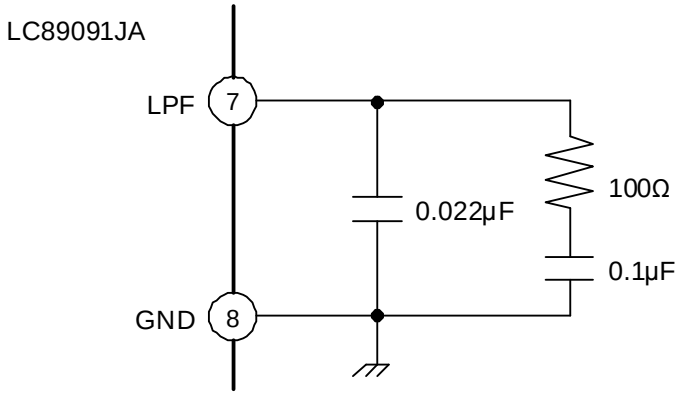


Figure 1-1 Mounting of PLL Loop Filter

1-4. MPIO Input Setting

• MPIO is an input/output pin and is possible an emphasis flag output or S/PDIF data input by register setting.
• MPIO output is the open-drain. (When using it as an output, a pull-up resistor needs.)
• MPIO is set as an emphasis flag output after power-on and outputs a "Hi-Z" when S/PDIF data dose not input. However, "L" will be outputted, if S/PDIF data is inputted and emphasis information is detected.
• The following notes has to follow when using MPIO as an input

[Notes]

• MPIO is changed to an input by MPSEL register.
• MPSEL register has to set while MPIO outputs a "Hi-Z".
• Dose not input S/PDIF data into RXIN until setting of MPSEL register is completed. If S/PDIF data with emphasis information inputs into RXIN, MPIO will output "L". For this reason, MPIO shorts out with output of a peripheral circuit part (optical module etc.).
• When using MPIO in an input, a pull-up resistor is unnecessary. (But, dose not become input open state)
• When not using a microcontroller, MPIO cannot be set as an input. Therefore, it becomes an output function.

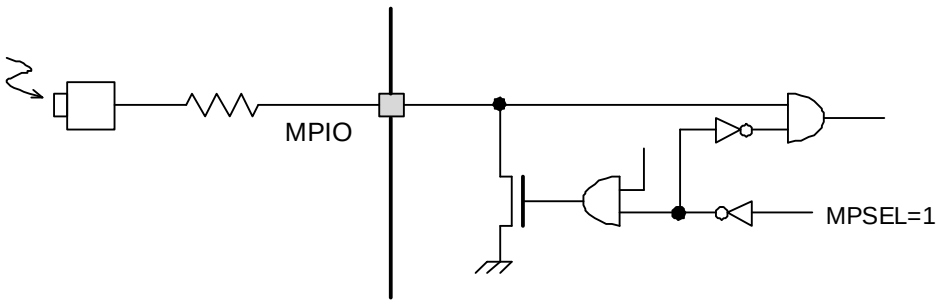


Figure 1-2 Input Setting of MPIO

1-5. Data Input to SDIN (A/D Converter Connection Example)

- SDIN is a serial audio data input pin.
- SDIN input data recommends the same format as demodulation data output.
- There is no format conversion function of SDIN input data.
- When PLL unlocks, DATAO output data switches from demodulation data to SDIN input data automatically.
- When not using SDIN, it connects with GND.

[Reference Information on Application]

- The example of the A/D converter (ADC) connection explains below.

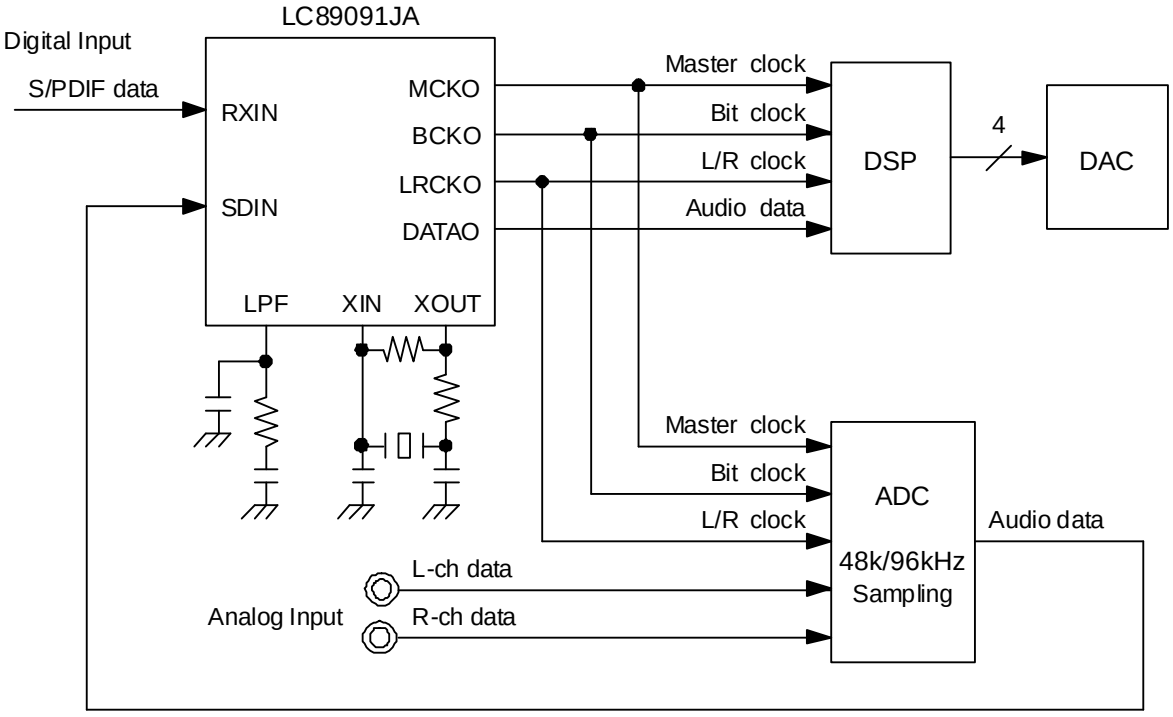
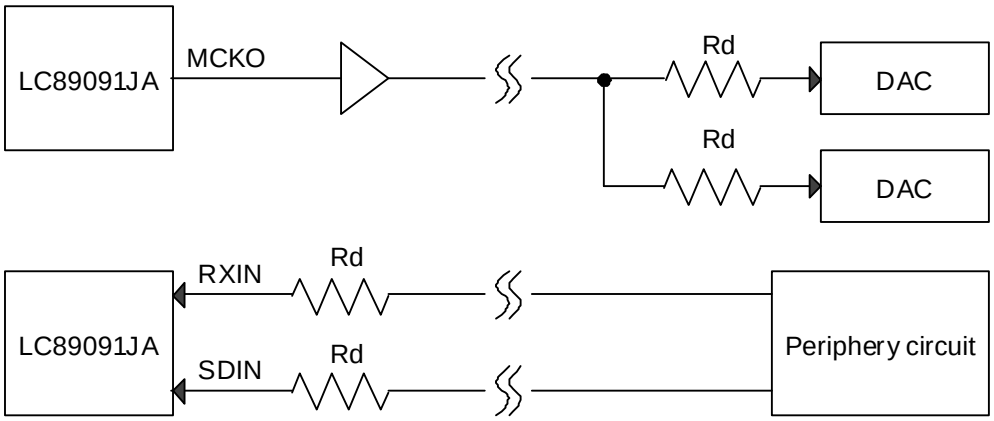


Figure 1-3 Example of A/D Converter Connection (Serial Data Input to SDIN)

- The ADC is slave operation. The clock supply to the LC89091JA from the ADC (ADC master operation) cannot be performed.
- The clock frequency from the LC89091JA to the ADC is set by XOUTCK register.
- XIN source clock supplies to ADC when PLL unlock, and PLL source clock supplies to ADC when PLL lock.
- In PLL unlocking operation process, PLL free-run clock output from MCKO, 2.7ms period that is while switching from PLL source clock to XIN source clock. (3-3-1-4 Reference) Although there is change of frequency, output clock holds continuity and switches. However, when this output clock affects the ADC operation, the ADC side needs to do reset processing.

1-6. Notes on Connecting Peripheral Devices

- The waveform dulls due to input gate capacities of devices when several devices are connected to output pin of the LC89091JA.
- A thin and long print pattern is also a factor to generate ringing in the waveform.
- As these depend on the mounting situation, a waveform at the input pin of the destination is measured with an FET probe for a low input capacity with high frequency. If the waveform is significantly dulled, please perform an appropriate operation such as inputting buffer to the LC89091JA output.
- Also, if the waveform has many ringings, insert a dumping resistor of ten to several hundreds ohm to the input pin side of the device where the signal is entered. Since the dumping resistor with too large resistance value makes the waveform dull and leads to deterioration of jitter performance, the resistance values shall be set to the minimum value.



*1: The damping resistors (Rd) are entered closest to the input pins.
*2: The buffer is entered closest to the output pin.

Figure 1-4 Insertion of Damping Resistors and Buffer

1-7. I/O buffer Absolute Maximum Ratings

- It is made not to exceed the absolute maximum rating of input/output pins in any states.
- There is possibility of destroying if absolute maximum rating is exceeded.

Table 1-1 Absolute Maximum Ratings of LC89091JA I/O Pins (Vdd=3.0v to 3.6v)

No.	Pin	I/O	Ratings	No.	Pin	I/O	Ratings
1	SCL	I	-0.3 to Vdd+0.3v (max.4.6v^{pp})	8	GND		0v
2	SDA	I	-0.3 to Vdd+0.3v (max.4.6v^{pp})	9	MCKO	O	-0.3 to 4.6v
		O	-0.3 to 4.6v	10	BCKO	O	-0.3 to 4.6v
3	ERR	O	-0.3 to 4.6v	11	LRCKO	O	-0.3 to 4.6v
4	GPO	O	-0.3 to 4.6v	12	DATAO	O	-0.3 to 4.6v
5	RXIN	I	-0.3 to Vdd+0.3v (max.4.6v^{pp})	13	XIN	I	-0.3 to Vdd+0.3v (max.4.6v^{pp})
6	MPIO	I	-0.3 to Vdd+0.3v (max.4.6v^{pp})	14	XOUT	O	-0.3 to 4.6v
		O	-0.3 to 4.6v	15	SDIN	I	-0.3 to Vdd+0.3v (max.4.6v^{pp})
7	LPF	O	-0.3 to 4.6v	16	VDD		-0.3 to 4.6v

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1-8. Microcontroller Interface Setting

- The microcontroller interface of the LC89091JA has adopted I^2C (Fast mode, 400k bps).
- SDA and SCL connecte to I^2C bus. LC89091JA operates on slave.
- A pull-up resistor is indispensable to SDA line.
- SDA line becomes "H" when I^2C bus line is free.
- SCL of the LC89091JA does not have an output function. Therefore, if SCL bus line is not free in any state, a pull-up resistor of SCL line is unnecessary. However, SCL line has to set as normal "H" in order to form Start and Stop conditions of I^2C.
- When not using a microcontorller interface, SCL and SDA connecte to GND.

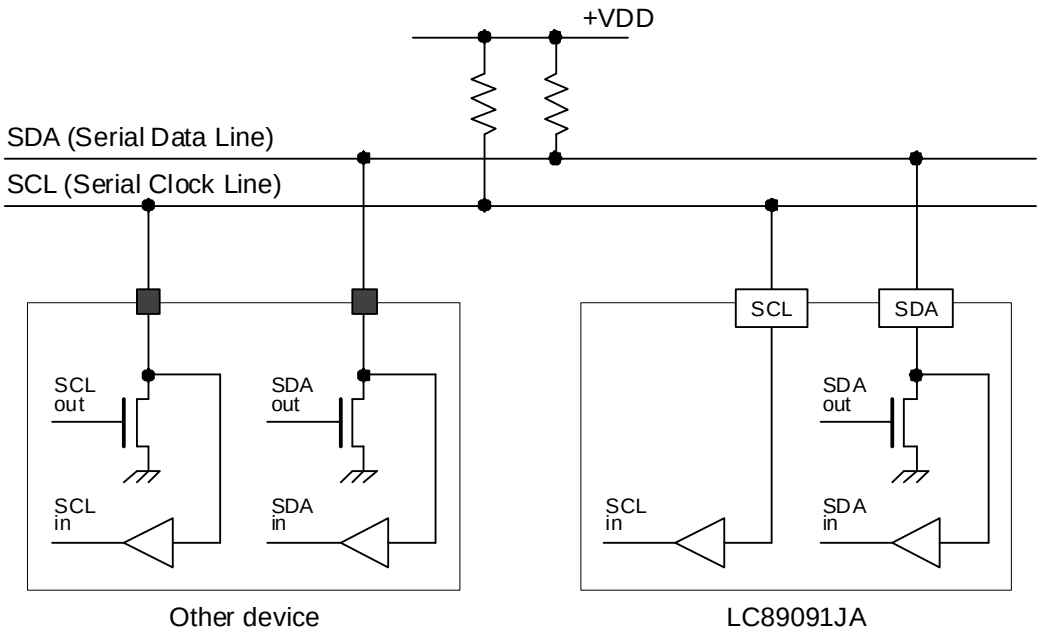


Figure 1-5 Connection of LC89091JA to I^2C Bus

1-9. Notes on when Microcontroller dosen't Use

- LC89091JA can be used in the initialization state of registers without being connected with microcontroller.
- SCL and SDA connect to GND.
- The S/PDIF digital input is only one system (RXIN).
- The S/PDIF of 32kHz to 192kHz sampling frequency can be receiving. But, input sampling frequency calculation value is not outputted.
- According to the sampling frequency of input data, output clock frequency is controlled automatically.

Table 1-2 Output Clock Frequency When not Using Microcontorller (Unit: Hz)

S/PDIF input	When PLL is locked Output clock frequency (automatic control)			When PLL is unlocked, Output clock frequency (XIN)
	MCKO	BCKO	LRCKO	
32k	16.3840M	2.0480M	32k	MCKO 24.576M BCKO: 6.144M LRCKO: 96k
44.1k	22.5792M	2.8224M	44.1k	
48k	24.5760M	3.0720M	48k	
64k	16.3840M	4.0960M	64k	
88.2k	22.5792M	5.6448M	88.2k	
96k	24.5760M	6.1440M	96k	
128k	16.3840M	8.1920M	128k	
176.4k	22.5792M	11.2896M	176.4k	
192k	24.5760M	12.2880M	192k	

- Oscillating circuit is configured that connection of a crystal oscillator or a clock input of external oscillation module.
- XIN always supplies 24.576-MHz clock.
- Oscillation amplifier is automatically stopped during PLL lock.
- Data output of DATAO and data input to SDIN are I^2S audio data format.
- Clock and data change automatically according to the state of PLL.
- Non-PCM information of bit 1 of the channel status outputs from GPO.
- Emphasis information of 50/15μs for consumer of the channel status outputs from MPIO.
- MPIO configures an open-drain output. MPIO needs a pull-up resistor.
- Input condition and output function when not using a micricintroller show to below.

Table 1-3 Input Condition and Output Function When not Using Microcontroller

No.	Name	I/O	Input condition Output function	No.	Name	I/O	Input condition Output function
1	SCL	I	Conect to GND	9	MCKO	O	Master clock output (auto)
2	SDA	I	Conect to GND	10	BCKO	O	Bit clock output (64fs)
3	ERR	O	PLL lock error flag output	11	LRCKO	O	LR channel clock output (fs)
4	GPO	O	Non-PCM flag output	12	DATAO	O	Audio data output
5	RXIN	I	S/PDIF input	13	XIN	I	Conect to crystal
6	MPIO	O	Emphasis flag output	14	XOUT	O	Conect to crystal
7	LPF	O	Conect to PLL loop filter	15	SDIN	I	External audio data input
8	GND		Conect to GND	16	VDD		3.3V power supply

2. System Reset

• LC89091JA is possible to do “power-on reset”, “register reset” and “power-down mode”

2-1. Power-on Reset

• LC89091JA features a built-in power-on reset circuit, and constantly monitors the power supply status.
• All the circuits are initialized by a power on reset.
• The timing chart of the power-on reset circuit shows to below.

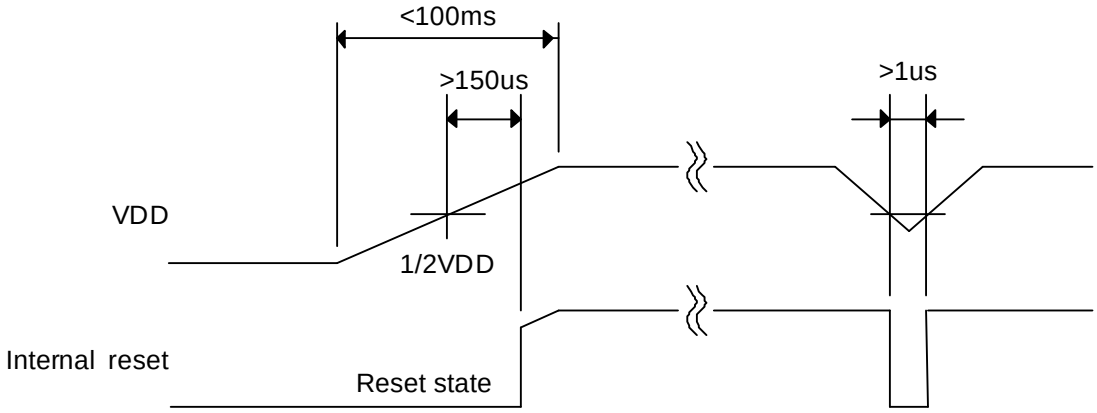


Figure 2-1 Power-on Reset Timing Chart

Table 2-1 Each Output pin State after Power-on Reset

Pin No.	Name	Output state	Pin No.	Name	Output state
3	ERR	H output	10	BCKO	XIN/4 output (6.144MHz)
4	GPO	L output (Non-PCM flag)	11	LRCKO	XIN//256 output (96kHz)
6	MPIO	Hi-Z output (Emphasis flag)	12	DATAO	SDIN output
9	MCKO	XIN output (24.576MHz)	14	XOUT	XIN reverse output

[Notes]
• The slope of power supply voltage is less than 100 ms.

2-2. Registor Reset (Power-down Mode)

• LC89091JA is possible to do "circuit initialization of those other than register" and "power-down mode" by using microcontroller interface. The next chapter “Microcontroller interface” explains register setting.

3. Microcontroller Interface
3-1. Contents of Register

- Using the microcontroller interface makes all functions of the LC89091JA usable.
- All the register setting of the LC89091JA relates to the input/output functions.

Table 3-1 Register Map of LC89091JA

R/W	Adr	D7	D6	D5	D4	D3	D2	D1	D0
R/W	00h	"0"	MPSEL	DATWT	ERRWT	ADMODE	AMPOPR	PDMODE	SYSRST
R/W	01h	"0"	"0"	XOUTCK	PRSEL1	PRSEL0	PLLDIV1	PLLDIV0	PLLACC
R/W	02h	NPMODE	ERRSEL	GPOSEL1	GPOSEL0	DATMUT	THRSEL	DINSEL	DAFORM
R	03h	0	0	0	ERRFLG	FSC3	FSC2	FSC1	FSC0
R	04h	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
R	05h	CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8
R	06h	CS23	CS22	CS21	CS20	CS19	CS18	CS17	CS16
R	07h	CS31	CS30	CS29	CS28	CS27	CS26	CS25	CS24
R	08h	CS39	CS38	CS37	CS36	CS35	CS34	CS33	CS32

·"0" is a reserved bit. Always must be set to "0".

Table 3-2 Register Setting Relevant to Input/Output Functions

Adr.	Register Name	LC89091JA pins										
		ERR	GPO	RXIN	MPIO	MCKO	BCKO	LRCKO	DATAO	XIN	XOUT	SDIN
00h	SYSRST	✓	✓	✓	✓				✓			✓
	PDMODE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	AMPOPR									✓	✓	
	ADMODE	✓	✓	✓	✓	✓	✓	✓	✓			✓
	ERRWT	✓							✓			
	DATWT	✓							✓			✓
	MPSEL				✓							
01h	PLLACC					✓						
	PLLDIV[1:0]					✓						
	PRSEL[1:0]					✓						
	XOUTCK					✓	✓	✓				
02h	DAFORM							✓	✓			
	DINSEL			✓	✓							
	THRSEL		✓									
	DATMUT								✓			✓
	GPOSEL		✓									
	ERRSEL	✓										
	NPMODE								✓			

3-2. Write Registers 1 (System)

3-2-1. SYSRST (Reset All Circuits Other than Registers)

[Initial state]

• LC89091JA is not a reset state.

[Explanation]

• SYSRST register resets circuits other than registers.
• The reset by SYSRST register does not reset other registers. Those register setting states are held.
• SYSRST register reset differs from the power-on reset which initializes all the circuits.
• The oscillation amplifier in the reset period by SYSRST register is an operating state, and clock outputs from each output clock pin.
• DATAO output during reset period is muted.

Table 3-3 Output State of Reset Period by SYSRST (" " is a register name)

Pin No.	Name	Output state	Pin No.	Name	Output state
3	ERR	H output	10	BCKO	"XOUTCK" is followed
4	GPO	"GPOSEL" is followed	11	LRCKO	"XOUTCK" is followed
6	MPIO	"MPSEL" is followed	12	DATAO	L output (Muted)
9	MCKO	"XOUTCK" is followed	14	XOUT	XIN reverse output

3-2-2. PDMODE (Power-down Mode)

[Initial state]

• LC89091JA is not a power-down state.

[Explanation]

• PDMODE register sets power-down mode.
• A power-down mode holds the setting state of register, but an output pin is fixed to "L" or "H" output. All of PLL and an oscillation amplifier circuit stop.

Table 3-4 Output State of Power-down Mode by PDMODE (" " is a register name)

Pin No.	Name	Output state	Pin No.	Name	Output state
3	ERR	H output	10	BCKO	L output
4	GPO	L output (H output when "GPOSEL"=11)	11	LRCKO	L output
6	MPIO	Hi-Z output (L output when "MPSEL"=0)	12	DATAO	L output
9	MCKO	L output	14	XOUT	H output

3-2-3. AMPOPR (Oscillation Amplifier Operation)

[Initial state]

• Oscillation amplifier stops automatically when PLL is locked. (for clock jitter reduction)

[Explanation]

• AMPOPR register sets when always operating oscillation amplifier without relation in PLL state.
• Whenever it sets oscillation amplifier as continuous operation mode, sampling frequency calculation processing of S/PDIF input data is performed without relation in the lock state of PLL.

[Notes]

• Even if it switches AMPOPR register during PLL locking, oscillation amplifier movement does not change. AMPOPR register is performed before the S/PDIF input, or it completes during PLL unlocking.
• The continuous operation mode of oscillation amplifier gets worse jitter, and influences sound quality.

3-2-3-1. Oscillation Amplifier Automatic Stop Function

• This chapter explains the automatic stop function of oscillation amplifier.

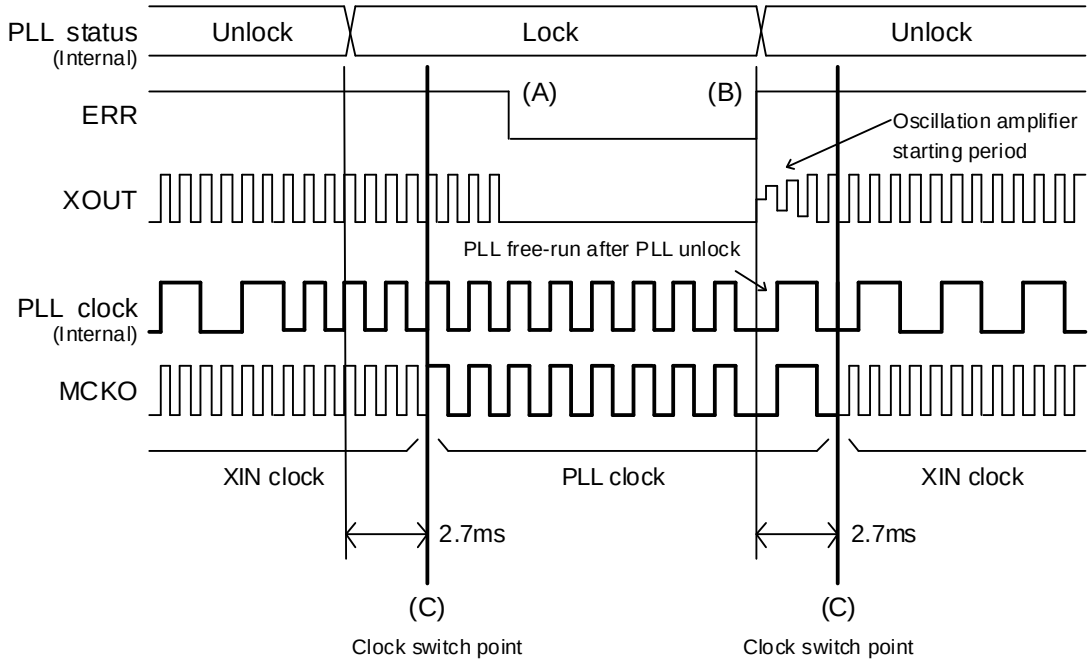


Figure 3-1 Clock Switch Timing Chart 1

• The oscillation amplifier is stopped at the falling edge of ERR in the course of PLL lock-in. (Fig. 3-1 (A))
• The oscillation amplifier operates at the rising edge of ERR in the course of PLL unlock. (Fig. 3-1 (B))
• The clock switches after about 2.7ms from the point of change in PLL state. (Fig. 3-1 (C))
• When PLL changes once again within 2.7ms from the point of change in PLL state, the clock does not switch. When PLL is locked again, the clock switch operation is canceled, and PLL clock output continues. (Fig. 3-2 (C)')

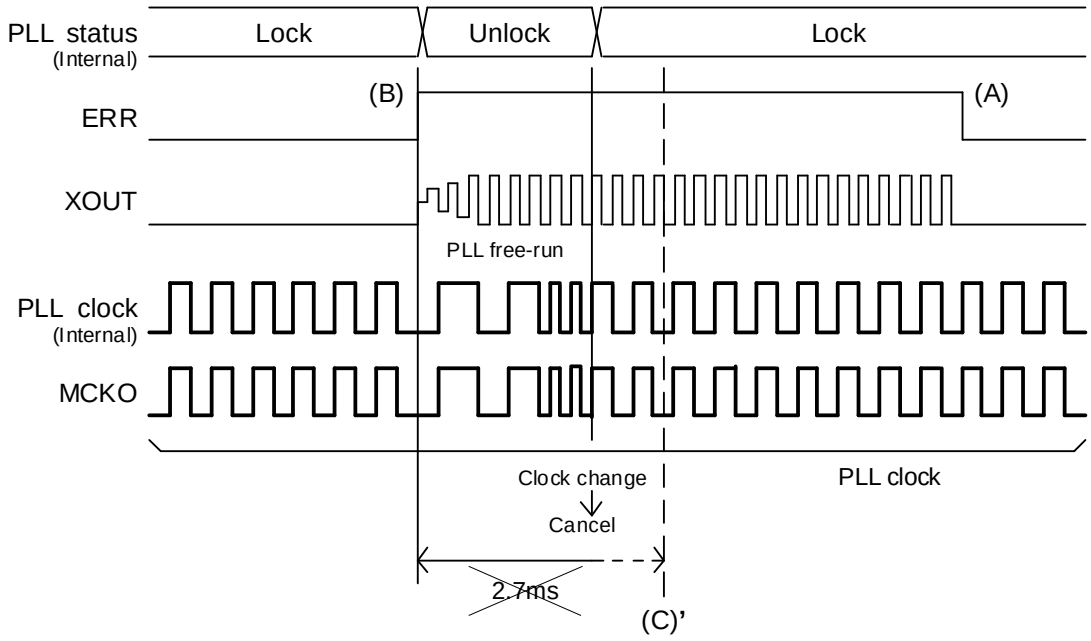


Figure 3-2 Clock Switch Timing Chart 2

3-2-4. ADMODE (S/PDIF Receiving Rejection Mode)

[Initial state]

• LC89091JA receives S/PDIF data, PLL locks, and the system operates with PLL clock.

[Explanation]

• ADMODE register always sets PLL as an unlocking state regardless of S/PDIF data input.
• PLL always is in an unlocking state by setting of S/PDIF receiving rejection mode, and LC89091JA operates with XIN clock. SDIN input data outputs fron DATAO. If data is not outputted to SDIN, DATAO becomes a mute output state.

Table 3-5 Output State of S/PDIF Receiving Rejection Mode by ADMODE (" " is a register name)

Pin No.	Name	Output state	Pin No.	Name	Output state
3	ERR	H output	10	BCKO	"XOUTCK"is followed
4	GPO	"GPOSEL" is followed	11	LRCKO	"XOUTCK" is followed
6	MPIO	"MPSEL" is followed	12	DATAO	SDIN output
9	MCKO	XIN output (24.576MHz)	14	XOUT	XIN reverse output

3-2-5. ERRWT (ERR Wait Time after PLL Lock)

[Initial state]

• PLL locks in S/PDIF input data, the preamble B is counted three times, and ERR error flag cancels ("L" output).

[Explanation]

• A period until ERR error flag is canceled (the preamble B count number) can be changed by ERRWT register.

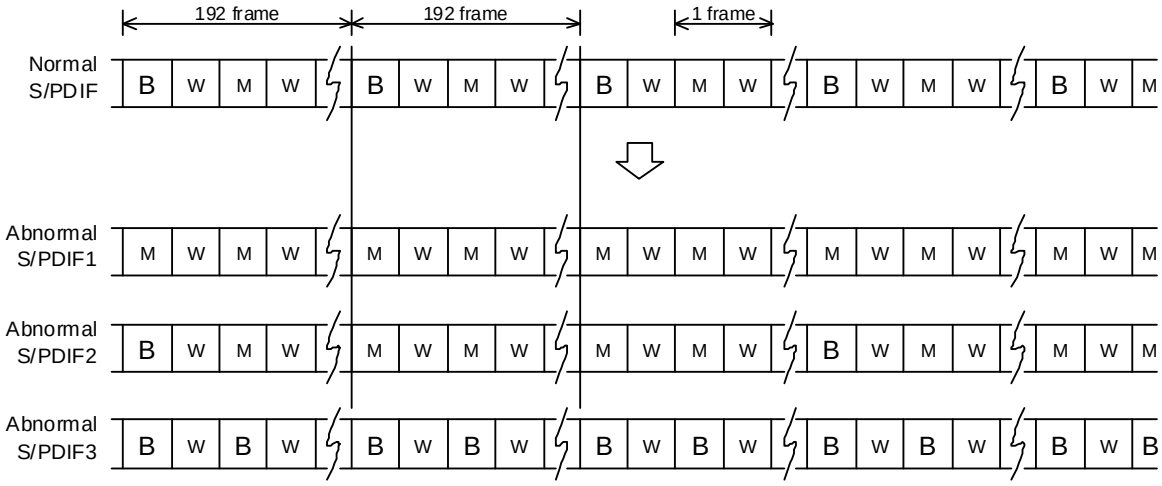
[PLL lock judging method]

• LC89091JA outputs the lock state of PLL from ERR.
• Usually, the ERR outputs "H" when PLL unlock, and outputs "L" when PLL lock.
• PLL synchronizes within 10ms after S/PDIF input.
• A lock judging is performed by detecting the preamble B pattern (192 every frame), after PLL synchronized with S/PDIF and the preamble M pattern (Lch) is detected the whole cycle of the preamble W pattern (Rch).
• ERR is not immediately set to "L" after lock judging. It holds "H" and is set to "L" until the preamble B pattern reaches the count number arranged by ERRWT register.
• The following is a period after S/PDIF is inputted until ERR error flag is canceled.

ERR release period = PLL synchronous period + Lock judging period + "H" maintenance period

[Correspondence to S/PDIF unusual transmission]

• Depending on DVD players, non-IEC60958-compliant S/PDIF may be sent until the playback operation stabilizes. For example, situations that the carrier of the preamble B which must be output for every 192 frames may not be output for a while after power on or that transmission of S/PDIF continues unstably (discontinuous output) may arise.
• The system requires a receiver that does not affect the peripheral circuits even when such an abnormal signal is received.
• The unusual transmitting example of S/PDIF shows to the following next page.



Abnormal S/PDIF1	Preamble B is not transmitted at all.
Abnormal S/PDIF2	Preamble B is irregularly transmitted.
Abnormal S/PDIF3	Preamble B is irregularly transmitted.

Figure 3-3 Abnormal Transmission of S/PDIF

- The LC89091JA determines that the preambles B, M and W are out of synchronization with the input S/PDIF if all these preambles do not conform to the IEC60958. Moreover, even if preambles M and W are appropriately received, the error flag is not cleared unless the preamble B is detected for a number of times set by the ERRWT register. An audio data is not output unless an error flag is released.
- When the carrier receives an unstable S/PDIF with the preamble B count of ERRWT register set to 3, the unstable operation is absorbed by setting to 6 the count of the preamble B if the error flag is output unstably. However, there may be a problem that the beginning of the music is cut off or other problems depending on the systems when ERR release period becomes long. As this depends on the system to be designed, please set an appropriate value to the ERRWT register according to the system to be developed.

3-2-6. DATWT (DATAO Wait Time after PLL Unlocked)

[Initial state]

• When PLL unlocks from the locking state, DATAO outputs SDIN input data after progress during the mute period for about 5.4ms.

[Explanation]

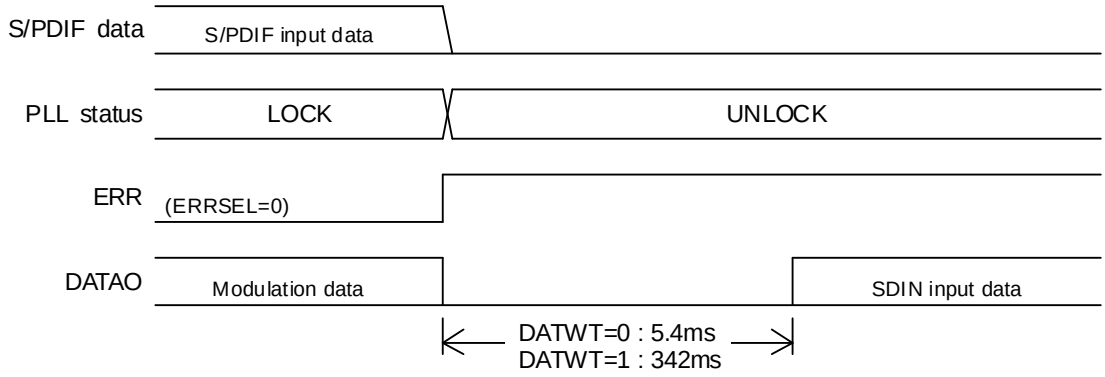
• The mute period of DATAO output data can change by DATWT register.
• This mute period counts with the 48-kHz clock generated from the XIN clock.

Table 3-6 DATAO Output Data Mute Period (XIN=24.576 MHz)

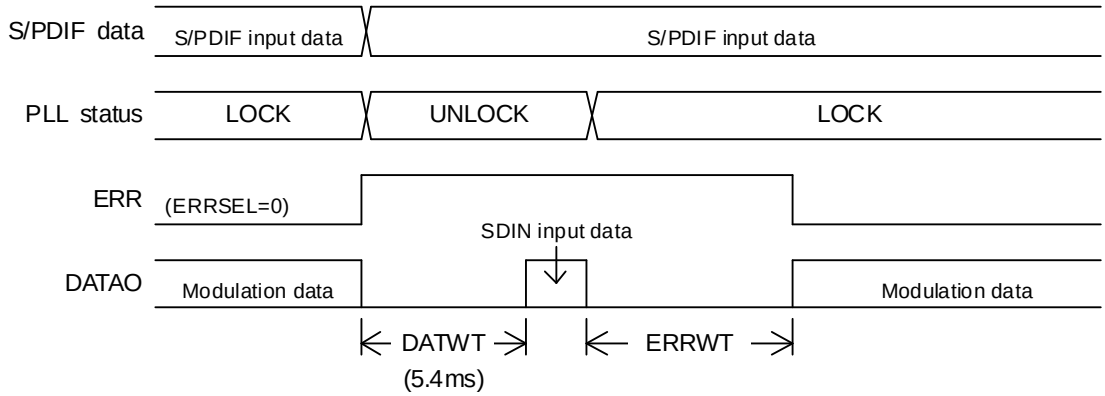
DATWT register	48kHz clock count number	Mute period (ms)
0	256	5.4
1	16384	342

[Notes]

• The period arranged by DATWT register appears after PLL unlocking (Fig. 3-4 (a)).
• When PLL re-locks after unlocking, the setting of output data mute period switches to ERRWT register after PLL re-lock (Fig. 3-4 (b)).



(a) When PLL unlocking state continues after PLL unlocked



(b) When PLL locking state continues after PLL re-locked (DATWT=0)

Figure 3-4 Output Data Mute Timing Chart 1

[Reference Information on Application]

- When detection of a preamble B signal takes time after switching S/PDIF input data, SDIN data may be outputted to the interval which switches like Fig. 3-4 (b). (For example: preamble B cycle is 6ms when fs=32kHz)
- When this SDIN data becomes a problem, please set it as DATWT=1. Thereby, when switching S/PDIF data, SDIN data becomes is hard to be outputted. (This operation is unnecessary if there is no data input to SDIN.)

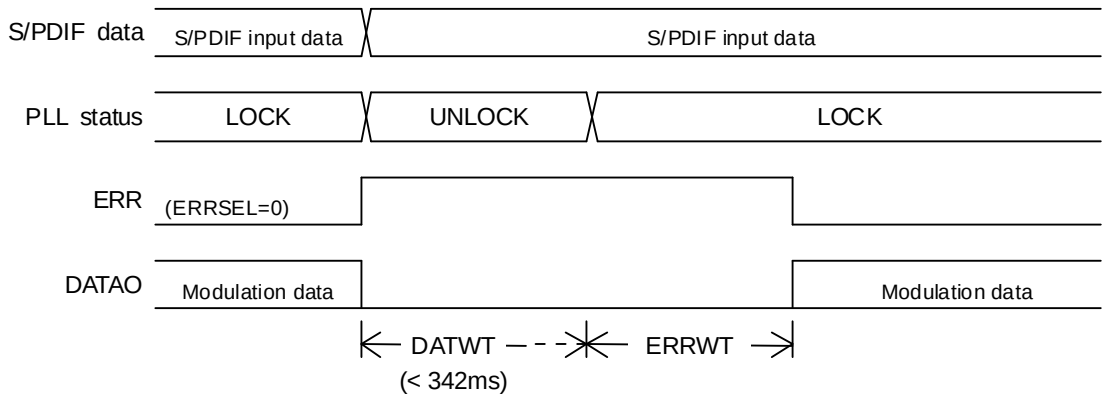


Figure 3-5 Output Data Mute Timing Chart 2

3-2-7. MPSEL (MPIO Setting)

[Initial state]

- MPIO outputs the emphasis flag of channel status.

[Explanation]

- MPIO is set as an input or an output by MPSEL register.

Table 3-7 Setting of MPIO

MPSEL register	I/O	Function
0	Output	Emphasis flag output of channel status
1	Input	S/PDIF data input for TTL input level

[Notes]

- When MPIO is set as an output, a pull-up resistor inserts
- When MPIO is no-load at an output setup, do not choose MPIO by DINSEL or THRSEL register.

[Reference Information on Application]

- Please refer to 1-4, 4-1, and 4-2 for the details of MPIO.

3-3. Write Registers 2 (Clock)

3-3-1. PLLACC, PLLDIV[1:0], and PRSEL[1:0] (PLL and X'tal Clock Setting)

[Initial state]

- PLL clock output frequency is automatically controlled according to an input sampling frequency. (Variable multiple output)
- MCKO output clock frequency to an input sampling frequency is below.

Table 3-8 MCKO Output Clock Frequency

Input sampling frequency (fs)	MCKO output clock frequency
32kHz, 44.1kHz, 48kHz	512fs
64kHz, 88.2kHz, 96kHz	256fs
128kHz, 176.4kHz, 192kHz	128fs

[Explanation]

- MCKO output clock frequency when the PLL is locked is selected from the following two types.
  1) Variable multiple output (set by PLLACC and PLLDIV[1:0] register)
  2) Fixed multiple output (set by PLLACC and PRSEL[1:0] register)

3-3-1-1. Variable Muliple Output

- Outputs a clock of the frequency obtained by multiplying the calculation result of the input fs by the constant value previously set.
- The frequency of the output clock can be set to narrow band against the data receiving of 32kHz to 192kHz.
- This is the same output form as the existing DIR, LC89058 and LC89075.

[How to set the variable multiple output]

- PLLACC register is set as 0.
- Determine the output clock frequency by PLLDIV[1:0] register.
- The table below lists the input fs and the output clock frequencies.
- All fs out of calculation range when the PLL is locked are output with the 256fs clock.

Table 3-9 PLL Clock Output Frequency When PLLACC=0 (figures in [ ] are multiples)

S/PDIF Input frequency (Hz)	PLLDIV[1:0]=00 (Hz)	PLLDIV[1:0]=01 (Hz)	PLLDIV[1:0]=10 (Hz)	PLLDIV[1:0]=11 (Hz)
32k	16.3840M [512fs]	8.1920M [256fs]	16.3840M [512fs]	8.1920M [256fs]
44.1k	22.5792M [512fs]	11.2896M [256fs]	22.5792M [512fs]	11.2896M [256fs]
48k	24.5760M [512fs]	12.2880M [256fs]	24.5760M [512fs]	12.2880M [256fs]
64k	16.3840M [256fs]	16.3840M [256fs]	32.7680M [512fs]	32.7680M [512fs]
88.2k	22.5792M [256fs]	22.5792M [256fs]	45.1584M [512fs]	45.1584M [512fs]
96k	24.5760M [256fs]	24.5760M [256fs]	49.1520M [512fs]	49.1520M [512fs]
128k	16.3840M [128fs]	16.3840M [128fs]	16.3840M [128fs]	16.3840M [128fs]
176.4k	22.5792M [128fs]	22.5792M [128fs]	22.5792M [128fs]	22.5792M [128fs]
192k	24.5760M [128fs]	24.5760M [128fs]	24.5760M [128fs]	24.5760M [128fs]
Other	[256fs]	[256fs]	[256fs]	[256fs]

[For example]

- PLLACC=0, PLLDIV[1:0]=00

  When receiving 48kHz data: MCKO=24.576MHz output
  When receiving 88.2kHz data: MCKO=22.579MHz output
  When receiving 176.4kHz data: MCKO=22.579MHz output

3-3-1-2. Fixed Muliple Output

- Outputs a clock of the frequency obtained by multiplying the input fs by the fixed constant value.
- This is the same output form as the existing DIR, LC89056, LC890561, and LC89057.

[How to set the fixed multiple output]

- PLLACC register is set as 1.
- Determine the output clock frequency by PRSEL[1:0] register.
- The table below lists the input fs and the output clock frequencies.

Table 3-10 PLL Clock Output Frequency When PLLACC=1 (figures in [ ] are multiples)

S/PDIF Input frequency (Hz)	PRSEL[1:0]=00 (Hz)	PRSEL[1:0]=01 (Hz)	PRSEL[1:0]=10 (Hz)	PRSEL[1:0]=11 (Hz)
32k	8.1920M [256fs]	16.3840M [512fs]	4.0960M [128fs]	Reserved Don't use.
44.1k	11.2896M [256fs]	22.5792M [512fs]	5.6448M [128fs]	
48k	12.2880M [256fs]	24.5760M [512fs]	6.1440M [128fs]	
64k	16.3840M [256fs]	32.7680M [512fs]	8.1920M [128fs]	
88.2k	22.5792M [256fs]	45.1584M [512fs]	11.2896M [128fs]	
96k	24.5760M [256fs]	49.1520M [512fs]	12.2880M [128fs]	
128k	32.7680M [256fs]	65.5360M [512fs]	16.3840M [128fs]	
176.4k	45.1584M [256fs]	90.3168M [512fs]	22.5792M [128fs]	
192k	49.1520M [256fs]	98.3040M [512fs]	24.5760M [128fs]	
Other	[256fs]	[512fs]	[128fs]	

[For example]

- PLLACC=1, PLLDIV[1:0]=00

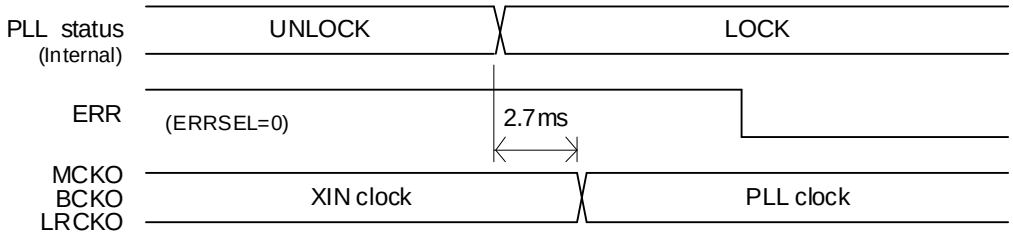
When receiving 48kHz data: MCKO=12.288MHz output
When receiving 88.2kHz data: MCKO=22.579MHz output
When receiving 176.4kHz data: MCKO=45.158MHz output

3-3-1-3. Notes on PLL Clock Setting

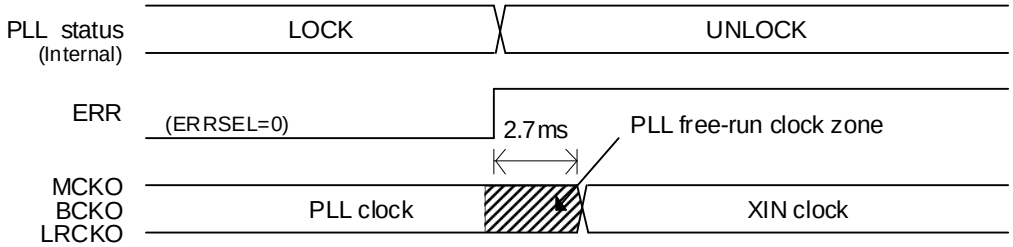
- Even if it switches PLLACC register during PLL lock, an output clock does not change. It recommends completing setting of PLLACC register during PLL unlocking.
- When PRSEL[1:0] =01 is set in the state of the fixed muliple output (PLLACC=1) and data of 128 kHz, 176.4 kHz, and 192 kHz is received, MCKO output a clock of 50MHz or more and AC characteristic cannot be guaranteed. Therefore, please make sure not to set the output clock to 512fs (PRSEL[1:0]=01) when receiving 128kHz, 176.4kHz, or 192kHz.
- LC89091JA locks with the 512fs clock constantly unlike the existing DIR. Therefore, PRSEL[1:0] register is set as the dividing ratio of 512fs clock. This changes only output clock when the output frequency is changed by PRSEL[1:0] register in the PLL lock state. However, a temporary gap is developed in the phase between the output data and the clock at this time. Consequently, a noise may be generated. It recommends the setting of variable multiple output (PLLACC=0) in the case that these operations are required. A variable multiple ouput holds continuity and switches a clock so that a phase shift may not arise at the time of the change of input data. This minimizes generating of a noise.

3-3-1-4. PLL Clock Switch Timing

- The output clock witches from the oscillation amplifier clock (XIN clock) to the PLL clock in the PLL lock-in process.
- The output clock witches from the PLL clock to the XIN clock in the PLL unlock process.
- The change of XIN clock and PLL clock is performed about 2.7ms after the PLL state changes. When switching a clock, ERR is "H" output and DATAO is a mute state.



(a): PLL lock-in process



(b): PLL unlock process

Figure 3-6 Clock Change Timing Chart

[Reference Information on Application]

- PLL free-run clock outputs during 2.7ms period until the PLL clock is switched to the XIN clock in the PLL unlock process. Moreover, the setting of PLLACC, PLLDIV [1:0], and PRSEL [1:0] register is held until the clock is switched. For example, when a lock error is generated after the S/PDIF of 96kHz is received with PLLACC=0 and PLLDIV[1:0]=00, MCKO continues to output 256fs (it is half the PLL clock) until the clock is switched. However, when PLL unlocks, the setting state at the lock is held until clock changes and MCKO outputs 1/2 of the PLL free-run clock (5M to 10MHz)
- PLL free-run clock frequency is output as follows by the input data sampling frequency or setting of register. In addition, a clock frequency has the variation in some by any sample.

Table 3-11 MCKO Output until Switche to XIN Clock after PLL Unlocking (PLL free-run clock)

S/PDIF input frequency	PLLACC=0				PLLACC=1		
	PLLDIV [1:0]=00	PLLDIV [1:0]=01	PLLDIV [1:0]=10	PLLDIV [1:0]=11	PRSEL [1:0]=00	PRSEL [1:0]=01	PRSEL [1:0]=10
32k 44.1kHz 48kHz	5M to 10M	3M to 5M	5M to 10M	3M to 5M	3M to 5M	5M to 10M	1M to 3M
64k 88.2kHz 96kHz	3M to 5M	3M to 5M	5M to 10M	5M to 10M	3M to 5M	5M to 10M	1M to 3M
128k 176.4kHz 192kHz	1M to 3M	1M to 3M	1M to 3M	1M to 3M	3M to 5M	5M to 10M	1M to 3M
Other	3M to 5M	3M to 5M	3M to 5M	3M to 5M	3M to 5M	5M to 10M	1M to 3M

Unit:Hz

3-3-2. XOUTCK (BCKO and LRCKO Output when PLL Unlock)

[Initial state]

• BCKO outputs 6.144MHz and LRCKO outputs 96kHz, while the system operates with XIN source clock,

[Explanation]

• When operating with the XIN source clock, BCKO and LRCKO output clock frequency can be changed by XOUTCK register.
• Please choose according to the operating condition of DSP or ADC.

Table 3-12 Output Clock Frequency while PLL Unlocking or XIN Source Clock Operating (XIN=24.576MHz)

Output pin	XOUTCK register	
	0	1
MCKO	24.576MHz	24.576MHz
BCKO	6.144MHz	3.072MHz
LRCKO	96kHz	48kHz

[Notes]

• XIN certainly connects a 24.576MHz oscillator, or always supplies a 24.576MHz clock.
• When clocks other than 24.576 MHz input, there is a possibility of malfunctioning. A guarantee of operation cannot be offered.

3-4. Write Registers 3 (Data)

3-3-1. DAFORM, DATMUT, NPMODE (DATAO Setting)

[Initial state]

• DATAO output data is I^2S format.
• SDIN input data outputs when PLL unlocks, and demodulation data output when PLL locks.
• Output data is not muted except the process in which a clock changes.

[Explanation]

• Please select the output data format of LC89091JA from two types by a setting registers.
• The clock polarity of LRCKO is changed by DAFORM register.

Table 3-13 Setting of DATAO and LRCKO output by DAFORM register

DAFORM register	DATAO output data format	LRCKO output polarity
0	24bits I^2S (initial)	"L": Lch data "H": Rch data
1	24bits MSB first left justified	"L": Rch data "H": Lch data

• DATAO output is muted by DATMUT register. DATMUT register is reflected only DATAO output and other output pins are not influenced (PLL error flag, non-PCM flag output, etc.).
• NPMODE register mutes DATAO output data, when non-PCM data is detected. NPMODE register is reflected only DATAO output and ERR outputs the PLL lock state ("L" output).

[Reference Information on Application]

• SDIN input data can be output to DATAO regardless of the PLL state by ADMODE register.
• NPMODE register detects the bit 1 of channel status (non-PCM data information), and processes output data. In the system not using non-PCM data, the bit stream data output from DATAO is easily muted by NPMODE register. Moreover, the system using non-PCM data can also ease the burden of data processing by this register.

3-4-2. DINSEL, THRSEL (S/PDIF Input/Output Data Setting)

[Initial state]

• S/PDIF data inputs to RXIN. However, the through output of S/PDIF data cannot be outputted.

[Explanation]

• S/PDIF input data to be demodulated is selected by DINSEL register.
• The input pins which can be selected are RXIN and MPIO. MPIO needs an input setting by MPSEL register.
• S/PDIF input data output to GPO is selected by THRSEL register.
• GPO output is set by GPOSEL register.

[Notes]

• When MPIO is no-load at an output setting, don't select MPIO by DINSEL and THRSEL register. When not following this, there is a possibility that current may flow and break superfluously inside the LC89091JA.

[Reference Information on Application]

• Please refer to 1-4, 4-1, and 4-2 for the details of MPIO, and S/PDIF input-and-output selector composition.

3-4-3. GPOSEL[1:0] (GPO Setting)

[Initial state]

• GPO outputs a bit1 of channel status (PCM / non-PCM classification bit).

[Explanation]

• GPO output is set by GPOSEL register.
• GPO can also be set as an extended bit of microcontroller register.

[Notes]

• When setting up GPO function, and MPIO is no-load with an output, a register setting has restrictions.

Table 3-14 GPO Output Function and Register Setting Limitations

Register				GPO output function and register setting limitations
GPOSEL[1:0]	MPSEL	THRSEL	DINSEL	
00	0	0	0	Channel status bit 1 output
	0	×	1	Don't set, when MPIO pin is no-load.
		1	×	
	1	×	×	Channel status bit 1 output
01	0	0	0	RXIN input data output
	0	×	1	Don't set, when MPIO pin is no-load.
		1	×	
	1	0	×	RXIN input data output
		1	×	MPIO input data output
10	0	0	0	"L" output
	0	×	1	Don't set, when MPIO pin is no-load.
		1	×	
	1	×	×	"L" output
11	0	0	0	"H"output
	0	×	1	Don't set, when MPIO pin is no-load.
		1	×	
	1	×	×	"H" output

[Reference Information on Application]

• It is also possible to use GPO as a control signal of peripheral circuitry. Please refer to 4-2 for details.

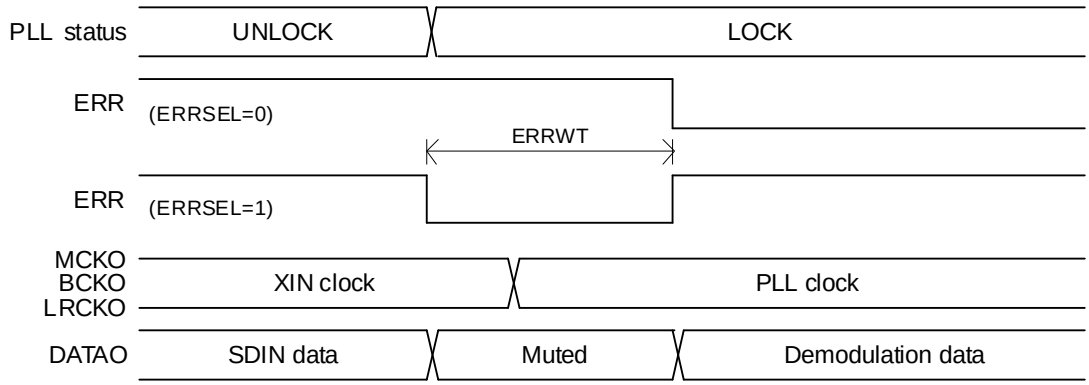
3-4-4. ERRSEL (ERR Setting)

[Initial state]

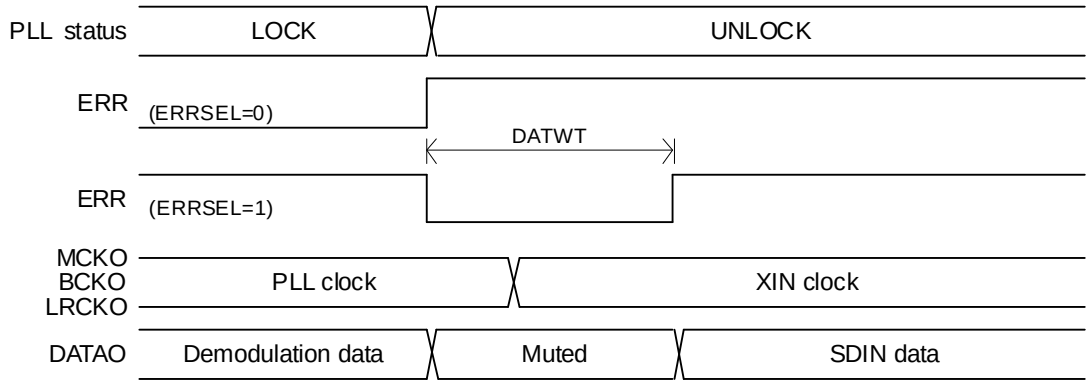
• ERR outputs a PLL lock error and a transmission error (parity error).

[Explanation]

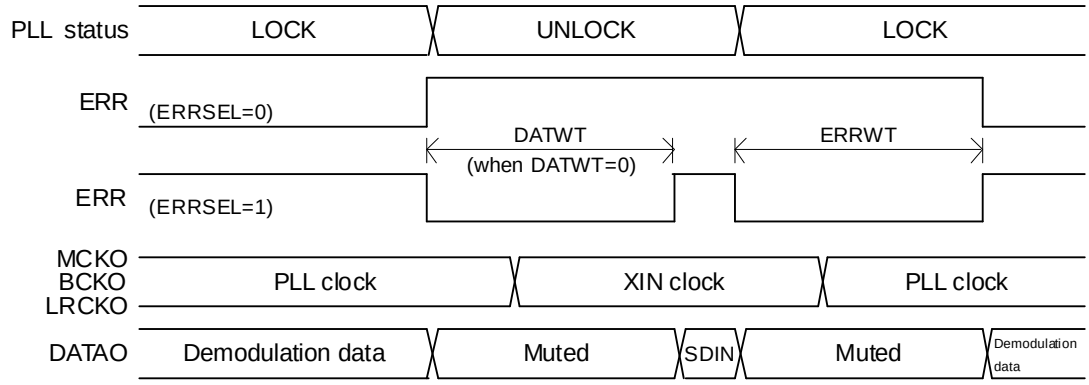
• ERR output is selected by ERRSEL register.
  1) PLL lock error and transmission error (parity error) output. (initial value)
  2) A signal output during DATAO output data mute period.
• When ERR is set as a signal output during the mute period of output data, "L" pulse outputs during the mute period of output data. Furthermore, the change of XIN and PLL clock is performed during the "L" pulse output.



(a): PLL lock-in process



(b): PLL unlock process



(c): PLL unlock and lock process

Figure 3-7 A Signal Output during DATAO Output Data Mute Period Timing Chart

[Reference Information on Application]

- ERR is outputted as both a mute signal and a clock change transient period signal by ERRSEL register. Here, the example of a mute circuit with an analog output signal using this signal is explained.
- Controlling the mute transistor with ERR output (ERRSEL=1) allows noises generated from DAC when the clock is switched to be reduced.
- In this circuit, when ERR turns to "L", a line between a collector and an emitter of the transistor that has been entered to the DAC output is turned on and the audio signal is muted. (An example reverses ERR signal and the mute transistor are controlled.)
- When the analog signal is muted, hfe of the forward direction for the transistor operates for a positive half-cycle mute and the reverse hfe operates for a negative half-cycle mute. Therefore, please use a dedicated mute transistor (for example, 2SC2878) for muting with the larger reverse hfe.
- An offset bias may be generated at the input unit due to a base current at the input phase depending on amplifiers. Since a saturation voltage VCE between the collector and the emitter of the 2SC2878 is small, there is a possibility that the DC bias fluctuates at the moment that the mute is performed when an offset is generated and becomes a pop noise. Therefore, Roff is inserted to reduce the DC bias when the mute is not set. Moreover, if the pop noise still remains, the transistor base is changed slowly by adding Rt and Ct. However, please examine thoroughly as the mute operation is delayed for that period.

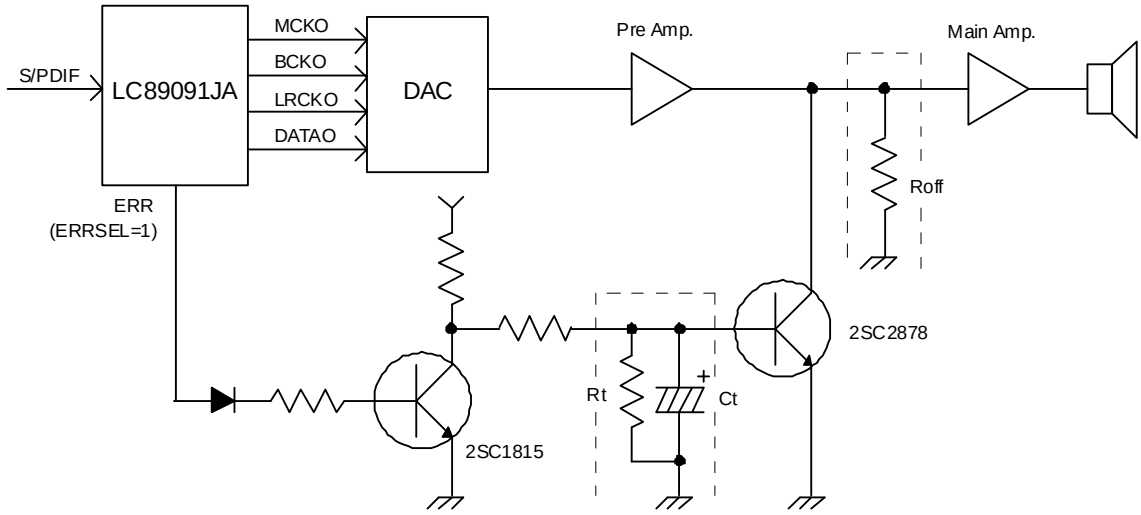


Figure 3-8 Example of Mute Circuit with ERR (ERRSEL=1)

[Notes]

- An output as shown in Fig. 3-7 (c) is not desirable for ERR becomes a control signal of mute transistor. It recommends setting mute output release in 342ms by DATWT register. (Fig. 3-9)

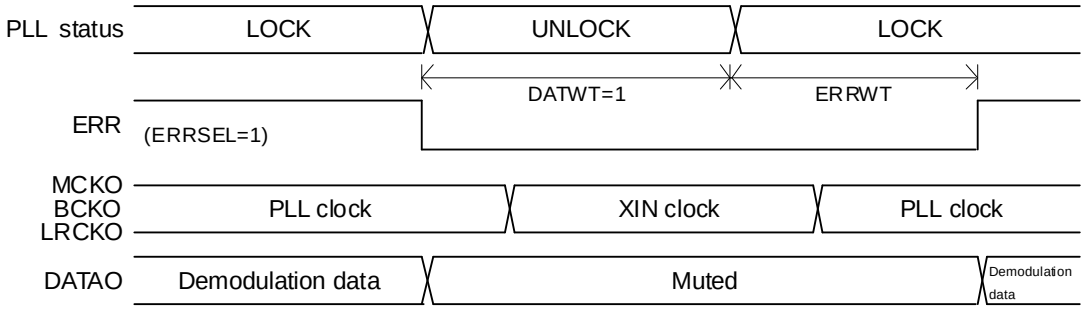


Figure 3-9 ERR Output Timing Chart when DATWT=1 (comparison with Fig. 3-7 (c))

• When ERR is set as ERRSEL=1, ERR output changes before 1 clock period of MCKO from clock change of LRCKO. This is for giving a margin to the timing of data processing (DSP etc) by keeping the edge of ERR signal from overlapping with the clock edge of BCKO or LRCKO.

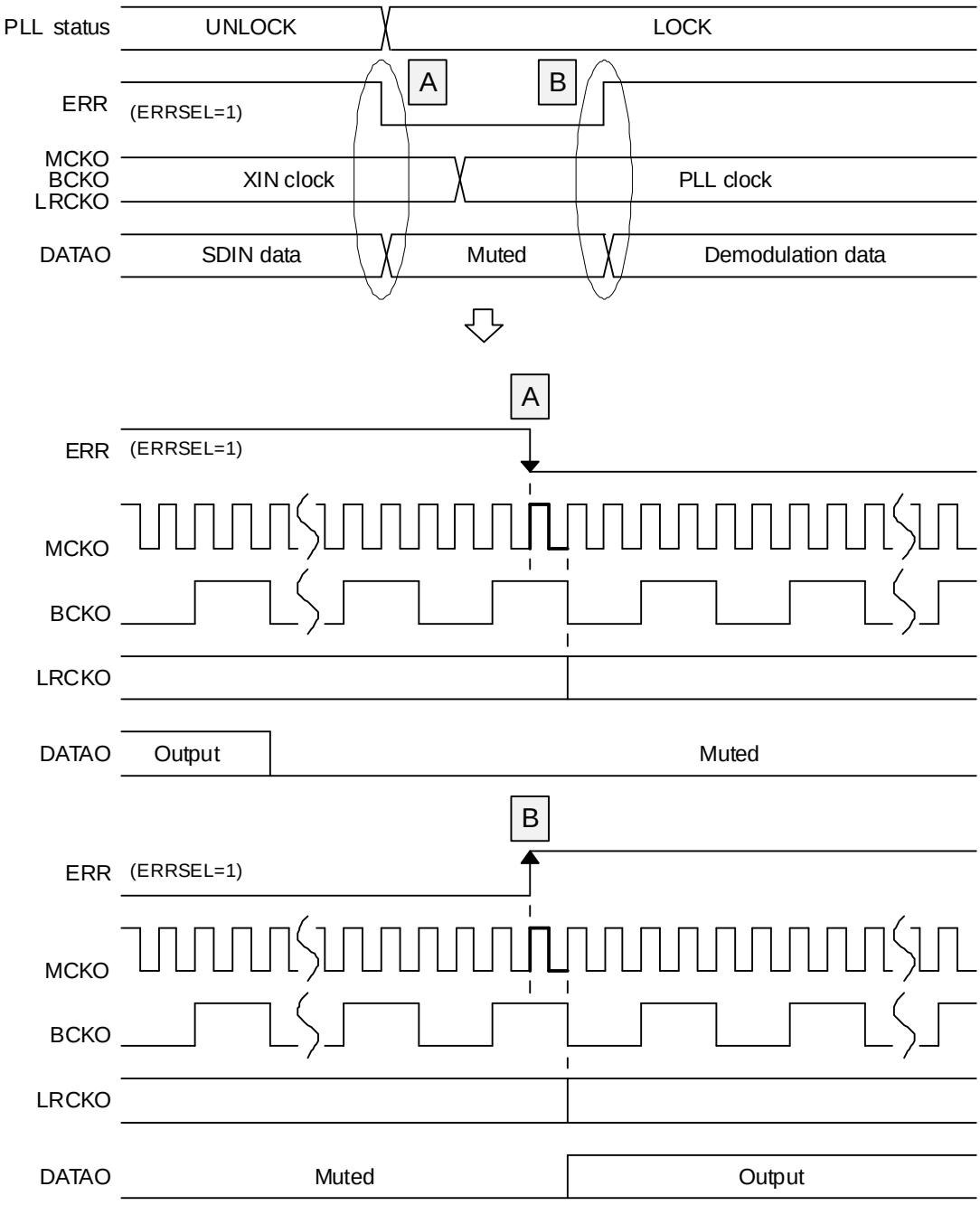


Figure 3-10 ERR Output Timing Chart when ERRSEL=1

3-5. Read Register

3-5-1. FSC[3:0] (S/PDIF Input Data Sampling Frequency Calculation Value)

[Explanation]

• LC89091JA can calculate the sampling frequency of demodulation data, and can read the result with a microcontroller interface. Sampling frequencies can be determined for signals whose sampling frequency information of channel status is not defined in the standards such as IEC60958 and CPR-1205.

Table 3-15 Read of S/PDIF Input Data Sampling Frequency Calculation Result

FSC[3:0]	Input sampling frequency calculation result	FSC[3:0]	Input sampling frequency calculation result
0000	44.1kHz	1000	88.2kHz
0001	Out of range	1001	-
0010	48kHz	1010	96kHz
0011	32kHz	1011	64kHz
0100	-	1100	176.4kHz
0101	-	1101	128kHz
0110	-	1110	192kHz
0111	-	1111	-

[How to calculation and use]

• Usually, calculate an input sampling frequency by using a clock supplied to XIN when PLL is locked and period until ERR error flag is canceled.
• The calculation is performed while PLL is locked in a situation that oscillation amplifier operates constantly.
• The result of fs calculation is stored in FSC[3:0] register.

[Notes]

• When fs of input data is not recognized in the calculation allowable range (fs ±3 to 4%), ERR outputs "H".
• The fs calculation with the setting that stops the oscillation amplifier automatically when the PLL is locked is performed during the H period of ERR. Then, the calculation is completed at the same time as the oscillation amplifier is stopped and the calculated value is retained. Therefore, the calculated value is retained until the PLL gets unlocked, in other words, until the oscillation amplifier starts its operation, and is never changed. Thus, it is not possible to recognize the change in fs to the extent that the PLL is not unlocked.

3-5-2. ERRFLG (Error Output Condition)

[Explanation]

• PLL lock state and transmission error state that are outputted from ERR can be read.
• It can read, also where ERR output is selected as DATAO data mute signal by ERRSEL register.

3-5-3. CS[39:0] (Channel Status Information)

[Explanation]

• The first 40bit channel status data can be read through the microcontroller interface.
• The channel status information that a processing speed against the S/PDIF input is an issue is output from a dedicated pin. This information is updated for every 192 frames.

Table 3-16 Dedicated Pins for Channel Status Data Output

No.	Pin	Channel status data	Output conditions	
			"L" output	"H" output
4	GPO	Bit 1	PCM audio data	Non-PCM audio data
6	MPIO	Bit 0,1,3,4,5	50/15μs pre-emphasis	No pre-emphasis

*: Pull-up resistor is inserted in Pin.6.

4. Additionaliy

4-1. S/PDIF Digital Input and Output Selector Configuration

• LC89091JA configures a maximum of two digital input terminals and one input through output terminal.

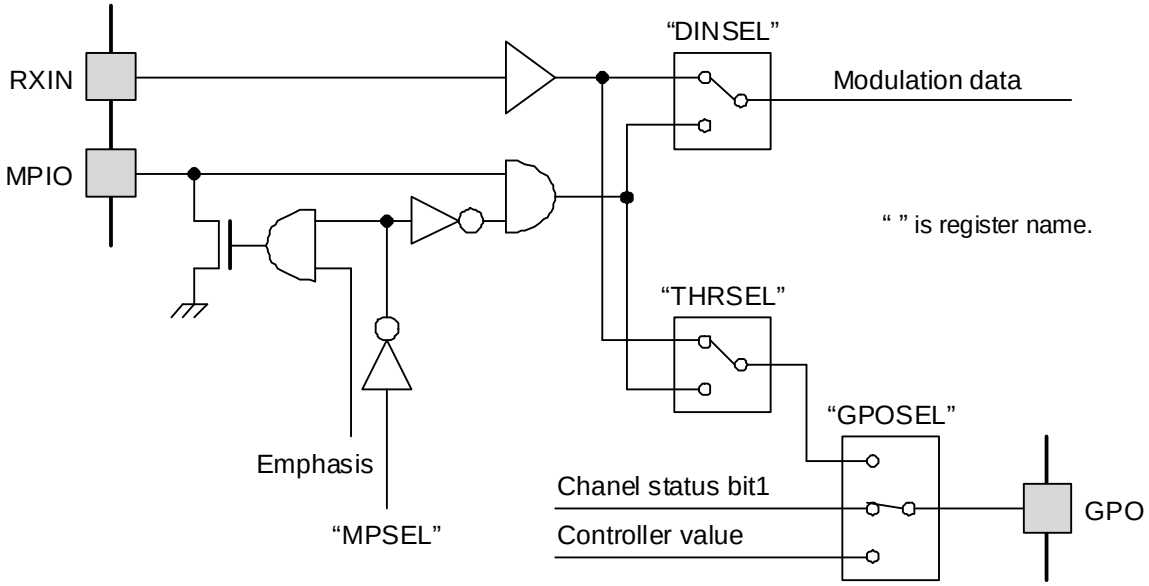


Figure 4-1 Internal Block of LC89091JA Digital Input/Output Terminal

[Setting of two digital input data and how to switch]

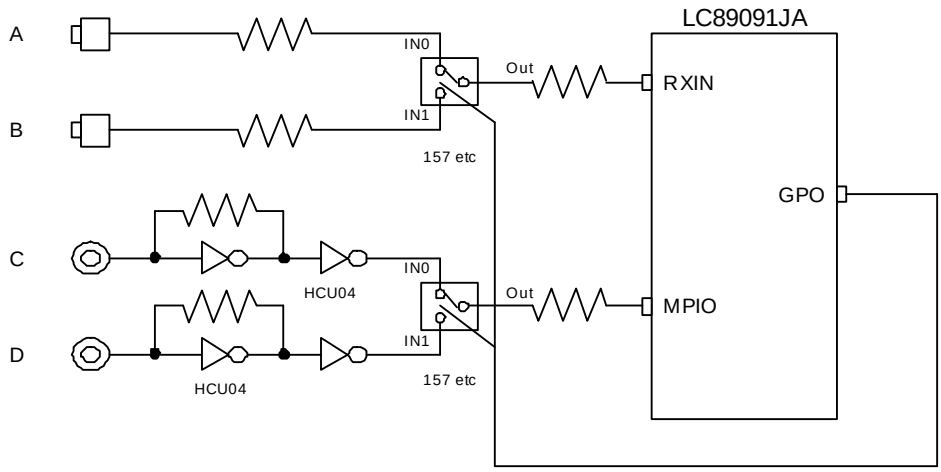
• MPIO immediately after power-on is a Hi-Z output. At first, MPIO sets as S/PDIF input by MPSEL register.
• Demodulation data is selected by DINSEL register.
• GPO output data is selected by THRSEL and GPOSEL register.
• Demodulation data and GPO output data can be selected each and it is possible to use as an output terminal for recording to recorder apparatus, such as DVD.

[Notes]

• GPO cannot output Non-PCM data flag.
• GPO is incapable of driving 75Ω transmission channel (150 Ω load). When a coaxial output is required, please connect a driver that has appropriate driving capability.
• MPIO cannot output an emphasis flag. Please get emphasis information from channel status read-out of microcontroller interface.
• Pull-up resistor is unnecessary for MPIO. However, it is required if MPIO may become to be in an input open state.

4-2. Extpand to S/PDIF Digital Input

- If a switch is prepared for peripheral circuitry, the digital input of a maximum of 4 systems can be configured.
- GPO is used as a control signal of an external selector circuit by GPOSEL register.
- S/PDIF input data (demodulation data) is selected by DINSEL and GPOSEL register.



Register		Demodulation data select	
DINSEL	GPOSEL[1:0]	RXIN	MPIO
0	10	A	×
	11	B	×
1	10	×	C
	11	×	D

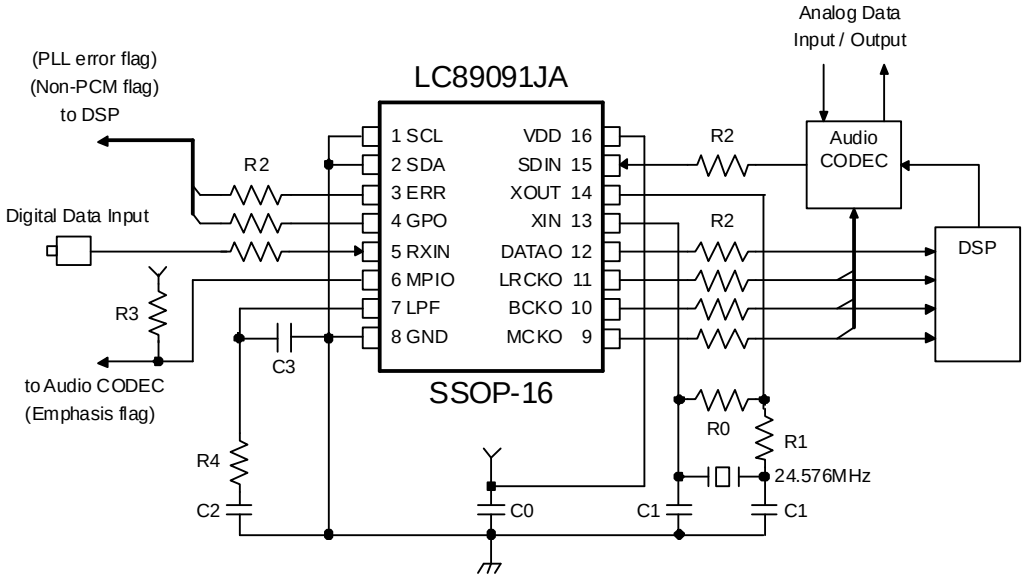
Figure 4-2 Expand to S/PDIF Digital Input by DINSEL and GPOSEL register

[Notes]

- GPO cannot output Non-PCM data flag and S/PDIF through data output.
- MPIO cannot output emphasis flag.

4-3. Application Circuit Example

4-3-1. Connection Example when Microcontroller Interface doesn't Use



Element Symbol	Recommended Parameter	Application
C0	0.01μF to 0.1μF	Power supply de-coupling capacitor
R0	1MΩ	Oscillation amplifier feedback resistor
R1	150Ω to 2.2kΩ	Oscillation amplifier current limit resistor
C1	1pF to 33pF	Quarts resonator load capacitor
R2	0 to 100Ω	Damping resistor
R3	10k to 100kΩ	Pull-up resistor
R4	100Ω	PLL loop filter resistor
C2	0.1μF	PLL loop filter capacitor
C3	0.022μF	PLL loop filter capacitor

Function	Pin name
S/PDIF digital data input	RXIN
S/PDIF digital data output	×
Clock source when PLL unlocked	XIN, XOUT
PLL lock error flag output	ERR
Demodulation data & clock output	MCKO, BCKO, LRCKO, DATAO
External serial audio data input	SDIN
Microcontroller interface input/output	×
Non-PCM flag output (channel status information)	GPO
Emphasis flag output (channel status information)	MPIO

Figure 4-3 For example, when Microcontroller Interface doesn't Use

[Notes]

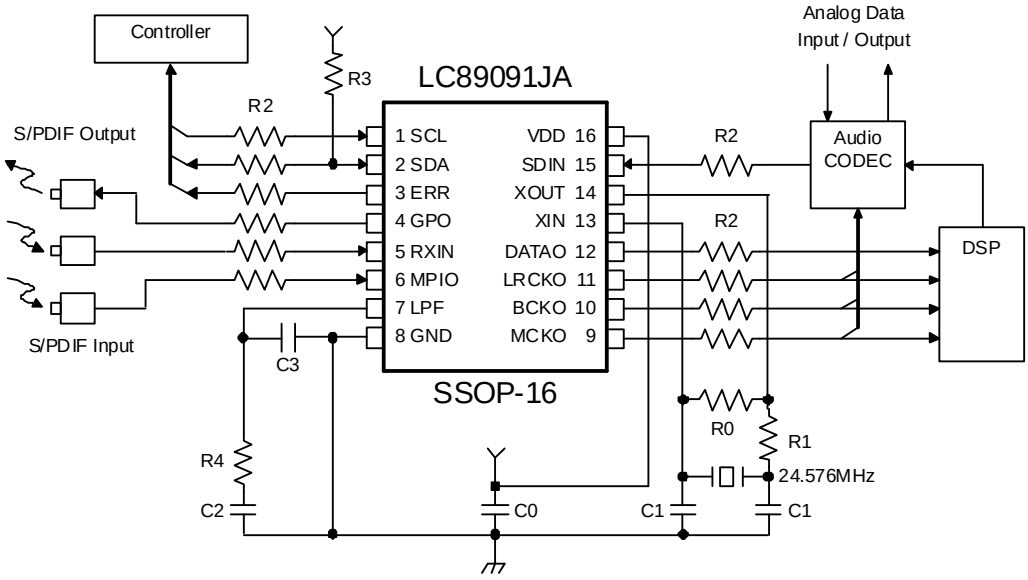
• Although an emphasis flag outputs from MPIO, be careful of polarity.

Table 4-1 MPIO Emphasis Flag Output

MPIO output	Output condition
H *	No emphasis infomation
L	50/15μs emphasis information

*: Pull-up resistor is inserted in MPIO.

4-3-2. Connection Example when Microcontroller Interface Uses



Element Symbol	Recommended Parameter	Application
C0	0.01μF to 0.1μF	Power supply de-coupling capacitor
R0	1MΩ	Oscillation amplifier feedback resistor
R1	150Ω to 2.2kΩ	Oscillation amplifier current limit resistor
C1	1pF to 33pF	Quarts resonator load capacitor
R2	0 to 100Ω	Damping resistor
R3	10k to 100kΩ	Pull-up resistor
R4	100Ω	PLL loop filter resistor
C2	0.1μF	PLL loop filter capacitor
C3	0.022μF	PLL loop filter capacitor

Function	Pin name
S/PDIF digital data input	RXIN, MPIO
S/PDIF digital data output	GPO
Clock source when PLL unlocked	XIN, XOUT
PLL lock error flag output	ERR
Demodulation data & clock output	MCKO, BCKO, LRCKO, DATAO
External serial audio data input	SDIN
Microcontroller interface input/output	SCL, SDA
Non-PCM flag output (channel status information)	×
Emphasis flag output (channel status information)	×

Figure 4-4 For example, when Microcontroller Interface Uses

[Reference Information on Application]

- Non-PCM information and emphasis information on channel status are read with microcontroller interface.
- When receiving non-PCM data and a noise occurs in the delay in system processing, it recommends setting of NPMODE register in advance. If non-PCM data is detected, DATAO output will be in a mute state. The data output which caused the noise can be controlled until non-PCM information is recognized with microcontroller interface.

5. Package Outline Drawing

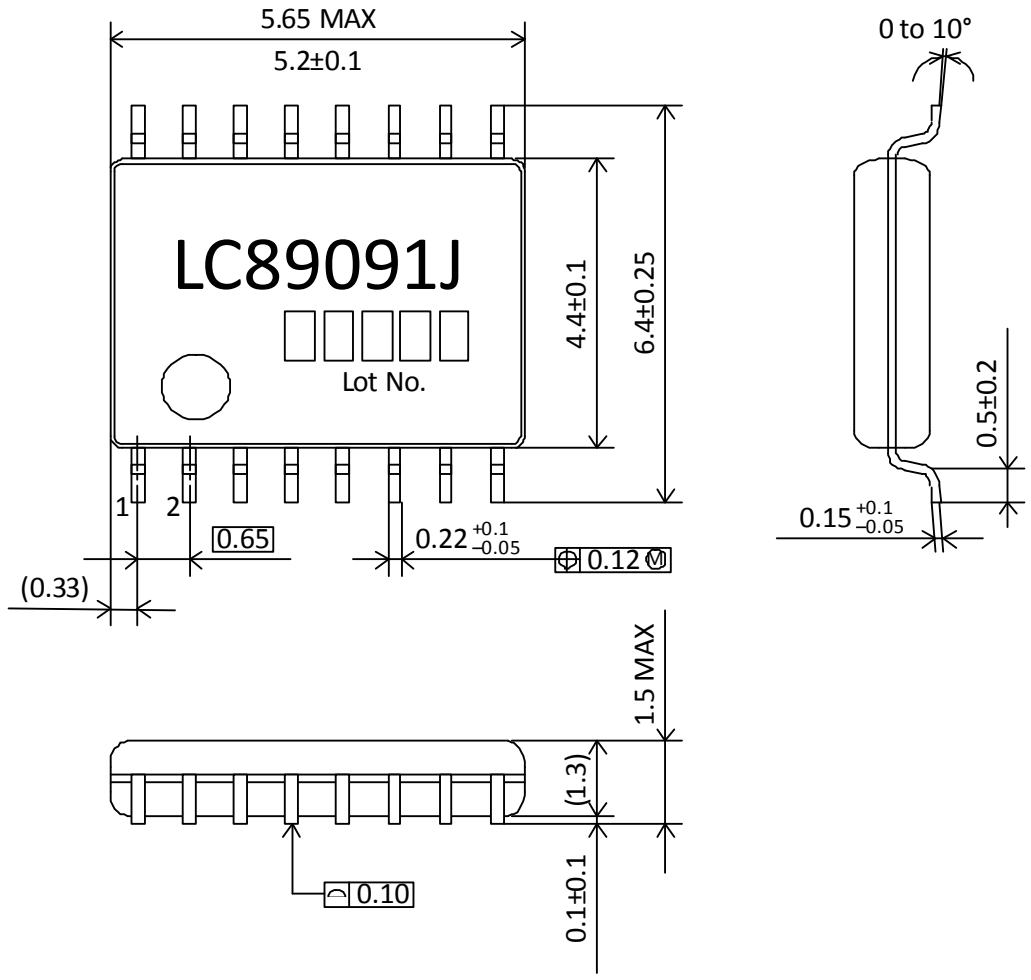


Figure 5-1 LC89091JA Package Outline Drawing (SSOP16, 225mil)

Table 5-1 Material & Lead Finish

Package molding compound	Epoxy
Lead frame material	Cu
Lead frame surface treatment	Solder(Pb free) plate
Mass	0.08g
Compliance	Pb-free, Halide free