LB11868V

Monolithic Digital IC

For Fan Motor

Variable Speed Single-phase Full-wave Pre-driver Application Note

ON Semiconductor®

Overview

LB11868V is a single-phase bipolar driving motor pre-driver with the variable speed function compatible with external PWM signal. With a few external parts, a highly-efficient and highly-silent variable drive fan motor with low power consumption can be achieved. This product is best suited for driving of the server requiring large air flow and large current and the fan motor of consumer appliances.

Function

- Single-phase full-wave driving pre-driver
- Variable speed control possible with external PWM input
- Current limiting circuit incorporated
- Reactive current cut circuit incorporated
- Minimum speed setting pin
- Soft start setting pin
- Start setting pin of on time
- Pch-FET kickback absorption setting pin
- Lock protection and automatic reset circuits incorporated
- FG (rotational speed detection) output, RD (lock detection) output
- Thermal shutdown circuit incorporated

Typical Applications

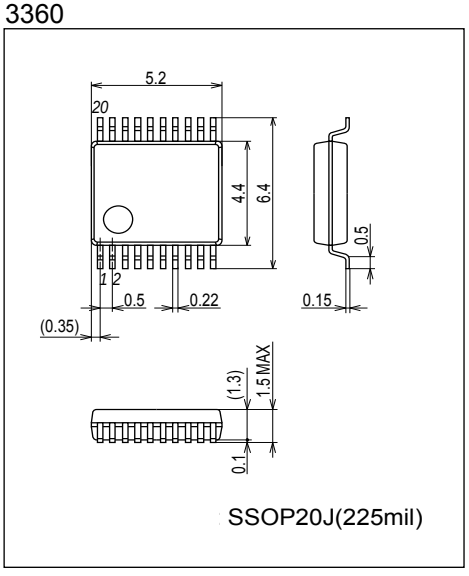
- Server
- Air conditioner
- Projector

Pin Assignment

Package Dimensions

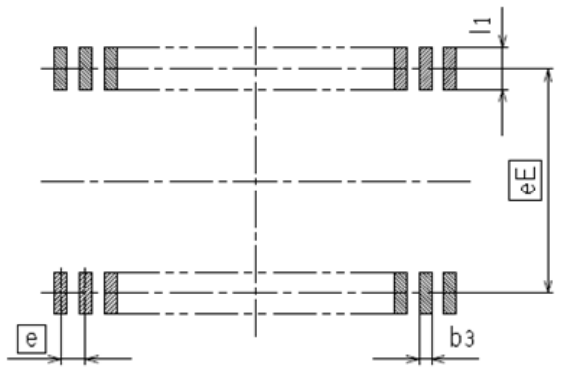
unit : mm (typ)

3360



Caution: The package dimension is a reference value, which is not a guaranteed value.

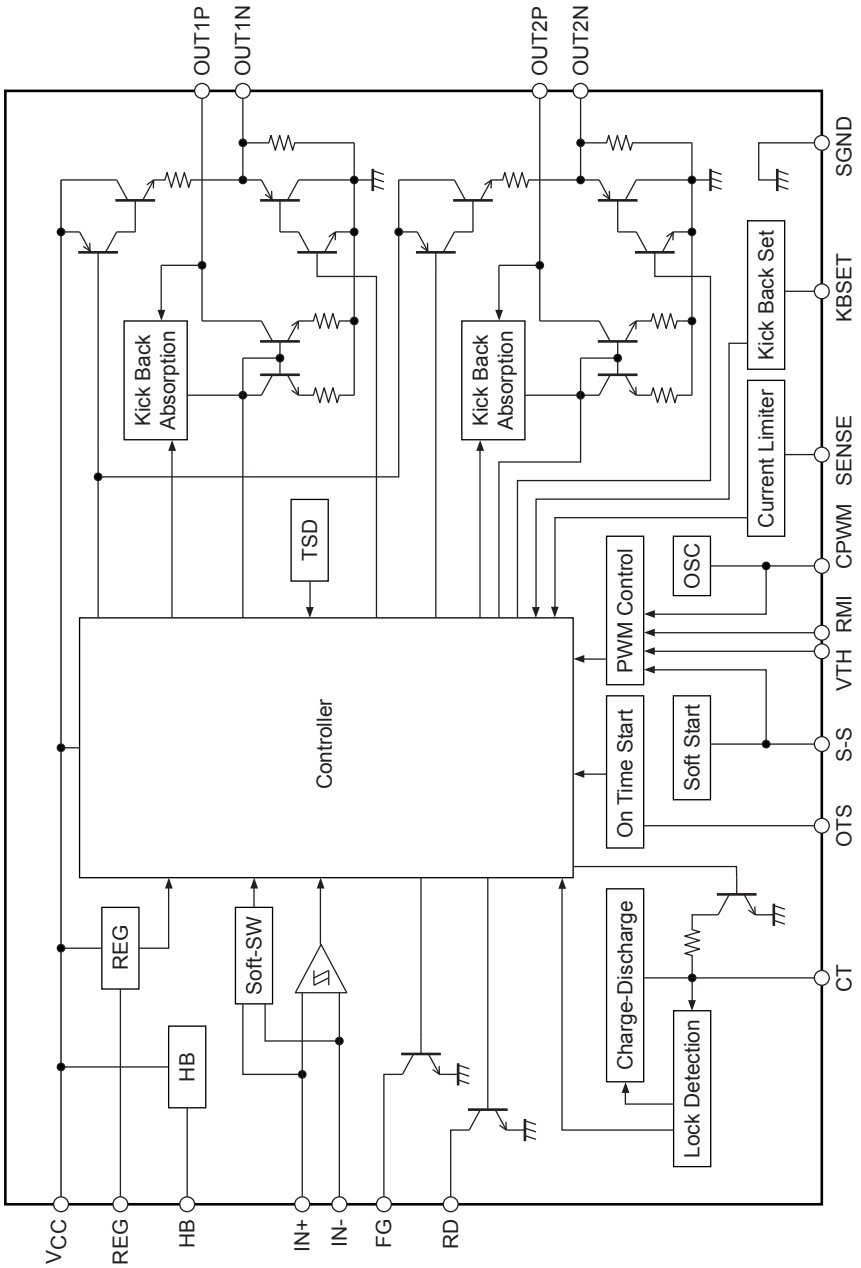
Recommended Soldering Footprint



(Unit:mm)

Reference Symbol	SSOP20J (225mil)
eE	5.80
e	0.50
b3	0.32
l1	1.00

Block diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} pin maximum supply voltage	V_{CC} max		18	V
OUTN pin maximum current	$I_{OUT}N$ max		30	mA
OUTN pin output withstand voltage	$V_{OUT}N$ max		18	V
OUTP pin maximum Sink current	$I_{OUT}P$ max		30	mA
Maximum inflow current at OUTP pin OFF	$I_{OUT}P$ off max	DUTY8% under	10	mA
OUTP pin output withstand voltage	$V_{OUT}P$ max	*1	19	V
VTH/RMI pins withstand voltage	VVTH/VRMI max		7	V
S-S pin withstand voltage	V_{S-S} max		7	V
OTS pin withstand voltage	V_{OTS} max		7	V
KBSET pin withstand voltage	V_{KBSET} max		7	V
FG/RD pin withstand voltage	$V_{FG/RD}$ max		19	V
FG/RD pin maximum Sink current	$I_{FG/RD}$ max		10	mA
REG pin maximum output current	I_{REG} max		10	mA
HB pin maximum output current	I_{HB} max		10	mA
Allowable power dissipation	Pd max	with specified substrate *2	800	mW
Operating temperature	Topr	*3	-30 to 95	°C
Storage temperature	Tstg		-55 to 150	°C

*1 The direct input from the power supply is improper. There must be resistance between OUTP and the power side power supply.

*2 Specified substrate: 114.3mm×76.1mm×1.6mm, glass epoxy board.

*3 Tj max=150°C must not be exceeded.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} Supply voltage	V_{CC}		4.0		16	V
VTH/RMI input voltage range	$V_{TH/RMI}$		0		4.0	V
Hall input voltage range	V_{ICM}		0.2		1.8	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	$I_{CC}1$	During drive	7.5	9.0	10.5	mA
	$I_{CC}2$	During lock protection	6.0	7.6	9.0	mA
REG voltage	V_{REG}	I_{REG} = 5mA	3.65	3.80	3.95	V
HB voltage	V_{HB}	I_{HB} = 5mA	1.14	1.24	1.34	V
Current limiting voltage	V_{LIM}		195	215	235	mV
CPWM pin "H" level voltage	$V_{CPWM}H$		2.35	2.50	2.65	V
CPWM pin "L" level voltage	$V_{CPWM}L$		0.65	0.80	0.95	V
CPWM pin charge current	$I_{CPWM}1$	V_{CPWM} = 0.5V	19	24	29	μA
CPWM pin discharge current	$I_{CPWM}2$	V_{CPWM} = 2.8V	19.5	24.5	29.5	μA
CPWM Oscillation frequency	FPWM	C = 220PF		32		kHz

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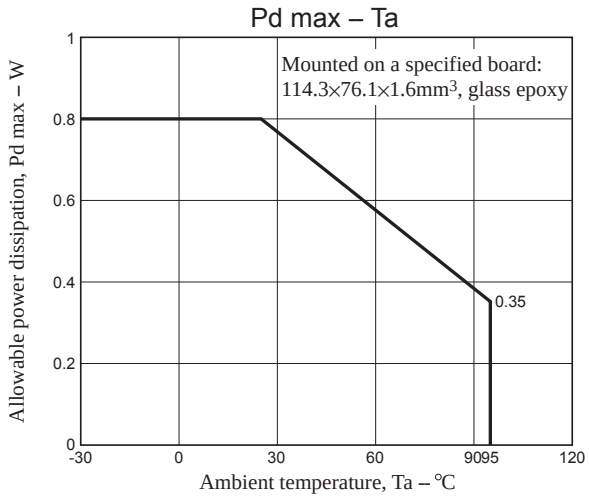
CT pin "H" level voltage	$V_{CT}H$		2.35	2.50	2.65	V
CT pin "L" level voltage	$V_{CT}L$		0.65	0.80	0.95	V
CT pin charge current	$I_{CT}1$	V_{CT} = 0.5V	1.6	2.0	2.4	μA
CT pin discharge current	$I_{CT}2$	V_{CT} = 2.8V	0.16	0.20	0.24	μA
CT pin charge/discharge ratio	R_{CT}	$I_{CT}1/I_{CT}2$	8	10	12	times
S-S pin discharge current	I_{S-S}	V_{S-S} = 1V	0.35	0.45	0.55	μA
OTS pin charge current	$I_{OTS}1$	V_{OTS}=0.5V	0.65	0.85	1.05	μA
OTS pin discharge current	$I_{OTS}2$	V_{OTS}=0.5V	50	58	66	μA
OTS pin threshold voltage	V_{OTS}		1.2	1.3	1.4	V
OUTN output H-level voltage	V_ONH	I_O = 1mA		V_{CC}-0.9	V_{CC}-1.0	V
		I_O = 10mA		V_{CC}-1.9	V_{CC}-2.1	V
OUTN output L-level voltage	V_ONL	IO = 10mA		0.9	1.05	V
OUTP output L-level voltage	V_OPL	IO = 10mA		0.4	0.55	V
Hall input sensitivity	V_{HN}	IN+, IN- differential voltage (including offset and hysteresis)		±10	±20	mV
FG/RD output L-level voltage	$V_{FG}L/_{RD}L$	$I_{FG/RD}$ = 5mA		0.2	0.3	V
FG/RD pin leakage current	$I_{FG}L/_{RD}L$	$V_{FG/RD}$ = 19V			10	μA
VTH/RMI pin bias current	I_{VTH}/I_{RMI}	CPWM = 2V, $V_{TH/RMI}$ = 1V			0.3	μA

*Design target value and no measurement is made. The thermal protection circuit is incorporated to protect the IC from burnout or thermal destruction. Since it operates outside the IC's guaranteed operating range, the customer's thermal design should be performed so that the thermal protection circuit will not be activated when the fan is running under normal operating conditions.



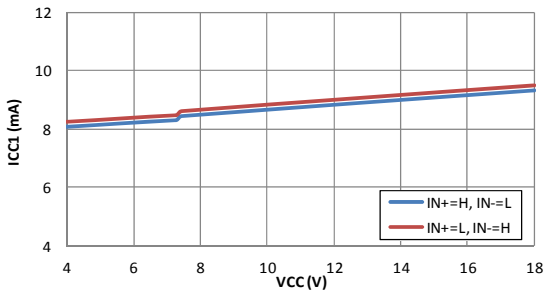


Figure1. Circuit current during drive vs VCC voltage

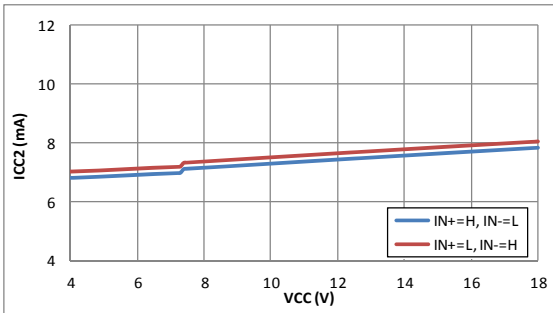


Figure2. Circuit current during lock protection vs VCC voltage

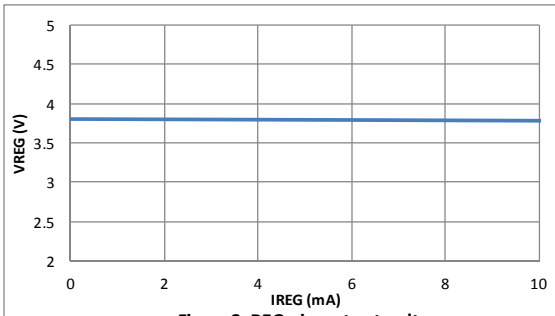


Figure3. REG pin output voltage vs Load current

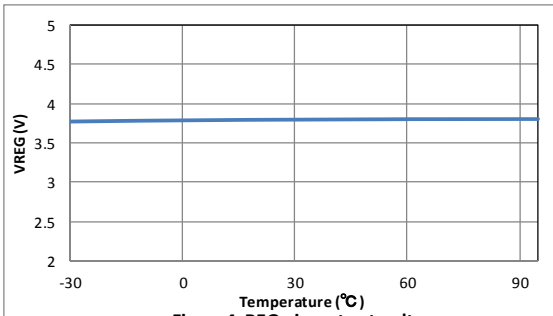


Figure4. REG pin output voltage vs Temperature

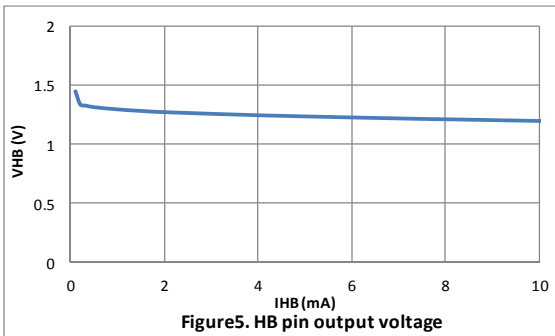


Figure5. HB pin output voltage vs Load current

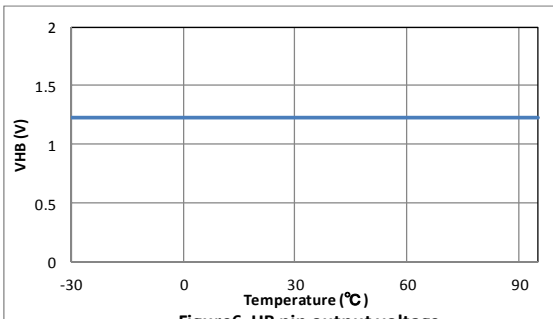


Figure6. HB pin output voltage vs Temperature

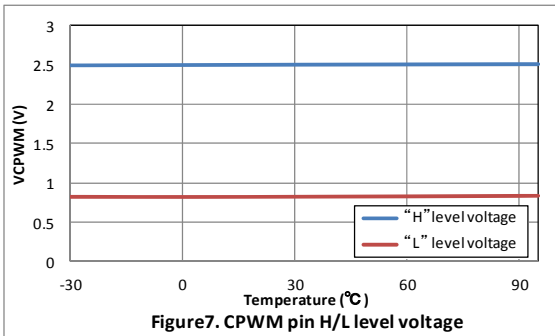


Figure7. CPWM pin H/L level voltage vs Temperature

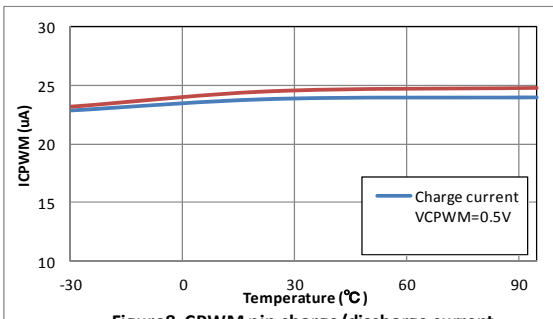


Figure8. CPWM pin charge/discharge current vs Temperature

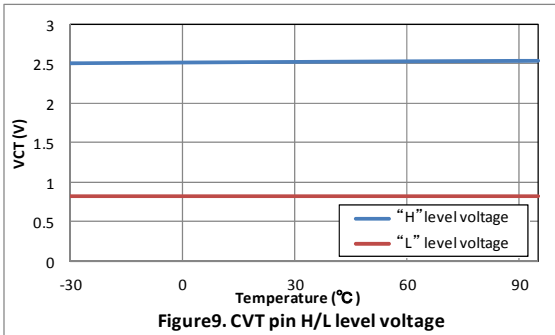


Figure9. CVT pin H/L level voltage vs Temperature

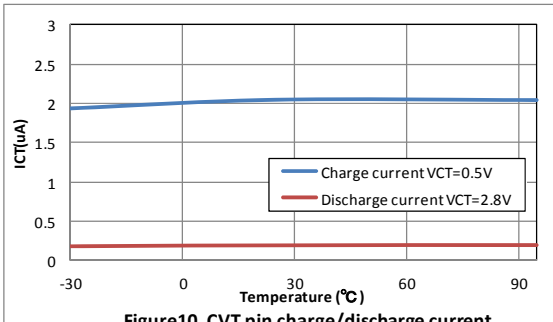


Figure10. CVT pin charge/discharge current vs Temperature

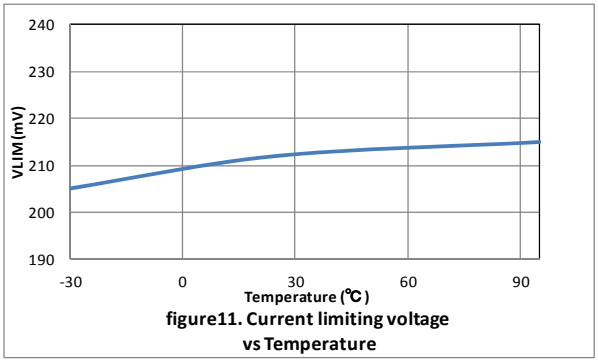


figure11. Current limiting voltage vs Temperature

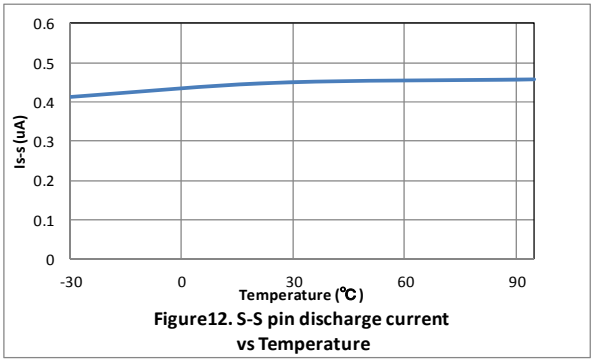


Figure12. S-S pin discharge current vs Temperature

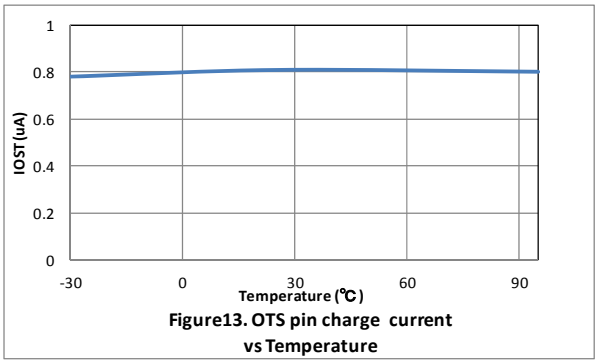


Figure13. OTS pin charge current vs Temperature

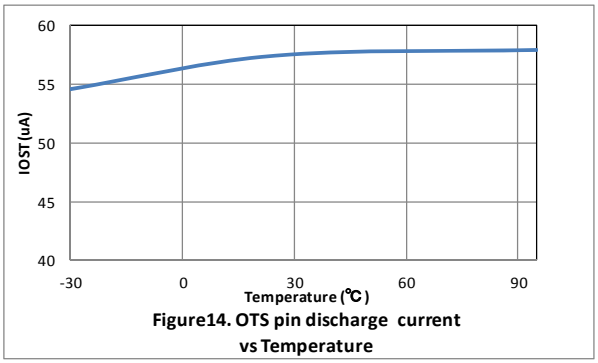


Figure14. OTS pin discharge current vs Temperature

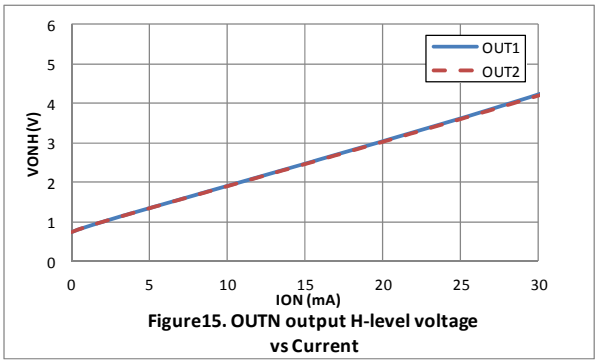


Figure15. OUTN output H-level voltage vs Current

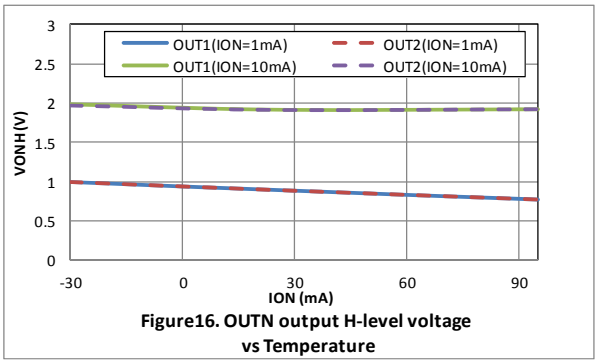


Figure16. OUTN output H-level voltage vs Temperature

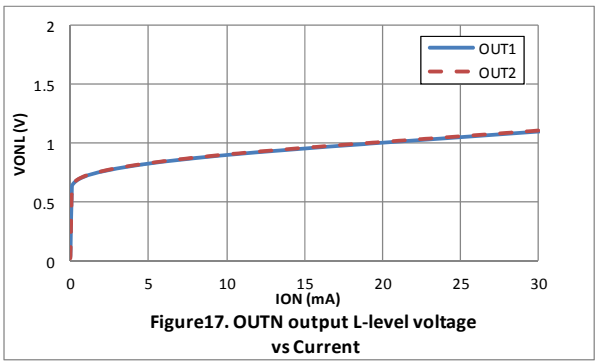


Figure17. OUTN output L-level voltage vs Current

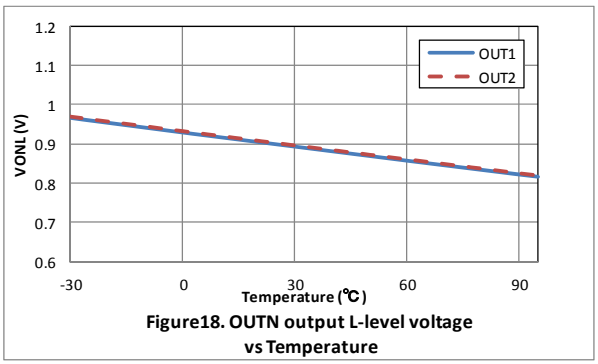


Figure18. OUTN output L-level voltage vs Temperature

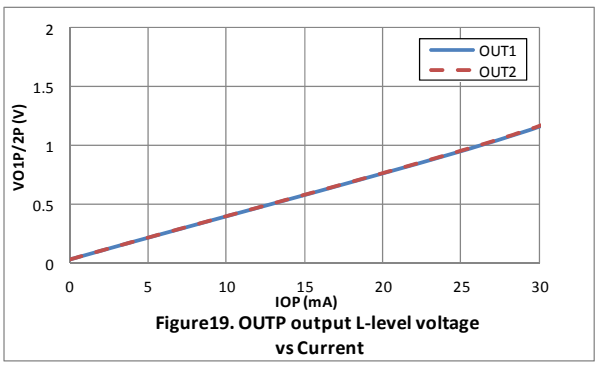


Figure19. OUTP output L-level voltage vs Current

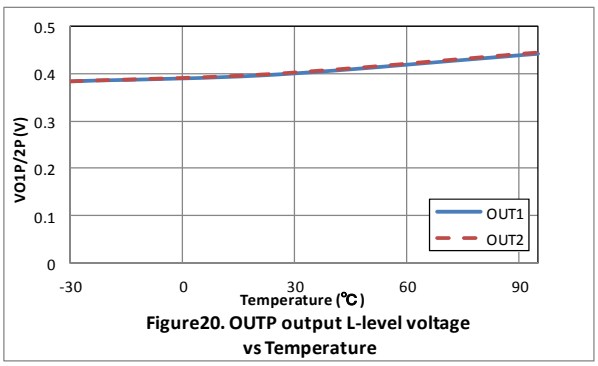


Figure20. OUTP output L-level voltage vs Temperature

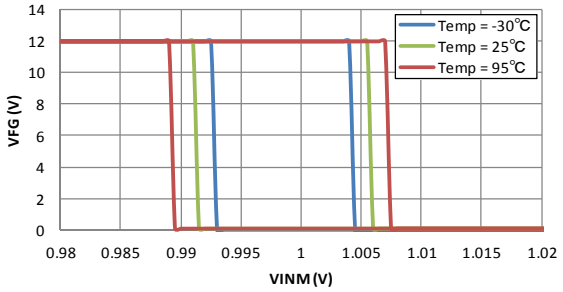


Figure21. Hall input hysteresis

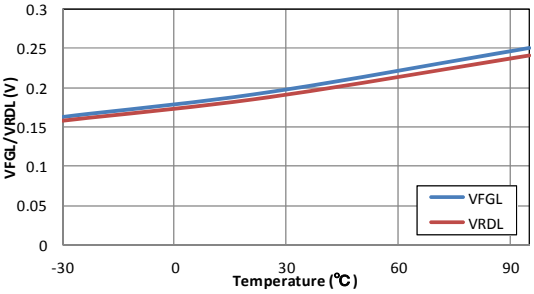


Figure22. FG/RD output L-level voltage vs Temperature

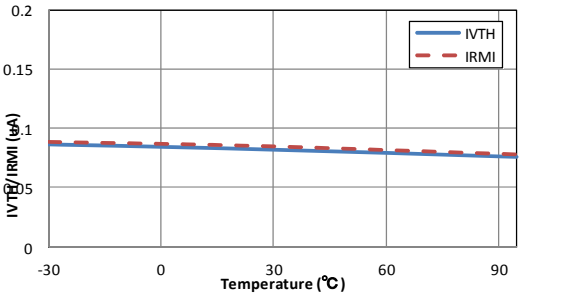
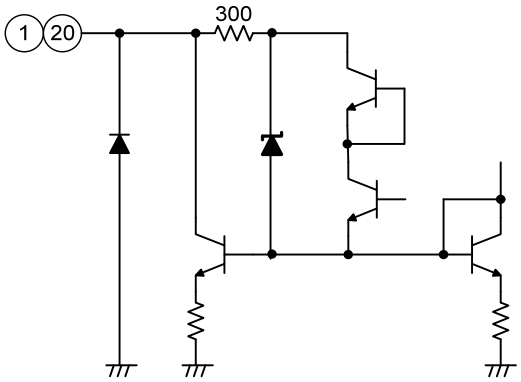
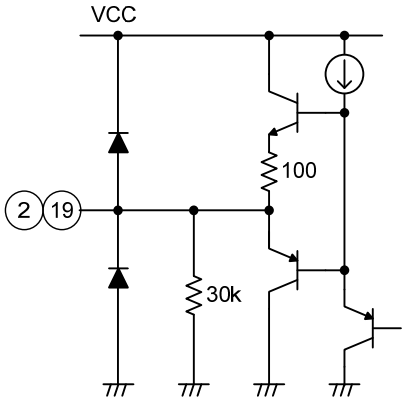
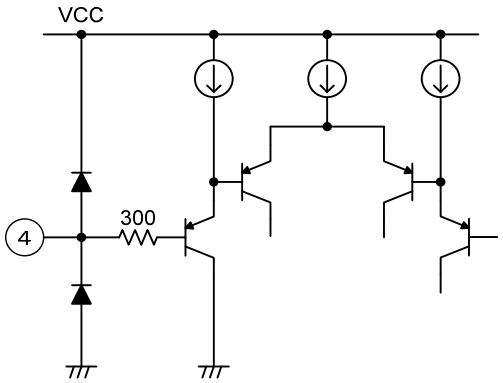
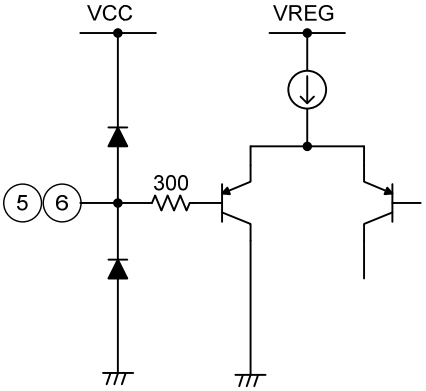


Figure23. VTH/RMI pin bias current vs Temperature

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1 20	OUT2P OUT1P	Output pin to drive P-ch FET. This pin is open collector.	
2 19	OUT2N OUT1N	Output pin to drive N-ch FET.	
3	VCC	Power supply pin. To stabilize VCC voltage, it is necessary to connect the capacitor to VCC and SGND pins as nearly as possible.	
4	SENSE	Current limiting detection pin. A drive current is detected by connecting a resistor between this pin and SGND. Connect this pin to SGND when it is not used.	
5	RMI	Minimum speed setting pin. Perform pull-up with REG when this pin is not used.	
6	VTH	Speed control pin. To apply DC voltage directly, connect a current limiting resistor to prevent inflow of large current. Connect this pin to GND when it is not used	

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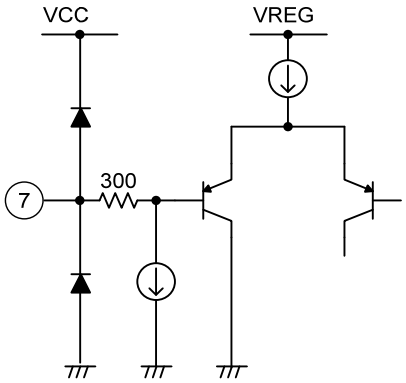
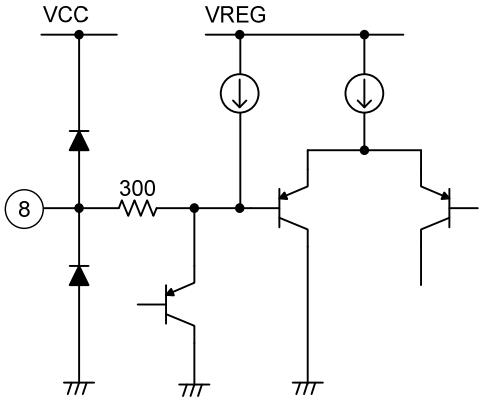
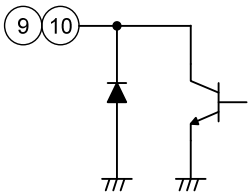
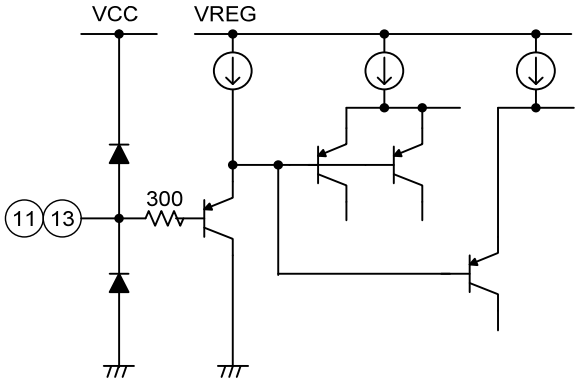
Pin No.	Pin name	Function	Equivalent circuit
7	CPWM	Pin to connect capacitor which generates PWM basic frequency. The capacitor must be connected between CPWM and GND. Do not leave this pin open.	
8	OTS	Pin to connect the ON-time start setting capacitor. Connect the capacitor between OTS and GND. Connect the pin to GND when it is not used.	
9	FG	The rotational signal output pin. This pin is open collector output. Leave the pin open when it is not used.	
10	RD	The lock detection signal output pin. In open collector output. Leave the pin open when it is not used.	
11 13	IN- IN+	Hall input pin. Input the opposite phase signal each other The connection between Hall element and these pins should be as short as possible to prevent noise. If noise is carried, insert the capacitor between IN^+ and IN^- pins.	

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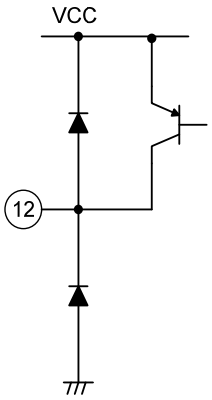
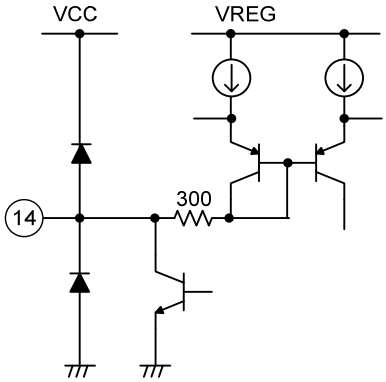
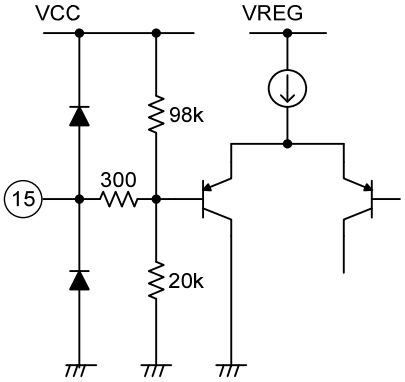
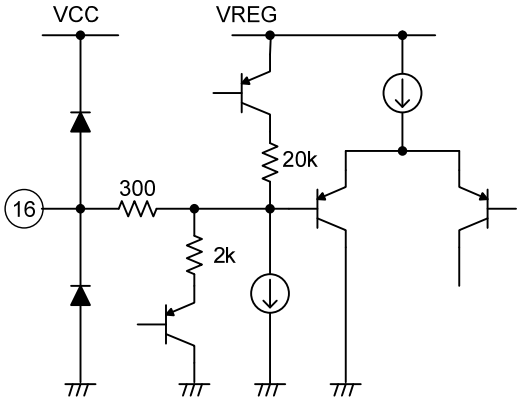
Pin No.	Pin name	Function	Equivalent circuit
12	HB	Regulated voltage output pin. It is used for Hall element. Leave the pin open when it is not used.	
14	CT	Pin to connect with the capacitor which generates the lock detection time. Connect the capacitor between CT pin and SGND. Connect the pin to SGND when it is not used (if lock protection is unnecessary)	
15	KBSET	Pch kickback absorption circuit setting pin. Open: The kickback absorption circuit is activated at a VCC voltage of 7.4V (typ) or above. Pull-down to SGND: Always OFF Pull-up to REG: Always ON; however, OFF when VCC is off.	
16	S-S	Pin to connect the soft-start time setting capacitor. Connect the capacitor between REG and S-S pin. Connect the pin to GND when it is not used.	

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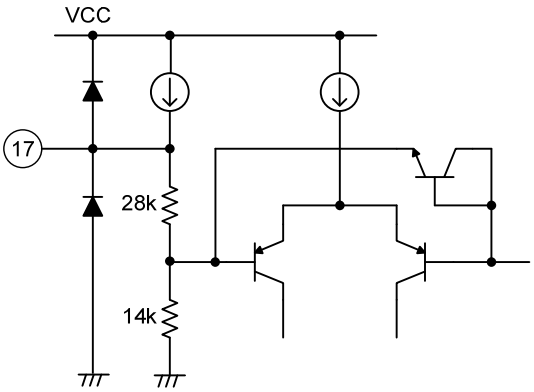
Pin No.	Pin name	Function	Equivalent circuit
17	REG	3.8V DC voltage output pin. For the REG oscillation prevention and stabilization, use a capacitor with 1µF or higher. The capacitor must be connected between REG and SGND pin as shortly and thickly as possible.	
18	SGND	GND pin.	

1. Operation overview

LB11868V is a single-phase bipolar driving motor pre-driver with the variable speed function compatible with external PWM signal. With a few external parts, a highly-efficient and highly-silent variable drive fan motor with low power consumption can be achieved.
It incorporates soft-start, lock protection, soft-switch function at phase switch, kick-back absorption function, FG output (revolution count) and RD (lock protection detection output). Therefore, this device supports various types of single-phase fan without complexity.

1.1 Truth table

(1) Drive & lock (CPWM=H VTH, RMI, S-S=L)

IN^-	IN^+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	RD	Mode
H	L	L	L	L	OFF	H	L	L	OUT1 → 2 drive
L	H		OFF	H	L	L	OFF	L	OUT2 → 1 drive
H	L	H	OFF	L	OFF	H	L	OFF	Lock protection
L	H		OFF	H	OFF	L	OFF	OFF	

(2) Speed control (CT, S-S=L)

VTH, RMI	CPWM	OTS	IN^-	IN^+	OUT1P	OUT1N	OUT2P	OUT2N	Mode
L	H	L	H	L	L	L	OFF	H	OUT1 → 2 drive
			L	H	OFF	H	L	L	OUT2 → 1 drive
H	L		H	L	OFF	L	OFF	H	Regeneration mode
			L	H	OFF	H	OFF	L	
H	L	H	H	L	OFF	L	OFF	L	Standby mode
			L	H	OFF	L	OFF	L	

For VTH, RMI, and S-S pins, refer to the timing chart.

1.2 Output waveform

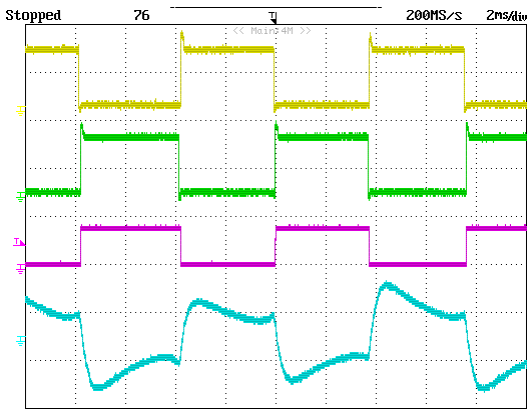


Fig1.2.1. Full Speed waveform

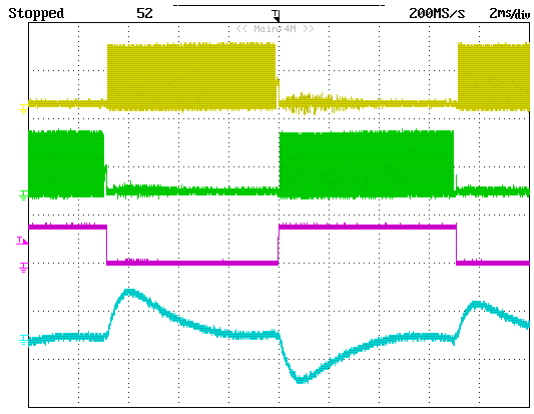


Fig1.2.2. PWM speed control waveform by VTH voltage input

OUT1, OUT2: The voltage at the both ends of coil.
Coil current: Coil Current which flows from OUT1 to OUT2.
The same applies to the waveforms shown later.

By applying VTH voltage, OUTP is turned on and off (Pch FET is turned on and off) to control speed.
Off time of Pch is determined by the resistor between gate and source connected to Pch as well as input capacitor of Pch FET. Therefore, use of Pch FET with small input capacitance is recommended. Longer off time leads to switching loss and heat generation.

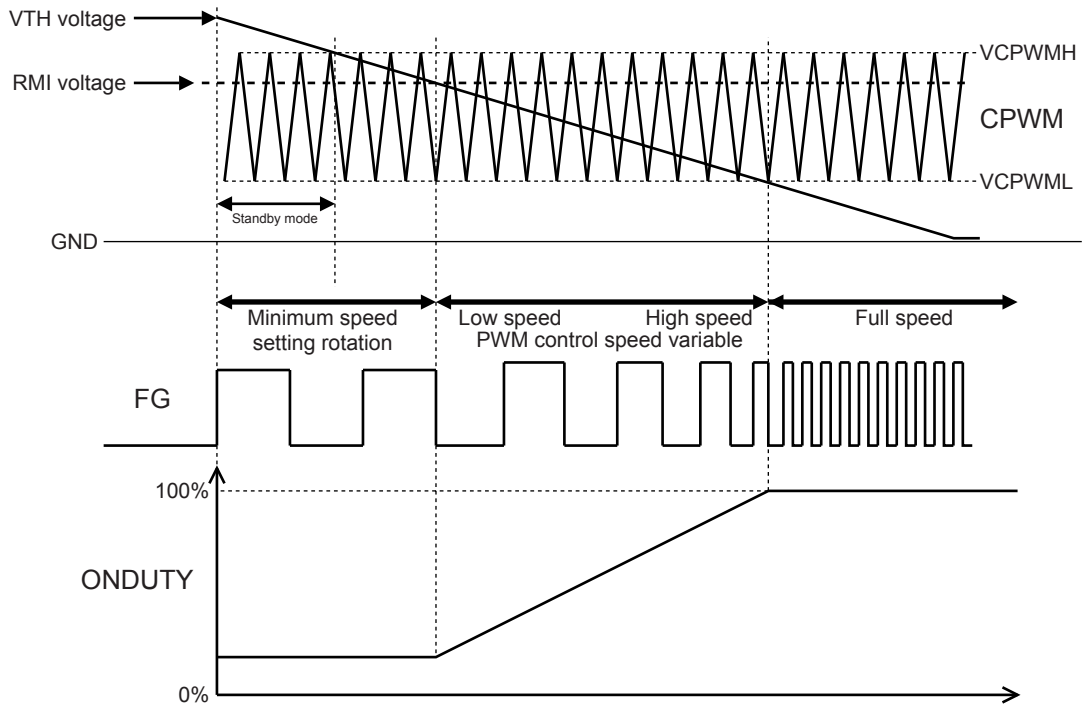
Since speed feedback circuit is not incorporated, caution is required for the variation in revolution by motor.

2. Speed control

2.1 VTH/RMI

The speed of fan is controllable by applying DC voltage to VTH pin.
You can also set a fan to lowest speed by setting RMI pin.

Control timing chart (Speed control)



(1) Minimum speed setting (standby) mode

The low-speed fan rotation is set by the minimum speed setting mode using RMI pin.
When the minimum speed is not set (RMI pin pulled up to REG), the motor stops.
If the VTH voltage rises when the lowest speed is not set (RMI pin is pulled up to REG), the fan stops and if the OTS pin capacitor is used, the standby mode is set.
Details of the standby mode are given in the section “Control timing chart (ON-time start, Lock protection).

(2) Low speed⇔high speed

PMW control is made by comparing the CPWM oscillation voltage (VCPWML⇔VCPEMH) and VTH voltage.
The drive mode is established when the VTH voltage is low.
Both upper and lower output FET are turned ON when the VTH voltage is low.
When the VTH voltage is high, Pch is turned off, and the coil current is regenerated inside the lower FET.
Therefore, as the VTH voltage decreases, the output ON-DUTY increases, causing an increase in the coil current and raising the motor rotation speed.
The upper output Pch is turned OFF when the VTH voltage is high, regenerating the coil current in the lower TR. Therefore, as the VTH voltage decreases, the output ON-DUTY increases, causing increase in the coil current, raising the motor rotation speed.
The rotational speed can be monitored using the FG output.

(3) Full speed mode

The full speed mode becomes effective when the VTH voltage is VCPWML or less. (Set VTH = GND when the speed control is not to be made.)

How to set CPWM frequency

To obtain CPWM frequency, use the following expressions.

T1=C*(VCPWMH-VCPWML)/ICPWM1

T2=C*(VCPWMH-VCPWML)/ICPWM2

F=1/(T1+T2)

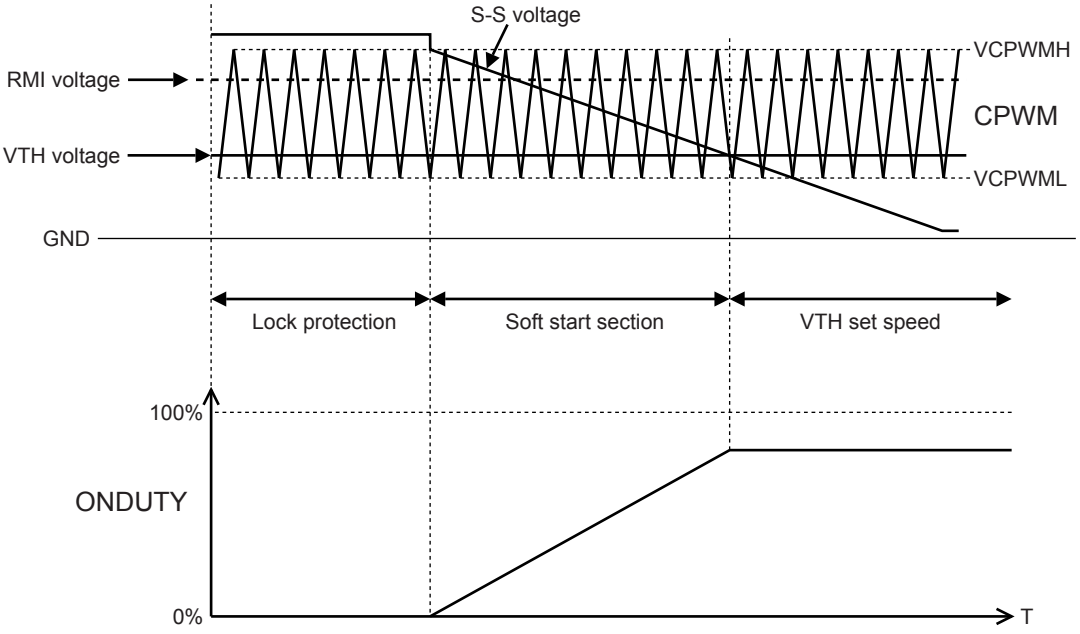
C: The value of capacitor between CT and GND.

2. 2 Soft-start

This IC incorporates soft-start function to suppress current during startup.
Soft-start is settable by connecting a capacitor between S-Spin and GND.

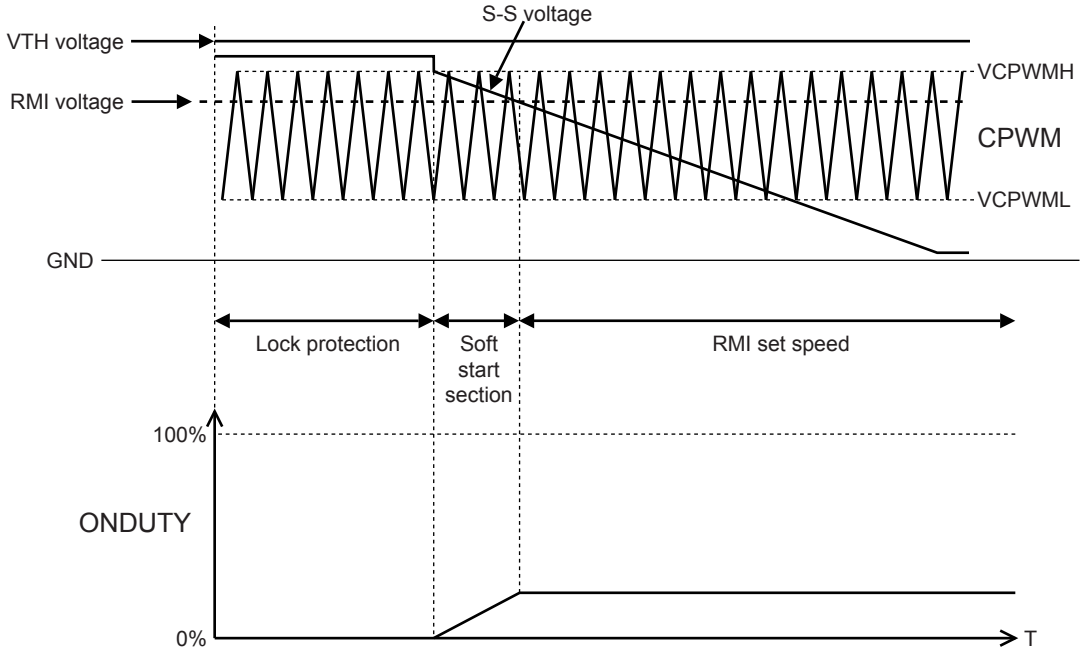
Control timing chart (Soft start)

(1) Where VTH < RMI voltage



During startup and after lock protection is released, S-S pin starts from VCPWMH voltage. Is-s constant current is released from the capacitor of S-S pin.
S-S pin voltage decreases gradually and on-duty of OUTP pin increases up to the on-duty set by VTH pin.

(2) At VTH > RMI voltage



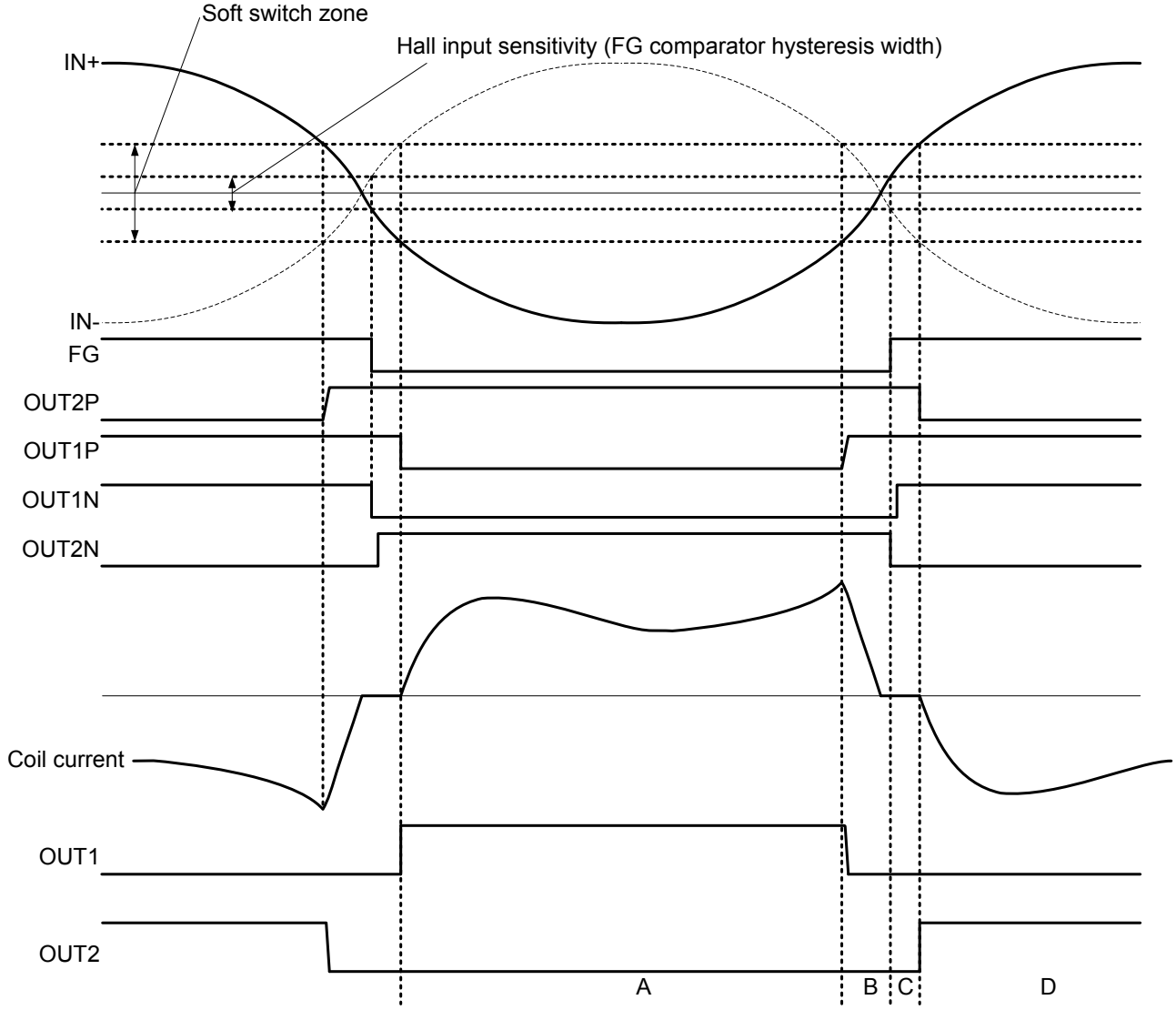
Where VTH>RMI, the on-duty increases up to the on-duty set by RMI pin.
Adjust the S-S pin voltage gradient by means of the capacitance of the capacitor between the S-S pin and REG.
Recommended capacitor: 0.1μ to 1μF

3. Switching method

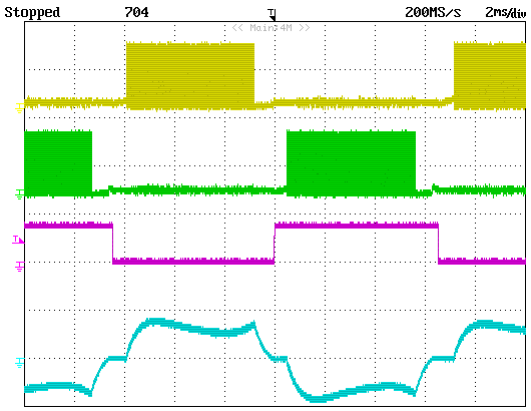
This IC detects the difference of 2 voltages between IN+ and IN- connected to 2 Hall elements respectively. At the timing of phase switch, this IC detects the difference of 2 voltages. When the difference is within +/- 30mV (typ), soft-switch is performed. In the soft-switch zone, reactive current is cut by turning off the upper FET before OUTP pin switches phase. In this way, efficiency improves and silent drive is realized.
If the amplitude of Hall elements is too narrow, the influence of soft-switch becomes too strong. Therefore, the amplitude should be +/- 100mV for the difference of the 2 voltages.

Control timing chart (soft switch, kick-back)

3.1 Where coil current is not present at phase switch



*The above chart is only for reference. Coil current as well as L value and R value of coil vary significantly depends on Hall input.



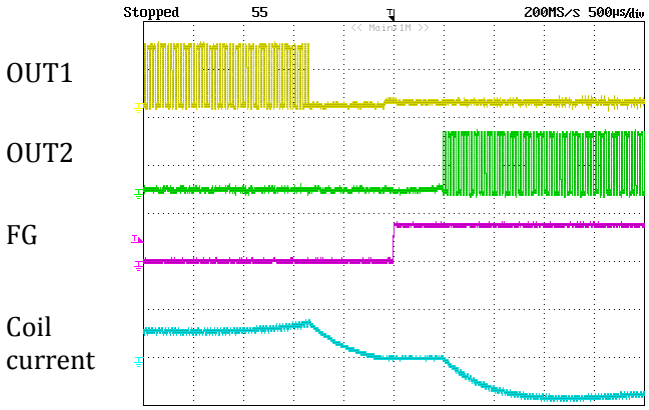
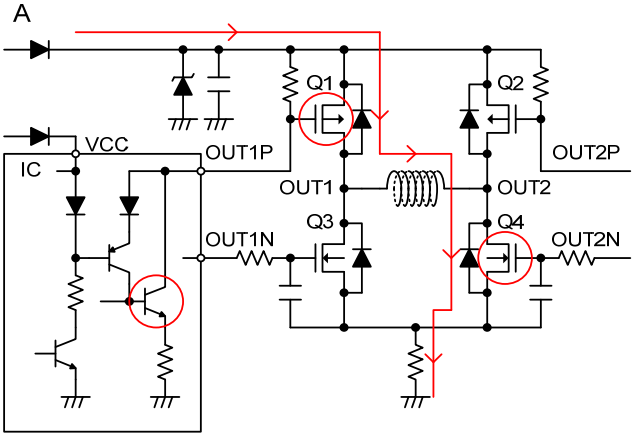


Fig3.1.1. Waveform without coil current at phase switch

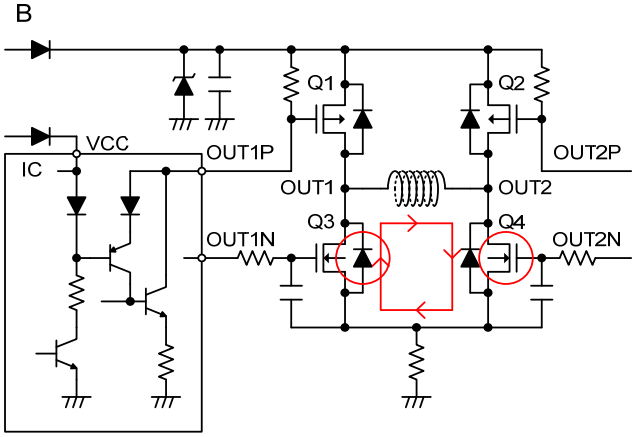
Fig3.1.2. Enlarged waveform

A



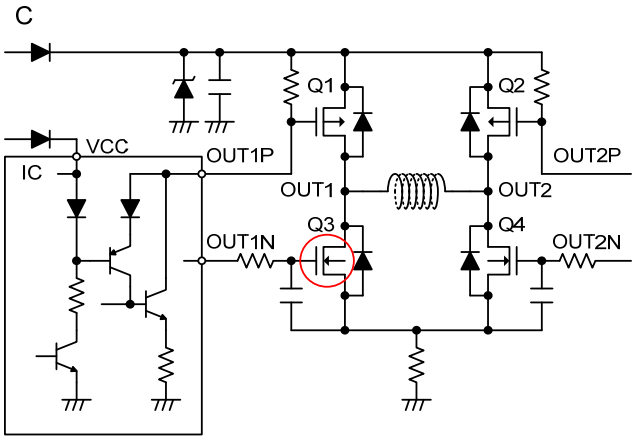
Q1 and Q4 are turned ON and current flows from power supply.

B



This is a soft-switch zone where Q1 is turned OFF and regeneration mode is set using Di of Q3 in which coil current dissipates gradually (whereby reactive current is cut down).

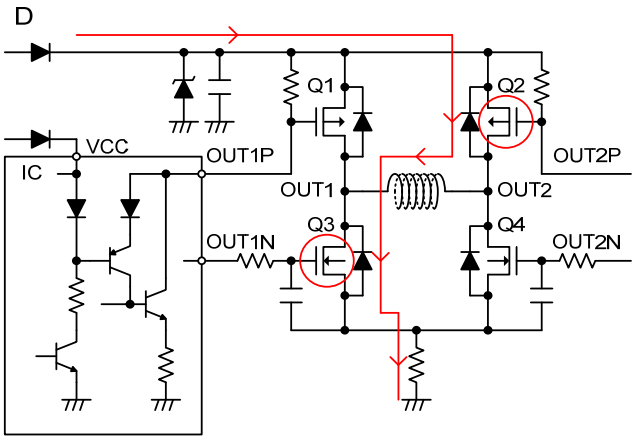
C



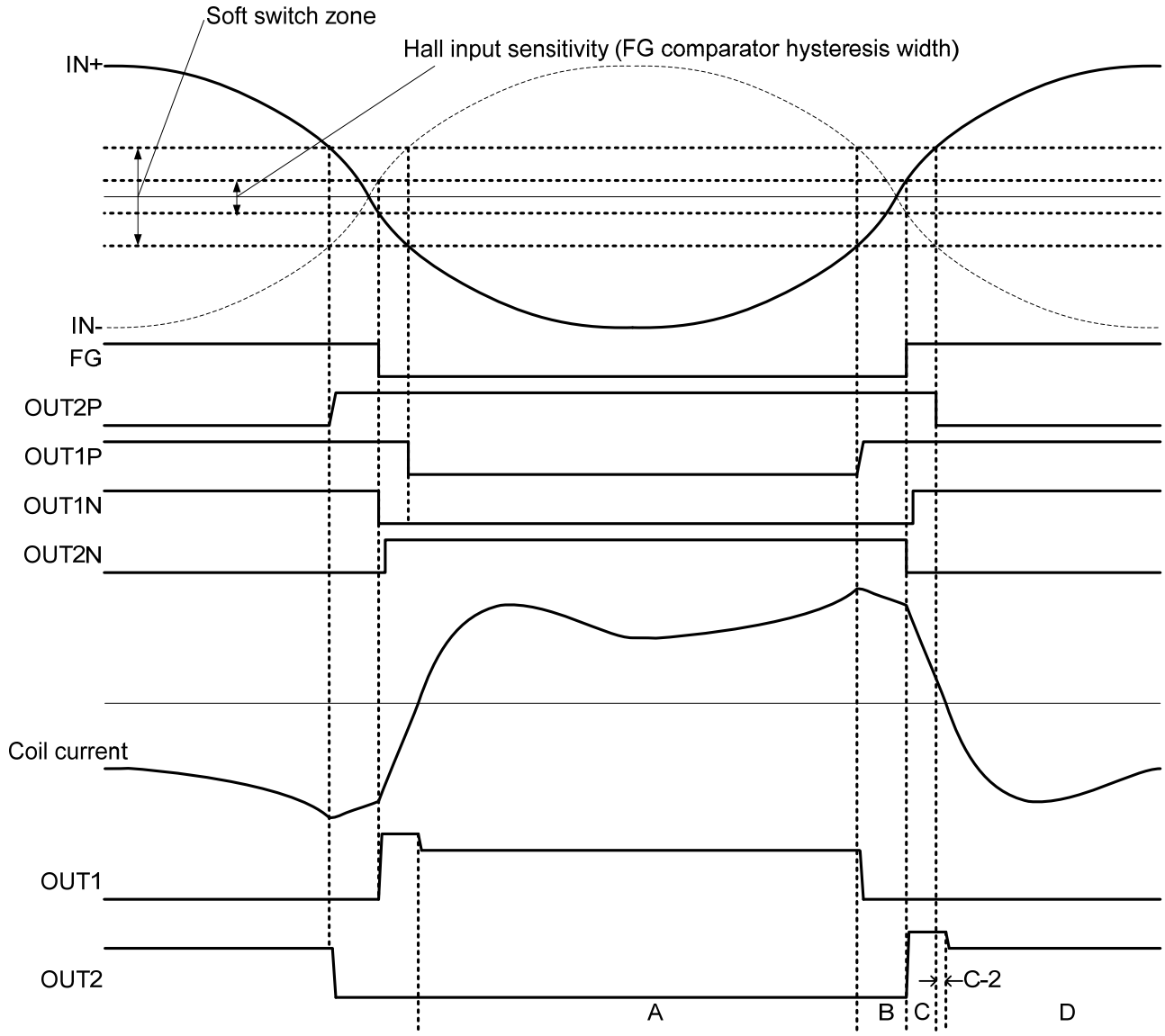
If regeneration mode does not dissipates the entire coil current while Q4 is OFF and Q3 is ON, current does not flow (the generation of kickback voltage is prevented).

Q2 and Q3 turn ON and current flow to the reverse direction.

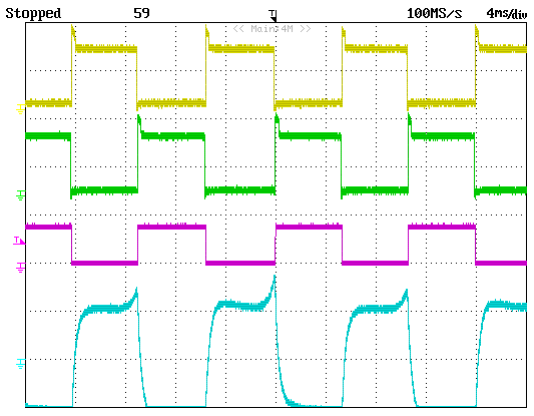
D

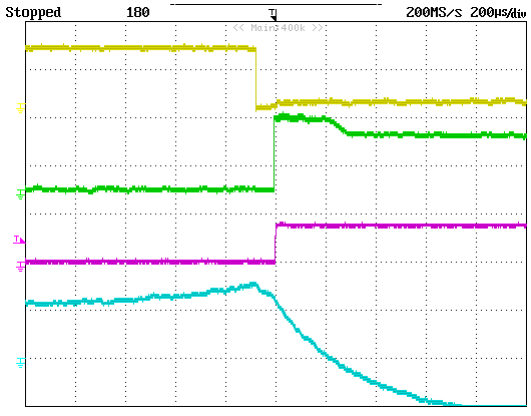


3.2 Where coil current is present at phase switch:



* The above chart is only for reference. Coil current as well as L value and R value of coil vary significantly depends on Hall input.





OUT1

OUT2

FG

Coil current

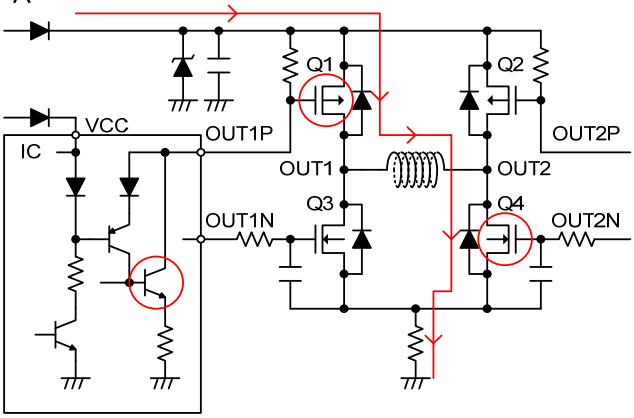
Fig3.2.1. Waveform with coil current at phase switch

Fig3.2.2. Enlarged waveform

If the reverse current is present at phase switch, kickback voltage is generated and the coil current flows back to power supply.
The countermeasure against such current is explained as follows.

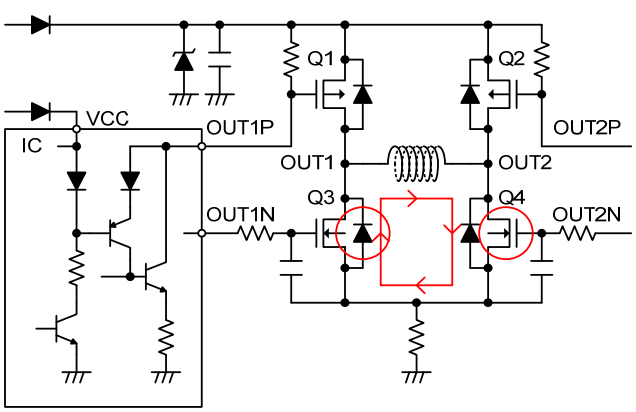
3.2-1 Without use of kickback absorption function (KBSET=GND)
Make sure to insert zener diode between power supply and GND to prevent over-voltage.

A



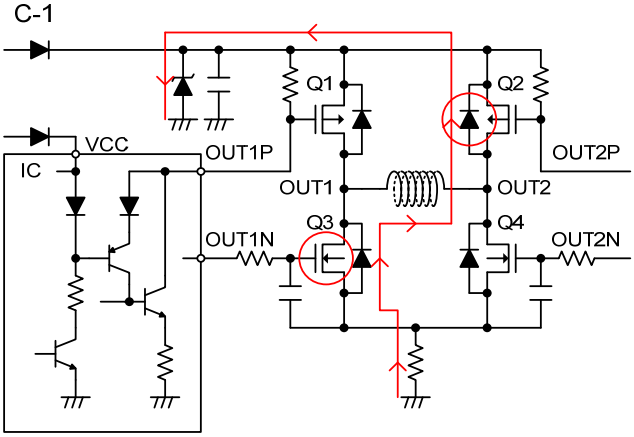
Q1 and Q4 are ON and current flow from power supply.

B



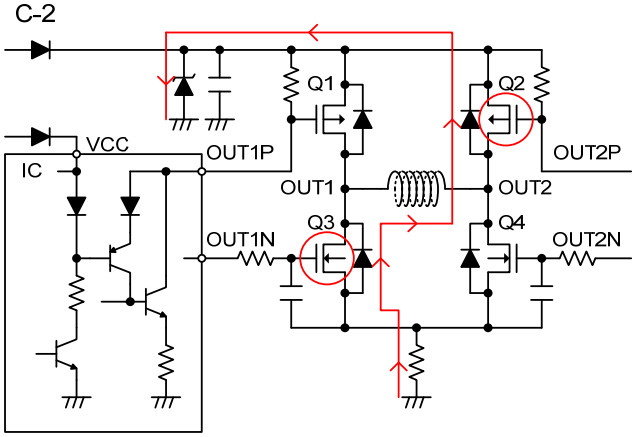
This is a soft-switch zone where Q1 is turned OFF and regeneration mode is set using Di of Q3 in which coil current dissipates gradually (whereby reactive current is cut down).

C-1



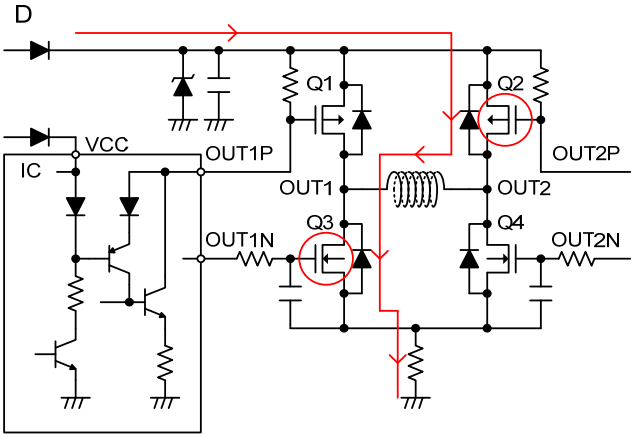
When Q4 is turned OFF, Coil current is still present and flows back to power supply from GND through Di of Q3 and Q2. The coil current is absorbed by capacitor and zener diode. Here, OUT voltage is higher than the supply voltage and caution is required.

C-2



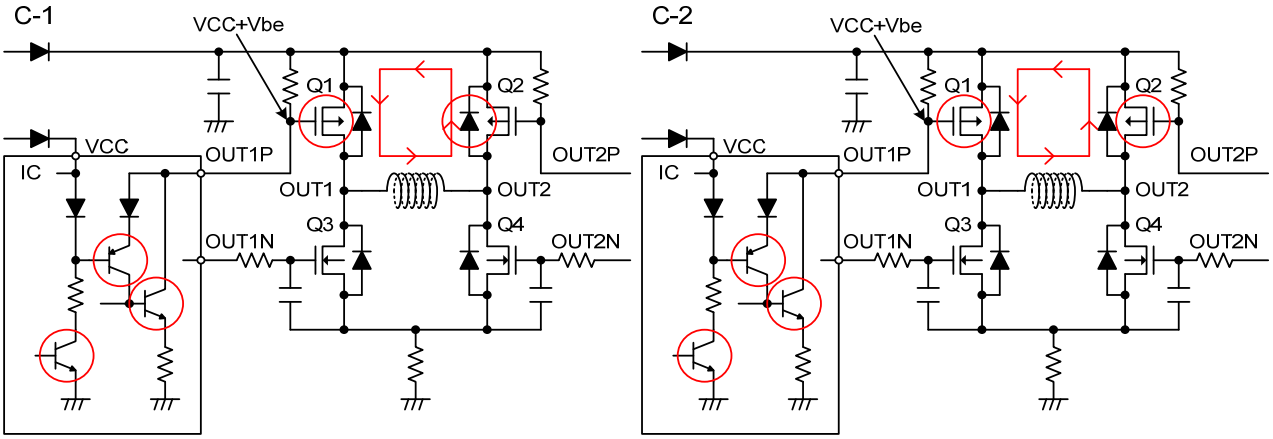
Q2 is ON and current flows back to power supply through Q2 which is repeated until the coil current dissipates entirely.

D



After the coil current dissipates entirely, current flows to the normal direction.

3.2-2 With the use of kickback absorption function (KBSET=VREG or OPEN)
The operation of A, B and D are the same.



The current flows back to power supply from GND through Di of Q3 and Q2. However, OUT1P voltage clamps to
VCC + Vbe (approximately 0.7V).
Hence when supply voltage increases, Q1 turns on and flows current to Di of Q2.
Since high voltage is impressed between D and S, FET that can withstand high voltage.
As Q2 turns ON, current flows from Q1 to Q2 until coil current dissipates entirely.

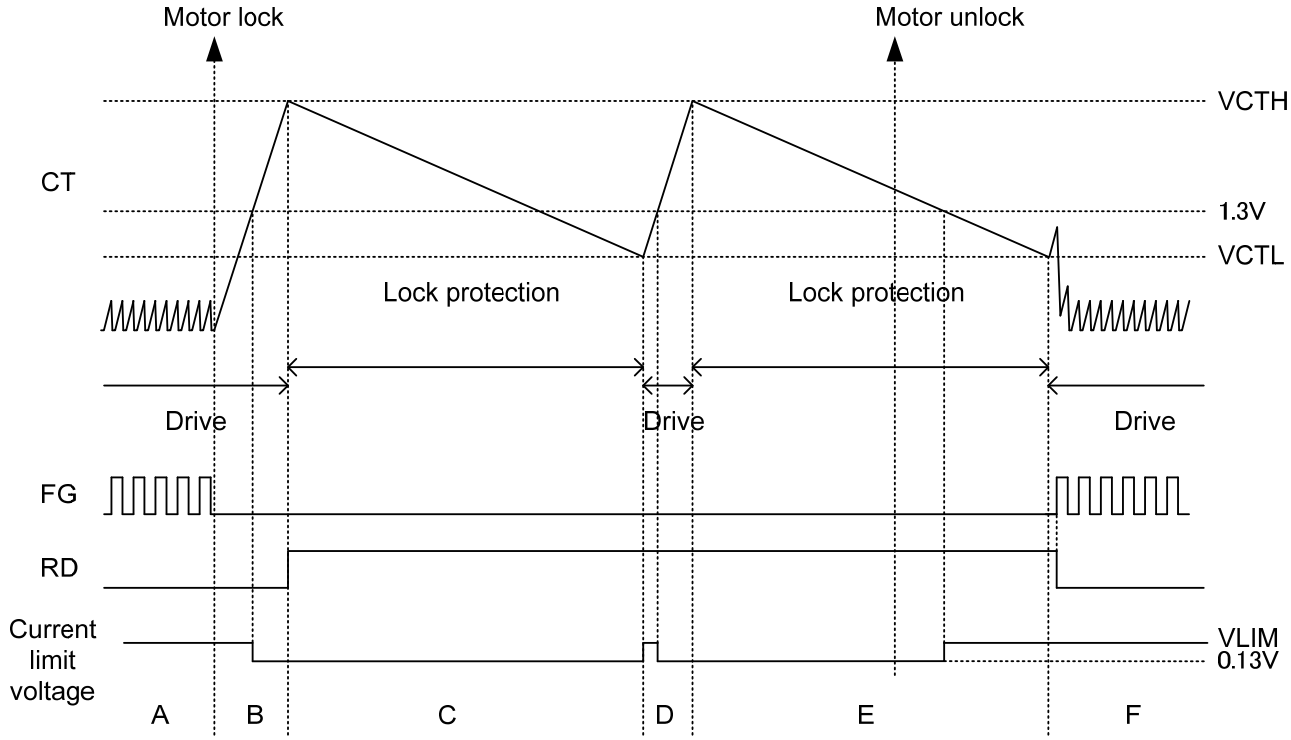
4. Functions

4.1 Lock Protection

This IC incorporated lock protection circuit and auto recovery circuit.

During lock detection, OUTP pin is turned off (the upper FET is turned OFF) to stop motor drive.

Control timing chart (Lock protection)



A) During normal motor drive, the capacitor of CT pin discharges current according to the switch of FG.

B) When the motor is locked, FG signal is stopped and the capacitor of CT pin starts charging. When the voltage of CT pin is 0.8V (typ) or higher, current limit voltage decreases to 0.13V (typ) to prevent over current.

C) When the voltage level of CT pin reaches to VCTH voltage, lock protection is set (see the table of truth values) and power supply to coil is stopped and the capacitor of CT pin discharges current.

D) When the voltage level of CT pin reaches to VCTL voltage, the motor runs and power is supplied to coil. However when motor does not run, the capacitor of CT pin starts charging like the case of B).

E) Even if motor lock state is released during lock protection, lock protection state continues until the voltage level of CT pin reaches to that of VCTL.

F) Motor starts rotation. If a capacitor is connected to S-S pin, motor rotation starts by soft-start.

How to set lock protection time

The approximate lock protection time can be obtained with the following expressions.

B Time from motor rotation to lock protection.

$T = C*VCTH/ICT1$

C Time from lock protection to restart

$T = C*(VCTH-VCTL)/ICT2$

D Time from restart to lock protection

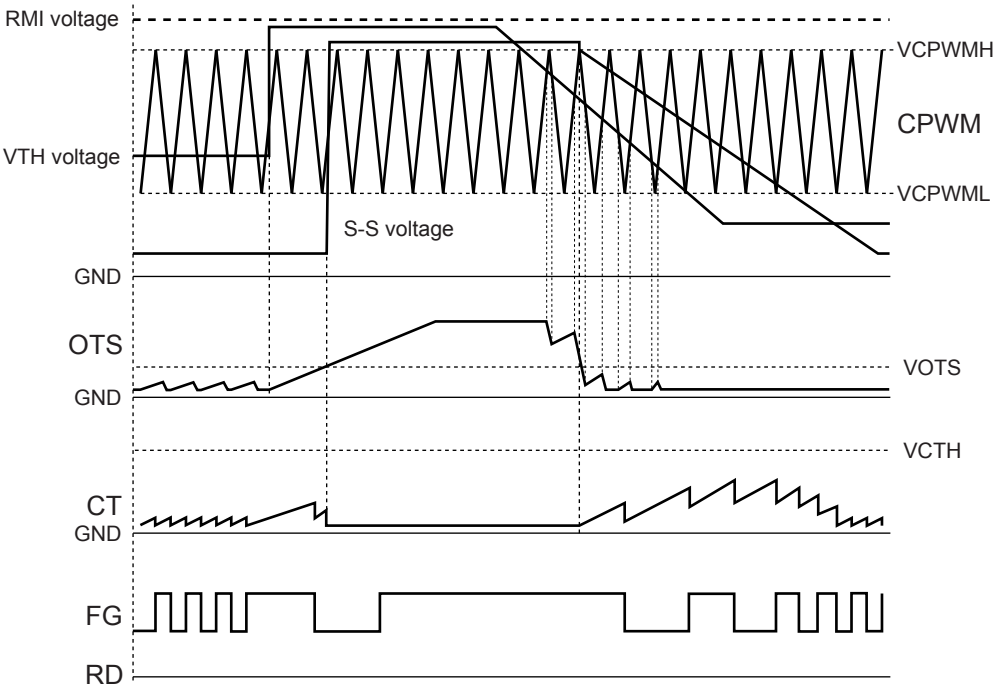
$T = C*(VCTH-VCTL)/ICT1$

C: Capacitance between CT and GND

4.2 On time start

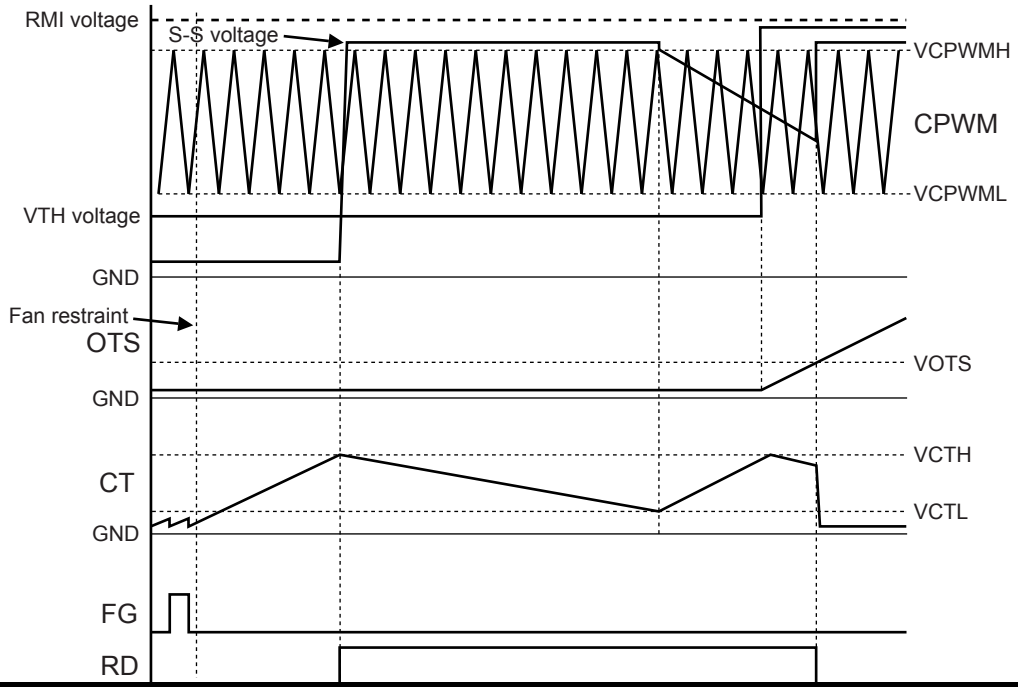
When lowest speed is not set by RMI pin, even when the motor is stopped by VTH pin, lock protection works as explained in 4.1. This function prevents delay time caused by lock protection during the startup by VTH pin so that the motor starts up immediately.
On time start is easily configurable by connecting a capacitor between OTS and GND.

Control timing chart (ON-time start)
(1) When a stop signal based on the VTH voltage has been input during normal rotation



When the output duty ratio based on the VTH/RMI input drops to below 1% or so, the OTS voltage rises, and when it reaches VOTS, the standby mode is established, the CT pin discharges, and the S-S pin is charged. In the standby mode, if the drive mode has been established again by the VTH/RMI input, the rotation is started immediately with soft start.
The CT pin discharges at the same time as the switching of FG. For details on lock protection, refer to (2).

(2) When a stop signal based on the VTH voltage has been input while the fan is constrained



When the fan is constrained, the CT pin voltage rises, and when it reaches VCTH, the lock protection mode is established, and OUTP is set to OFF and RD is set to OFF.
When the lock protection mode is established, the CT pin discharges, and when VCTL is reached, restart (soft start) is initiated. When rotation is started and the FG signal is switched, RD is set to low.
Note: RD is also set to low when the standby mode is established when locked.

4.3 Current limiter

This IC incorporates current limiter to prevent over current.
Current limiter is adjusted by the RF resistor between SENSE pin and GND.
When the voltage of SENSE pin reaches to the voltage level of VLIM (typ: 0.225V), current limit is set and OUTP is turned OFF.
In order to prevent error operation, when the voltage of SENSE pin exceeds the voltage level of VLIM, neglected time of 3μA is set.
When a motor is locked, the voltage of CT pin increases and when the voltage of CT pin exceeds 0.8V, current limit voltage decreases to 0.13V for the further over current protection.

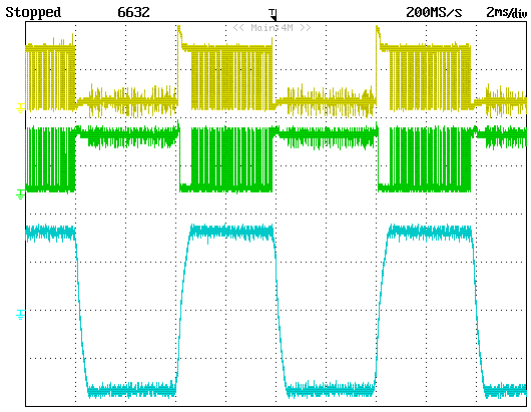


Fig4.3.1. Current limit operation

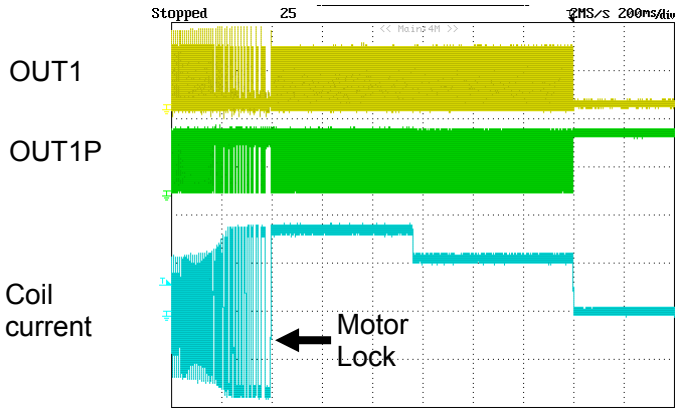
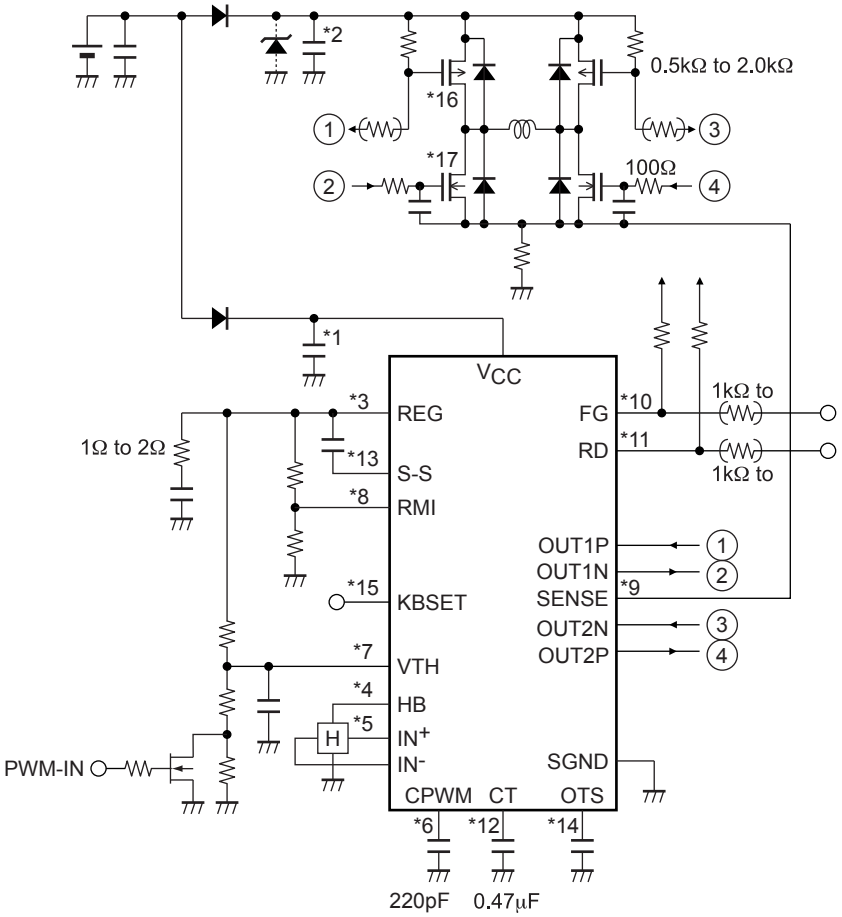


Fig4.3.2. Current limit operation during lock state

4.4 Thermal protection circuit

LB11868V incorporates thermal shutdown circuit. When the junction temperature of the IC reaches to 180° (typ), OUTP turns OFF and stops the motor operation.
The thermal shutdown circuit is used to prevent smoke and fire, which does not guarantee the IC operation at 180°.
Make sure that the design does not the exceed the condition of Tjmax=150°.

5. Application Circuit Example



*1. Power stabilization capacitor

For the power stabilization capacitor on the signal side, use the capacitance of 1μF or more.
Connect V_{CC} and SGND with a thick and shortest pattern.

*2. Power stabilization capacitor on the power side

For the power stabilization capacitor on the power side, use the capacitance of 1μF or more.
Connect the power supply on the power side and GND with a thick and shortest pattern.
When the IC is used for a fan with a high current level, insert a zener diode between the power supply on the power side and GND.

*3. REG pin

3.8V constant-voltage output pin. For the REG oscillation prevention and stabilization, use a capacitor with capacitance of 1μF or more. Connect the REG pin and SGND with a thick and shortest pattern.

*4. HB pin

Used for Hall device bias purposes.

*5. IN^+, IN^- pins

Hall signal input pin.
The connection between Hall element and these pins should be as short and thick as possible to prevent the influence of noise.
If noise is carried, insert a capacitor between IN^+ and IN^- pins.
The Hall input circuit functions as a comparator with hysteresis (15mV).
This also has a soft switch section with ±30mV (input signal differential voltage).
It is also recommended that the Hall input is at the minimum level of 100mV (p-p).

*6. CPWM pin

Pin to connect the capacitor for generation of the PWM basic frequency
The use of CP = 220pF causes oscillation at f = 30kHz (typical), which is the basic frequency of PWM.
As this is used also for the current limiting canceling signal, ON-time start function and Soft start function, be sure to connect the capacitor even when the speed control is not made.

*7. RMI pin

Minimum speed setting pin.
Perform pull-up with REG when this pin is not to be used.
If the IC power supply is likely to be turned OFF first when the pin is used with external power supply, be sure to insert the current limiting resistor to prevent inflow of large current. (The same applies to the VTH pin.)

*8. VTH pin

Speed control pin.
Connect this pin to GND when it is not used (at full speed).
For the control method, refer to the timing chart.
For control with pulse input, insert the current limiting resistor and use the pin with the frequency of 20kHz to 100kHz (20kHz to 50kHz recommended).

*9. SENSE pin

Current limiting detection pin.
When the pin voltage exceeds VLIM, the current is limited and the operation enters the lower regeneration mode.
Connect this pin to GND when it is not to be used.

*10. FG pin

Rotational speed detection pin.
Open collector output that can detect rotational speeds by the FG output in response to the phase switching signal.
Keep this pin open when it is not to be used.
It is recommended that a current-limiting resistor with a resistance of 1kΩ or more be inserted in order to protect the pin during unplugging and plugging the connector or when mistakes are made in connection.

*11. RD pin

Lock detection pin
In open collector output, L upon rotation and H when locked (using pull-up resistance).
Keep this pin open when it is not to be used.

*12. CT pin

Pin to connect the lock detection capacitor.
The constant-current charge and discharge circuits incorporated cause locking when the pin voltage becomes VCTH and unlocking when it is VCTL.
Connect the pin to GND when it is not to be used (locking not necessary).

*13. S-S pin

Pin to connect the soft-start setting capacitor.
Connect the capacitor between REG and S-S pin.
This pin enables setting of the soft start time according to the capacity of the capacitor.
See the timing char.
Connect the pin to GND when it is not to be used.

*14. OTS pin

Pin to connect the ON-time start setting capacitor.
A constant-current charging circuit and a discharging circuit based on the control duty ratio are incorporated, and when the pin voltage exceeds VOTS, the CT pin is discharged and the S-S pin is charged.
Connect the pin to GND when it is not to be used (when the lowest speed setting is used).

*15. KBSET pin

Pch kickback absorption circuit setting pin.
Open: The kickback absorption circuit is activated at a VCC voltage of 7.4V (typ) or above.
Pull-down to GND: Always OFF
Pull-up to REG: Always ON (but when the IC power is OFF, the kickback absorption circuit is OFF)
If the Pch load is to be reduced due to the large fan current, short the KBSET pin to GND, and use a zener diode between the power supply on the power side and GND.
Kickback absorption circuit ON: At OUTPOFF, the OUTP voltage is clamped at VCC + 0.85V (at room temperature and inflow current 5mA (typ)).
Kickback absorption circuit OFF: At OUTPOFF, the OUTP voltage is clamped at 18V or so (at room temperature and inflow current 5mA (typ)) in order to protect the pin.
At OUTPOFF, the maximum inflow current must not be exceeded.

*16. Pch FET

If the Pch kickback absorption circuit is activated and a zener diode between the power supply and GND is not used, the kickback during phase switching is absorbed by Pch.
Since the circuit is activated with a high voltage difference between the drain and source, select a FET with sufficiently high capability.

*17. Nch FET

If the Nch gate voltage fluctuates significantly due to the effects of switching, insert a capacitor between the gate and GND.
Since an Nch diode is used during coil current regeneration, select a FET with sufficiently high capability.

Evaluation board manual

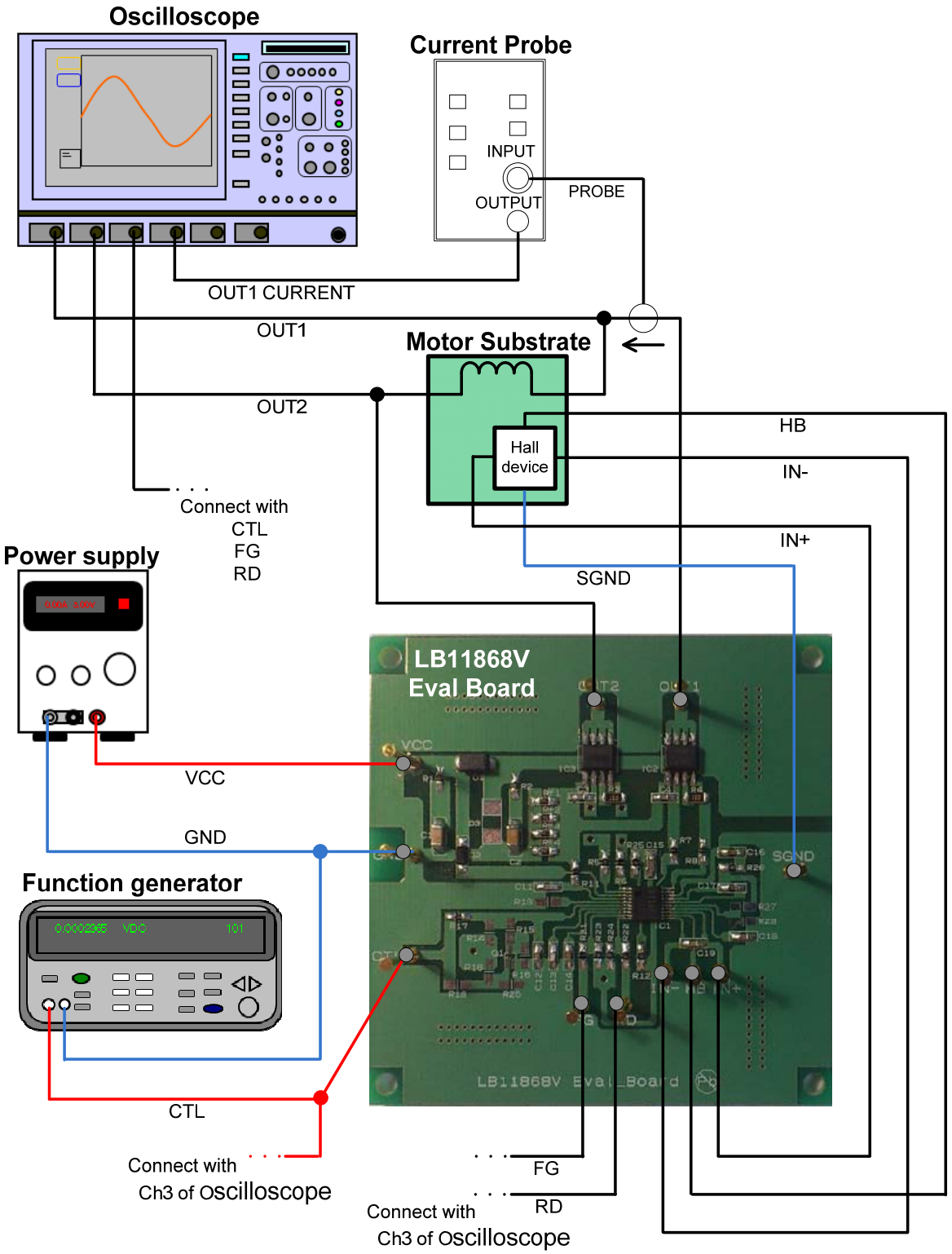


Table: Required Equipment

Equipment	Efficiency
Power supply	12V-3A
Function generator	DC 0V to VREG
Oscilloscope	4 channel
Current probe	
LB11868V Evaluation Board	
Motor	12V type

Test Procedure:

1. Connect the test setup as shown above.

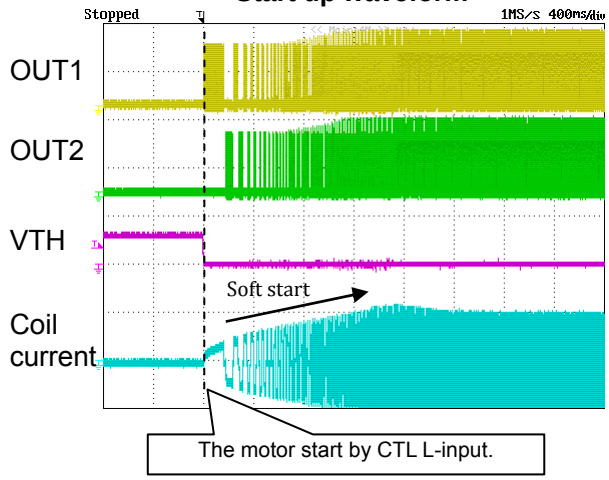
2. Initial check
   Start up the motor at VCC = 12V.
   CTL=0V (full speed)
   Confirm that the motor rotates smoothly.

3. Startup check
   Check whether the motor has started up with stability.
   Start up the motor at VCC = 4V and 12V.
   When the CTL voltage is lower than VCPWH (typ = 2.5V), the motor starts up.
   And then check whether the motor starts up at each VCC voltage

   Check some waveforms. (Startup waveforms)
   Check the OUT1, OUT2 and VTH voltage waveform with the scopes of CH1, CH2 and CH3, and the output current waveform of OUT1 with the scope of CH4 by the oscilloscope.

   ex) The waveforms vary by individual motors.

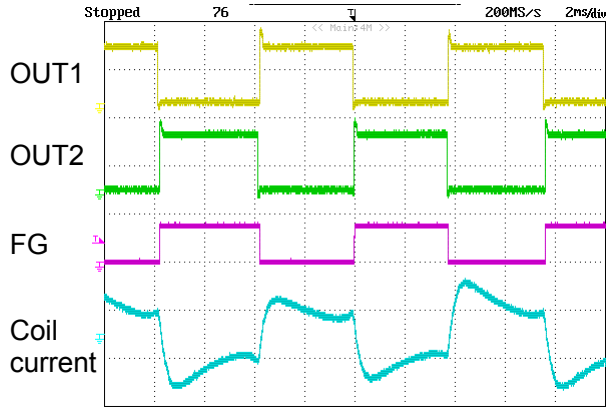
Start up waveform



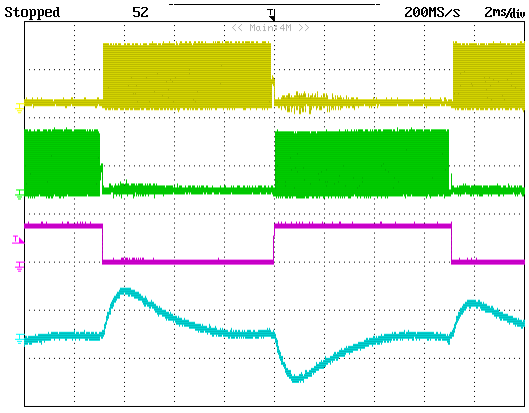
4. Normal rotation check
   Check some waveforms.
   Supply VCC=12V.
   VTH<VCPWL (typical=0.8V); Full Speed mode
   VCPWL< VTH <VCPWL; PWM Speed control mode
   Check the OUT1, OUT2 and FG voltage waveform with the scopes of CH1, CH2 and CH3, and the output current waveform of OUT1 with the scopes of CH4 by the oscilloscope.

   ex) The waveforms vary by individual motors.

Full Speed waveform



PWM speed control waveform



5. Lock detection and automatic reset check

Check the lock detection behavior.

Supply VCC=12V.

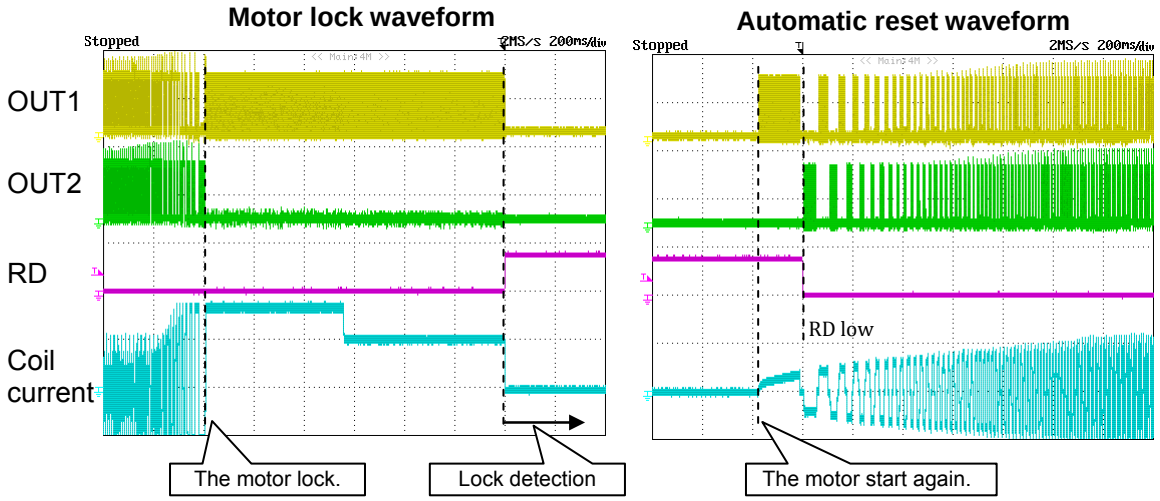
Confirm that the signal of OUT1 and OUT2 are off and RD become H-level when the motor is stopped forcibly by hand.

Then, check the waveform of OUT1, OUT2 and RD voltage in the scopes of CH1, CH2 and CH3, and the output current waveform of OUT1 in the scope of CH4 by the oscilloscope.

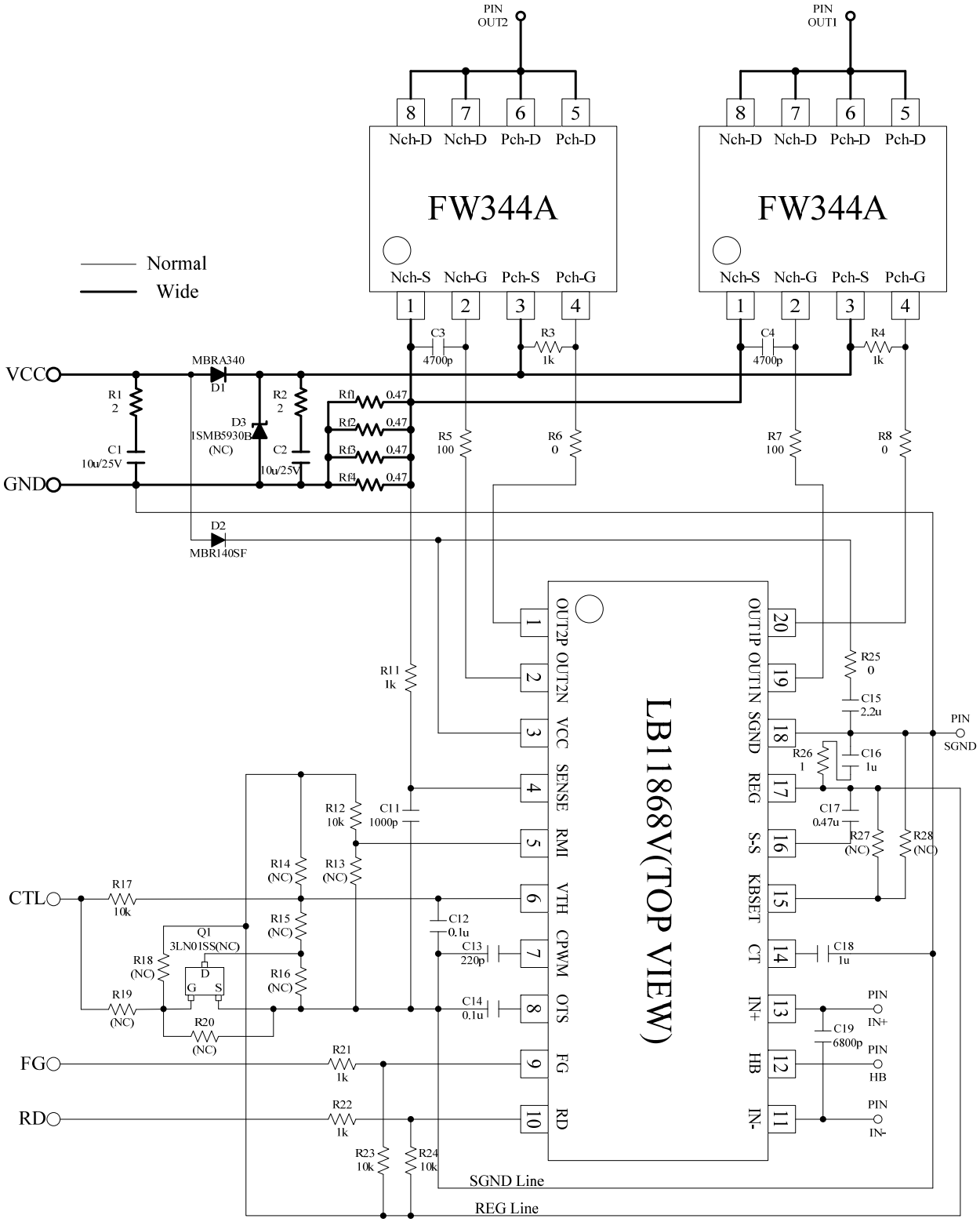
Then, check the behavior of automatic reset after motor stop.

A motor restarts from the stop state. Then RD voltage becomes L-level when OUT1 and OUT2 switch once.

ex) Waveform varies by individual motor.



Evaluation board circuit diagram

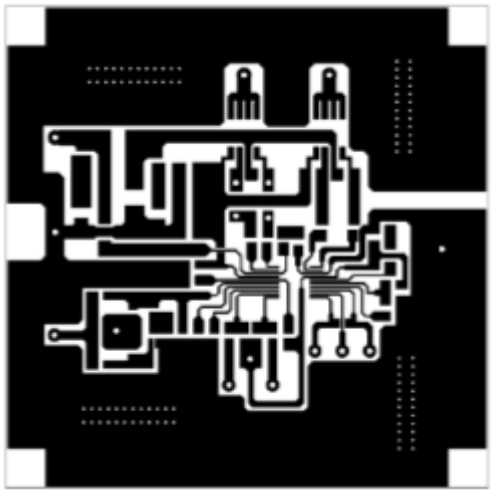


Bill of Materials for LV11868V Evaluation Board

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
IC1	1	Motor Pre-Driver	-	-	SSOP20J (225mil)	ON Semiconductor	LB11868V	No	yes
Tr1,Tr2	2`	P-ch/N-ch MOSFET	-	-	SOIC8	ON Semiconductor	FW344A	No	yes
D1	1	schottky barrier diode	-	-	SMA	ON Semiconductor	MBRA340T3G	No	yes
D2	1	schottky barrier diode	-	-	SOD-123LF	ON Semiconductor	MBR140SFT3G	No	yes
R1,R2	2	resistor	2.2(0.1 W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD2R2J	yes	yes
R3,R4	2	resistor	1k(0.33 W)	±5%	3216 (1206Inch)	ROHM	ESR18EZPJ102	yes	yes
R5,R7	2	resistor	100(0.1 W)	±5%	1608 (0603Inch)	KOA	RK73K1JTD101J	yes	yes
R6,R8,R25	3	resistor (Jumper)	0(0.1W)	±5%	1608 (0603Inch)	KOA	RK73Z1JTTD0ΩJ	yes	yes
R11,R21,R22	3	resistor	1k(0.1 W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD102J	yes	yes
R12,R17,R23. R24	4	resistor	10k(0.1 W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD103J	yes	yes
R26	1	resistor	1(0.1W)	±5%	1608 (0603Inch)	KOA	RK73B1JTTD1R0J	yes	yes
Rf1,Rf2,Rf3,Rf 4	4	SENSE resistor	0.47(0. 25W)	±5%	2012 (0805Inch)	ROHM	MCR10EZHJLR47	yes	yes
C1,C2	2	VCC Bypass capacitor	10uF/2 5V	±10%	3216 (1206Inch)	MURATA	GRM31CB31E106K A	yes	yes
C3,C4	2	capacitor	4700pF /50V	±10%	1608 (0603Inch)	MURATA	GRM188B11H472K	yes	yes
C11	1	capacitor	1000pF /50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H102J	yes	yes
C12,C14	2	capacitor	0.1uF/2 5V	±10%	1608 (0603Inch)	MURATA	GRM188R11E104K	yes	yes
C13	1	capacitor	220pF/ 50V	±5%	1608 (0603Inch)	MURATA	GRM1882C1H221J	yes	yes
C15	1	capacitor	2.2uF/2 5V	±10%	2012 (0805Inch)	MURATA	GRM219B31E225K	yes	yes
C16,C18	2	capacitor	1uF/25 V	±10%	1608 (0603Inch)	MURATA	GRM188B31E105K	yes	yes
C17	1	capacitor	0.47uF/ 25V	±10%	1608 (0603Inch)	MURATA	GRM188B31E474K	yes	yes
C19	1	capacitor	6800pF /50V	±10%	1608 (0603Inch)	MURATA	GRM188B11H682K	yes	yes
TP1-TP12	11	Test points	-	-	-	MAC8	ST-1-3	yes	yes

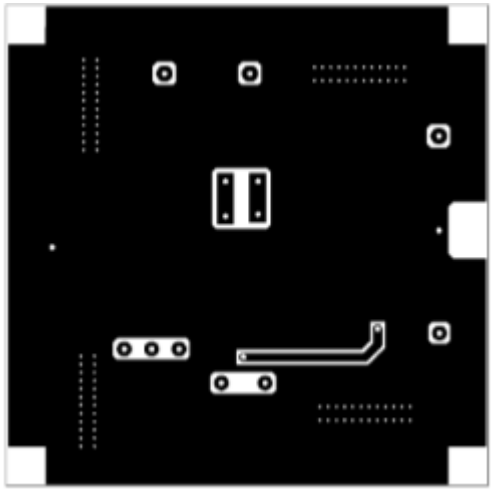
Evaluation Board PCB Design

70.5mm



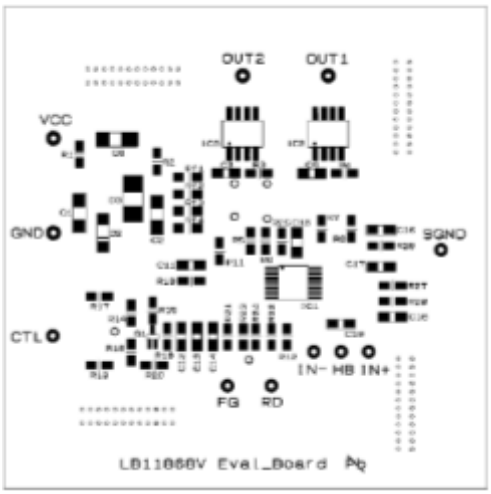
(Top side/ Pattern)

70.5mm

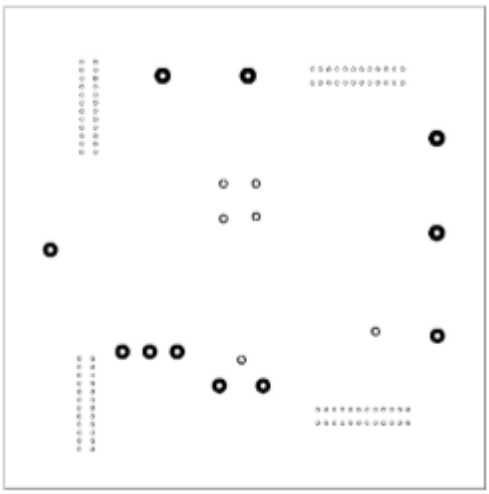


70.5mm

(Back side/ Pattern)



(Top side/ Resist & Silk)



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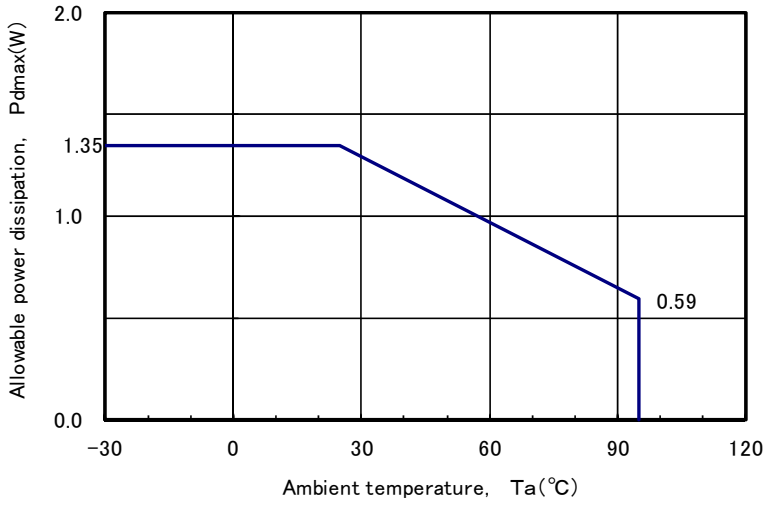

Mount on evaluation board ;
70.5 x 70.5 x 1.6 mm3
Two layer glass epoxy board

Pdmax - Ta