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Designing a Two-Switch Forward Board Driven by the NCL30125

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APPLICATION NOTE

The two−switch forward topology is widely used in high output power combined with low output voltage application. The isolated forward converters are simple and robust. The two−switch structure improves the efficiency since the clamp network is removed.

Most of the current solutions are using a pulse transformer to drive the floating high side MOSFET. The cost and the space of this component are not negligible. For this reason, the NCL30125 integrates both low side and high side driver with the bootstrap technique in order to generate the voltage supply needed for the high side driver. This technique is normally used in half−bridge application. Indeed, compared to the two−switch forward topology, the low side driver is turned on in opposition compared to the high side driver. This operation is useful to refresh the bootstrap capacitor but the two−switch forward topology is less friendly. To be able to use the bootstrap technique, an external switch is added to refresh the capacitor. The current capability of this additional switch is adjusted to handle the magnetization current during the off time. Please note that the freewheel diode connected between the HB node and the ground is not needed anymore.

The NCL30125 also contains all the necessary functions usually embedded in today modern power supply designs. The controller's features include a current mode operation up to 1 MHz, a high voltage start−up current source with dynamic self−supply (DSS), brown−out detection, adjustable soft−start and dedicated OVP/OTP input. The NCL30125 is available on SOIC16 package.

This application note focuses on the design of an adapter driven by the NCL30125. The equations developed are further used to build a 300−W adapter.

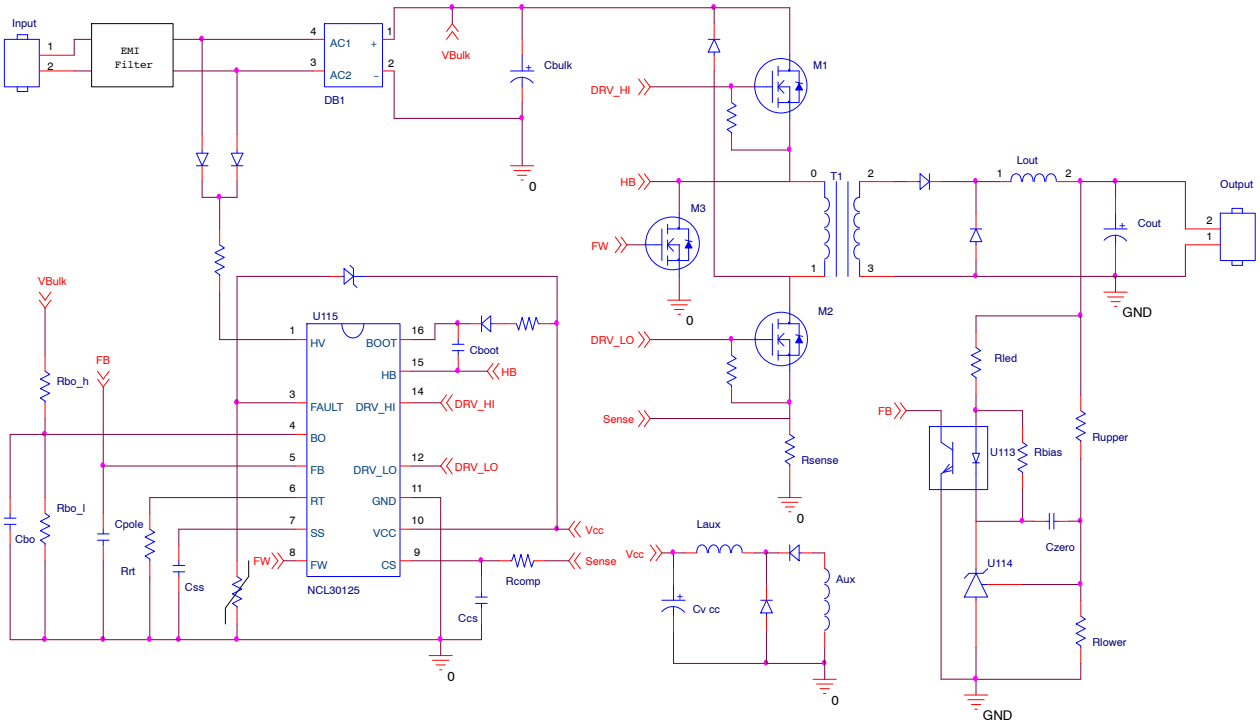

Figure 1. Typical Application Schematic

Introduction

Let's go first in more details through the NCL30125 features.

Current−mode Operation with Internal Ramp Compensation

Implementing peak current mode control operating at fixed switching frequency, the NCL30125 offers an internal ramp compensation signal that can easily by summed up to the sensed current. The controller can thus prevents the appearance of sub−harmonic oscillations.

Adjustable Switching Frequency

A resistor to ground precisely sets the switching frequency between 50 kHz and a maximum of 1 MHz.

Internal Brown−Out Protection

A portion of the input mains (or the rectified bulk rail) is brought to the BO pin via a resistive network. When the voltage on this pin is too low, the part stops pulsing. No re−start attempt is made until the controller senses that the voltage is back within its normal range. When the brown−out comparator senses the voltage is acceptable, it sends a general reset to the controller (latched states are released) and authorizes re−start. Please note that a re−start is always synchronized with a $V_{cc(on)}$ transition event for a clean start−up sequence. If V_{cc} is naturally above $V_{cc(on)}$ when the BO circuit recovers, re−start is immediate. An external transistor pulling down the BO pin to ground during operation will shut−off the controller after the end of the BO timer.

High−Voltage Start−up with DSS

Low standby power results cannot be obtained with the classical resistive start−up network. In this part, a high−voltage current−source provides the necessary current at start−up and turns off afterwards. The dynamic Self−Supply (DSS) restarting the start−up current source to supply the controller if the V_{cc} voltage transiently drops.

EMI Jittering

An internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. Since the bulk capacitor ripple brings a natural jittering at low line, the jittering modulation is enabled only at high line.

Adjustable Soft−start

A soft−start precludes the main power switch from being stressed upon start−up. In this controller, the soft−start is externally adjusted with a capacitor. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup or BO event.

Skip Cycle Feature

When the power supply loads are decreasing to a low level, the duty cycle also decreases to the minimum value the controller can offer. If the output loads disappear, the converter runs at the minimum duty cycle fixed by the leading edge blanking duration and propagation delay. It often delivers too much energy to the secondary side and it trips the voltage supervisor. To avoid this problem, the skip cycle pin is able to (1) adjust the frozen peak current (2) set the skip voltage threshold. Both parameters are linked by the V_{FB} to current setpoint division ratio.

Fault Input

The NCL30125 includes a dedicated fault input accessible via the Fault pin. It can be used to sense an overvoltage condition on the adapter and latch off the controller by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 2.5 V. The controller is also disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault (by the means of an NTC).

OVP Protection on V_{cc}

It is sometimes interesting to implement a circuit protection by sensing the V_{cc} level. This is what this controller does by monitoring its V_{cc} pin. When the voltage on this pin exceeds 25.5 V typical, the pulses are immediately stopped and the part enters in autorecovery mode.

Short−circuit/Overload Protection

Short−circuit and especially overload protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.5−V maximum peak current limit is activated, an error flag is asserted and a time period starts, thanks to the OCP timer. When the fault is validated, all pulses are stopped and the controller enters an auto−recovery burst mode, with a soft−start sequence at the beginning of each cycle. An internal timer keeps the pulses off for 1 s typically which, associated to the pulsing re−try period, ensures a duty−cycle in fault mode less than 10%, independent from the line level. As soon as the fault disappears, the SMPS resumes operation. Please note that A version is auto−recovery as we just described, B version does not and latch off in case of a short−circuit.

Power Stage Dimensioning

The design of the power stage driven by the two−switch forward controller can be divided in 12 steps:

1. Specification of the Adapter
2. Transformer Design
3. Sense Resistance
4. LC Output Filter
5. Freewheeling Diode
6. Output diode or synchronous rectification MOSFET
7. Bulk Capacitor
8. Brown Out

9. Switching Frequency
10. Soft−start
11. Bootstrap Capacitor
12. Ramp Compensation

Step 1: Specification of the Adapter

In order to illustrate this application note, a 5−V/300−W adapter will be the design example. The specifications are detailed in Table 1.

Table 1. SPECIFICATION OF THE 5−V, 300−W ADAPTER

Parameter	Symbol	Value
Minimum Input Voltage	$V_{in,min}$	176 V rms
Maximum Input Voltage	$V_{in,max}$	265 V rms
Output Voltage	V_{out}	5 V
Nominal Output Power	$P_{out(nom)}$	300 W
Switching Frequency at $V_{in,min}$, $P_{out(nom)}$	F_{sw}	100 kHz
Efficiency	η	90%

Step 2: Transformer Design

The principal component in an adapter is the transformer. The whole structure works around this part so we will start the design with its characteristics. Three mains parameters are needed to define a transformer:

1. Primary to Secondary Turns Ratio (N_{ps})
2. Primary Inductance (L_p)
3. Primary to Auxiliary Winding Turns Ratio (N_{aux})

Primary to Secondary Turns Ratio (N_{ps})

For a classical buck configuration, the output voltage is equal to the input voltage multiplied by the duty ratio. Since the forward converter is nothing else than an isolated buck converter, the output voltage can be defined by:

$$V_{out} = N_{PS}.DC.V_{in} \qquad \text{(eq. 1)}$$

Where:

N_{PS} is the primary to secondary turns ratio (N_S/N_P)

DC is the duty cycle defined by the controller

By rearranging the Equation 1 and including the efficiency parameter, the turns ratio can be extracted in the worst case. The worst case mean when the voltage on the bulk capacitor is at the minimum threshold, including the ripple and at the maximum duty cycle.

$$N_{PS} = \frac{V_{out}}{\eta.V_{bulk\_min}.DC_{max}} \qquad \text{(eq. 2)}$$

Regarding the maximum duty ratio, two values can be selected. The first one will be to take the maximum value allowed by the controller so 48 % for the NCL30125. In this case, no margin is taken and in load transient case, the response can be limited by the maximum duty ratio. So the second option will be to include some margins to avoid wrong over current protection or output voltage drop. 40% seems to be a good trade off.

Applying the Equation 2 to our adaptor specification:

$$N_{PS} = \frac{5}{0.9 \times 199 \times 0.4} = 0.070 \qquad \text{(eq. 3)}$$

Let us pick a turns ratio of 0.07 or $1/N_{ps}$ = 14.29. In the above equation, we assume the secondary rectification drop negligible. If a diode is used, the diode forward drop will need to be added on the numerator term.

Transformer Current

Knowing the turns ratio, we need to define the primary peak current to compute transformer inductance. Let's start from the secondary side current. The peak current will be the addition of two parameters: the output current delivered to the load called I_{out} and the half of the current ripple named ΔI_L. The literature demonstrates that 30% of the output current is a good trade for the second parameter.

$$I_{s\_pk} = I_{out} + \frac{\Delta I_L}{2} \qquad \text{(eq. 4)}$$

For our example, the secondary peak current will be:

$$I_{s\_pk} = 60 + \frac{0.3 \times 60}{2} = 69\ A \qquad \text{(eq. 5)}$$

We can now reflect this current to the primary affected by the turns ratio.

$$I_{p\_pk} = I_{s\_pk} \times N_{PS} \qquad \text{(eq. 6)}$$

$$I_{p\_valley} = \left(I_{out} - \frac{\Delta I_L}{2}\right) N_{PS} \qquad \text{(eq. 7)}$$

To this secondary side current reflected on the primary, the magnetization current needs to be added. Again, different articles and works showed that 10% of the peak current brought a good balance.

$$I_{p\_pk\_real} = I_{p\_pk} \times 1.1 \qquad \text{(eq. 8)}$$

Applying these two equations 9 and 10 and to our study gives :

$$I_{p\_valley} = \left(60 - \frac{18}{2}\right)0.07 = 3.57\ A \qquad \text{(eq. 9)}$$

$$I_{p\_pk\_real} = 69 \times 0.07 \times 1.1 = 5.31\ A \qquad \text{(eq. 10)}$$

Having the primary peak current value, we can now calculate the primary inductance of the transformer:

$$L_{mag} = \frac{V_{bulk\_min}}{10\% I_{p\_pk} \frac{F_{SW}}{DC_{max}}} \qquad \text{(eq. 11)}$$

$$L_{mag} = \frac{176\sqrt{2} - 50}{4.85 \times 0.1 \frac{100k}{0.4}} = 1.63\ mH \qquad \text{(eq. 12)}$$

Where the 50−V number is the bulk ripple at the minimum input voltage.

Finally, the primary side RMS current also needed to build the transformer is defined by:

$$I_{p\_rms} = \sqrt{DC_{max}\left[I_{p\_pk\_real}^2 - I_{p\_pk\_real} \times \Delta I_L \times N_{PS} + \frac{\left(\Delta I_L \times N_{PS}\right)^2}{3}\right]} \quad \text{(eq. 13)}$$

$$I_{p\_rms} = \sqrt{0.4\left[5.31^2 - 5.31 \times 18 \times 0.07 + \frac{(18 \times 0.07)^2}{3}\right]} = 2.97\ A \quad \text{(eq. 14)}$$

The three mains transformer characteristics have been calculated in the above section:

1. Primary to Secondary Turns Ratio
2. Primary rms Current
3. Primary Inductance

Step 3: Sense Resistance

Since we know what will be the primary peak current, we need to send this information to the controller via the CS pin. To do that, the current information has to be converted to the voltage dimension. This is the role of the sense resistance. To define this resistance, we need to place the converter in the worst condition so at the minimum input voltage and full load. This current parameter has been already computed thanks to the Equation 10. In order to place the overcurrent limit above the nominal output current, we will apply 10% margin. From controller side, voltage limit is defined by V_{ILimit} parameter (typically 0.5 V).

According to the above explanation, the sense resistance should be:

$$R_{sense} = \frac{V_{ILlimit}}{I_{p\_pk\_real} \times 1.1} \quad \text{(eq. 15)}$$

For the 5−V/300−W application, the final value will be:

$$R_{sense} = \frac{0.5}{5.31 \times 1.1} = 86\ m\Omega \quad \text{(eq. 16)}$$

Step 4: LC Output Filter

In order to determine the output capacitor and inductance that will create the filter, we need to define three parameters. The two first ones, useful for the capacitor, are the maximum output voltage drop accepted during transient load (50% of the maximum output current) and the crossover frequency of this LC filter. Most of the time, we choose 10% of the selected switching frequency. In our case, the switching frequency is 100 kHz so 10−kHz crossover frequency is a good trade off. Regarding the ripple, 4% of the output voltage is an acceptable value so 50 mV here.

$$f_c = 10\ kHz \quad \text{(eq. 17)}$$

$$\Delta V_{out} = 200\ mV \quad \text{(eq. 18)}$$

The last parameter will be output current ripple. A lot of argument can be seen in the literature, but most of the time, 30% of the output current is a good start.

$$\Delta I_L = 30\% \times I_{out} \quad \text{(eq. 19)}$$

An electrolytic capacitor is defined by two parameters: the capacitance and the resistor also called Equivalent Series Resistor (ESR). In order to achieve the voltage drop requirement according to the output current step, both C_{out} and R_{ESR} must satisfy the below equation:

$$C_{out} \geq \frac{\Delta I_{out}}{2\pi \times f_c \times \Delta V_{out}} \quad \text{(eq. 20)}$$

$$R_{ESR} \leq \frac{\Delta V_{out}}{\Delta I_{out}} \quad \text{(eq. 21)}$$

Applying these formulas to our design:

$$C_{out} \geq \frac{30}{2\pi \times 10\ k \times 200\ m} \geq 2.39\ mF \quad \text{(eq. 22)}$$

$$R_{ESR} \leq \frac{200\ m}{30} \leq 6.67\ m\Omega \quad \text{(eq. 23)}$$

Please also note that the rms current flowing into the capacitor must be taken into account. We will be able to calculation when the inductance will be fixed.

So now, let us calculate the inductance:

$$L_{out} = \frac{V_{out}}{\Delta I_L}\frac{\left(1 - DC_{min}\right)}{f_{sw}} = \frac{5}{18}\frac{(1 - 0.21)}{100\ k} = 2.19\ \mu H \quad \text{(eq. 24)}$$

Where DC_{min} is the minimum duty cycle defined by the controller ($DC_{min} = \frac{V_{out}}{\eta \times BV_{bulk\_max} \times N_{ps}}$)

Like for the capacitor, the rms currents will be needed to select the right component.

$$I_{Lout\_rms} = I_{out}\sqrt{1 + \frac{1}{12}\left(\frac{1 - DC_{min}}{\tau_L}\right)^2} \quad \text{(eq. 25)}$$

$$I_{Cout\_rms} = I_{out}\frac{1 - DC_{min}}{\sqrt{12} \times \tau_L} \quad \text{(eq. 26)}$$

Where:

$$\tau = \frac{L_{out}}{\frac{V_{out}}{I_{out}}\frac{1}{f_{sw}}}$$

Step 5: Freewheeling Diode

During the off time, the magnetization current needs to go back to zero before the next cycle to avoid the flux run away into the transformer. This behavior is guaranteed by the freewheel diodes. To evaluate the average current, the magnetization peak current at the maximum duty ratio is needed:

$$I_{mag\_peak} = \frac{V_{bulk\_min}}{L_{mag}} \frac{DC_{max}}{F_{sw}} \quad \text{(eq. 27)}$$

$$I_{mag\_peak} = \frac{176\sqrt{2} - 50}{2.0\ m} \frac{0.4}{100\ k} = 0.40\ A \quad \text{(eq. 28)}$$

Since the magnetization current is flowing through the diode during the off time, the average current is:

$$I_{mag\_avg} = \frac{\frac{DC_{max}}{F_{sw}} \cdot \frac{I_{mag\_peak}}{2}}{T_{sw}} \quad \text{(eq. 29)}$$

$$I_{mag\_avg} = \frac{\frac{0.4}{100\ k} \cdot \frac{0.40}{2}}{10\ \mu} 80\ mA \quad \text{(eq. 30)}$$

In our case, one of the freewheel diode is replaced by a MOSFET. The configuration is needed to refresh the bootstrap capacitor before start−up or in deep skip cycle mode. The same current will go through the MOSFET.

Step 6: Output Diode or Synchronous Rectification MOSFET

The main parameter when you define the secondary side rectifier is related to the reverse voltage. This voltage is linked to the maximum input voltage affected by the turns ratio.

$$V_r = N_{PS} \times V_{bulk\_max} \quad \text{(eq. 31)}$$

$$V_r = 0.07 \times 264\sqrt{2} = 26.1\ V \quad \text{(eq. 32)}$$

With some margin, a MOSFET with a BV_{DSS} at 40 V will be a good choice for this design. In order to limit the power dissipation, three NTMFS5C450NL MOSFETs will be put in parallel. The $R_{DS(on)}$ of this reference is 3.45 mΩ @ 110 °C.

The main warming contributor for this high output current application will be the conduction losses. For the forward MOSFET that is turned on in the same time as the primary MOSFETs, the conduction losses are only linked to the $R_{DS(on)}$.

$$P_{MOS\_Forward} = \left(\frac{I_{out}^2}{nber1}\right) \times DC_{max} \times R_{DS(on)} \quad \text{(eq. 33)}$$

Where nber1 is the number of the MOSFET put in parallel. We consider that the current will be equally shared between each MOSFET.

$$P_{MOS\_Forward} = \left(\frac{60^2}{3}\right) \times 0.4 \times 3.45\ m = 1.65\ W \quad \text{(eq. 34)}$$

Regarding the freewheel MOSFET that are turned on during the off time, two conduction losses need to be calculated. The first one is the same as the forward MOSFET and linked to the $R_{DS(on)}$ resistor.

The second one is related to the delay between the forward switch turn off and freewheel MOSFET turn on. This delay is defined by the synchronous rectification controller itself. In our case with the NCP4306, the delay is 30 ns. During this duration, the MOSFET body diode will take over the current.

$$P_{MOS\_FW1} = \left(\frac{I_{out}^2}{nber2}\right) \times (1 - DC_{max}) \times R_{DS(on)} \quad \text{(eq. 35)}$$

$$P_{MOS\_FW2} = V_f \times I_{out} \times F_{SW} \times t_{delay} \quad \text{(eq. 36)}$$

Where nber2 is the number of the freewheel MOSFET put in parallel and V_f the MOSFET body diode forward voltage.

Applying these previous equations to the design under study will lead to:

$$P_{MOS\_FW1} = \left(\frac{60^2}{3}\right) \times (1 - 0.4) \times 3.45\ m = 2.49\ W \quad \text{(eq. 37)}$$

$$P_{MOS\_FW2} = 0.72 \times 60 \times 100\ k \times 30\ n = 0.13\ W \quad \text{(eq. 38)}$$

$$P_{MOS\_FW\_total} = P_{MOS\_FW1} + P_{MOS\_FW2} = 2.62\ W \quad \text{(eq. 39)}$$

With this amount of power into the MOSFETs, a heatsink will be necessary to avoid temperature run away. We can consider a maximum ambient temperature T_{ambmax} around 65°C. Regarding the MOSFETs, we will set the maximum junction temperature T_{jmaxM} at 130°C. Taking in account the SO8FL package thermal resistance ($R_{\theta j\_cM}$ = 1.2°C/W) and also case to heatsink resistance ($R_{\theta j\_hM}$ = 1.0°C/W), the needed heatsink thermal resistance can be evaluated:

$$R_{\theta h\_aMOS} = \frac{T_{jmaxM} - T_{ambmax}}{P_{MOS}} - R_{\theta j\_cM} - R_{\theta c\_hM} \quad \text{(eq. 40)}$$

So the maximal heatsink thermal resistance for the each forward MOSFET is:

$$R_{\theta h\_aMOS\_Forward} = \frac{130 - 65}{1.65} - 1.2 - 1.0 = 37\frac{°C}{W} \quad \text{(eq. 41)}$$

$$R_{\theta h\_aMOS\_FW} = \frac{130 - 65}{2.62} - 1.2 - 1.0 = 22.6\frac{°C}{W} \quad \text{(eq. 42)}$$

Step 7: Bulk capacitor

The input filtering capacitor also called bulk capacitor is to need to ensure a minimum input voltage and delivered the maximum output power affected by the efficiency. The rms current in addition to the rated voltage has also to be carefully consider to not affect the capacitor life time.

Considering the minimum input voltage and the target efficiency, the minimum capacitor should be:

$$C_{bulk} = \frac{2P_{out}\left[\frac{1}{4F_{line}} + \frac{\arcsin\left(\frac{V_{bulk\_min}}{VIN_{minDC}}\right)}{2\pi F_{line}}\right]}{\eta\left(VIN_{minDC}^{2} - V_{bulk\_min}^{2}\right)} \quad \text{(eq. 43)}$$

Where:

- VIN_{minDC} is the peak input voltage at low mains $(176\sqrt{2})$
- F_{line} is the input voltage frequency at low mains
- V_{bulk_min} is the minimum voltage target on the bulk capacitor

In our design, the minimum bulk capacitor is:

$$C_{bulk} \geq \frac{2 \times 300\left[\frac{1}{4\times 50} + \frac{\arcsin\left(\frac{176\sqrt{2}-50}{176\sqrt{2}}\right)}{2\pi\times 50}\right]}{0.9\left(\left(176\sqrt{2}\right)^{2} - \left(176\sqrt{2} - 50\right)^{2}\right)} = 236\ \mu F \quad \text{(eq. 44)}$$

Let's us put two 150−μF capacitor in parallel.

With a very simple simulation, we can deduced the new minimum bulk voltage including the ripple: 211 V.

If all calculations are needed, please read the reference [1], chapter 6.

$$t_{cb} = \frac{1}{4F_{line}} - \frac{\arcsin\left(\frac{V_{bulk\_min}}{VIN_{minDC}}\right)}{2\pi F_{line}} = \quad \text{(eq. 45)}$$

$$= \frac{1}{4 \times 50} - \frac{\arcsin\left(\frac{210}{176\sqrt{2}}\right)}{2\pi \times 50} = 1.79\ ms$$

$$t_{db} = \frac{1}{2\pi F_{line}}\arcsin\left(\frac{V_{bulk\_min}}{VIN_{minDC}}\right) = \quad \text{(eq. 46)}$$

$$= \frac{1}{2\pi \times 50}\arcsin\left(\frac{210}{176\sqrt{2}}\right) = 3.21\ ms$$

Calculate the peak current in the bulk capacitor:

$$I_{bulk\_pk} = 2 \times C_{bulk} \times VIN_{minDC} \times \cos\left(2\pi F_{line} t_{db}\right) \times \pi F_{line}$$

$$I_{bulk\_pk} = 2 \times 300\ \mu \times 176\sqrt{2} \times \cos(2\pi \times 50 \times 3.21\ m) \times$$

$$\times \pi \times 50 = 12.48\ A \quad \text{(eq. 47)}$$

Then, calculate the load peak and minimum current values:

$$I_{load\_max} = \frac{P_{out}}{\eta V_{bulk\_min}} = \frac{300}{0.9 \times 210} = 1.58\ A \quad \text{(eq. 48)}$$

$$I_{load\_min} = \frac{P_{out}}{\eta VIN_{minDC}} = \frac{300}{0.9 \times 176\sqrt{2}} = 1.34\ A \quad \text{(eq. 49)}$$

Calculate the diode peak current and deduce the associated down slope from the peak value to t_{cb}:

$$I_{diode\_pk} = I_{load\_max} + I_{bulk\_pk} = 1.58 + 12.48 = 14.06\ A \quad \text{(eq. 50)}$$

$$S_{diode} = \frac{I_{diode\_pk} - I_{load\_min}}{t_{cb}} = \frac{14.06 - 1.33}{1.79\ m} = 7125\frac{A}{s} \quad \text{(eq. 51)}$$

The diode conduction time and his average current can be deduced:

$$t_{diode\_c} = \frac{I_{diode\_pk}}{S_{diode}} = \frac{14.06}{7125} = 1.97\ ms \quad \text{(eq. 52)}$$

$$I_{diode\_avg} = I_{diode\_pk} \times t_{diode\_c} \times F_{line} = \quad \text{(eq. 53)}$$

$$= 14.06 \times 1.97\ m \times 50 = 1.39\ A$$

And finally, the low frequency rms current of the bulk capacitor can be evaluated:

$$I_{bulk\_rmsLF} = I_{diode\_avg}\sqrt{\frac{2}{3F_{line}t_{diode\_c}} - 1} \quad \text{(eq. 54)}$$

$$I_{bulk\_rmsLF} = 1.39\sqrt{\frac{2}{3 \times 50 \times 1.97\ m} - 1} = 3.33\ A \quad \text{(eq. 55)}$$

The total rms current of the bulk capacitor is the combination of the low frequency rms current and the high frequency rms current linked to the controller switching frequency:

$$I_{bulk\_rmsTOT} = \sqrt{I_{bulk\_rmsLF}^{2} + I_{bulk\_rmsHF}^{2}} \quad \text{(eq. 56)}$$

The primary rms current (HF current) was calculated for the transformer design, equation 14 so the final rms current can be evaluated to:

$$I_{bulk\_rmsTOT} = \sqrt{3.33^2 + 2.97^2} = 4.46\ A \quad \text{(eq. 57)}$$

Please note that the bulk capacitor rms current capability is higher at high frequency so a derating factor can be applied for I_{bulk_rmsHF}. Also, the input voltage impedance and the EMI filter can affect the low frequency rms current. The two previous point will lead to a lower real rms current.

Step 8: Brown Out

The NCL30125 controller integrates a dedicated brown out pin in order to avoid over stress on the converter with too low input voltage. Lets assume a 40−μA target current into the BO bridge resistors and a starting point to 176 V rms.

The lower resistor values will be defined by the controller BO ON threshold (0.8 V) and the bridge current:

$$R_{BO\_lower} = \frac{V_{BO(on)}}{I_{bridge}} \quad \text{(eq. 58)}$$

$$HR_{BO\_lower} = \frac{0.8}{40\ \mu} = 20\ k\Omega \quad \text{(eq. 59)}$$

The upper resistance can be calculated according to the target minimum input voltage:

$$R_{BO\_upper} = \frac{VIN_{BO(on)}\sqrt{2} - V_{BO(on)}}{I_{bridge}} \quad \text{(eq. 60)}$$

$$R_{BO\_upper} = \frac{176\sqrt{2} - 0.8}{40\ \mu} = 6.2\ M\Omega \quad \text{(eq. 61)}$$

If we select a normalized 20−kΩ resistor for the R_{BO_lower} and 6.2 MΩ for R_{BO_upper}, the new BO thresholds are:

$$VIN_{BO(on)} = V_{BO(on)}\frac{R_{BO\_lower} + R_{BO\_upper}}{R_{BO\_lower}\sqrt{2}} = = 0.8\frac{20\ k + 6.2\ M}{20\ k\sqrt{2}} = 176\ Vrms \quad \text{(eq. 62)}$$

$$VIN_{BO(off)} = V_{BO(off)}\frac{R_{BO\_lower} + R_{BO\_upper}}{R_{BO\_lower}\sqrt{2}} = = 0.7\frac{20\ k + 6.2\ M}{20\ k\sqrt{2}} = 154\ Vrms \quad \text{(eq. 63)}$$

Step 9: Switching Frequency

As mentioned in the NCL30125 datasheet, the switching frequency is following the below equation:

$$R_{RT} = \left(\frac{1}{f_{sw}} - 120\ n\right).10^7 \quad \text{(eq. 64)}$$

The switching frequency target is 100 kHz so the corresponding resistor is:

$$R_{RT} = \left(\frac{1}{100\ k} - 120\ n\right).10^7 = 98.8\ k\Omega \quad \text{(eq. 65)}$$

Step 10: Soft−Start

The soft start can be adjusted thanks to the dedicated pin. The needed capacitance for defined soft start duration is:

$$C_{SS} = \frac{I_{SS}.T_{SS}}{2.0}V \quad \text{(eq. 66)}$$

$$C_{SS} = \frac{5.2\ \mu \times 4\ m}{2} = 10\ nF \quad \text{(eq. 67)}$$

Step 11: Bootstrap Capacitor

The bootstrap capacitor purpose is to store the energy during the off time and supply the floating high side driver during the on time when the MOSFETs are turned on.

The high side UVLO threshold is 8 V according to the datasheet. If we assume a 12−V minimum voltage on the V_{cc} pin and take some marging to have a proper MOSFET drive:

$$\Delta V = V_{cc(min)} - V_{f\_boot} - \left(UVLO_{driver} + Margin\right) = = 12 - 0.8 - (8.0 + 2) = 1.2\ V \quad \text{(eq. 68)}$$

Then, the total load on the DRV_HI pin has to be computed. We have of course the MOSFET with its total gate charge Q_G and the second part is related to pull down resistor placed between the gate and the source MSOFET pin and the controller consumption itself. The combination of these parameters gives:

$$C_{boot} \geq \frac{Q_G + \frac{DC_{max}}{F_{sw}}\left(\frac{V_{cc(min)} + V_{f\_boot}}{R_{PD}} + I_{boot1}\right)}{\Delta V} \quad \text{(eq. 69)}$$

Applying this equation to our example:

$$C_{boot} \geq \frac{75n + \frac{0.4}{100\ k}\left(\frac{12+0.8}{47\ k} + 700\ \mu\right)}{1.2} = 66\ nF \quad \text{(eq. 70)}$$

Step 12: Ramp Compensation

In order to know if an external ramp compensation is needed, we need to evaluation the natural ramp brought by the magnetization inductance:

$$S_a = \frac{V_{bulk\_min}}{L_{mag}}R_{sense} = \frac{210}{1.63\ m} \times 86\ m = 11\ mV/\mu s \quad \text{(eq. 71)}$$

We also need the on time slope seen on the secondary side:

$$S_n = \frac{N_{PS}V_{bulk\_min} - V_{out}}{I_{out}}N_{PS}R_{sense} \quad \text{(eq. 72)}$$

Applying this equation to our design we lead to:

$$S_n = \frac{70\ m \times 210 - 5}{2.19\ \mu} \times 70\ m \times 86\ m = 27\ mV/\mu s \quad \text{(eq. 73)}$$

From the two previous equations, we can compute the m_c parameter:

$$m_c = 1 + \frac{S_a}{S_n} = 1 + \frac{11}{27} = 1.41 \quad \text{(eq. 74)}$$

The literature demonstrates the relationship between m_c and the Q factor. Mc parameter needs to be adjusted in order to reduce the Q factor to 1 that corresponding to 50% ramp compensation.

$$Q = \frac{1}{\pi[m_c(1 - DC_{max}) - 0.5]} = = \frac{1}{\pi[1.4 \times (1 - 0.4) - 0.5]} = 0.94 \quad \text{(eq. 75)}$$

In our case, we can see that the natural slope brings enough ramp compensation to maintain the Q factor below 1. If it is not case, the new m_c will have to be calculated following the Equation 76 and the needed adding slope estimated (eq. 77).

$$m_{c\_new} = \frac{\frac{1}{\pi} + 0.5}{1 - DC_{max}} \quad \text{(eq. 76)}$$

$$S_{add} = S_n(m_{c\_new} - 1) - S_a \quad \text{(eq. 77)}$$

Finally, the resistor in series with the CS pin and the sense resistor will be:

$$R_{comp} = R_{ramp}\frac{S_{add}}{S_{ramp}} \quad \text{(eq. 78)}$$

Where:

- R_{ramp} is the internal resistance (26.5 kΩ)
- S_{ramp} is the internal ramp affected by the switching frequency $(\frac{V_{ramp}}{DC_{maxIC}} T_{sw})$

In our case, since the magnetization inductance does the jog, the compensation resistor will be inserted just to filter the CS pin.

Conclusion

This paper summarizes the key steps when dimensioning a NCL30125 two−switch forward board. The proposed approach being systematic, it can be easily applied to other applications. All the equations (and more) presented have been implemented inside a Mathcad® spreadsheet that can be downloaded from our website [5].

The process has been illustrated by the example of the 300−W, 5−V output voltage evaluation board. You can find the experimental results of the 300−W adapter in the "A 300−W adapter with NCL30125" [3]. Implementation details (Schematic, BOM, GERBER file…) can be found on our web site [4].

More details on the circuit operation can be found in its data sheet [2].

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