

Charging Capacitive Loads with eFuse



ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

Introduction

The eFuse protection devices are used for limiting the system load current in the events of overload or short circuit. Many applications employ On Semiconductor eFuses at the power input stage of the system between the main power input connector and DC-DC converters or power regulators. The systems utilizing eFuse protection devices at the power input stage may represent inductive, resistive, capacitive or mixed types of loads.

One of the common load characteristics for various systems is large capacitive load, typically starting from 1mF all the way to few hundred milli Farads. The challenge presented by such load to an overcurrent protection system is large inrush current due to the excessive capacitance which will cause the device to shut down during startup.

Typical way of handling the device startup into a large capacitive load with eFuses is to control the output slew rate by slowing it down.

This application note describes the Auto-Retry feature of the eFuses which can aid in rapid output capacitor charging to a target voltage without slowing down the output slew rate.

Typical application

The Figure 1 shows the typical arrangement of the eFuse before the system which is protected from overcurrent (or possibly overvoltage as well) and utilizing a large input capacitance designated as C_{OUT} on the eFuse side.

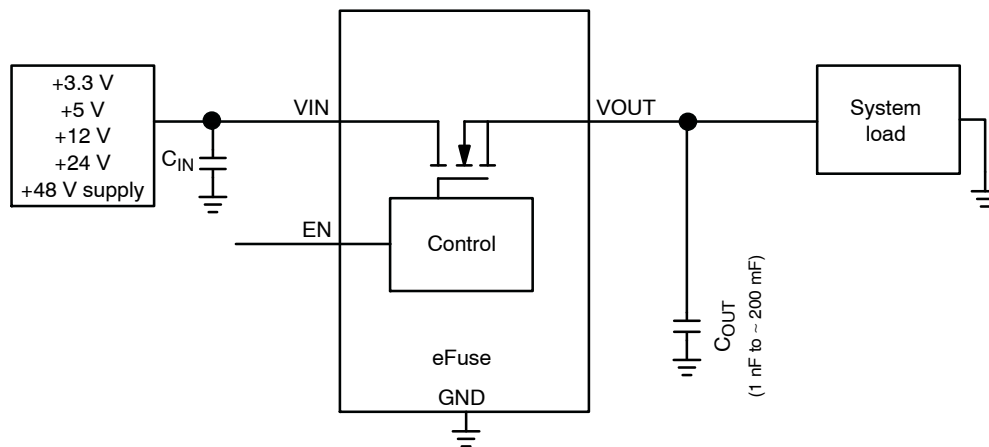


Figure 1. eFuse Protecting a System with Large Input Capacitance from Overcurrent

In order to avoid the turn off during a startup the slew rate can be slowed down, usually by the means of adding a capacitor to the dVdt pin of the given eFuse. Alternatively, an auto-retry feature of the eFuse can be utilized which allows the inrush current in the limited amount to flow through the internal FET during the startup while charging the output capacitance COUT.

When the eFuse with Auto-Retry feature is selected the output voltage slew rate limitation does not need to be set; the user would just set a desired current limit level (typically using an RLIM current limit setting resistor) and configure the device with minimum slew rate which is usually done by leaving dVdt pin unconnected. Once the eFuse is enabled through the Enable pin, the main power FET is turned on and the COUT capacitance starts charging. The inrush current is normally proportional to the product of COUT and the output voltage slew rate, however; in this case it will be limited by the current limit setting of the eFuse.

While the current limit mode is active the internal power FET will be heating up due to the dissipated power which is a product of limited current flowing through it as well as the VDS difference or voltage potential between VIN and VOUT. At some point after reaching the thermal shutdown temperature (which varies between 150°C to 200°C

depending on the eFuse) the FET will be shut off leaving the VOUT precharged to a certain value being kept by a large capacitance COUT. As soon as the FET cools down by a hysteresis temperature threshold (typically between 20°C and 40°C) it is being turned on again and the current limited by the programmed current limit level again flows through it, further charging up the output capacitance. This process continues until the VOUT is charged to the voltage of VIN or until the large output capacitance is fully charged to the VIN voltage. The process will represent a gradually increasing VOUT voltage and multiple short bursts of current flowing through FET, where each burst is limited to a set programmed value. The width and time interval between bursts will depend on the thermal properties of the eFuse power FET device, package type and environmental temperature.

Measurement and Operation

As an example, consider a 12 V application with extremely large output capacitance of 150 mF. The eFuse used in this example is NIS5020MT2 which is a 12 V eFuse device with Auto-Retry feature. The Figure 2 shows the measurement snapshot with input voltage, output voltage, input current, and Enable/Fault pin of the NIS5020 device.

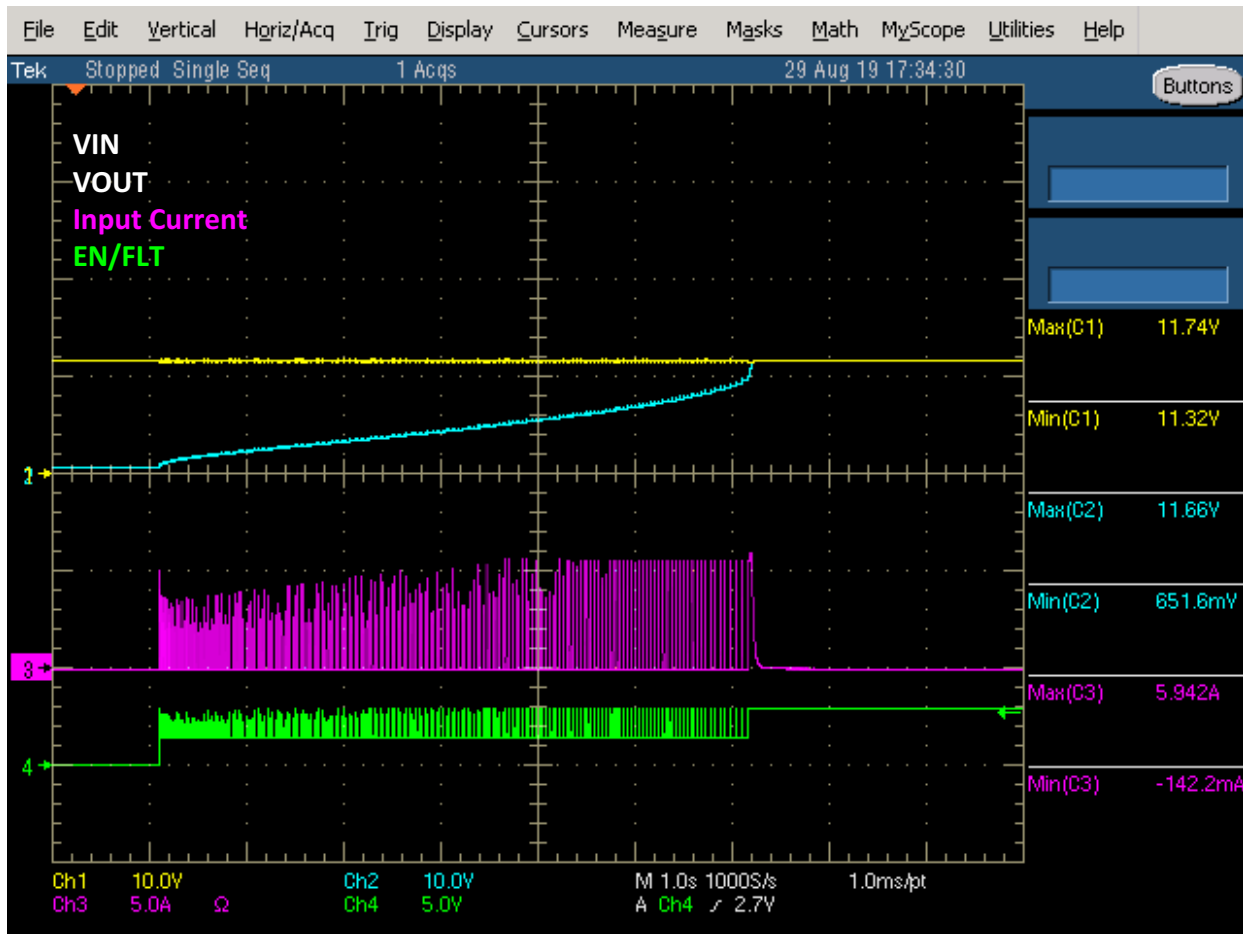


Figure 2. Charging 150 mF Output capacitance with 12 V NIS5020 Series eFuse

AND9955/D

The initial voltage at the input is 12 V, eFuse is disabled by the means of the grounded Enable/Fault pin. The current limit is set to about 6 A. Once the Enable pin is released the eFuse is enabled and initial inrush current is limited to about 6 A and the eFuse performs multiple On and Off cycles gradually charging the VOUT output voltage to a target value of 12 V. This can be seen in Figure 2.

We can observe that the current On and Off cycles are much denser at the beginning once the eFuse has just been

turned on, which makes sense because at that point of time the VOUT output voltage is very low and the VDS voltage potential for the internal FET is very large thus resulting in a huge heat dissipation and causing more often restart cycles of the FET. However, as soon as VOUT voltage increases the power dissipation becomes less for the internal FET and that results in a less frequent restart cycles, this can be observed from Figure 3, a zoomed version of snapshot in Figure 2.

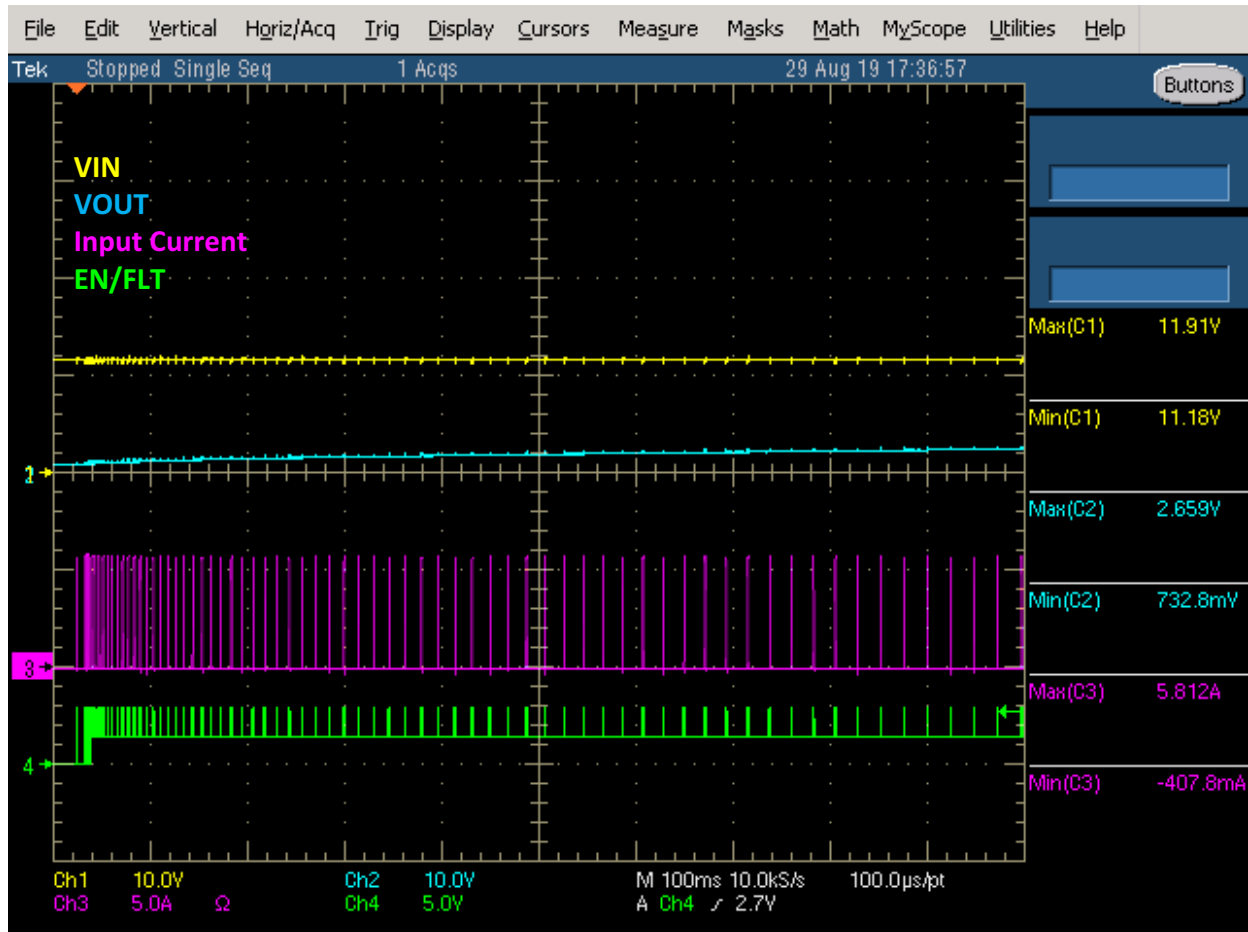


Figure 3. Beginning Phase of Output Capacitor Charging using NIS5020

Once the output voltage is charged to the level of the input voltage the large current spikes stop, given the fact that external aside from the capacitor has not turned on yet.

We can also see the Enable/Fault pin going from 3 V to 1.4 V during the eFuse restart cycles when capacitance is

charged; this is compliant to the operating mode of the NIS5020 series eFuses where the En/FLT pin is at 1.4 V during the thermal shutdown phase and 3 V during the normal operating phase and it can be observed from Figure 4.



Figure 4. Restart Cycles and Enable/Fault Pin Levels of NIS5020 during Output Capacitance Charging

Another example of output capacitance charging during a startup would be with NIS3070, multichannel 48 V circuit breaker type eFuse. In that eFuse, the load current is allowed to flow above programmed ILIM level as long as it does not exceed the 1.5x/2x (depending on the part number) of the ILIM threshold, or as long as the main FET(s) is not overhead or the trip timer runs out. Trip timer starts counting to 400 µs the moment the load current exceeds the ILIM level. In this example, the current limit was set to about 2.8 A and only one of the four channels is utilized. The output capacitance is 3.76 mF and the input voltage is 48 V.

Once the channel is enabled, the current limited to ILIM level of around 2.8 A is flowing through the internal power FET in multiple bursts, as the number of bursts increases, the output voltage gets charged closer to 48 V. For the NIS3070 eFuse the FAULT pin is always pulled low as long as the device is in overcurrent mode, which is the mode it would be in during the large output capacitance charging. As soon as the output voltage is charged to 48 V the open-drain fault indication FAULT pin is released and pulled high. This can be observed in Figure 5.

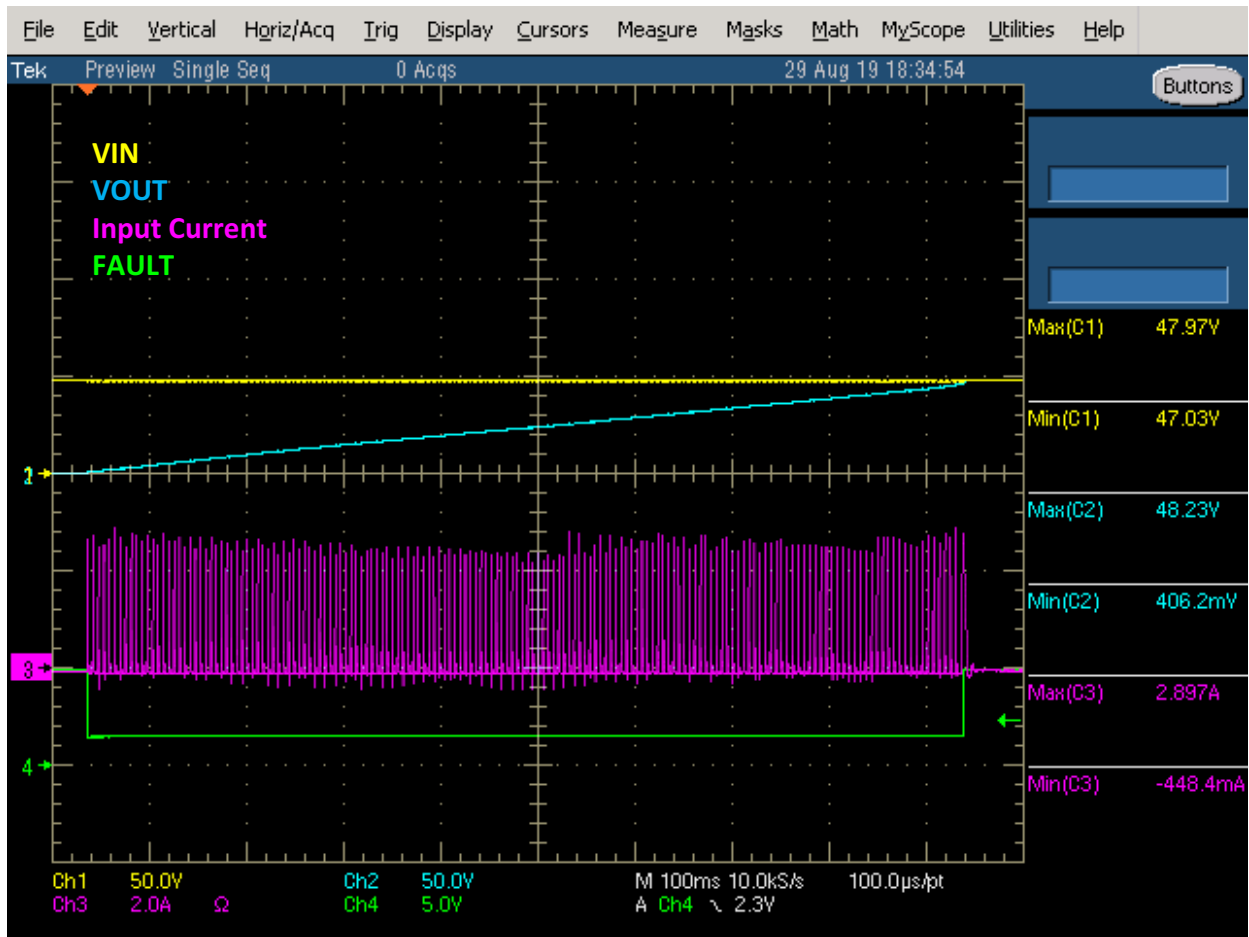


Figure 5. NIS3070 Multichannel eFuse Charging Output Capacitance of 3.76 mF to 48 V

The zoomed view of input current waveform can be seen in Figure 6. The internal FET is conducting limited current and is shut down once it overheats, then restarts again once the internal temperature is down by hysteresis threshold of

around 27°C (typical for NIS3070 eFuse). In the current zoomed snapshot area, the output voltage reached about half the target voltage of 48 V.

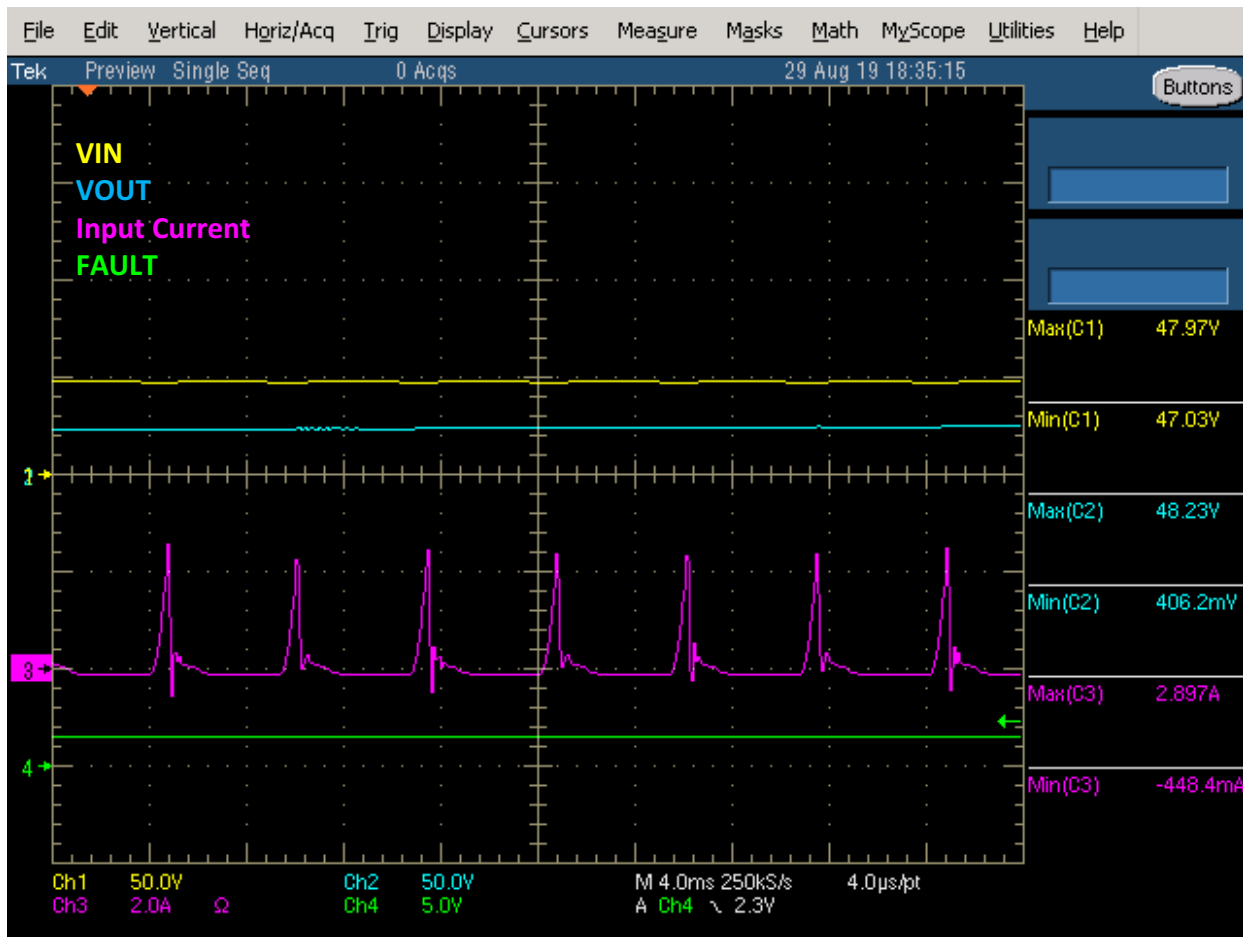


Figure 6. NIS3070, Snapshot of Multiple Current Bursts during Output Capacitance Charging

Conclusion

The Auto-Retry feature of the eFuses is valuable not only for the applications requiring a restart after the cleared fault events but also for the applications involving large or extremely large output capacitance which needs to be precharged to the target input voltage upon the startup. This method of charging the large output capacitance can be typically faster than just slowing down the output voltage

slew rate; additionally, it is safe for the internal power FET of the eFuse since the internal temperature sensor with thermal protection feature does not allow the FET to overheat to a temperature dangerous to a limit where the FET damage can occur. The inrush current can also be set to any desired value during a startup phase. The method can be safely applied to the Auto-Retry eFuses of all voltages from 3 V to 48 V.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
 Literature Distribution Center for ON Semiconductor
 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
 Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative