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ONA10IV I²C Register Definitions

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APPLICATION NOTE

Overview

This document provides a basic description of the ONA10IV I2C interface and capabilities, along with the I2C register map and detailed register tables for all available device registers. Default register states and digital audio interface settings are also provided.

Table 1. ONA10IV RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min (Note 1)	Typ	Max	Unit
T_A	Operating Temperature Range	−40	–	85	°C
DV_{DD}	Digital Supply Voltage Range	1.62	–	1.98	V
PV_{DD}	Power Supply Voltage Range (2s – Battery Configuration)	5.5	–	9.0	V
	Power Supply Voltage Range (3s – Battery Configuration)	7.5	–	14.0	V
Z_L	Load Inductance	–	10	–	μH
	Load Resistance	4	–	–	Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. Minimum passive component values include temperature, tolerance, and aging.

I²C Interface

The ONA10IV supports I²C Fast Mode operation up to 1 Mbit/s. This device also supports multiple−byte I²C read/write operations.

ONA10IV Default I²C Register Map Configuration

Upon power−up, the device is placed in software shutdown mode. I²C communication is enabled. The default digital audio interface (DAI) configuration upon power−on or after software reset is as shown in Table 2 below. In addition, several features are enabled by default (Note 1), including:

- Temperature Foldback Protection (TFB)
- Automatic Gain Control (AGC)
- Speaker V/I Sense (Note 2)

The default battery configuration is set to 3S, for use with a PVDD voltage range of 7.5 V to 14 V.

Also by default, edge rate control (ERC) is set to 3.5 V/ns and spread−spectrum modulation is disabled.

For further details on default register settings, see the ‘Reset Value’ for each register in the register summary table on the following page.

NOTE 1: Over−Temperature Protection (OTP), a die−protection feature, is always active and is not capable of being disabled.

NOTE 2: Although the speaker V/I sense circuitry is enabled by default, sense data transmission on DATAO needs to be enabled.

Table 2. DEFAULT AUDIO PATH CONFIGURATION

Register Address	Reset Value	Configuration
0x01	00h	Device in Shutdown mode; Default features enabled.
0x06	06h	I2S @ fs = 48 kHz; Frame delayed by 1 CKI; Data clocked on falling edge
0x07	55h	Sample width = 24−bit; Slot−width = 24−bit
0x08	00h	Data Input = PCM format; Slot 0 (Left channel) selected
0x09	00h	Maximum allowable volume set to 0 dB (full volume)
0x0A	0Eh	Volume up/down ramp enabled @ 3.75 dB/ms; Volume change made at input signal zero−crossing; Amplifier output un−muted.
0x0B	00h	Class D amplifier gain = 16 dB (maximum)

I²C REGISTER DESCRIPTION

REGISTER SUMMARY

ADDR	Register	Type	Reset Values	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	DEVICE_ID	R	0x86	DEV_ID					VER_ID		
0x01	PWR_CTRL	R/W	0x00	TFB_PD	BATT_CFG	AGC_PD	IVSNS_PD	AMP_PD	SD_N	STBY	RST
0x02	INT_FLAG	R/W1C	0x00	RESERVED		TFB_I	AGC_I	CERR_I	TERR_I	IERR_I	VERR_I
0x03	INT_MASK	R/W	0x00	RESERVED	ALL_MASK	TFB_M	AGC_M	CERR_M	TERR_M	IERR_M	VERR_M
0x04	ERR_STAT	R	0x00	RESERVED		TFB	AGC	CERR	TERR	IERR	VERR
0x05	ERR_CTRL	R/W	0x00	RESERVED		MRCV	MAX_ARCV		ARCV_T	ARCV_I	ARCV_C
0x06	DAI_CTRL1	R/W	0x06	BEDGE_DAI	FORMAT	DAI		FS			
0x07	DAI_CTRL2	R/W	0x55	SAMPW		SLOTW		FRM_DLY		FRM_POL	FRCK _MODE
0x08	DAI_CTRL3	R/W	0x00	RESERVED				PDM_MODE	A_SLOT		
0x09	MAX_VOL	R/W	0x00	MAX_VOL							
0x0A	VOL_CTRL	R/W	0x0E	RESERVED			VOL_RAMP		AVOL_UP	AVOL_DN	MUTE
0x0B	GAIN_CTRL1	R/W	0x00	RESERVED			PCM_AMP_GAIN				
0x0C	GAIN_CTRL2	R/W	0x40	RESERVED	PDM_DAC_MAP		PDM_AMP_GAIN				
0x0D	EMI_CTRL	R/W	0x1C	RESERVED			AMP_ERC		SS_MOD		
0x0E	AGC_BATT	R/W	0x00	BATT_DEBO	BATT_RTH		BATT_ATH				
0x0F	AGC_CTRL1	R/W	0x00	AGC_HOLD				AGC_ATTACK			
0x10	AGC_CTRL2	R/W	0x00	RESERVED	AGC_MAX_ATT			AGC_RELEASE			
0x11	AGC_CTRL3	R/W	0x00	RESERVED						AGC_TIMEOUT	
0x12	MAGC_CTRL1	R/W	0x00	RX_SLOT8	RX_SLOT7	RX_SLOT6	RX_SLOT5	RX_SLOT4	RX_SLOT3	RX_SLOT2	RX_SLOT1
0x13	MAGC_CTRL2	R/W	0x00	TX_SLOT8	TX_SLOT7	TX_SLOT6	TX_SLOT5	TX_SLOT4	TX_SLOT3	TX_SLOT2	TX_SLOT1
0x14	MAGC_CTRL3	R/W	0x00	RESERVED					MAGC_ODRV		MAGC_EN
0x15	SENSE_CTRL	R/W	0x00	T_HOLD		T_ATTACK		T_ATH		T_SAMP	
0x16	T_SENSE_OUT1	R	0x00	T_SENSE_OUT<7:0>							
0x17	T_SENSE_OUT2	R	0x00	RESERVED					T_SENSE_OUT<10:8>		
0x18	DATAO_CTRL1	R/W	0x00	RESERVED			HPF_BP	PDM_OUT		DATA_ODRV	
0x19	DATAO_CTRL2	R/W	0x08	I_DATAO_TX	V_DATAO_TX	I_SLOT			V_SLOT		
0x1A	DATAO_CTRL3	R/W	0x02	RESERVED				T_DATAO _TX	T_SLOT		

REGISTER DETAILS

Table 3. 0x00: DEVICE_ID
Address: 0x00
Type: R
Reset Value: 1000_0110 (0x86)

Bit #	Name	Size (Bits)	Function
7:3	DEV_ID	5	Device ID: 5'b10000
2:0	VER_ID	3	Device version ID

Table 4. 0x01: PWR_CTRL
Address: 0x01
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7	TFB_PD		Thermal Foldback Disable: **0 | Normal Operation** 1 | Thermal foldback disabled. Thermal protection remains enabled.
6	BATT_CFG	1	Battery Configuration: **0 | PV_{DD} within 3S Battery Range (7.5 V to 14 V)** 1 | PV_{DD} within 2S Battery Range (5.5 V to 9 V)
5	AGC_PD	1	Automatic Gain Control Disable: **0 | Normal operation** 1 | Automatic Gain Control disabled.
4	IVSNS_PD	1	Speaker Current and Voltage Sense Disable: **0 | Normal operation** 1 | IV Sense disabled
3	AMP_PD	1	Amplifier Disable: **0 | Normal operation** 1 | Class D amplifier disabled
2	SD_N	1	Forces SHUTDOWN power state: **0 | SHUTDOWN power state** 1 | Normal operation
1	STBY	1	Forces STANDBY power state: **0 | Normal operation** 1 | STANDBY power state
0	RST	1	Software Reset Resets all internal blocks and I^2C registers to default values: **0 | No change** 1 | Software reset

Table 5. 0x02: INT_FLAG
Address: 0x02
Type: R/W1C
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:6	Reserved	2	
5	TFB_I	1	Device in thermal foldback state: **0 | No change to active status.** 1 | TFB active status changed.
4	AGC_I	1	Device in local automatic gain control (AGC) state: **0 | No change to active status.** 1 | AGC active status changed.
3	CERR_I	1	Clock Rate Error. This flag is set if either of the clocks (CKI, or FRCK) are not present or do not meet required timing: **0 | No change to error status.** 1 | Clock error fault status changed.
2	TERR_I	1	Over−Temperature Error: **0 | No change to error status.** 1 | Over−temperature fault status changed.
1	IERR_I	1	Over−Current Error: **0 | No change to error status.** 1 | Over−current fault status changed.
0	VERR_I	1	Under−Voltage Error: **0 | No change to error status.** 1 | Under−voltage fault status changed.

2. The interrupt flag register indicates that a change has occurred. The active status is found in the error status register.

Table 6. 0x03: INT_MASK
Address: 0x03
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7	Reserved	1	
6	ALL_MASK	1	Masks all interrupts: **0 | Interrupts can individually be enabled.** 1 | All interrupts masked.
5	TFB_M	1	Thermal Foldback Mask: **0 | TFB Interrupt Enabled** 1 | TFB Interrupt Masked
4	AGC_M	1	AGC Active Mask: **0 | AGC Interrupt Enabled** 1 | AGC Interrupt Masked
3	CERR_M	1	Clock Rate Error Mask: **0 | CERR Interrupt Enabled** 1 | CERR Interrupt Masked
2	TERR_M	1	Over−Temperature Error Mask: **0 | TERR Interrupt Enabled** 1 | TERR Interrupt Masked
1	IERR_M	1	Over−Current Error Mask: **0 | IERR Interrupt Enabled** 1 | IERR Interrupt Masked
0	VERR_M	1	Under−Voltage Error Mask: **0 | VERR Interrupt Enabled** 1 | VERR Interrupt Masked

Table 7. 0x04: ERR_STAT (Read Only)
Address: 0x04
Type: R
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:6	Reserved	2	
5	TFB	1	Thermal Foldback Active: This bit is set if the ONA10IV is automatically adjusting the volume due to the die temperature. **0 | Normal operation.** 1 | TFB Active.
4	AGC	1	Automatic Gain Control Active: This bit is set if the ONA10IV is automatically adjusting the gain or in AGC_TIME-OUT. **0 | Normal operation.** 1 | AGC Active.
3	CERR	1	Clock Rate Error: This bit is set if any of the clocks (MCK, CKI, or FRCK) are not present or do not meet required timing. This includes if the SAMPW setting does not correspond to the FS register setting. **0 | Normal operation.** 1 | Clock error fault detected.
2	TERR	1	Over−Temperature Error: **0 | Normal operation.** 1 | Over−temperature fault detected.
1	IERR	1	Over−Current Error: **0 | Normal operation.** 1 | Over−current fault detected.
0	VERR	1	Under−Voltage Error: **0 | Normal operation.** 1 | Under−voltage fault detected.

3. The error status register always shows the active status of the error whereas the interrupt flag register indicates that a change has occurred.

Table 8. 0x05: ERR_CTRL
Address: 0x05
Type: R/W
Reset Value: 0000_0111 (0x07)

Bit #	Name	Size (Bits)	Function
7:6	Reserved	2	
5	MRCV (Write Only)	1	Manual Fault Recovery: **0 | Normal Operation** 1 | Attempts to immediately recover any controls that are set for manual recovery.
4:3	MAX_ARCV	2	Automatic Fault Recovery Attempts: **00 | Always attempts to auto−recover** 01 | 1 Attempt then goes into STANDBY 10 | 3 Attempts then goes into STANDBY 11 | 7 Attempts then goes into STANDBY
2	ARCV_T	1	Over−Temperature Recovery Control: 0| Manual Recovery for an Over Temperature Fault **1 | Automatic Recovery for an Over Temperature Fault**
1	ARCV_I	1	Over−Current Recovery Control: 0 | Manual Recovery for an Over Current Fault **1 | Automatic Recovery for an Over Current Fault**
0	ARCV_C	1	Clock Recovery Control: 0 | Manual Recovery for an Clock Fault **1 | Automatic Recovery for an Clock Fault**

Table 9. 0x06: DAI_CTRL1
Address: 0x06
Type: R/W
Reset Value: 0000_0110 (0x06)

Bit #	Name	Size (Bits)	Function
7	BEDGE_DAI	1	CKI Active Edge Select for the digital audio input (PCM or PDM input): **0 | Data is clocked on the falling edge** 1 | Data is clocked on the rising edge
6	FORMAT	1	Digital Audio Interface Format (I^2S−Only): These are default formats used for the I^2S digital audio interface. **0 | I^2S; Frame delayed by 1 CKI. FRCK is low for the left channel.** 1 | Left−justified; No frame delay. FRCK is high for the left channel.
5:4	DAI	2	Digital Audio Interface: This determines the digital audio interface. For the DAI controls, some register settings are dedicated to I^2S or TDM. If utilizing the MAGC feature, please program the SLOTW/SAMPW settings prior to DAI. **00 | I^2S** 01 | TDM2 10 | TDM4 11 | TDM8
3:0	FS	4	Sampling Frequency: The CERR flag is set if the FS register is not set to the expected frequency. 0x00 | Reserved 0x01 | Reserved 0x02 | 16 kHz 0x03 | 22.05 kHz 0x04 | 32 kHz 0x05 | 44.1 kHz **0x06 | 48 kHz** 0x07 | Reserved 0x08 | 96 kHz All Else| Reserved

Table 10. 0x07: DAI_CTRL2
Address: 0x07
Type: R/W
Reset Value: 0101_0101 (0x55)

Bit #	Name	Size (Bits)	Function
7:6	SAMPW	2	Sample Width: Sets the number of CKIs for the sampled data. This value should never be larger than the slot width, SLOTW. If SAMPW>SLOTW then the SAMPW setting is ignored and SAMPW = SLOTW. 00 | 16 **01 | 24** 10 | 32 11 | Reserved
5:4	SLOTW	2	Slot Width: Sets the number of CKIs within a frame. 00 | 16 **01 | 24** 10 | 32 11 | Reserved
3:2	FRM_DLY	2	Frame Delay *(TDM−Only):* Sets the number of CKI serial bits delay after FRCK before the frame begins. 00 | 0 **01 | 1** 10 | 2 11 | 3
1	FRM_POL	1	FRCK Polarity Control: **0 | Normal Operation (For I2S, Low = Left Slot)** 1 | FRCK is inverted (Low = Right Slot)
0	FRCK_MODE	1	FRCK Mode *(TDM−Only):* If DAI = 00 then this is ignored. 0 | 50% duty cycle **1 | Pulse (1 CKI) mode**

Table 11. 0x08: DAI_CTRL3
Address: 0x08
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:4	Reserved	4	
3	PDM_MODE	1	PDM Interface Enable: This mode can only be switched in standby or shutdown. **0 | ONA10IV expects PCM interface** 1 | ONA10IV expects PDM Interface
2:0	A_SLOT	3	Selects the slot that audio data is extracted from: For I^2S and left−justified (DAI = 00), only slots 0 (left) and 1 (right) are used. **000 | Slot 1 from DAI to output (For I^2S, LJ, or TDM)** 001 | Slot 2 from DAI to output (For I^2S, LJ, or TDM) 010 | Slot 3 from DAI to output (TDM only; DAI = 10 or 11) 011 | Slot 4 from DAI to output (TDM only; DAI = 10 or 11) 100 | Slot 5 from DAI to output (TDM only; DAI = 11) 101 | Slot 6 from DAI to output (TDM only; DAI = 11) 110 | Slot 7 from DAI to output (TDM only; DAI = 11) 111 | Slot 8 from DAI to output (TDM only; DAI = 11)

Table 12. 0x09: MAX_VOL
Address: 0x09
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:0	MAX_VOL	8	Maximum Allowable Volume: When this register is programmed while active, the maximum volume will step through each setting at the programmed volume ramp (VOL_RAMP) until it reaches the target setting. **0x00 | 0.0 dB** 0x01 | −0.375 dB 0x02 | −0.750 dB 0x03 | Decreasing in ~0.375 dB steps… 0xFD | −94.875 dB 0xFE | −95.25 dB 0xFF | AMP MUTE

Table 13. 0x0A: VOL_CTRL
Address: 0x0A
Type: R/W
Reset Value: 0000_1110 (0x0E)

Bit #	Name	Size (Bits)	Function
7:5	Reserved	3	
4:3	VOL_RAMP	2	Rate to ramp volume up and down: Each step is 0.375 dB 00 | 0.01 ms/step **01 | 0.10 ms/step** 10 | 0.50 ms/step 11 | 1.00 ms/step
2	AVOL_UP	1	Automatic Volume Ramp Up: 0 | Disabled **1 | Ramp volume up from MUTE or previous MAX_VOL setting**
1	AVOL_DN	1	Automatic Volume Ramp Down: 0 | Disabled **1 | Ramp volume down in MUTE or previous MAX_VOL setting**
0	MUTE	1	Mute: **0| Normal operation** 1| Mute amplifier output Note: Asserting the MUTE bit bypasses the volume ramp controls and mutes the output signal immediately; this may cause an audible artifact (pop). To avoid this, mute output signals by writing 0xFF to the MAX_VOL register (register 0x09) and un−mute signals by writing the previous or desired volume level setting to the MAX_VOL register.

Table 14. 0x0B: GAIN_CTRL1
Address: 0x0B
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:5	Reserved	3	
4:0	PCM_AMP_GAIN	5	Selects the gain of the class D amplifier for PCM mode: **0x00 | +16.0 dB** 0x08 | +12.0 dB 0x0E | +9.0 dB 0x14 | +6.0 dB 0x1A | +3.0 dB

Table 15. 0x0C: GAIN_CTRL2
Address: 0x0C
Type: R/W
Reset Value: 0000_0000 (0x40)

Bit #	Name	Size (Bits)	Function
7	Reserved	1	
6:5	PDM_DAC_MAP	2	Selects the voltage mapping of the DAC in PDM mode: 00 | 7.23 dBV 01 | 4.31 dBV **10 | −0.13 dBV** 11 | −9.68 dBV
4:0	PDM_AMP_GAIN	5	Selects the gain of the class D amplifier for PDM mode: **0x00 | +16.0 dB** 0x08 | +12.0 dB 0x0E | +9.0 dB 0x14 | +6.0 dB 0x1A | +3.0 dB

Table 16. 0x0D: EMI_CTRL
Address: 0x0D
Type: R/W
Reset Value: 0001_1100 (0x1C)

Bit #	Name	Size (Bits)	Function
7:5	Reserved	3	
4:3	AMP_ERC	2	Output Edge Rate Control (ERC): Sets the rise and fall rates of the class−D outputs. 00 | 1.00 V/ns 01 | 0.75 V/ns 10 | 0.50 V/ns **11 | ~3.50 V/ns**
2:0	SS_MOD	3	Spread Spectrum Modulation Percentage (± %): Sets the spread spectrum modulation of the class−D amplifier. A setting of 000 results in a ±5.3% modulation of the speaker amplifier's output frequency. A setting of 100 disables spread−spectrum modulation. 000 | 5.3 001 | 7.0 010 | 10.6 011 | 21.2 **100 | 0.0** 101 | 3.0 110 | 3.6 111 | 4.2

Table 17. 0x0E: AGC_BATT
Address: 0x0E
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:5	Reserved	3	
4:0	BATT_ATH	5	Selects the trip point at which the automatic gain control initiates the AGC_HOLD timer. If the BAT_CFG = H then 3S battery values are used, if BAT_CFG = L then 2S battery values are used. See datasheet Figure 23. **0x00 | 9.763 V for 3S (6.511 V for 2S)** 0x01 | 9.835 V for 3S (6.559 V for 2S) 0x02 | 9.907 V for 3S (6.607 V for 2S) 0x03 | Increasing by 72 mV for 3S and 48mV for 2S 0x1D | 11.851 V for 3S (7.903 V for 2S) 0x1E | 11.923 V for 3S (7.951 V for 2S) 0x1F | 11.995 V for 3S (7.999 V for 2S)

Table 18. 0x0F: AGC_CTRL1
Address: 0x0F
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:4	AGC_HOLD	4	AGC wait time before starting AGC_RELEASE: See datasheet Figure 23. **0x00 | 10 ms** 0x01 | 45 ms 0x02 | 80 ms Increasing in 35 ms steps such that … 0x0D | 465 ms 0x0E | 500 ms 0x0F | Infinite Hold until AGC_TIMEOUT
3:0	AGC_ATTACK	4	AGC gain decrease ramp rate: See datasheet Figure 23. **0x00 | 10 μs/dB** 0x01 | 45 μs/dB 0x02 | 80 μs/dB Increasing in 35/dB μs steps such that … 0x0D | 465 μs/dB 0x0E | 500 μs/dB 0x0F | 535 μs/dB

Table 19. 0x10: AGC_CTRL2
Address: 0x10
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7	Reserved	1	
6:4	AGC_MAX_ATT	3	Maximum AGC attenuation level setting: See datasheet figure 23. **000 | −9 dB** 001 | −8 dB 010 | −7 dB 011 | −6 dB 100 | −5 dB 101 | −4 dB 110 | −3 dB 111 | −2 dB
3:0	AGC_RELEASE	4	AGC gain increase ramp rate: Steps are in 70 ms/dB. See datasheet Figure 23. **0x00 | 5 ms/dB** 0x01 | 75 ms/dB 0x02 | 145 ms/dB Decreasing in 70 ms/dB steps such that … 0x0D | 915 ms/dB 0x0E | 985 ms/dB 0x0F | 1055 ms/dB

Table 20. 0x11: AGC_CTRL3
Address: 0x11
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:2	Reserved	6	
1:0	AGC_TIMEOUT	2	Time after reaching MAX_AGC_ATT before going into STANDBY: To exit STANDBY from an AGC_TIMEOUT, the chip must be reset or AGC_TIMEOUT disabled **00 | Disabled (will not enter STANDBY)** 01 | 565 ms 10 | 775 ms 11 | 985 ms

Table 21. 0x12: MAGC_CTRL1
Address: 0x12
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7	RX_SLOT8	1	Sets the ONA10IV to listen and react to slot 8 on the MAGC bus: **0 | Ignores slot 8.** 1 | Listens to and reacts to slot 8
6	RX_SLOT7	1	Sets the ONA10IV to listen and react to slot 7 on the MAGC bus: **0 | Ignores slot 7.** 1 | Listens to and reacts to slot 7
5	RX_SLOT6	1	Sets the ONA10IV to listen and react to slot 6 on the MAGC bus: **0 | Ignores slot 6.** 1 | Listens to and reacts to slot 6
4	RX_SLOT5	1	Sets the ONA10IV to listen and react to slot 5 on the MAGC bus: **0 | Ignores slot 5.** 1 | Listens to and reacts to slot 5
3	RX_SLOT4	1	Sets the ONA10IV to listen and react to slot 4 on the MAGC bus: **0 | Ignores slot 4.** 1 | Listens to and reacts to slot 4
2	RX_SLOT3	1	Sets the ONA10IV to listen and react to slot 3 on the MAGC bus: **0 | Ignores slot 3.** 1 | Listens to and reacts to slot 3
1	RX_SLOT2	1	Sets the ONA10IV to listen and react to slot 2 on the MAGC bus: **0 | Ignores slot 2.** 1 | Listens to and reacts to slot 2
0	RX_SLOT1	1	Sets the ONA10IV to listen and react to slot 1 on the MAGC bus: **0 | Ignores slot 1.** 1 | Listens to and reacts to slot 1

Table 22. 0x13: MAGC_CTRL2
Address: 0x13
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7	TX_SLOT8	1	Gain information transmission on slot 8 of the MAGC bus: **0 | MAGC is HiZ during slot 8** 1 | Device transmits slot 8
6	TX_SLOT7	1	Gain information transmission on slot 7 of the MAGC bus: **0 | MAGC is HiZ during slot 7** 1 | Device transmits slot 7
5	TX_SLOT6	1	Gain information transmission on slot 6 of the MAGC bus: **0 | MAGC is HiZ during slot 6** 1 | Device transmits slot 6
4	TX_SLOT5	1	Gain information transmission on slot 5 of the MAGC bus: **0 | MAGC is HiZ during slot 5** 1 | Device transmits slot 5
3	TX_SLOT4	1	Gain information transmission on slot 4 of the MAGC bus: **0 | MAGC is HiZ during slot 4** 1 | Device transmits slot 4
2	TX_SLOT3	1	Gain information transmission on slot 3 of the MAGC bus: **0 | MAGC is HiZ during slot 3** 1 | Device transmits slot 3
1	TX_SLOT2	1	Gain information transmission on slot 2 of the MAGC bus: **0 | MAGC is HiZ during slot 2** 1 | Device transmits slot 2
0	TX_SLOT1	1	Gain information transmission on slot 1 of the MAGC bus: **0 | MAGC is HiZ during slot 1** 1 | Device transmits slot 1

Table 23. 0x14: MAGC_CTRL3
Address: 0x14
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:3	Reserved	5	Reserved
2:1	MAGC_ODRV	2	Selects the drive capability of the MAGC output driver: **00 | 100% Drive** 01 | 75% Drive 10 | 50% Drive 11 | 25% Drive
0	MAGC_EN	1	Enables transmission on the MAGC output: **0 | Disabled** 1 | Transmission enabled

Table 24. 0x15: SENSE_CTRL
Address: 0x15
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:6	T_HOLD	2	Length of time the chip waits below the T_{LIM}(recovery) before it begins to increase the volume: If automatic recovery (ARCV_T) is not enabled, then the chip will wait in T_HOLD until MRCV is written to. **00 | 10 ms** 01 | 45 ms 10 | 80 ms 11 | 115 ms
5:4	T_ATTACK	2	The rate at which the TERR will decrease the volume: The initial step down in volume will occur immediately (<10 μs). Maximum attenuation is −12 dB. Release timing is determined by AGC_RELEASE. **00 | ~2 ms/step** 01 | ~4 ms/step 10 | ~6 ms/step 11 | ~8 ms/step
3:2	T_ATH	2	The attack threshold for an over−temperature error (TERR): The recover threshold is always ~10 °C lower **00 | ~140 °C (~130 °C Recovery)** 01 | ~130 °C (~120 °C Recovery) 10 | ~120 °C (~110 °C Recovery) 11 | ~110 °C (~100 °C Recovery)
1:0	T_SAMP	2	The rate at which the die temperature is sampled: When a temperature error is detected the temperature sense is forced to be constantly on. **00 | Every 40 ms** 01 | Every 20 ms 10 | Every 10 ms 11 | Constantly on

Table 25. 0x16: T_SENSE_OUT1
Address: 0x16
Type: R
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:0	T_SENSE_OUT	8	Displays the signed output word of the die temperature sense ADC: **Temperature Sense Encoding** **LSB** **Units** T_SENSE_OUT1 Bit: 7 6 5 4 3 2 1 0 Value: 2^5 2^4 2^3 2^2 2^1 2^0 2^{-1} 2^{-2} °C

Table 26. 0x17: T_SENSE_OUT2
Address: 0x17
Type: R
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:3	Reserved	5	
2:0	T_SENSE_OUT	3	Displays the signed output word of the die temperature sense ADC: **MSB** **Units** T_SENSE_OUT2 Bit: 10 9 8 Value: $-(2^{8})$ 2^7 2^6 °C

Table 27. 0x18: DATAO_CTRL1
Address: 0x18
Type: R/W
Reset Value: 0000_0000 (0x00)

Bit #	Name	Size (Bits)	Function
7:5	Reserved	3	Reserved
4	HPF_BP	1	Bypass the high pass filters in the current and voltage sense such that DC signals can pass (i.e. – for DC gain error trim, if required): **0 | Normal operation** 1 | High pass filter bypassed
3:2	PDM_OUT	2	Sets which CKI edge the current and voltage PDM sense data is sent on. **00 | PDM ISNS data = falling edge, VSNS data = rising edge** 01 | PDM ISNS data = rising edge, VSNS data = falling edge 10 | Reserved 11 | Reserved
1:0	DATA_ODRV	2	Selects the drive strength of the DATAO output driver. **00 | 100% Drive** 01 | 75% Drive 10 | 50% Drive 11 | 25% Drive

Table 28. 0x19: DATAO_CTRL2
Address: 0x19
Type: R/W
Reset Value: 0000_1000 (0x08)

Bit #	Name	Size (Bits)	Function
7	I_DATAO_TX	1	Enables current sense data to be sent out onto DATAO: **0 | Speaker Current sense data transmission disabled** 1 | Speaker Current sense data transmission enabled
6	V_DATAO_TX	1	Enables voltage sense data to be sent out onto DATAO: **0 | Speaker Voltage sense data transmission disabled** 1 | Speaker Voltage sense data transmission enabled
5:3	I_SLOT	3	Selects the slot that will transmit speaker current sense data: 000 | Slot 1 (DAI = 01,10, or 11) **001 | Slot 2 (DAI = 01,10, or 11)** 010 | Slot 3 (DAI = 10 or 11) 011 | Slot 4 (DAI = 10 or 11) 100 | Slot 5 (DAI = 11) 101 | Slot 6 (DAI = 11) 110 | Slot 7 (DAI = 11) 111 | Slot 8 (DAI = 11)
2:0	V_SLOT	3	Selects the slot that will transmit speaker voltage data: **000 | Slot 1 (DAI = 01,10, or 11)** 001 | Slot 2 (DAI = 01,10, or 11) 010 | Slot 3 (DAI = 10 or 11) 011 | Slot 4 (DAI = 10 or 11) 100 | Slot 5 (DAI = 11) 101 | Slot 6 (DAI = 11) 110 | Slot 7 (DAI = 11) 111 | Slot 8 (DAI = 11)

4. In case sense data is programmed to the same slot, the slot priority is current (dominant), voltage, and then temperature.

Table 29. 0x1A: DATAO_CTRL3
Address: 0x1A
Type: R/W
Reset Value: 0000_0010 (0x02)

Bit #	Name	Size (Bits)	Function
7:4	Reserved	4	Reserved
3	T_DATAO_TX	1	Enables die temperature data to be sent out onto DATAO: **0 | Die temperature sense data transmission disabled** 1 | Die temperature sense data transmission enabled
2:0	T_SLOT	3	Selects the slot that die−temperature data will be transmitted on: 000 | Slot 1 (DAI = 01,10, or 11) 001 | Slot 2 (DAI = 01,10, or 11) **010 | Slot 3 (DAI = 10 or 11)** 011 | Slot 4 (DAI = 10 or 11) 100 | Slot 5 (DAI = 11) 101 | Slot 6 (DAI = 11) 110 | Slot 7 (DAI = 11) 111 | Slot 8 (DAI = 11)

5. In case sense data is programmed to the same slot, the slot priority is current (dominant), voltage, and then temperature.

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