AND9897/D

AR0825AT Register Reference

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APPLICATION NOTE

Introduction

This reference document describes the AR0825AT registers. Summary and detailed information are presented in separate sections:

- "Register Lists and Default Values" on page 3
- "Register Descriptions" on page 50

NOTE: Throughout this document, green1 corresponds to greenR; green2 corresponds to greenB.

Conventions and Notations

This document follows the conventions and notations described below.

- Hexadecimal numbers have a 0x prefix
- Binary numbers have 0b prefix
  Example: 0b1010 = 0xA

Register Address Space

The AR0825AT provides a 16-bit register address space accessed through a serial interface. Each register location is 8 or 16 bits in size.

The address space is divided into the five major regions shown in Table 1.

Table 1. ADDRESS SPACE REGIONS

Address Range	Description
0x0000−0x0FFF	Reserved
0x1000−0x1FFF	Reserved
0x2000−0x2FFF	Manufacturer−specific registers (read−only and read−write dynamic registers)
0x3000−0x3FFF	Manufacturer-specific registers (read−only and read−write dynamic registers)
0x4000−0x50FF	Reserved (undefined)
0x5100−0x517F	Manufacturer-specific registers (read−only and read−write dynamic registers)
0x5180−0xFFFF	Reserved (undefined)

Register Notation

The underlying mechanism for reading and writing registers provides byte write capability. However, it is convenient to consider some registers as multiple adjacent bytes. The AR0825AT uses 8−bit and 16−bit registers, all implemented as 1 or more bytes at naturally aligned, contiguous locations in the address space.

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x301C is an 8−bit register at address 0x301C, and R0x3000−1 is a 16−bit register at address 0x3000−0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that chip_version_reg is a 16−bit register.

Register Aliases

A consequence of the internal architecture of the AR0825AT is that some registers are decoded at multiple addresses. The effect of reading or writing a register through any of its aliases is identical.

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the chip_version_reg register are referred to as chip_version_reg[3:0] or R0x0000−1[3:0].

Bit Field Aliases

In addition to the register aliases described above, some register fields are aliased in multiple places. For example, R0x301C (mode_select) only has one operational bit, R0x301C[0]. This bit is aliased to R0x301A−B[2]. The effect of reading or writing a bit field through any of its aliases is identical.

Byte Ordering

Registers that occupy more than 1 byte of address space are shown with the lowest address in the highest−order byte lane to match the byte−ordering on the bus. For example, the model_id register is R0x3000−1. In the register table the default value is shown as 0x1557. This means that a READ from address 0x3000 would return 0x15, and a READ from address 0x3001 would return 0x57. When reading this register as two 8−bit transfers on the serial interface, the 0x15 will appear on the serial interface first, followed by the 0x57.

Address Alignment

All register addresses are aligned naturally. Registers that occupy two bytes of address space are aligned to even 16-bit addresses.

Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 2.

Table 2. DATA FORMATS

Name	Description
FIX16	Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = −128, 0xFFFF = −0.0039065
UFIX16	Unsigned fixed−point, 16−bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5
FLP32	Signed floating−point, 32−bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0

Register Behavior

Registers vary from "read−only," "read/write," and "read, write−1−to−clear."

DOUBLE−BUFFERED REGISTERS

Some sensor settings cannot be changed during frame readout. For example, changing x_addr_start partway through frame readout would result in inconsistent row lengths within a frame. To avoid this, the AR0825AT double−buffers many registers by implementing a "pending" and a "live" version. READs and WRITEs access the pending register; the live register controls the sensor operation.

The value in the pending register is transferred to a live register at a fixed point in the frame timing, called frame start. Frame start is defined as the point at which the first dark row is read out internally to the sensor. In the register tables the "Buffering" column shows which registers or register fields are single− or double−buffered.

Buffering

In register tables, buffering shows the timing with which a newly−written register value takes effect. The notation used is:

Blank – Unbuffered. By default register update takes effect immediately.

S – Single frame sync'd. Register update in frame N takes effect in frame N+1.

D –Double frame sync'd. Register update in frame N takes effect in frame N+2.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. If the masked bad frame option is enabled, both LV and FV are inhibited for these frames so that the vertical blanking time between frames is extended by the frame time.

In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

Blank – No. Changing the register value will not produce a

bad frame.
Y − Yes. Changing the register value might produce a bad frame.
YM − Yes. But the bad frame will be masked out when mask_corrupted_frames (R0x301A[9]) is set to “1”.

Embedded

In register tables, the embedded column notes whether or not the register is present in the perframe embedded data. The notation used is:
Blank – By default, a register is not present in the embedded data
E – The register is present in the embedded data.

Locked

In register tables, locked notes whether writes to the register are protected by R0x3010. The notation used is
Blank – By default, writes to a register are not protected by R0x3010
L – Writes to the register are protected by R0x3010.

REGISTER LISTS AND DEFAULT VALUES

Table 3. MANUFACTURER−SPECIFIC 2 REGISTER LIST
1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x2000	FRAME_COUNT2_	???? ???? ???? ????	65535 (0xFFFF)
R0x2002	FRAME_COUNT_	???? ???? ???? ????	65535 (0xFFFF)
R0x2004	OTPM_STATUS	???? ???? ???? ????	0 (0x0000)
R0x2006	GPI_STATUS	0000 0??? 0??? ????	0 (0x0000)
R0x2008	FRAME_STATUS	0000 0000 0000 ????	0 (0x0000)
R0x200A	DATAPATH_STATUS	0000 0000 00?? 00??	0 (0x0000)
R0x2020	EXPOSURE_T1_ROW	???? ???? ???? ????	0 (0x0000)
R0x2022	EXPOSURE_T2_ROW	???? ???? ???? ????	0 (0x0000)
R0x2024	EXPOSURE_T3_ROW	???? ???? ???? ????	0 (0x0000)
R0x2026	EXPOSURE_T4_ROW	???? ???? ???? ????	0 (0x0000)
R0x2028	EXPOSURE_T1_CLK_U	0000 0??? ???? ????	0 (0x0000)
R0x202A	EXPOSURE_T1_CLK_L	???? ???? ???? ????	0 (0x0000)
R0x202C	EXPOSURE_T2_CLK_U	0000 0??? ???? ????	0 (0x0000)
R0x202E	EXPOSURE_T2_CLK_L	???? ???? ???? ????	0 (0x0000)
R0x2030	EXPOSURE_T3_CLK_U	0000 0??? ???? ????	0 (0x0000)
R0x2032	EXPOSURE_T3_CLK_L	???? ???? ???? ????	0 (0x0000)
R0x2034	EXPOSURE_T4_CLK_U	0000 0??? ???? ????	0 (0x0000)
R0x2036	EXPOSURE_T4_CLK_L	???? ???? ???? ????	0 (0x0000)

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1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x2040	RATIO_ACTUAL_T1_T2	0000 ???? ???? ????	32 (0x0020)
R0x2042	RATIO_ACTUAL_T2_T3	0000 ???? ???? ????	32 (0x0020)
R0x2044	RATIO_ACTUAL_T3_T4	0000 ???? ???? ????	32 (0x0020)
R0x2046	RATIO_ACTUAL_T2_T1	???? ???? ???? ????	1024 (0x0400)
R0x2048	RATIO_ACTUAL_T1_T3_MSB	0000 0000 0000 000?	0 (0x0000)
R0x204A	RATIO_ACTUAL_T1_T3	???? ???? ???? ????	32 (0x0020)
R0x204C	RATIO_ACTUAL_T1_T4_MSB	0000 0000 0000 000?	0 (0x0000)
R0x204E	RATIO_ACTUAL_T1_T4	???? ???? ???? ????	32 (0x0020)
R0x2050	RATIO_ACTUAL_GAIN1	0000 ???? ???? ????	32 (0x0020)
R0x2054	RATIO_ACTUAL_GAIN2_MSB	0000 0000 0000 000?	0 (0x0000)
R0x2056	RATIO_ACTUAL_GAIN2	???? ???? ???? ????	32 (0x0020)
R0x2058	RATIO_ACTUAL_GAIN3_MSB	0000 0000 0000 000?	0 (0x0000)
R0x205A	RATIO_ACTUAL_GAIN3	???? ???? ???? ????	32 (0x0020)
R0x205C	DATA_FORMAT_ACTUAL	000? ???? 000? ????	5132 (0x140C)
R0x2060	ASIL_STATUS_00	dddd dddd dd00 000d	0 (0x0000)
R0x2062	ASIL_STATUS_01	dddd dddd dddd dddd	0 (0x0000)
R0x2064	ASIL_STATUS_02	0ddd dddd 0ddd 00dd	0 (0x0000)
R0x2066	ASIL_STATUS_03	0000 0000 dd00 000d	0 (0x0000)
R0x2068	ASIL_STARTUP_STATUS_00	0000 0000 000d dddd	0 (0x0000)
R0x206A	ATR_CHECK_CRT_CRC_VALUE	dddd dddd dddd dddd	0 (0x0000)
R0x206C	RRC_CHECK_ADDR_CRC_VALUE	dddd dddd dddd dddd	0 (0x0000)
R0x206E	DELAY_BUFFER_CRC_FAULTS_PER_FRAME	dddd dddd dddd dddd	0 (0x0000)
R0x2070	DELAY_BUFFER_CRC_FAULT_FRAMES	dddd dddd dddd dddd	0 (0x0000)
R0x2072	FUSE_PIXEL_DEFECT_COUNT	0000 0000 ???? ????	0 (0x0000)
R0x2076	ASIL_STATUS_04	00dd dddd dddd dddd	0 (0x0000)

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Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x207C	ASIL_STATUS_07	0000 0000 0000 000d	0 (0x0000)
R0x207E	ASIL_STATUS_08	0000 0000 dddd dddd	0 (0x0000)
R0x2080	ASIL_EXT_CLK_COUNT_MSB	0000 0000 00dd dddd	0 (0x0000)
R0x2082	ASIL_EXT_CLK_COUNT_LSB	dddd dddd dddd dddd	0 (0x0000)
R0x2084	ASIL_CLK_PIX_COUNT_MSB	0000 0000 00dd dddd	0 (0x0000)
R0x2086	ASIL_CLK_PIX_COUNT_LSB	dddd dddd dddd dddd	0 (0x0000)
R0x2088	ASIL_CLK_OP_COUNT_MSB	0000 0000 00dd dddd	0 (0x0000)
R0x208A	ASIL_CLK_OP_COUNT_LSB	dddd dddd dddd dddd	0 (0x0000)
R0x208C	ASIL_CLK_REG_COUNT_MSB	0000 0000 00dd dddd	0 (0x0000)
R0x208E	ASIL_CLK_REG_COUNT_LSB	dddd dddd dddd dddd	0 (0x0000)
R0x2090	ASIL_CLK_PIX_COUNT_100_EXT	0000 0ddd dddd dddd	0 (0x0000)
R0x2092	ASIL_CLK_OP_COUNT_100_EXT	0000 0ddd dddd dddd	0 (0x0000)
R0x2094	ASIL_CLK_REG_COUNT_100_EXT	0000 0ddd dddd dddd	0 (0x0000)
R0x209C	I2C_WRT_COUNT	???? ???? ???? ????	0 (0x0000)
R0x20B2	TEMPSENS1_DATA_REG	000? ???? ???? ????	0 (0x0000)
R0x20B4	TEMPVSENS0_BOOST_MEAS_0	???? ???? ???? ????	0 (0x0000)
R0x20B6	TEMPVSENS0_BOOST_MEAS_1	???? ???? ???? ????	0 (0x0000)
R0x20B8	TEMPVSENS0_BOOST_MEAS_2	???? ???? ???? ????	0 (0x0000)
R0x20BA	TEMPVSENS0_BOOST_MEAS_3	???? ???? ???? ????	0 (0x0000)
R0x20BC	TEMPVSENS0_BOOST_MEAS_4	???? ???? ???? ????	0 (0x0000)
R0x20BE	TEMPVSENS0_BOOST_MEAS_5	???? ???? ???? ????	0 (0x0000)
R0x20C0	TEMPVSENS0_BOOST_MEAS_6	???? ???? ???? ????	0 (0x0000)
R0x20C2	TEMPVSENS0_BOOST_MEAS_7	???? ???? ???? ????	0 (0x0000)
R0x20C4	TEMPVSENS0_BOOST_MEAS_8	???? ???? ???? ????	0 (0x0000)
R0x20C6	TEMPVSENS0_BOOST_MEAS_9	???? ???? ???? ????	0 (0x0000)

Table 3. MANUFACTURER−SPECIFIC 2 REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x20C8	TEMPVSENS0_BOOST_MEAS_10	???? ???? ???? ????	0 (0x0000)
R0x20CA	TEMPVSENS0_BOOST_MEAS_11	???? ???? ???? ????	0 (0x0000)
R0x20CC	TEMPVSENS0_BOOST_MEAS_12	???? ???? ???? ????	0 (0x0000)
R0x20CE	TEMPVSENS0_BOOST_MEAS_13	???? ???? ???? ????	0 (0x0000)
R0x20D0	TEMPVSENS0_BOOST_MEAS_14	???? ???? ???? ????	0 (0x0000)
R0x20D2	TEMPVSENS0_BOOST_MEAS_15	???? ???? ???? ????	0 (0x0000)
R0x20D4	TEMPVSENS0_BOOST_MEAS_16	???? ???? ???? ????	0 (0x0000)
R0x20D6	TEMPVSENS0_BOOST_MEAS_17	???? ???? ???? ????	0 (0x0000)
R0x20EC	TEMPVSENS1_VMON_MEAS_0	???? ???? ???? ????	0 (0x0000)
R0x20FE	TEMPSENS1_DATA_K_REG	000? ???? ???? ????	0 (0x0000)
R0x2150	AE_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x2152	AE_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x2154	AE_HIST_BEGIN_H	???? ???? ???? ????	0 (0x0000)
R0x2156	AE_HIST_BEGIN_L	???? ???? ???? ????	0 (0x0000)
R0x2158	AE_HIST_END_H	???? ???? ???? ????	0 (0x0000)
R0x215A	AE_HIST_END_L	???? ???? ???? ????	0 (0x0000)
R0x215C	AE_LOW_END_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x215E	AE_LOW_END_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x2160	AE_PERC_LOW_END	???? ???? ???? ????	0 (0x0000)
R0x2162	AE_NORM_ABS_DEV	???? ???? ???? ????	0 (0x0000)
R0x2250	AE_MEAN2_H	???? ???? ???? ????	0 (0x0000)
R0x2252	AE_MEAN2_L	???? ???? ???? ????	0 (0x0000)
R0x2254	AE_HIST2_BEGIN_H	???? ???? ???? ????	0 (0x0000)
R0x2256	AE_HIST2_BEGIN_L	???? ???? ???? ????	0 (0x0000)
R0x2258	AE_HIST2_END_H	???? ???? ???? ????	0 (0x0000)

Table 3. MANUFACTURER−SPECIFIC 2 REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x225A	AE_HIST2_END_L	???? ???? ???? ????	0 (0x0000)
R0x225C	AE_LOW2_END_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x225E	AE_LOW2_END_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x2260	AE_PERC2_LOW_END	???? ???? ???? ????	0 (0x0000)
R0x2262	AE_NORM2_ABS_DEV	???? ???? ???? ????	0 (0x0000)
R0x226E	AE_STATS_STATUS	???? ???? ???? ????	0 (0x0000)
R0x2280	AE_X0_Y0_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x2282	AE_X0_Y0_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x2284	AE_X0_Y1_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x2286	AE_X0_Y1_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x2288	AE_X0_Y2_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x228A	AE_X0_Y2_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x228C	AE_X0_Y3_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x228E	AE_X0_Y3_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22A0	AE_X1_Y0_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22A2	AE_X1_Y0_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22A4	AE_X1_Y1_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22A6	AE_X1_Y1_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22A8	AE_X1_Y2_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22AA	AE_X1_Y2_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22AC	AE_X1_Y3_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22AE	AE_X1_Y3_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22B0	AE_X2_Y0_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22B2	AE_X2_Y0_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22B4	AE_X2_Y1_MEAN_H	???? ???? ???? ????	0 (0x0000)

Table 3. MANUFACTURER−SPECIFIC 2 REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x22B6	AE_X2_Y1_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22B8	AE_X2_Y2_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22BA	AE_X2_Y2_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22BC	AE_X2_Y3_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22BE	AE_X2_Y3_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22C0	AE_X3_Y0_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22C2	AE_X3_Y0_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22C4	AE_X3_Y1_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22C6	AE_X3_Y1_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22C8	AE_X3_Y2_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22CA	AE_X3_Y2_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22CC	AE_X3_Y3_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x22CE	AE_X3_Y3_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x22F6	AE_MEAN3_H	???? ???? ???? ????	0 (0x0000)
R0x22F8	AE_MEAN3_L	???? ???? ???? ????	0 (0x0000)
R0x22FA	AE_HIST3_BEGIN_H	???? ???? ???? ????	0 (0x0000)
R0x22FC	AE_HIST3_BEGIN_L	???? ???? ???? ????	0 (0x0000)
R0x22FE	AE_HIST3_END_H	???? ???? ???? ????	0 (0x0000)
R0x2500	CTX_RD_DATA_REG	???? ???? ???? ????	0 (0x0000)
R0x2510	SEQ_DATA_PORT	dddd dddd dddd dddd	0 (0x0000)
R0x2512	SEQ_CTRL_PORT	?dd0 00dd dddd dddd	32768 (0x8000)
R0x2F0A	AE_HIST3_END_L	???? ???? ???? ????	0 (0x0000)
R0x2F0C	AE_LOW3_END_MEAN_H	???? ???? ???? ????	0 (0x0000)
R0x2F0E	AE_LOW3_END_MEAN_L	???? ???? ???? ????	0 (0x0000)
R0x2F36	TEMPSENS_CLK_DIV	0000 0000 dddd dddd	19 (0x0013)

Table 3. MANUFACTURER−SPECIFIC 2 REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x2F48	AE_PERC3_LOW_END	???? ???? ???? ????	0 (0x0000)
R0x2F4E	AE_NORM3_ABS_DEV	???? ???? ???? ????	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3000	CHIP_VERSION_REG	???? ???? ???? ????	5463 (0x1557)
R0x3002	Y_ADDR_START_	0000 dddd dddd dddd	0 (0x0000)
R0x3004	X_ADDR_START_	000d dddd dddd dddd	0 (0x0000)
R0x3006	Y_ADDR_END_	0000 dddd dddd dddd	2167 (0x0877)
R0x3008	X_ADDR_END_	000d dddd dddd dddd	3847 (0x0F07)
R0x300A	FRAME_LENGTH_LINES_	dddd dddd dddd dddd	2416 (0x0970)
R0x300C	LINE_LENGTH_PCK_	dddd dddd dddd ddd0	1076 (0x0434)
R0x300E	REVISION_NUMBER	???? ???? ???? ????	12582 (0x3126)
R0x3010	LOCK_CONTROL	dddd dddd dddd dddd	48879 (0xBEEF)
R0x3012	COARSE_INTEGRATION_TIME_	dddd dddd dddd dddd	16 (0x0010)
R0x3014	FINE_INTEGRATION_TIME_	dddd dddd dddd dddd	0 (0x0000)
R0x3016	COARSE_INTEGRATION_TIME_CB	dddd dddd dddd dddd	18 (0x0012)
R0x301A	RESET_REGISTER	dddd dddd dd0d dddd	88 (0x0058)
R0x301C	MODE_SELECT_	0000 000d	0 (0x00)
R0x301D	IMAGE_ORIENTATION_	0000 00dd	0 (0x00)
R0x301E	DATA_PEDESTAL_	0ddd dddd dddd dddd	168 (0x00A8)
R0x3021	SOFTWARE_RESET_	0000 000d	0 (0x00)
R0x3022	GROUPED_PARAMETER_HOLD_	0000 000d	0 (0x00)
R0x3023	MASK_CORRUPTED_FRAMES_	0000 000d	0 (0x00)
R0x302A	VT_PIX_CLK_DIV	dddd dddd dddd dddd	6 (0x0006)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x302C	VT_SYS_CLK_DIV	dddd dddd dddd dddd	1793 (0x0701)
R0x302E	PRE_PLL_CLK_DIV	dddd dddd dddd dddd	9 (0x0009)
R0x3030	PLL_MULTIPLIER	dddd dddd dddd dddd	224 (0x00E0)
R0x3032	SCALING_MODE	0000 0000 00dd 00dd	0 (0x0000)
R0x3034	CTX_CONTROL_REG	dddd dddd dddd dddd	2048 (0x0800)
R0x3036	OP_WORD_CLK_DIV	dddd dddd dddd dddd	12 (0x000C)
R0x3038	OP_SYS_CLK_DIV	dddd dddd dddd dddd	1 (0x0001)
R0x303A	PLL_MULTIPLIER_ANA	0000 dddd dddd dddd	134 (0x0086)
R0x303C	PRE_PLL_CLK_DIV_ANA	00dd 00dd 00dd dddd	3 (0x0003)
R0x303E	LINE_LENGTH_PCK_CB	dddd dddd dddd ddd0	1076 (0x0434)
R0x3040	READ_MODE	dddd dd00 00dd dddd	0 (0x0000)
R0x3044	DARK_CONTROL	dddd dddd dd00 00dd	1024 (0x0400)
R0x3046	FLASH	0000 000d d0dd dddd	0 (0x0000)
R0x3048	FLASH2	dddd dddd dddd dddd	256 (0x0100)
R0x3056	GREEN1_GAIN	0000 0ddd dddd dddd	128 (0x0080)
R0x3058	BLUE_GAIN	0000 0ddd dddd dddd	128 (0x0080)
R0x305A	RED_GAIN	0000 0ddd dddd dddd	128 (0x0080)
R0x305C	GREEN2_GAIN	0000 0ddd dddd dddd	128 (0x0080)
R0x305E	GLOBAL_GAIN	0000 0ddd dddd dddd	128 (0x0080)
R0x3064	SMIA_TEST	ddd0 00dd dddd 0000	256 (0x0100)
R0x3066	CTX_WR_DATA_REG	dddd dddd dddd dddd	0 (0x0000)
R0x306E	DATAPATH_SELECT	dddd dddd dddd 00dd	36880 (0x9010)
R0x3070	TEST_PATTERN_MODE_	dddd dddd dddd dddd	0 (0x0000)
R0x3072	TEST_DATA_RED_	0ddd dddd dddd dddd	0 (0x0000)
R0x3074	TEST_DATA_GREENR_	0ddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3076	TEST_DATA_BLUE_	0ddd dddd dddd dddd	0 (0x0000)
R0x3078	TEST_DATA_GREENB_	0ddd dddd dddd dddd	0 (0x0000)
R0x307A	TEST_RAW_MODE	dddd dddd dddd dddd	0 (0x0000)
R0x3082	OPERATION_MODE_CTRL	dddd dd0d dddd dddd	4 (0x0004)
R0x3084	OPERATION_MODE_CTRL_CB	dddd dd00 dddd dddd	4 (0x0004)
R0x308A	X_ADDR_START_CB	000d dddd dddd dddd	0 (0x0000)
R0x308C	Y_ADDR_START_CB	0000 dddd dddd dddd	0 (0x0000)
R0x308E	X_ADDR_END_CB	000d dddd dddd dddd	3847 (0x0F07)
R0x3090	Y_ADDR_END_CB	0000 dddd dddd dddd	2167 (0x0877)
R0x30AA	FRAME_LENGTH_LINES_CB	dddd dddd dddd dddd	1208 (0x04B8)
R0x30B0	DIGITAL_TEST	0dd0 dddd dddd ddd0	2048 (0x0800)
R0x30B8	TEMPSENS1_CTRL_REG	dddd dddd dddd dddd	0 (0x0000)
R0x30BA	DIGITAL_CTRL	dddd dddd 00dd 00dd	4353 (0x1101)
R0x30BC	GREEN1_GAIN_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x30BE	BLUE_GAIN_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x30C0	RED_GAIN_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x30C2	GREEN2_GAIN_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x30C4	GLOBAL_GAIN_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x30CA	TEMPSENS1_CALIB1	dddd dddd dddd dddd	0 (0x0000)
R0x30CC	TEMPSENS1_CALIB2	dddd dddd dddd dddd	0 (0x0000)
R0x30DC	TRIGGER_DELAY	dddd dddd dddd dddd	32 (0x0020)
R0x3100	DLO_CONTROL0	ddd0 dddd 0000 000d	0 (0x0000)
R0x3102	DLO_CONTROL1	dddd dddd dddd dddd	20544 (0x5040)
R0x3104	DLO_CONTROL2	dddd dddd dddd dddd	20544 (0x5040)
R0x3106	DLO_CONTROL3	dddd dddd dddd dddd	20544 (0x5040)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3108	DLO_CONTROL4	0000 dddd dddd dddd	3000 (0x0BB8)
R0x310A	DLO_CONTROL5	0000 dddd dddd dddd	3000 (0x0BB8)
R0x310C	DLO_CONTROL6	0000 dddd dddd dddd	3000 (0x0BB8)
R0x3110	HDR_CONTROL0	dddd dddd 000d 000d	1 (0x0001)
R0x3140	AE_ROI_X_START_OFFSET	000d dddd dddd ddd0	0 (0x0000)
R0x3142	AE_ROI_Y_START_OFFSET	0000 dddd dddd ddd0	0 (0x0000)
R0x3144	AE_ROI_X_SIZE	000d dddd dddd ddd0	2052 (0x0804)
R0x3146	AE_ROI_Y_SIZE	0000 dddd dddd ddd0	1556 (0x0614)
R0x3148	AE_HIST_BEGIN_PERC	dddd dddd dddd dddd	0 (0x0000)
R0x314A	AE_HIST_END_PERC	dddd dddd dddd dddd	65535 (0xFFFF)
R0x314C	AE_HIST_DIV	dddd dddd dddd dddd	256 (0x0100)
R0x314E	AE_NORM_WIDTH_MIN	dddd dddd dddd dddd	32 (0x0020)
R0x31AC	DATA_FORMAT_BITS	d00d dddd 000d dddd	5132 (0x140C)
R0x31AE	SERIAL_FORMAT	0000 00dd 0000 0ddd	516 (0x0204)
R0x31B0	FRAME_PREAMBLE	0000 0000 dddd dddd	83 (0x0053)
R0x31B2	LINE_PREAMBLE	0000 0000 dddd dddd	59 (0x003B)
R0x31BC	MIPI_TIMING_4	dddd dddd dddd dddd	5894 (0x1706)
R0x31BE	MIPI_CONFIG_STATUS	dddd dddd dddd dddd	35 (0x0023)
R0x31C6	HISPI_CONTROL	0ddd dddd dddd dddd	0 (0x0000)
R0x31C8	MIPI_DESKEW_PAT_WIDTH	dddd dddd dddd dddd	0 (0x0000)
R0x31CE	MIPI_CMOS_TOGGLE_TEST	d000 00dd dddd dddd	0 (0x0000)
R0x31D0	COMPANDING	0000 0000 0000 000d	0 (0x0000)
R0x31D2	STAT_FRAME_ID	dddd dddd dddd dddd	0 (0x0000)
R0x31D6	I2C_WRT_CHECKSUM	dddd dddd dddd dddd	65535 (0xFFFF)
R0x31E0	PIX_DEF_ID	d000 0000 0000 0ddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x31F8	MIPI_CONFIG_2	0000 0000 0000 00dd	0 (0x0000)
R0x31FA	MIPI_F1_F2_ADT	00dd dddd 00dd dddd	12336 (0x3030)
R0x31FC	MIPI_F3_F4_ADT	00dd dddd 00dd dddd	12336 (0x3030)
R0x31FE	CUSTOMER_REV	???? ???? ???? ????	50 (0x0032)
R0x3212	COARSE_INTEGRATION_TIME2	dddd dddd dddd dddd	2 (0x0002)
R0x3214	COARSE_INTEGRATION_TIME2_CB	dddd dddd dddd dddd	2 (0x0002)
R0x3216	COARSE_INTEGRATION_TIME3	dddd dddd dddd dddd	1 (0x0001)
R0x3218	COARSE_INTEGRATION_TIME3_CB	dddd dddd dddd dddd	1 (0x0001)
R0x321A	COARSE_INTEGRATION_TIME4	dddd dddd dddd dddd	0 (0x0000)
R0x321C	COARSE_INTEGRATION_TIME4_CB	dddd dddd dddd dddd	0 (0x0000)
R0x3238	EXPOSURE_RATIO	d000 0ddd 0ddd 0ddd	546 (0x0222)
R0x323A	EXPOSURE_RATIO_CB	d000 0ddd 0ddd 0ddd	546 (0x0222)
R0x323C	ROW_TX_ENABLE	dddd dddd dddd dddd	33825 (0x8421)
R0x323E	ROW_TX_ENABLE_CB	dddd dddd dddd dddd	15 (0x000F)
R0x3240	AE_ROI2_X_START_OFFSET	000d dddd dddd ddd0	0 (0x0000)
R0x3242	AE_ROI2_Y_START_OFFSET	0000 dddd dddd ddd0	0 (0x0000)
R0x3244	AE_ROI2_X_SIZE	000d dddd dddd ddd0	2052 (0x0804)
R0x3246	AE_ROI2_Y_SIZE	0000 dddd dddd ddd0	1556 (0x0614)
R0x3248	AE_HIST2_BEGIN_PERC	dddd dddd dddd dddd	0 (0x0000)
R0x324A	AE_HIST2_END_PERC	dddd dddd dddd dddd	65535 (0xFFFF)
R0x324C	AE_HIST2_DIV	dddd dddd dddd dddd	256 (0x0100)
R0x324E	AE_NORM2_WIDTH_MIN	dddd dddd dddd dddd	32 (0x0020)
R0x3264	AE_ROI3_X_START_OFFSET	000d dddd dddd ddd0	0 (0x0000)
R0x3266	AE_ROI3_Y_START_OFFSET	0000 dddd dddd ddd0	0 (0x0000)
R0x3268	AE_ROI3_X_SIZE	000d dddd dddd ddd0	2052 (0x0804)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x326A	AE_ROI3_Y_SIZE	0000 dddd dddd ddd0	1556 (0x0614)
R0x326C	AE_HIST3_BEGIN_PERC	dddd dddd dddd dddd	0 (0x0000)
R0x3270	AE_X1_START_OFFSET	000d dddd dddd ddd0	0 (0x0000)
R0x3272	AE_X2_START_OFFSET	000d dddd dddd ddd0	0 (0x0000)
R0x3274	AE_X3_START_OFFSET	000d dddd dddd ddd0	0 (0x0000)
R0x3276	AE_Y1_START_OFFSET	0000 dddd dddd ddd0	0 (0x0000)
R0x3278	AE_Y2_START_OFFSET	0000 dddd dddd ddd0	0 (0x0000)
R0x327A	AE_Y3_START_OFFSET	0000 dddd dddd ddd0	0 (0x0000)
R0x327C	AE_STATS_CONTROL	dddd dddd dddd dddd	28784 (0x7070)
R0x327E	AE_STATS_CONTROL2	dddd dddd dddd dddd	28784 (0x7070)
R0x3280	T1_BARRIER_C0	0000 dddd dddd dddd	3000 (0x0BB8)
R0x3282	T1_BARRIER_C1	0000 dddd dddd dddd	3000 (0x0BB8)
R0x3284	T1_BARRIER_C2	0000 dddd dddd dddd	3000 (0x0BB8)
R0x3286	T1_BARRIER_C3	0000 dddd dddd dddd	3000 (0x0BB8)
R0x3288	T2_BARRIER_C0	0000 dddd dddd dddd	3500 (0x0DAC)
R0x328A	T2_BARRIER_C1	0000 dddd dddd dddd	3500 (0x0DAC)
R0x328C	T2_BARRIER_C2	0000 dddd dddd dddd	3500 (0x0DAC)
R0x328E	T2_BARRIER_C3	0000 dddd dddd dddd	3500 (0x0DAC)
R0x3290	T3_BARRIER_C0	0000 dddd dddd dddd	3500 (0x0DAC)
R0x3292	T3_BARRIER_C1	0000 dddd dddd dddd	3500 (0x0DAC)
R0x3294	T3_BARRIER_C2	0000 dddd dddd dddd	3500 (0x0DAC)
R0x3296	T3_BARRIER_C3	0000 dddd dddd dddd	3500 (0x0DAC)
R0x3298	T4_BARRIER_C0	0000 dddd dddd dddd	3500 (0x0DAC)
R0x329A	T4_BARRIER_C1	0000 dddd dddd dddd	3500 (0x0DAC)
R0x329C	T4_BARRIER_C2	0000 dddd dddd dddd	3500 (0x0DAC)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x329E	T4_BARRIER_C3	0000 dddd dddd dddd	3500 (0x0DAC)
R0x32A8	ATR_CHECK_CONTROL	dddd dddd dddd dddd	0 (0x0000)
R0x32AA	ATR_CHECK_ROWTYPES0	dddd dddd dddd dddd	12816 (0x3210)
R0x32AC	ATR_CHECK_ROWTYPES1	dddd dddd dddd dddd	30292 (0x7654)
R0x32AE	ATR_CHECK_ROWTYPES2	dddd dddd dddd dddd	47768 (0xBA98)
R0x32B0	ATR_CHECK_ROWTYPES3	dddd dddd dddd dddd	65244 (0xFEDC)
R0x32BA	ATR_CHECK_ZT_LO_THRESH	00dd dddd dddd dddd	0 (0x0000)
R0x32BC	ATR_CHECK_ZT_HI_THRESH	00dd dddd dddd dddd	0 (0x0000)
R0x32BE	ATR_CHECK_MT_EXPECT1	00dd dddd dddd dddd	0 (0x0000)
R0x32C0	ATR_CHECK_MT_EXPECT2	00dd dddd dddd dddd	0 (0x0000)
R0x32C2	ATR_CHECK_PT_LO_THRESH	00dd dddd dddd dddd	0 (0x0000)
R0x32C4	ATR_CHECK_PT_HI_THRESH	00dd dddd dddd dddd	0 (0x0000)
R0x32C6	RRC_CHECK_LO_THRESH	00dd dddd dddd dddd	0 (0x0000)
R0x32C8	RRC_CHECK_HI_THRESH	00dd dddd dddd dddd	0 (0x0000)
R0x32CA	ATR_CHECK_CRT_CRC_EXPECT	dddd dddd dddd dddd	0 (0x0000)
R0x32CC	RRC_CHECK_ADDR_CRC_EXPECT	dddd dddd dddd dddd	0 (0x0000)
R0x32F0	AE_HIST3_END_PERC	dddd dddd dddd dddd	65535 (0xFFFF)
R0x32F2	AE_HIST3_DIV	dddd dddd dddd dddd	512 (0x0200)
R0x32F4	AE_NORM3_WIDTH_MIN	dddd dddd dddd dddd	32 (0x0020)
R0x32F6	MIDDLE_INTEGRATION_CTRL	000d dddd 000d dddd	0 (0x0000)
R0x32FC	READ_MODE2	d0dd dddd 00dd dddd	2304 (0x0900)
R0x3300	GREEN1_GAIN2_	0000 0ddd dddd dddd	512 (0x0200)
R0x3302	BLUE_GAIN2_	0000 0ddd dddd dddd	512 (0x0200)
R0x3304	RED_GAIN2_	0000 0ddd dddd dddd	512 (0x0200)
R0x3306	GREEN2_GAIN2_	0000 0ddd dddd dddd	512 (0x0200)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3308	GLOBAL_GAIN2_	0000 0ddd dddd dddd	512 (0x0200)
R0x330A	GREEN1_GAIN2_CB	0000 0ddd dddd dddd	512 (0x0200)
R0x330C	BLUE_GAIN2_CB	0000 0ddd dddd dddd	512 (0x0200)
R0x330E	RED_GAIN2_CB	0000 0ddd dddd dddd	512 (0x0200)
R0x3310	GREEN2_GAIN2_CB	0000 0ddd dddd dddd	512 (0x0200)
R0x3312	GLOBAL_GAIN2_CB	0000 0ddd dddd dddd	512 (0x0200)
R0x3316	OTPM_WRT_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x3318	IREG_WRT_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x331A	PDIM_WRT_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x331C	M3ROM_CALC_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x331E	OTPM_CALC_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x3320	IREG_CALC_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x3322	PDIM_CALC_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x3324	CRC_CONTROL_REG	dddd dddd dddd dddd	32768 (0x8000)
R0x3326	CRC_EMB_WRT_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x332A	CRC_EMB_CALC_CHECKSUM	dddd dddd dddd dddd	0 (0x0000)
R0x332C	CRC_FR_WRT_CHECKSUM_LOW	dddd dddd dddd dddd	0 (0x0000)
R0x332E	CRC_FR_CALC_CHECKSUM_LOW	dddd dddd dddd dddd	0 (0x0000)
R0x3342	MIPI_F1_PDT_EDT	00dd dddd 00dd dddd	4652 (0x122C)
R0x3344	MIPI_F1_VDT_VC	0000 00dd 00dd dddd	17 (0x0011)
R0x3346	MIPI_F2_PDT_EDT	00dd dddd 00dd dddd	4652 (0x122C)
R0x3348	MIPI_F2_VDT_VC	0000 00dd 00dd dddd	273 (0x0111)
R0x334A	MIPI_F3_PDT_EDT	00dd dddd 00dd dddd	4652 (0x122C)
R0x334C	MIPI_F3_VDT_VC	0000 00dd 00dd dddd	529 (0x0211)
R0x334E	MIPI_F4_PDT_EDT	00dd dddd 00dd dddd	4652 (0x122C)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3350	MIPI_F4_VDT_VC	0000 00dd 00dd dddd	785 (0x0311)
R0x3352	MIPI_DT_VC_CONFIG	dd00 0000 0000 ddd0	0 (0x0000)
R0x3354	I2C_RD_CHECKSUM	dddd dddd dddd dddd	65535 (0xFFFF)
R0x3356	CRC_DTR_WRT_CHECKSUM_LOW	dddd dddd dddd dddd	0 (0x0000)
R0x3358	CRC_DTR_CALC_CHECKSUM_LOW	dddd dddd dddd dddd	0 (0x0000)
R0x335C	CRC_FR_DTR_CALC_CHECKSUM_HIGH	dddd dddd dddd dddd	0 (0x0000)
R0x335E	CRC_FR_DTR_WRT_CHECKSUM_HIGH	dddd dddd dddd dddd	0 (0x0000)
R0x3362	DC_GAIN	dddd dddd dddd dddd	1 (0x0001)
R0x3364	DCG_TRIM	0000 0ddd dddd dddd	42 (0x002A)
R0x3366	ANALOG_GAIN	dddd dddd dddd dddd	0 (0x0000)
R0x3368	ANALOG_GAIN_CB	0ddd 0ddd 0ddd 0ddd	0 (0x0000)
R0x336A	ANALOG_GAIN2	dddd dddd dddd dddd	0 (0x0000)
R0x336C	ANALOG_GAIN2_CB	dddd dddd dddd dddd	0 (0x0000)
R0x336E	DATAPATH_SELECT2	0d00 0000 dddd dddd	0 (0x0000)
R0x3370	DBLC_CONTROL	dddd dddd dddd dddd	256 (0x0100)
R0x3372	DBLC_FS0_CONTROL	dddd dddd dddd dddd	28687 (0x700F)
R0x3374	DBLC_FS1_CONTROL	dddd dddd dddd dddd	28687 (0x700F)
R0x3376	DBLC_FS2_CONTROL	dddd dddd dddd dddd	28687 (0x700F)
R0x3378	DBLC_FS3_CONTROL	dddd dddd dddd dddd	28687 (0x700F)
R0x337E	DBLC_OFFSET0	dddd dddd dddd dddd	0 (0x0000)
R0x3380	DBLC_OFFSET1	dddd dddd dddd dddd	0 (0x0000)
R0x3382	DBLC_WEIGHT0	0000 0000 dddd dddd	255 (0x00FF)
R0x3384	DBLC_WEIGHT1	0000 0000 dddd dddd	255 (0x00FF)
R0x3386	DBLC_PEDESTAL	00dd dddd dddd dddd	0 (0x0000)
R0x3388	TPG_CONTROL	0000 dddd dddd dd0d	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x338A	TPG_COLOR0_GR1_HI	0000 0000 dddd dddd	0 (0x0000)
R0x338C	TPG_COLOR0_GR1_LO	dddd dddd dddd dddd	256 (0x0100)
R0x338E	TPG_COLOR0_RED_HI	0000 0000 dddd dddd	0 (0x0000)
R0x3390	TPG_COLOR0_RED_LO	dddd dddd dddd dddd	512 (0x0200)
R0x3392	TPG_COLOR0_BLU_HI	0000 0000 dddd dddd	0 (0x0000)
R0x3394	TPG_COLOR0_BLU_LO	dddd dddd dddd dddd	768 (0x0300)
R0x3396	TPG_COLOR0_GR2_HI	0000 0000 dddd dddd	0 (0x0000)
R0x3398	TPG_COLOR0_GR2_LO	dddd dddd dddd dddd	1024 (0x0400)
R0x339A	TPG_COLOR1_GR1_HI	0000 0000 dddd dddd	0 (0x0000)
R0x339C	TPG_COLOR1_GR1_LO	dddd dddd dddd dddd	1280 (0x0500)
R0x339E	TPG_COLOR1_RED_HI	0000 0000 dddd dddd	0 (0x0000)
R0x33A0	TPG_COLOR1_RED_LO	dddd dddd dddd dddd	1536 (0x0600)
R0x33A2	TPG_COLOR1_BLU_HI	0000 0000 dddd dddd	0 (0x0000)
R0x33A4	TPG_COLOR1_BLU_LO	dddd dddd dddd dddd	1792 (0x0700)
R0x33A6	TPG_COLOR1_GR2_HI	0000 0000 dddd dddd	0 (0x0000)
R0x33A8	TPG_COLOR1_GR2_LO	dddd dddd dddd dddd	2048 (0x0800)
R0x33AA	TPG_STDPAT_REGION1	000d dddd dddd dddd	7939 (0x1F03)
R0x33AC	TPG_STDPAT_REGION2	000d dddd dddd dddd	2048 (0x0800)
R0x33AE	TPG_NOISE1_REGION	000d dddd dddd dddd	4099 (0x1003)
R0x33B0	TPG_NOISE2_REGION	000d dddd dddd dddd	0 (0x0000)
R0x33B2	TPG_NOISE2_AMPLITUDE	dddd dddd dddd dddd	0 (0x0000)
R0x33B4	TPG_BLOB_X1	000d dddd dddd dddd	0 (0x0000)
R0x33B6	TPG_BLOB_Y1	0000 dddd dddd dddd	0 (0x0000)
R0x33B8	TPG_BLOB_X2	000d dddd dddd dddd	0 (0x0000)
R0x33BA	TPG_BLOB_Y2	0000 dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x33BC	TPG_HDR_RATIOS	00dd 0ddd 0ddd 0ddd	8192 (0x2000)
R0x33BE	ANALOG_LOW_GAIN	0000 0000 dddd dddd	0 (0x0000)
R0x33C0	OC_LUT_00	dddd dddd dddd dddd	8192 (0x2000)
R0x33C2	OC_LUT_01	dddd dddd dddd dddd	16384 (0x4000)
R0x33C4	OC_LUT_02	dddd dddd dddd dddd	32768 (0x8000)
R0x33C6	OC_LUT_03	dddd dddd dddd dddd	33280 (0x8200)
R0x33C8	OC_LUT_04	dddd dddd dddd dddd	34304 (0x8600)
R0x33CA	OC_LUT_05	dddd dddd dddd dddd	36352 (0x8E00)
R0x33CC	OC_LUT_06	dddd dddd dddd dddd	40448 (0x9E00)
R0x33CE	OC_LUT_07	dddd dddd dddd dddd	48640 (0xBE00)
R0x33D0	OC_LUT_08	dddd dddd dddd dddd	49664 (0xC200)
R0x33D2	OC_LUT_09	dddd dddd dddd dddd	51712 (0xCA00)
R0x33D4	OC_LUT_10	dddd dddd dddd dddd	55808 (0xDA00)
R0x33D6	OC_LUT_11	dddd dddd dddd dddd	64000 (0xFA00)
R0x33D8	OC_LUT_12	dddd dddd dddd dddd	64000 (0xFA00)
R0x33DA	OC_LUT_13	dddd dddd dddd dddd	64000 (0xFA00)
R0x33DC	OC_LUT_14	dddd dddd dddd dddd	64000 (0xFA00)
R0x33DE	OC_LUT_15	dddd dddd dddd dddd	64000 (0xFA00)
R0x33E0	TEST_ASIL_ROWS	dddd dddd dddd dddd	272 (0x0110)
R0x33EE	TEST_CTRL	0000 dddd 0ddd dddd	3904 (0x0F40)
R0x33F2	DUMMY_PIXEL_VALUE	0000 dddd dddd dddd	4 (0x0004)
R0x33F6	OC_LUT_CONTROL	0000 0000 0000 0ddd	0 (0x0000)
R0x3402	X_OUTPUT_CONTROL	d00d dddd dddd ddd0	3848 (0x0F08)
R0x3406	X_OUTPUT_CONTROL_CB	d00d dddd dddd ddd0	3848 (0x0F08)
R0x340A	GPIO_CONTROL1	dddd dddd dddd dddd	247 (0x00F7)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x340C	GPIO_CONTROL2	0000 dddd dddd dddd	0 (0x0000)
R0x340E	GPIO_SELECT	dddd dddd dddd dddd	528 (0x0210)
R0x3410	LOW_POWER_CONTROL	0000 0000 000d 000d	16 (0x0010)
R0x3418	LRE_GAIN_GRR_RED	dddd dddd dddd dddd	0 (0x0000)
R0x341A	LRE_GAIN_BLU_GRB	dddd dddd dddd dddd	0 (0x0000)
R0x341C	LRE_GAIN_GRR_RED_CB	dddd dddd dddd dddd	0 (0x0000)
R0x341E	LRE_GAIN_BLU_GRB_CB	dddd dddd dddd dddd	0 (0x0000)
R0x3420	I2CIDS0	dddd dddd dddd dddd	12320 (0x3020)
R0x3422	I2CIDS1	dddd dddd dddd dddd	28268 (0x6E6C)
R0x3424	I2CIDS2	dddd dddd dddd dddd	20544 (0x5040)
R0x3426	I2CIDS3	???? ???? ???? ????	28768 (0x7060)
R0x34C0	FUSE_ID1	???? ???? ???? ????	0 (0x0000)
R0x34C2	FUSE_ID2	???? ???? ???? ????	0 (0x0000)
R0x34C4	FUSE_ID3	???? ???? ???? ????	0 (0x0000)
R0x34C6	FUSE_ID4	???? ???? ???? ????	0 (0x0000)
R0x34C8	FUSE_ID5	???? ???? ???? ????	0 (0x0000)
R0x34CA	FUSE_ID6	???? ???? ???? ????	0 (0x0000)
R0x34CC	FUSE_ID7	???? ???? ???? ????	0 (0x0000)
R0x34CE	FUSE_ID8	???? ???? ???? ????	0 (0x0000)
R0x34DC	ASIL_EXT_CLK_COUNT_MSB_EXPECT	0000 0000 00dd dddd	0 (0x0000)
R0x34DE	ASIL_EXT_CLK_COUNT_LSB_EXPECT	dddd dddd dddd dddd	0 (0x0000)
R0x34E0	ASIL_CLK_PIX_COUNT_MSB_EXPECT	0000 0000 00dd dddd	0 (0x0000)
R0x34E2	ASIL_CLK_PIX_COUNT_LSB_EXPECT	dddd dddd dddd dddd	0 (0x0000)
R0x34E4	ASIL_CLK_OP_COUNT_MSB_EXPECT	0000 0000 00dd dddd	0 (0x0000)
R0x34E6	ASIL_CLK_OP_COUNT_LSB_EXPECT	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x34E8	ASIL_CLK_REG_COUNT_MSB_EXPECT	0000 0000 00dd dddd	0 (0x0000)
R0x34EA	ASIL_CLK_REG_COUNT_LSB_EXPECT	dddd dddd dddd dddd	0 (0x0000)
R0x34EC	ASIL_CLK_PIX_COUNT_100_EXT_EXPECT	0000 0ddd dddd dddd	0 (0x0000)
R0x34EE	ASIL_CLK_OP_COUNT_100_EXT_EXPECT	0000 0ddd dddd dddd	0 (0x0000)
R0x34F0	ASIL_CLK_REG_COUNT_100_EXT_EXPECT	0000 0ddd dddd dddd	0 (0x0000)
R0x34F2	ASIL_CLK_COUNT_THRESHOLD	dddd dddd dddd dddd	0 (0x0000)
R0x34F4	ASIL_CLK_COUNT_100_THRESHOLD	0000 dddd dddd dddd	0 (0x0000)
R0x35A0	GREEN1_GAIN_T2	0000 0ddd dddd dddd	128 (0x0080)
R0x35A2	BLUE_GAIN_T2	0000 0ddd dddd dddd	128 (0x0080)
R0x35A4	RED_GAIN_T2	0000 0ddd dddd dddd	128 (0x0080)
R0x35A6	GREEN2_GAIN_T2	0000 0ddd dddd dddd	128 (0x0080)
R0x35A8	GREEN1_GAIN_T3	0000 0ddd dddd dddd	128 (0x0080)
R0x35AA	BLUE_GAIN_T3	0000 0ddd dddd dddd	128 (0x0080)
R0x35AC	RED_GAIN_T3	0000 0ddd dddd dddd	128 (0x0080)
R0x35AE	GREEN2_GAIN_T3	0000 0ddd dddd dddd	128 (0x0080)
R0x35B0	GREEN1_GAIN_T4	0000 0ddd dddd dddd	128 (0x0080)
R0x35B2	BLUE_GAIN_T4	0000 0ddd dddd dddd	128 (0x0080)
R0x35B4	RED_GAIN_T4	0000 0ddd dddd dddd	128 (0x0080)
R0x35B6	GREEN2_GAIN_T4	0000 0ddd dddd dddd	128 (0x0080)
R0x35C0	GREEN1_GAIN_T2_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35C2	BLUE_GAIN_T2_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35C4	RED_GAIN_T2_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35C6	GREEN2_GAIN_T2_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35C8	GREEN1_GAIN_T3_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35CA	BLUE_GAIN_T3_CB	0000 0ddd dddd dddd	128 (0x0080)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x35CC	RED_GAIN_T3_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35CE	GREEN2_GAIN_T3_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35D0	GREEN1_GAIN_T4_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35D2	BLUE_GAIN_T4_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35D4	RED_GAIN_T4_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x35D6	GREEN2_GAIN_T4_CB	0000 0ddd dddd dddd	128 (0x0080)
R0x37A0	COARSE_INTEGRATION_AD_TIME	dddd dddd dddd dddd	1 (0x0001)
R0x37A2	COARSE_INTEGRATION_AD_TIME_CB	dddd dddd dddd dddd	1 (0x0001)
R0x37A4	COARSE_INTEGRATION_AD_TIME2	dddd dddd dddd dddd	0 (0x0000)
R0x37A6	COARSE_INTEGRATION_AD_TIME2_CB	dddd dddd dddd dddd	0 (0x0000)
R0x37A8	COARSE_INTEGRATION_AD_TIME3	dddd dddd dddd dddd	0 (0x0000)
R0x37AA	COARSE_INTEGRATION_AD_TIME3_CB	dddd dddd dddd dddd	0 (0x0000)
R0x37AC	COARSE_INTEGRATION_AD_TIME4	dddd dddd dddd dddd	0 (0x0000)
R0x37AE	COARSE_INTEGRATION_AD_TIME4_CB	dddd dddd dddd dddd	0 (0x0000)
R0x37E0	ROW_TX_RO_ENABLE	dddd dddd dddd dddd	33825 (0x8421)
R0x37E2	ROW_TX_RO_ENABLE_CB	dddd dddd dddd dddd	15 (0x000F)
R0x3C06	CONFIGURE_BUFFERS1	dddd dddd dddd dddd	5252 (0x1484)
R0x3C08	CONFIGURE_BUFFERS2	dddd d00d dddd dddd	12 (0x000C)
R0x3C0A	DELAY_BUFFER_CRC_FAULT_CONTROL	dddd dddd dddd 0ddd	0 (0x0000)
R0x3C0E	NOISE_LIMIT_LEVEL	dddd dddd dddd dddd	65535 (0xFFFF)
R0x3C10	TEMPVSENS_BOOST_CAL_SLOPE_00	0000 dddd dddd dddd	0 (0x0000)
R0x3C12	TEMPVSENS_BOOST_CAL_SLOPE_01	0000 dddd dddd dddd	0 (0x0000)
R0x3C14	TEMPVSENS_BOOST_CAL_SLOPE_02	0000 dddd dddd dddd	0 (0x0000)
R0x3C16	TEMPVSENS_BOOST_CAL_SLOPE_03	0000 dddd dddd dddd	0 (0x0000)
R0x3C18	TEMPVSENS_BOOST_CAL_SLOPE_04	0000 dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3C1A	TEMPVSENS_BOOST_CAL_SLOPE_05	0000 dddd dddd dddd	0 (0x0000)
R0x3C1C	TEMPVSENS_BOOST_CAL_SLOPE_06	0000 dddd dddd dddd	0 (0x0000)
R0x3C1E	TEMPVSENS_BOOST_CAL_SLOPE_07	0000 dddd dddd dddd	0 (0x0000)
R0x3C20	TEMPVSENS_BOOST_CAL_SLOPE_08	0000 dddd dddd dddd	0 (0x0000)
R0x3C22	TEMPVSENS_BOOST_CAL_SLOPE_09	0000 dddd dddd dddd	0 (0x0000)
R0x3C24	TEMPVSENS_BOOST_CAL_SLOPE_10	0000 dddd dddd dddd	0 (0x0000)
R0x3C26	TEMPVSENS_BOOST_CAL_SLOPE_11	0000 dddd dddd dddd	0 (0x0000)
R0x3C28	TEMPVSENS_BOOST_CAL_SLOPE_12	0000 dddd dddd dddd	0 (0x0000)
R0x3C2A	TEMPVSENS_BOOST_CAL_SLOPE_13	0000 dddd dddd dddd	0 (0x0000)
R0x3C2C	TEMPVSENS_BOOST_CAL_SLOPE_14	0000 dddd dddd dddd	0 (0x0000)
R0x3C2E	TEMPVSENS_BOOST_CAL_SLOPE_15	0000 dddd dddd dddd	0 (0x0000)
R0x3C30	TEMPVSENS_BOOST_CAL_SLOPE_16	0000 dddd dddd dddd	0 (0x0000)
R0x3C32	TEMPVSENS_BOOST_CAL_SLOPE_17	0000 dddd dddd dddd	0 (0x0000)
R0x3C34	TEMPVSENS_BOOST_CAL_SLOPE_18	0000 dddd dddd dddd	0 (0x0000)
R0x3C36	TEMPVSENS_BOOST_CAL_SLOPE_19	0000 dddd dddd dddd	0 (0x0000)
R0x3C38	TEMPVSENS_BOOST_CAL_SLOPE_20	0000 dddd dddd dddd	0 (0x0000)
R0x3C40	TEMPVSENS_BOOST_CAL_OFFSET_12	0000 dddd dddd dddd	0 (0x0000)
R0x3C42	TEMPVSENS_BOOST_CAL_OFFSET_14	0000 dddd dddd dddd	0 (0x0000)
R0x3C44	TEMPVSENS_BOOST_CAL_OFFSET_15	0000 dddd dddd dddd	0 (0x0000)
R0x3C46	TEMPVSENS_BOOST_CAL_OFFSET_16	0000 dddd dddd dddd	0 (0x0000)
R0x3C48	TEMPVSENS_BOOST_CAL_OFFSET_17	0000 dddd dddd dddd	0 (0x0000)
R0x3C4A	TEMPVSENS_BOOST_CAL_OFFSET_18	0000 dddd dddd dddd	0 (0x0000)
R0x3C4C	TEMPVSENS_BOOST_CAL_OFFSET_19	0000 dddd dddd dddd	0 (0x0000)
R0x3C4E	TEMPVSENS_BOOST_CAL_OFFSET_20	0000 dddd dddd dddd	0 (0x0000)
R0x3C60	TEMPVSENS1_VMON_CAL_SLOPE_0	0000 dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3C70	DBLC_SEPARATE_DISABLE	0000 0000 0000 000d	0 (0x0000)
R0x3C72	TEMP_FLAG_CONTROL	0000 0000 0000 000d	1 (0x0001)
R0x3C74	DBLC_CONTROL_CB	0000 0000 0000 00dd	0 (0x0000)
R0x3E6E	TEMPVSENS1_TMG_CTRL_K0	dddd dddd dddd dddd	8000 (0x1F40)
R0x3E70	TEMPVSENS1_TMG_CTRL_K1	000d dddd 0ddd dddd	272 (0x0110)
R0x3E98	TEMPVSENS1_EN_CTRL	dddd 00dd 000d dddd	16384 (0x4000)
R0x3EE0	TEMPVSENS1_FLAG_CTRL_EXT	0000 0ddd 0ddd dddd	1792 (0x0700)
R0x3EE2	TEMPSENS1_CTRL_REG_EXT	0000 0000 0000 0ddd	0 (0x0000)
R0x3EE4	TEMPVSENS0_SHUTTER_RESET_EN	0000 0000 0000 0ddd	7 (0x0007)
R0x3F60	ASIL_CHECK_ENABLES_00	dddd dddd dd00 000d	0 (0x0000)
R0x3F62	ASIL_CHECK_ENABLES_01	dddd dddd dddd dddd	0 (0x0000)
R0x3F64	ASIL_CHECK_ENABLES_02	0ddd dddd 0ddd 000d	0 (0x0000)
R0x3F66	ASIL_STARTUP_ENABLES_00	0000 0000 dd0d dddd	3 (0x0003)
R0x3F68	ASIL_PIN_ENABLES_00	dddd dddd dd00 000d	0 (0x0000)
R0x3F6A	ASIL_PIN_ENABLES_01	dddd dddd dddd dddd	0 (0x0000)
R0x3F6C	ASIL_PIN_ENABLES_02	0ddd dddd 0ddd 000d	0 (0x0000)
R0x3F6E	ASIL_STARTUP_PIN_ENABLES_00	0000 0000 000d dddd	0 (0x0000)
R0x3F70	PROCESS_DTR	0000 dddd dddd ddd0	0 (0x0000)
R0x3F72	ASIL_CRC_ENABLES	0000 0000 0000 000d	0 (0x0000)
R0x3F74	ASIL_CHECK_ENABLES_04	00dd dddd dddd dddd	0 (0x0000)
R0x3F76	ASIL_PIN_ENABLES_04	00dd dddd dddd dddd	0 (0x0000)
R0x3F7C	ASIL_CHECK_ENABLES_07	0000 0000 0000 000d	0 (0x0000)
R0x3F7E	ASIL_PIN_ENABLES_07	0000 0000 0000 000d	0 (0x0000)
R0x3F92	TEMPVSENS1_TMG_CTRL	dddd dddd dddd dddd	5120 (0x1400)
R0x3F96	TEMPVSENS1_FLAG_CTRL	dddd dddd dddd dddd	53310 (0xD03E)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x3F9A	TEMPVSENS0_BOOST_SAMP_CTRL	dddd 000d dddd dddd	0 (0x0000)
R0x3F9C	TEMPVSENS1_AUTO_VREF4_PULSE	dddd dddd dddd dddd	63568 (0xF850)
R0x3F9E	TEMPVSENS1_PEDESTAL_VREF16	0ddd dddd dddd dddd	16518 (0x4086)
R0x3FC2	TEMPVSENS1_TMG_CTRL_EX	0000 0000 00dd dddd	0 (0x0000)
R0x5100	EMBED_CRC_MAP00	dddd dddd dddd dddd	3 (0x0003)
R0x5102	EMBED_CRC_MAP01	dddd dddd dddd dddd	6 (0x0006)
R0x5104	EMBED_CRC_MAP02	dddd dddd dddd dddd	4096 (0x1000)
R0x5106	EMBED_CRC_MAP03	dddd dddd dddd dddd	0 (0x0000)
R0x5108	EMBED_CRC_MAP04	dddd dddd dddd dddd	2 (0x0002)
R0x510A	EMBED_CRC_MAP05	dddd dddd dddd dddd	0 (0x0000)
R0x510C	EMBED_CRC_MAP06	dddd dddd dddd dddd	0 (0x0000)
R0x510E	EMBED_CRC_MAP07	dddd dddd dddd dddd	0 (0x0000)
R0x5110	EMBED_CRC_MAP08	dddd dddd dddd dddd	0 (0x0000)
R0x5112	EMBED_CRC_MAP09	dddd dddd dddd dddd	0 (0x0000)
R0x5114	EMBED_CRC_MAP10	dddd dddd dddd dddd	64 (0x0040)
R0x5116	EMBED_CRC_MAP11	dddd dddd dddd dddd	0 (0x0000)
R0x5118	EMBED_CRC_MAP12	dddd dddd dddd dddd	0 (0x0000)
R0x511A	EMBED_CRC_MAP13	dddd dddd dddd dddd	0 (0x0000)
R0x511C	EMBED_CRC_MAP14	dddd dddd dddd dddd	0 (0x0000)
R0x511E	EMBED_CRC_MAP15	dddd dddd dddd dddd	0 (0x0000)
R0x5120	EMBED_CRC_MAP16	dddd dddd dddd dddd	2 (0x0002)
R0x5122	EMBED_CRC_MAP17	dddd dddd dddd dddd	16384 (0x4000)
R0x5124	EMBED_CRC_MAP18	dddd dddd dddd dddd	0 (0x0000)
R0x5126	EMBED_CRC_MAP19	dddd dddd dddd dddd	0 (0x0000)
R0x5128	EMBED_CRC_MAP20	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x512A	EMBED_CRC_MAP21	dddd dddd dddd dddd	0 (0x0000)
R0x512C	EMBED_CRC_MAP22	dddd dddd dddd dddd	0 (0x0000)
R0x512E	EMBED_CRC_MAP23	dddd dddd dddd dddd	0 (0x0000)
R0x5130	EMBED_CRC_MAP24	dddd dddd dddd dddd	0 (0x0000)
R0x5132	EMBED_CRC_MAP25	dddd dddd dddd dddd	1472 (0x05C0)
R0x5134	EMBED_CRC_MAP26	dddd dddd dddd dddd	0 (0x0000)
R0x5136	EMBED_CRC_MAP27	dddd dddd dddd dddd	16 (0x0010)
R0x5138	EMBED_CRC_MAP28	dddd dddd dddd dddd	0 (0x0000)
R0x513A	EMBED_CRC_MAP29	dddd dddd dddd dddd	0 (0x0000)
R0x513C	EMBED_CRC_MAP30	dddd dddd dddd dddd	0 (0x0000)
R0x513E	EMBED_CRC_MAP31	dddd dddd dddd dddd	0 (0x0000)
R0x5140	EMBED_CRC_MAP32	dddd dddd dddd dddd	0 (0x0000)
R0x5142	EMBED_CRC_MAP33	dddd dddd dddd dddd	0 (0x0000)
R0x5144	EMBED_CRC_MAP34	dddd dddd dddd dddd	0 (0x0000)
R0x5146	EMBED_CRC_MAP35	dddd dddd dddd dddd	0 (0x0000)
R0x5148	EMBED_CRC_MAP36	dddd dddd dddd dddd	0 (0x0000)
R0x514A	EMBED_CRC_MAP37	dddd dddd dddd dddd	0 (0x0000)
R0x514C	EMBED_CRC_MAP38	dddd dddd dddd dddd	0 (0x0000)
R0x514E	EMBED_CRC_MAP39	dddd dddd dddd dddd	0 (0x0000)
R0x5150	EMBED_CRC_MAP40	dddd dddd dddd dddd	0 (0x0000)
R0x5152	EMBED_CRC_MAP41	dddd dddd dddd dddd	0 (0x0000)
R0x5154	EMBED_CRC_MAP42	dddd dddd dddd dddd	0 (0x0000)
R0x5156	EMBED_CRC_MAP43	dddd dddd dddd dddd	0 (0x0000)
R0x5158	EMBED_CRC_MAP44	dddd dddd dddd dddd	16384 (0x4000)
R0x515A	EMBED_CRC_MAP45	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x515C	EMBED_CRC_MAP46	dddd dddd dddd dddd	0 (0x0000)
R0x515E	EMBED_CRC_MAP47	dddd dddd dddd dddd	8 (0x0008)
R0x5160	EMBED_CRC_MAP48	dddd dddd dddd dddd	0 (0x0000)
R0x5162	EMBED_CRC_MAP49	dddd dddd dddd dddd	16384 (0x4000)
R0x5164	EMBED_CRC_MAP50	dddd dddd dddd dddd	0 (0x0000)
R0x5166	EMBED_CRC_MAP51	dddd dddd dddd dddd	0 (0x0000)
R0x5168	EMBED_CRC_MAP52	dddd dddd dddd dddd	0 (0x0000)
R0x516A	EMBED_CRC_MAP53	dddd dddd dddd dddd	0 (0x0000)
R0x516C	EMBED_CRC_MAP54	dddd dddd dddd dddd	0 (0x0000)
R0x516E	EMBED_CRC_MAP55	dddd dddd dddd dddd	0 (0x0000)
R0x5170	EMBED_CRC_MAP56	dddd dddd dddd dddd	0 (0x0000)
R0x5172	EMBED_CRC_MAP57	dddd dddd dddd dddd	0 (0x0000)
R0x5174	EMBED_CRC_MAP58	dddd dddd dddd dddd	0 (0x0000)
R0x5176	EMBED_CRC_MAP59	dddd dddd dddd dddd	0 (0x0000)
R0x5178	EMBED_CRC_MAP60	dddd dddd dddd dddd	0 (0x0000)
R0x517A	EMBED_CRC_MAP61	dddd dddd dddd dddd	0 (0x0000)
R0x517C	EMBED_CRC_MAP62	dddd dddd dddd dddd	0 (0x0000)
R0x517E	EMBED_CRC_MAP63	dddd dddd dddd dddd	0 (0x0000)
R0x559E	ODP_CRC_FAULT_CONTROL	00dd 0ddd 00dd 0ddd	0 (0x0000)
R0x55A0	ODP_CRC_FAULTS_PER_FRAME	???? ???? ???? ????	0 (0x0000)
R0x55A2	ODP_CRC_FAULT_FRAMES	???? ???? ???? ????	0 (0x0000)
R0x55A4	SCALER_CRC_FAULTS_PER_FRAME	???? ???? ???? ????	0 (0x0000)
R0x55A6	SCALER_CRC_FAULT_FRAMES	???? ???? ???? ????	0 (0x0000)
R0x5800	ASIL_CHECK_ENABLES_08	0000 0000 dddd dddd	0 (0x0000)
R0x5802	ASIL_PIN_ENABLES_08	0000 0000 dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0x5900	ATR_CHECK_OT_BASE	00dd dddd dddd dddd	0 (0x0000)
R0x5902	ATR_CHECK_OT_LO_OFFSET	00dd dddd dddd dddd	0 (0x0000)
R0x5904	ATR_CHECK_OT_HI_OFFSET	00dd dddd dddd dddd	0 (0x0000)
R0x5906	ATR_CHECK_GT_EXPECT1	00dd dddd dddd dddd	0 (0x0000)
R0x5908	ATR_CHECK_GT_EXPECT2	00dd dddd dddd dddd	0 (0x0000)
R0x590A	RRC_CHECK_LO_THRESH2	00dd dddd dddd dddd	0 (0x0000)
R0x590C	ATR_PEDESTAL_SELECT0	dddd dddd dddd dddd	0 (0x0000)
R0x590E	ATR_PEDESTAL_SELECT1	dddd dddd dddd dddd	0 (0x0000)
R0x5910	ATR_PEDESTAL0	00dd dddd dddd dddd	0 (0x0000)
R0x5912	ATR_PEDESTAL1	00dd dddd dddd dddd	14336 (0x3800)
R0x5914	ATR_PEDESTAL2	00dd dddd dddd dddd	2048 (0x0800)
R0x5916	ATR_PEDESTAL3	00dd dddd dddd dddd	4095 (0x0FFF)
R0x5918	ATC_PEDESTAL	dddd dddd dddd dddd	120 (0x0078)
R0xF000	CSS_COMMAND	dddd dddd dddd dddd	32768 (0x8000)
R0xF008	CSS_ERROR	???? ???? ???? ????	0 (0x0000)
R0xF00A	CSS_INFO	???? ???? ???? ????	0 (0x0000)
R0xF00C	CSS_PAGE	0000 0000 0000 00dd	0 (0x0000)
R0xF100	CSS_PARAMS_0	dddd dddd dddd dddd	0 (0x0000)
R0xF102	CSS_PARAMS_1	dddd dddd dddd dddd	0 (0x0000)
R0xF104	CSS_PARAMS_2	dddd dddd dddd dddd	0 (0x0000)
R0xF106	CSS_PARAMS_3	dddd dddd dddd dddd	0 (0x0000)
R0xF108	CSS_PARAMS_4	dddd dddd dddd dddd	0 (0x0000)
R0xF10A	CSS_PARAMS_5	dddd dddd dddd dddd	0 (0x0000)
R0xF10C	CSS_PARAMS_6	dddd dddd dddd dddd	0 (0x0000)
R0xF10E	CSS_PARAMS_7	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF110	CSS_PARAMS_8	dddd dddd dddd dddd	0 (0x0000)
R0xF112	CSS_PARAMS_9	dddd dddd dddd dddd	0 (0x0000)
R0xF114	CSS_PARAMS_10	dddd dddd dddd dddd	0 (0x0000)
R0xF116	CSS_PARAMS_11	dddd dddd dddd dddd	0 (0x0000)
R0xF118	CSS_PARAMS_12	dddd dddd dddd dddd	0 (0x0000)
R0xF11A	CSS_PARAMS_13	dddd dddd dddd dddd	0 (0x0000)
R0xF11C	CSS_PARAMS_14	dddd dddd dddd dddd	0 (0x0000)
R0xF11E	CSS_PARAMS_15	dddd dddd dddd dddd	0 (0x0000)
R0xF120	CSS_PARAMS_16	dddd dddd dddd dddd	0 (0x0000)
R0xF122	CSS_PARAMS_17	dddd dddd dddd dddd	0 (0x0000)
R0xF124	CSS_PARAMS_18	dddd dddd dddd dddd	0 (0x0000)
R0xF126	CSS_PARAMS_19	dddd dddd dddd dddd	0 (0x0000)
R0xF128	CSS_PARAMS_20	dddd dddd dddd dddd	0 (0x0000)
R0xF12A	CSS_PARAMS_21	dddd dddd dddd dddd	0 (0x0000)
R0xF12C	CSS_PARAMS_22	dddd dddd dddd dddd	0 (0x0000)
R0xF12E	CSS_PARAMS_23	dddd dddd dddd dddd	0 (0x0000)
R0xF130	CSS_PARAMS_24	dddd dddd dddd dddd	0 (0x0000)
R0xF132	CSS_PARAMS_25	dddd dddd dddd dddd	0 (0x0000)
R0xF134	CSS_PARAMS_26	dddd dddd dddd dddd	0 (0x0000)
R0xF136	CSS_PARAMS_27	dddd dddd dddd dddd	0 (0x0000)
R0xF138	CSS_PARAMS_28	dddd dddd dddd dddd	0 (0x0000)
R0xF13A	CSS_PARAMS_29	dddd dddd dddd dddd	0 (0x0000)
R0xF13C	CSS_PARAMS_30	dddd dddd dddd dddd	0 (0x0000)
R0xF13E	CSS_PARAMS_31	dddd dddd dddd dddd	0 (0x0000)
R0xF140	CSS_PARAMS_32	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF142	CSS_PARAMS_33	dddd dddd dddd dddd	0 (0x0000)
R0xF144	CSS_PARAMS_34	dddd dddd dddd dddd	0 (0x0000)
R0xF146	CSS_PARAMS_35	dddd dddd dddd dddd	0 (0x0000)
R0xF148	CSS_PARAMS_36	dddd dddd dddd dddd	0 (0x0000)
R0xF14A	CSS_PARAMS_37	dddd dddd dddd dddd	0 (0x0000)
R0xF14C	CSS_PARAMS_38	dddd dddd dddd dddd	0 (0x0000)
R0xF14E	CSS_PARAMS_39	dddd dddd dddd dddd	0 (0x0000)
R0xF150	CSS_PARAMS_40	dddd dddd dddd dddd	0 (0x0000)
R0xF152	CSS_PARAMS_41	dddd dddd dddd dddd	0 (0x0000)
R0xF154	CSS_PARAMS_42	dddd dddd dddd dddd	0 (0x0000)
R0xF156	CSS_PARAMS_43	dddd dddd dddd dddd	0 (0x0000)
R0xF158	CSS_PARAMS_44	dddd dddd dddd dddd	0 (0x0000)
R0xF15A	CSS_PARAMS_45	dddd dddd dddd dddd	0 (0x0000)
R0xF15C	CSS_PARAMS_46	dddd dddd dddd dddd	0 (0x0000)
R0xF15E	CSS_PARAMS_47	dddd dddd dddd dddd	0 (0x0000)
R0xF160	CSS_PARAMS_48	dddd dddd dddd dddd	0 (0x0000)
R0xF162	CSS_PARAMS_49	dddd dddd dddd dddd	0 (0x0000)
R0xF164	CSS_PARAMS_50	dddd dddd dddd dddd	0 (0x0000)
R0xF166	CSS_PARAMS_51	dddd dddd dddd dddd	0 (0x0000)
R0xF168	CSS_PARAMS_52	dddd dddd dddd dddd	0 (0x0000)
R0xF16A	CSS_PARAMS_53	dddd dddd dddd dddd	0 (0x0000)
R0xF16C	CSS_PARAMS_54	dddd dddd dddd dddd	0 (0x0000)
R0xF16E	CSS_PARAMS_55	dddd dddd dddd dddd	0 (0x0000)
R0xF170	CSS_PARAMS_56	dddd dddd dddd dddd	0 (0x0000)
R0xF172	CSS_PARAMS_57	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF174	CSS_PARAMS_58	dddd dddd dddd dddd	0 (0x0000)
R0xF176	CSS_PARAMS_59	dddd dddd dddd dddd	0 (0x0000)
R0xF178	CSS_PARAMS_60	dddd dddd dddd dddd	0 (0x0000)
R0xF17A	CSS_PARAMS_61	dddd dddd dddd dddd	0 (0x0000)
R0xF17C	CSS_PARAMS_62	dddd dddd dddd dddd	0 (0x0000)
R0xF17E	CSS_PARAMS_63	dddd dddd dddd dddd	0 (0x0000)
R0xF180	CSS_PARAMS_64	dddd dddd dddd dddd	0 (0x0000)
R0xF182	CSS_PARAMS_65	dddd dddd dddd dddd	0 (0x0000)
R0xF184	CSS_PARAMS_66	dddd dddd dddd dddd	0 (0x0000)
R0xF186	CSS_PARAMS_67	dddd dddd dddd dddd	0 (0x0000)
R0xF188	CSS_PARAMS_68	dddd dddd dddd dddd	0 (0x0000)
R0xF18A	CSS_PARAMS_69	dddd dddd dddd dddd	0 (0x0000)
R0xF18C	CSS_PARAMS_70	dddd dddd dddd dddd	0 (0x0000)
R0xF18E	CSS_PARAMS_71	dddd dddd dddd dddd	0 (0x0000)
R0xF190	CSS_PARAMS_72	dddd dddd dddd dddd	0 (0x0000)
R0xF192	CSS_PARAMS_73	dddd dddd dddd dddd	0 (0x0000)
R0xF194	CSS_PARAMS_74	dddd dddd dddd dddd	0 (0x0000)
R0xF196	CSS_PARAMS_75	dddd dddd dddd dddd	0 (0x0000)
R0xF198	CSS_PARAMS_76	dddd dddd dddd dddd	0 (0x0000)
R0xF19A	CSS_PARAMS_77	dddd dddd dddd dddd	0 (0x0000)
R0xF19C	CSS_PARAMS_78	dddd dddd dddd dddd	0 (0x0000)
R0xF19E	CSS_PARAMS_79	dddd dddd dddd dddd	0 (0x0000)
R0xF1A0	CSS_PARAMS_80	dddd dddd dddd dddd	0 (0x0000)
R0xF1A2	CSS_PARAMS_81	dddd dddd dddd dddd	0 (0x0000)
R0xF1A4	CSS_PARAMS_82	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF1A6	CSS_PARAMS_83	dddd dddd dddd dddd	0 (0x0000)
R0xF1A8	CSS_PARAMS_84	dddd dddd dddd dddd	0 (0x0000)
R0xF1AA	CSS_PARAMS_85	dddd dddd dddd dddd	0 (0x0000)
R0xF1AC	CSS_PARAMS_86	dddd dddd dddd dddd	0 (0x0000)
R0xF1AE	CSS_PARAMS_87	dddd dddd dddd dddd	0 (0x0000)
R0xF1B0	CSS_PARAMS_88	dddd dddd dddd dddd	0 (0x0000)
R0xF1B2	CSS_PARAMS_89	dddd dddd dddd dddd	0 (0x0000)
R0xF1B4	CSS_PARAMS_90	dddd dddd dddd dddd	0 (0x0000)
R0xF1B6	CSS_PARAMS_91	dddd dddd dddd dddd	0 (0x0000)
R0xF1B8	CSS_PARAMS_92	dddd dddd dddd dddd	0 (0x0000)
R0xF1BA	CSS_PARAMS_93	dddd dddd dddd dddd	0 (0x0000)
R0xF1BC	CSS_PARAMS_94	dddd dddd dddd dddd	0 (0x0000)
R0xF1BE	CSS_PARAMS_95	dddd dddd dddd dddd	0 (0x0000)
R0xF1C0	CSS_PARAMS_96	dddd dddd dddd dddd	0 (0x0000)
R0xF1C2	CSS_PARAMS_97	dddd dddd dddd dddd	0 (0x0000)
R0xF1C4	CSS_PARAMS_98	dddd dddd dddd dddd	0 (0x0000)
R0xF1C6	CSS_PARAMS_99	dddd dddd dddd dddd	0 (0x0000)
R0xF1C8	CSS_PARAMS_100	dddd dddd dddd dddd	0 (0x0000)
R0xF1CA	CSS_PARAMS_101	dddd dddd dddd dddd	0 (0x0000)
R0xF1CC	CSS_PARAMS_102	dddd dddd dddd dddd	0 (0x0000)
R0xF1CE	CSS_PARAMS_103	dddd dddd dddd dddd	0 (0x0000)
R0xF1D0	CSS_PARAMS_104	dddd dddd dddd dddd	0 (0x0000)
R0xF1D2	CSS_PARAMS_105	dddd dddd dddd dddd	0 (0x0000)
R0xF1D4	CSS_PARAMS_106	dddd dddd dddd dddd	0 (0x0000)
R0xF1D6	CSS_PARAMS_107	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF1D8	CSS_PARAMS_108	dddd dddd dddd dddd	0 (0x0000)
R0xF1DA	CSS_PARAMS_109	dddd dddd dddd dddd	0 (0x0000)
R0xF1DC	CSS_PARAMS_110	dddd dddd dddd dddd	0 (0x0000)
R0xF1DE	CSS_PARAMS_111	dddd dddd dddd dddd	0 (0x0000)
R0xF1E0	CSS_PARAMS_112	dddd dddd dddd dddd	0 (0x0000)
R0xF1E2	CSS_PARAMS_113	dddd dddd dddd dddd	0 (0x0000)
R0xF1E4	CSS_PARAMS_114	dddd dddd dddd dddd	0 (0x0000)
R0xF1E6	CSS_PARAMS_115	dddd dddd dddd dddd	0 (0x0000)
R0xF1E8	CSS_PARAMS_116	dddd dddd dddd dddd	0 (0x0000)
R0xF1EA	CSS_PARAMS_117	dddd dddd dddd dddd	0 (0x0000)
R0xF1EC	CSS_PARAMS_118	dddd dddd dddd dddd	0 (0x0000)
R0xF1EE	CSS_PARAMS_119	dddd dddd dddd dddd	0 (0x0000)
R0xF1F0	CSS_PARAMS_120	dddd dddd dddd dddd	0 (0x0000)
R0xF1F2	CSS_PARAMS_121	dddd dddd dddd dddd	0 (0x0000)
R0xF1F4	CSS_PARAMS_122	dddd dddd dddd dddd	0 (0x0000)
R0xF1F6	CSS_PARAMS_123	dddd dddd dddd dddd	0 (0x0000)
R0xF1F8	CSS_PARAMS_124	dddd dddd dddd dddd	0 (0x0000)
R0xF1FA	CSS_PARAMS_125	dddd dddd dddd dddd	0 (0x0000)
R0xF1FC	CSS_PARAMS_126	dddd dddd dddd dddd	0 (0x0000)
R0xF1FE	CSS_PARAMS_127	dddd dddd dddd dddd	0 (0x0000)
R0xF200	CSS_PARAMS_128	dddd dddd dddd dddd	0 (0x0000)
R0xF202	CSS_PARAMS_129	dddd dddd dddd dddd	0 (0x0000)
R0xF204	CSS_PARAMS_130	dddd dddd dddd dddd	0 (0x0000)
R0xF206	CSS_PARAMS_131	dddd dddd dddd dddd	0 (0x0000)
R0xF208	CSS_PARAMS_132	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF20A	CSS_PARAMS_133	dddd dddd dddd dddd	0 (0x0000)
R0xF20C	CSS_PARAMS_134	dddd dddd dddd dddd	0 (0x0000)
R0xF20E	CSS_PARAMS_135	dddd dddd dddd dddd	0 (0x0000)
R0xF210	CSS_PARAMS_136	dddd dddd dddd dddd	0 (0x0000)
R0xF212	CSS_PARAMS_137	dddd dddd dddd dddd	0 (0x0000)
R0xF214	CSS_PARAMS_138	dddd dddd dddd dddd	0 (0x0000)
R0xF216	CSS_PARAMS_139	dddd dddd dddd dddd	0 (0x0000)
R0xF218	CSS_PARAMS_140	dddd dddd dddd dddd	0 (0x0000)
R0xF21A	CSS_PARAMS_141	dddd dddd dddd dddd	0 (0x0000)
R0xF21C	CSS_PARAMS_142	dddd dddd dddd dddd	0 (0x0000)
R0xF21E	CSS_PARAMS_143	dddd dddd dddd dddd	0 (0x0000)
R0xF220	CSS_PARAMS_144	dddd dddd dddd dddd	0 (0x0000)
R0xF222	CSS_PARAMS_145	dddd dddd dddd dddd	0 (0x0000)
R0xF224	CSS_PARAMS_146	dddd dddd dddd dddd	0 (0x0000)
R0xF226	CSS_PARAMS_147	dddd dddd dddd dddd	0 (0x0000)
R0xF228	CSS_PARAMS_148	dddd dddd dddd dddd	0 (0x0000)
R0xF22A	CSS_PARAMS_149	dddd dddd dddd dddd	0 (0x0000)
R0xF22C	CSS_PARAMS_150	dddd dddd dddd dddd	0 (0x0000)
R0xF22E	CSS_PARAMS_151	dddd dddd dddd dddd	0 (0x0000)
R0xF230	CSS_PARAMS_152	dddd dddd dddd dddd	0 (0x0000)
R0xF232	CSS_PARAMS_153	dddd dddd dddd dddd	0 (0x0000)
R0xF234	CSS_PARAMS_154	dddd dddd dddd dddd	0 (0x0000)
R0xF236	CSS_PARAMS_155	dddd dddd dddd dddd	0 (0x0000)
R0xF238	CSS_PARAMS_156	dddd dddd dddd dddd	0 (0x0000)
R0xF23A	CSS_PARAMS_157	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF23C	CSS_PARAMS_158	dddd dddd dddd dddd	0 (0x0000)
R0xF23E	CSS_PARAMS_159	dddd dddd dddd dddd	0 (0x0000)
R0xF240	CSS_PARAMS_160	dddd dddd dddd dddd	0 (0x0000)
R0xF242	CSS_PARAMS_161	dddd dddd dddd dddd	0 (0x0000)
R0xF244	CSS_PARAMS_162	dddd dddd dddd dddd	0 (0x0000)
R0xF246	CSS_PARAMS_163	dddd dddd dddd dddd	0 (0x0000)
R0xF248	CSS_PARAMS_164	dddd dddd dddd dddd	0 (0x0000)
R0xF24A	CSS_PARAMS_165	dddd dddd dddd dddd	0 (0x0000)
R0xF24C	CSS_PARAMS_166	dddd dddd dddd dddd	0 (0x0000)
R0xF24E	CSS_PARAMS_167	dddd dddd dddd dddd	0 (0x0000)
R0xF250	CSS_PARAMS_168	dddd dddd dddd dddd	0 (0x0000)
R0xF252	CSS_PARAMS_169	dddd dddd dddd dddd	0 (0x0000)
R0xF254	CSS_PARAMS_170	dddd dddd dddd dddd	0 (0x0000)
R0xF256	CSS_PARAMS_171	dddd dddd dddd dddd	0 (0x0000)
R0xF258	CSS_PARAMS_172	dddd dddd dddd dddd	0 (0x0000)
R0xF25A	CSS_PARAMS_173	dddd dddd dddd dddd	0 (0x0000)
R0xF25C	CSS_PARAMS_174	dddd dddd dddd dddd	0 (0x0000)
R0xF25E	CSS_PARAMS_175	dddd dddd dddd dddd	0 (0x0000)
R0xF260	CSS_PARAMS_176	dddd dddd dddd dddd	0 (0x0000)
R0xF262	CSS_PARAMS_177	dddd dddd dddd dddd	0 (0x0000)
R0xF264	CSS_PARAMS_178	dddd dddd dddd dddd	0 (0x0000)
R0xF266	CSS_PARAMS_179	dddd dddd dddd dddd	0 (0x0000)
R0xF268	CSS_PARAMS_180	dddd dddd dddd dddd	0 (0x0000)
R0xF26A	CSS_PARAMS_181	dddd dddd dddd dddd	0 (0x0000)
R0xF26C	CSS_PARAMS_182	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF26E	CSS_PARAMS_183	dddd dddd dddd dddd	0 (0x0000)
R0xF270	CSS_PARAMS_184	dddd dddd dddd dddd	0 (0x0000)
R0xF272	CSS_PARAMS_185	dddd dddd dddd dddd	0 (0x0000)
R0xF274	CSS_PARAMS_186	dddd dddd dddd dddd	0 (0x0000)
R0xF276	CSS_PARAMS_187	dddd dddd dddd dddd	0 (0x0000)
R0xF278	CSS_PARAMS_188	dddd dddd dddd dddd	0 (0x0000)
R0xF27A	CSS_PARAMS_189	dddd dddd dddd dddd	0 (0x0000)
R0xF27C	CSS_PARAMS_190	dddd dddd dddd dddd	0 (0x0000)
R0xF27E	CSS_PARAMS_191	dddd dddd dddd dddd	0 (0x0000)
R0xF280	CSS_PARAMS_192	dddd dddd dddd dddd	0 (0x0000)
R0xF282	CSS_PARAMS_193	dddd dddd dddd dddd	0 (0x0000)
R0xF284	CSS_PARAMS_194	dddd dddd dddd dddd	0 (0x0000)
R0xF286	CSS_PARAMS_195	dddd dddd dddd dddd	0 (0x0000)
R0xF288	CSS_PARAMS_196	dddd dddd dddd dddd	0 (0x0000)
R0xF28A	CSS_PARAMS_197	dddd dddd dddd dddd	0 (0x0000)
R0xF28C	CSS_PARAMS_198	dddd dddd dddd dddd	0 (0x0000)
R0xF28E	CSS_PARAMS_199	dddd dddd dddd dddd	0 (0x0000)
R0xF290	CSS_PARAMS_200	dddd dddd dddd dddd	0 (0x0000)
R0xF292	CSS_PARAMS_201	dddd dddd dddd dddd	0 (0x0000)
R0xF294	CSS_PARAMS_202	dddd dddd dddd dddd	0 (0x0000)
R0xF296	CSS_PARAMS_203	dddd dddd dddd dddd	0 (0x0000)
R0xF298	CSS_PARAMS_204	dddd dddd dddd dddd	0 (0x0000)
R0xF29A	CSS_PARAMS_205	dddd dddd dddd dddd	0 (0x0000)
R0xF29C	CSS_PARAMS_206	dddd dddd dddd dddd	0 (0x0000)
R0xF29E	CSS_PARAMS_207	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF2A0	CSS_PARAMS_208	dddd dddd dddd dddd	0 (0x0000)
R0xF2A2	CSS_PARAMS_209	dddd dddd dddd dddd	0 (0x0000)
R0xF2A4	CSS_PARAMS_210	dddd dddd dddd dddd	0 (0x0000)
R0xF2A6	CSS_PARAMS_211	dddd dddd dddd dddd	0 (0x0000)
R0xF2A8	CSS_PARAMS_212	dddd dddd dddd dddd	0 (0x0000)
R0xF2AA	CSS_PARAMS_213	dddd dddd dddd dddd	0 (0x0000)
R0xF2AC	CSS_PARAMS_214	dddd dddd dddd dddd	0 (0x0000)
R0xF2AE	CSS_PARAMS_215	dddd dddd dddd dddd	0 (0x0000)
R0xF2B0	CSS_PARAMS_216	dddd dddd dddd dddd	0 (0x0000)
R0xF2B2	CSS_PARAMS_217	dddd dddd dddd dddd	0 (0x0000)
R0xF2B4	CSS_PARAMS_218	dddd dddd dddd dddd	0 (0x0000)
R0xF2B6	CSS_PARAMS_219	dddd dddd dddd dddd	0 (0x0000)
R0xF2B8	CSS_PARAMS_220	dddd dddd dddd dddd	0 (0x0000)
R0xF2BA	CSS_PARAMS_221	dddd dddd dddd dddd	0 (0x0000)
R0xF2BC	CSS_PARAMS_222	dddd dddd dddd dddd	0 (0x0000)
R0xF2BE	CSS_PARAMS_223	dddd dddd dddd dddd	0 (0x0000)
R0xF2C0	CSS_PARAMS_224	dddd dddd dddd dddd	0 (0x0000)
R0xF2C2	CSS_PARAMS_225	dddd dddd dddd dddd	0 (0x0000)
R0xF2C4	CSS_PARAMS_226	dddd dddd dddd dddd	0 (0x0000)
R0xF2C6	CSS_PARAMS_227	dddd dddd dddd dddd	0 (0x0000)
R0xF2C8	CSS_PARAMS_228	dddd dddd dddd dddd	0 (0x0000)
R0xF2CA	CSS_PARAMS_229	dddd dddd dddd dddd	0 (0x0000)
R0xF2CC	CSS_PARAMS_230	dddd dddd dddd dddd	0 (0x0000)
R0xF2CE	CSS_PARAMS_231	dddd dddd dddd dddd	0 (0x0000)
R0xF2D0	CSS_PARAMS_232	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF2D2	CSS_PARAMS_233	dddd dddd dddd dddd	0 (0x0000)
R0xF2D4	CSS_PARAMS_234	dddd dddd dddd dddd	0 (0x0000)
R0xF2D6	CSS_PARAMS_235	dddd dddd dddd dddd	0 (0x0000)
R0xF2D8	CSS_PARAMS_236	dddd dddd dddd dddd	0 (0x0000)
R0xF2DA	CSS_PARAMS_237	dddd dddd dddd dddd	0 (0x0000)
R0xF2DC	CSS_PARAMS_238	dddd dddd dddd dddd	0 (0x0000)
R0xF2DE	CSS_PARAMS_239	dddd dddd dddd dddd	0 (0x0000)
R0xF2E0	CSS_PARAMS_240	dddd dddd dddd dddd	0 (0x0000)
R0xF2E2	CSS_PARAMS_241	dddd dddd dddd dddd	0 (0x0000)
R0xF2E4	CSS_PARAMS_242	dddd dddd dddd dddd	0 (0x0000)
R0xF2E6	CSS_PARAMS_243	dddd dddd dddd dddd	0 (0x0000)
R0xF2E8	CSS_PARAMS_244	dddd dddd dddd dddd	0 (0x0000)
R0xF2EA	CSS_PARAMS_245	dddd dddd dddd dddd	0 (0x0000)
R0xF2EC	CSS_PARAMS_246	dddd dddd dddd dddd	0 (0x0000)
R0xF2EE	CSS_PARAMS_247	dddd dddd dddd dddd	0 (0x0000)
R0xF2F0	CSS_PARAMS_248	dddd dddd dddd dddd	0 (0x0000)
R0xF2F2	CSS_PARAMS_249	dddd dddd dddd dddd	0 (0x0000)
R0xF2F4	CSS_PARAMS_250	dddd dddd dddd dddd	0 (0x0000)
R0xF2F6	CSS_PARAMS_251	dddd dddd dddd dddd	0 (0x0000)
R0xF2F8	CSS_PARAMS_252	dddd dddd dddd dddd	0 (0x0000)
R0xF2FA	CSS_PARAMS_253	dddd dddd dddd dddd	0 (0x0000)
R0xF2FC	CSS_PARAMS_254	dddd dddd dddd dddd	0 (0x0000)
R0xF2FE	CSS_PARAMS_255	dddd dddd dddd dddd	0 (0x0000)
R0xF300	CSS_PARAMS_256	dddd dddd dddd dddd	0 (0x0000)
R0xF302	CSS_PARAMS_257	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF304	CSS_PARAMS_258	dddd dddd dddd dddd	0 (0x0000)
R0xF306	CSS_PARAMS_259	dddd dddd dddd dddd	0 (0x0000)
R0xF308	CSS_PARAMS_260	dddd dddd dddd dddd	0 (0x0000)
R0xF30A	CSS_PARAMS_261	dddd dddd dddd dddd	0 (0x0000)
R0xF30C	CSS_PARAMS_262	dddd dddd dddd dddd	0 (0x0000)
R0xF30E	CSS_PARAMS_263	dddd dddd dddd dddd	0 (0x0000)
R0xF310	CSS_PARAMS_264	dddd dddd dddd dddd	0 (0x0000)
R0xF312	CSS_PARAMS_265	dddd dddd dddd dddd	0 (0x0000)
R0xF314	CSS_PARAMS_266	dddd dddd dddd dddd	0 (0x0000)
R0xF316	CSS_PARAMS_267	dddd dddd dddd dddd	0 (0x0000)
R0xF318	CSS_PARAMS_268	dddd dddd dddd dddd	0 (0x0000)
R0xF31A	CSS_PARAMS_269	dddd dddd dddd dddd	0 (0x0000)
R0xF31C	CSS_PARAMS_270	dddd dddd dddd dddd	0 (0x0000)
R0xF31E	CSS_PARAMS_271	dddd dddd dddd dddd	0 (0x0000)
R0xF320	CSS_PARAMS_272	dddd dddd dddd dddd	0 (0x0000)
R0xF322	CSS_PARAMS_273	dddd dddd dddd dddd	0 (0x0000)
R0xF324	CSS_PARAMS_274	dddd dddd dddd dddd	0 (0x0000)
R0xF326	CSS_PARAMS_275	dddd dddd dddd dddd	0 (0x0000)
R0xF328	CSS_PARAMS_276	dddd dddd dddd dddd	0 (0x0000)
R0xF32A	CSS_PARAMS_277	dddd dddd dddd dddd	0 (0x0000)
R0xF32C	CSS_PARAMS_278	dddd dddd dddd dddd	0 (0x0000)
R0xF32E	CSS_PARAMS_279	dddd dddd dddd dddd	0 (0x0000)
R0xF330	CSS_PARAMS_280	dddd dddd dddd dddd	0 (0x0000)
R0xF332	CSS_PARAMS_281	dddd dddd dddd dddd	0 (0x0000)
R0xF334	CSS_PARAMS_282	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF336	CSS_PARAMS_283	dddd dddd dddd dddd	0 (0x0000)
R0xF338	CSS_PARAMS_284	dddd dddd dddd dddd	0 (0x0000)
R0xF33A	CSS_PARAMS_285	dddd dddd dddd dddd	0 (0x0000)
R0xF33C	CSS_PARAMS_286	dddd dddd dddd dddd	0 (0x0000)
R0xF33E	CSS_PARAMS_287	dddd dddd dddd dddd	0 (0x0000)
R0xF340	CSS_PARAMS_288	dddd dddd dddd dddd	0 (0x0000)
R0xF342	CSS_PARAMS_289	dddd dddd dddd dddd	0 (0x0000)
R0xF344	CSS_PARAMS_290	dddd dddd dddd dddd	0 (0x0000)
R0xF346	CSS_PARAMS_291	dddd dddd dddd dddd	0 (0x0000)
R0xF348	CSS_PARAMS_292	dddd dddd dddd dddd	0 (0x0000)
R0xF34A	CSS_PARAMS_293	dddd dddd dddd dddd	0 (0x0000)
R0xF34C	CSS_PARAMS_294	dddd dddd dddd dddd	0 (0x0000)
R0xF34E	CSS_PARAMS_295	dddd dddd dddd dddd	0 (0x0000)
R0xF350	CSS_PARAMS_296	dddd dddd dddd dddd	0 (0x0000)
R0xF352	CSS_PARAMS_297	dddd dddd dddd dddd	0 (0x0000)
R0xF354	CSS_PARAMS_298	dddd dddd dddd dddd	0 (0x0000)
R0xF356	CSS_PARAMS_299	dddd dddd dddd dddd	0 (0x0000)
R0xF358	CSS_PARAMS_300	dddd dddd dddd dddd	0 (0x0000)
R0xF35A	CSS_PARAMS_301	dddd dddd dddd dddd	0 (0x0000)
R0xF35C	CSS_PARAMS_302	dddd dddd dddd dddd	0 (0x0000)
R0xF35E	CSS_PARAMS_303	dddd dddd dddd dddd	0 (0x0000)
R0xF360	CSS_PARAMS_304	dddd dddd dddd dddd	0 (0x0000)
R0xF362	CSS_PARAMS_305	dddd dddd dddd dddd	0 (0x0000)
R0xF364	CSS_PARAMS_306	dddd dddd dddd dddd	0 (0x0000)
R0xF366	CSS_PARAMS_307	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF368	CSS_PARAMS_308	dddd dddd dddd dddd	0 (0x0000)
R0xF36A	CSS_PARAMS_309	dddd dddd dddd dddd	0 (0x0000)
R0xF36C	CSS_PARAMS_310	dddd dddd dddd dddd	0 (0x0000)
R0xF36E	CSS_PARAMS_311	dddd dddd dddd dddd	0 (0x0000)
R0xF370	CSS_PARAMS_312	dddd dddd dddd dddd	0 (0x0000)
R0xF372	CSS_PARAMS_313	dddd dddd dddd dddd	0 (0x0000)
R0xF374	CSS_PARAMS_314	dddd dddd dddd dddd	0 (0x0000)
R0xF376	CSS_PARAMS_315	dddd dddd dddd dddd	0 (0x0000)
R0xF378	CSS_PARAMS_316	dddd dddd dddd dddd	0 (0x0000)
R0xF37A	CSS_PARAMS_317	dddd dddd dddd dddd	0 (0x0000)
R0xF37C	CSS_PARAMS_318	dddd dddd dddd dddd	0 (0x0000)
R0xF37E	CSS_PARAMS_319	dddd dddd dddd dddd	0 (0x0000)
R0xF380	CSS_PARAMS_320	dddd dddd dddd dddd	0 (0x0000)
R0xF382	CSS_PARAMS_321	dddd dddd dddd dddd	0 (0x0000)
R0xF384	CSS_PARAMS_322	dddd dddd dddd dddd	0 (0x0000)
R0xF386	CSS_PARAMS_323	dddd dddd dddd dddd	0 (0x0000)
R0xF388	CSS_PARAMS_324	dddd dddd dddd dddd	0 (0x0000)
R0xF38A	CSS_PARAMS_325	dddd dddd dddd dddd	0 (0x0000)
R0xF38C	CSS_PARAMS_326	dddd dddd dddd dddd	0 (0x0000)
R0xF38E	CSS_PARAMS_327	dddd dddd dddd dddd	0 (0x0000)
R0xF390	CSS_PARAMS_328	dddd dddd dddd dddd	0 (0x0000)
R0xF392	CSS_PARAMS_329	dddd dddd dddd dddd	0 (0x0000)
R0xF394	CSS_PARAMS_330	dddd dddd dddd dddd	0 (0x0000)
R0xF396	CSS_PARAMS_331	dddd dddd dddd dddd	0 (0x0000)
R0xF398	CSS_PARAMS_332	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF39A	CSS_PARAMS_333	dddd dddd dddd dddd	0 (0x0000)
R0xF39C	CSS_PARAMS_334	dddd dddd dddd dddd	0 (0x0000)
R0xF39E	CSS_PARAMS_335	dddd dddd dddd dddd	0 (0x0000)
R0xF3A0	CSS_PARAMS_336	dddd dddd dddd dddd	0 (0x0000)
R0xF3A2	CSS_PARAMS_337	dddd dddd dddd dddd	0 (0x0000)
R0xF3A4	CSS_PARAMS_338	dddd dddd dddd dddd	0 (0x0000)
R0xF3A6	CSS_PARAMS_339	dddd dddd dddd dddd	0 (0x0000)
R0xF3A8	CSS_PARAMS_340	dddd dddd dddd dddd	0 (0x0000)
R0xF3AA	CSS_PARAMS_341	dddd dddd dddd dddd	0 (0x0000)
R0xF3AC	CSS_PARAMS_342	dddd dddd dddd dddd	0 (0x0000)
R0xF3AE	CSS_PARAMS_343	dddd dddd dddd dddd	0 (0x0000)
R0xF3B0	CSS_PARAMS_344	dddd dddd dddd dddd	0 (0x0000)
R0xF3B2	CSS_PARAMS_345	dddd dddd dddd dddd	0 (0x0000)
R0xF3B4	CSS_PARAMS_346	dddd dddd dddd dddd	0 (0x0000)
R0xF3B6	CSS_PARAMS_347	dddd dddd dddd dddd	0 (0x0000)
R0xF3B8	CSS_PARAMS_348	dddd dddd dddd dddd	0 (0x0000)
R0xF3BA	CSS_PARAMS_349	dddd dddd dddd dddd	0 (0x0000)
R0xF3BC	CSS_PARAMS_350	dddd dddd dddd dddd	0 (0x0000)
R0xF3BE	CSS_PARAMS_351	dddd dddd dddd dddd	0 (0x0000)
R0xF3C0	CSS_PARAMS_352	dddd dddd dddd dddd	0 (0x0000)
R0xF3C2	CSS_PARAMS_353	dddd dddd dddd dddd	0 (0x0000)
R0xF3C4	CSS_PARAMS_354	dddd dddd dddd dddd	0 (0x0000)
R0xF3C6	CSS_PARAMS_355	dddd dddd dddd dddd	0 (0x0000)
R0xF3C8	CSS_PARAMS_356	dddd dddd dddd dddd	0 (0x0000)
R0xF3CA	CSS_PARAMS_357	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF3CC	CSS_PARAMS_358	dddd dddd dddd dddd	0 (0x0000)
R0xF3CE	CSS_PARAMS_359	dddd dddd dddd dddd	0 (0x0000)
R0xF3D0	CSS_PARAMS_360	dddd dddd dddd dddd	0 (0x0000)
R0xF3D2	CSS_PARAMS_361	dddd dddd dddd dddd	0 (0x0000)
R0xF3D4	CSS_PARAMS_362	dddd dddd dddd dddd	0 (0x0000)
R0xF3D6	CSS_PARAMS_363	dddd dddd dddd dddd	0 (0x0000)
R0xF3D8	CSS_PARAMS_364	dddd dddd dddd dddd	0 (0x0000)
R0xF3DA	CSS_PARAMS_365	dddd dddd dddd dddd	0 (0x0000)
R0xF3DC	CSS_PARAMS_366	dddd dddd dddd dddd	0 (0x0000)
R0xF3DE	CSS_PARAMS_367	dddd dddd dddd dddd	0 (0x0000)
R0xF3E0	CSS_PARAMS_368	dddd dddd dddd dddd	0 (0x0000)
R0xF3E2	CSS_PARAMS_369	dddd dddd dddd dddd	0 (0x0000)
R0xF3E4	CSS_PARAMS_370	dddd dddd dddd dddd	0 (0x0000)
R0xF3E6	CSS_PARAMS_371	dddd dddd dddd dddd	0 (0x0000)
R0xF3E8	CSS_PARAMS_372	dddd dddd dddd dddd	0 (0x0000)
R0xF3EA	CSS_PARAMS_373	dddd dddd dddd dddd	0 (0x0000)
R0xF3EC	CSS_PARAMS_374	dddd dddd dddd dddd	0 (0x0000)
R0xF3EE	CSS_PARAMS_375	dddd dddd dddd dddd	0 (0x0000)
R0xF3F0	CSS_PARAMS_376	dddd dddd dddd dddd	0 (0x0000)
R0xF3F2	CSS_PARAMS_377	dddd dddd dddd dddd	0 (0x0000)
R0xF3F4	CSS_PARAMS_378	dddd dddd dddd dddd	0 (0x0000)
R0xF3F6	CSS_PARAMS_379	dddd dddd dddd dddd	0 (0x0000)
R0xF3F8	CSS_PARAMS_380	dddd dddd dddd dddd	0 (0x0000)
R0xF3FA	CSS_PARAMS_381	dddd dddd dddd dddd	0 (0x0000)
R0xF3FC	CSS_PARAMS_382	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF3FE	CSS_PARAMS_383	dddd dddd dddd dddd	0 (0x0000)
R0xF400	CSS_PARAMS_384	dddd dddd dddd dddd	0 (0x0000)
R0xF402	CSS_PARAMS_385	dddd dddd dddd dddd	0 (0x0000)
R0xF404	CSS_PARAMS_386	dddd dddd dddd dddd	0 (0x0000)
R0xF406	CSS_PARAMS_387	dddd dddd dddd dddd	0 (0x0000)
R0xF408	CSS_PARAMS_388	dddd dddd dddd dddd	0 (0x0000)
R0xF40A	CSS_PARAMS_389	dddd dddd dddd dddd	0 (0x0000)
R0xF40C	CSS_PARAMS_390	dddd dddd dddd dddd	0 (0x0000)
R0xF40E	CSS_PARAMS_391	dddd dddd dddd dddd	0 (0x0000)
R0xF410	CSS_PARAMS_392	dddd dddd dddd dddd	0 (0x0000)
R0xF412	CSS_PARAMS_393	dddd dddd dddd dddd	0 (0x0000)
R0xF414	CSS_PARAMS_394	dddd dddd dddd dddd	0 (0x0000)
R0xF416	CSS_PARAMS_395	dddd dddd dddd dddd	0 (0x0000)
R0xF418	CSS_PARAMS_396	dddd dddd dddd dddd	0 (0x0000)
R0xF41A	CSS_PARAMS_397	dddd dddd dddd dddd	0 (0x0000)
R0xF41C	CSS_PARAMS_398	dddd dddd dddd dddd	0 (0x0000)
R0xF41E	CSS_PARAMS_399	dddd dddd dddd dddd	0 (0x0000)
R0xF420	CSS_PARAMS_400	dddd dddd dddd dddd	0 (0x0000)
R0xF422	CSS_PARAMS_401	dddd dddd dddd dddd	0 (0x0000)
R0xF424	CSS_PARAMS_402	dddd dddd dddd dddd	0 (0x0000)
R0xF426	CSS_PARAMS_403	dddd dddd dddd dddd	0 (0x0000)
R0xF428	CSS_PARAMS_404	dddd dddd dddd dddd	0 (0x0000)
R0xF42A	CSS_PARAMS_405	dddd dddd dddd dddd	0 (0x0000)
R0xF42C	CSS_PARAMS_406	dddd dddd dddd dddd	0 (0x0000)
R0xF42E	CSS_PARAMS_407	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF430	CSS_PARAMS_408	dddd dddd dddd dddd	0 (0x0000)
R0xF432	CSS_PARAMS_409	dddd dddd dddd dddd	0 (0x0000)
R0xF434	CSS_PARAMS_410	dddd dddd dddd dddd	0 (0x0000)
R0xF436	CSS_PARAMS_411	dddd dddd dddd dddd	0 (0x0000)
R0xF438	CSS_PARAMS_412	dddd dddd dddd dddd	0 (0x0000)
R0xF43A	CSS_PARAMS_413	dddd dddd dddd dddd	0 (0x0000)
R0xF43C	CSS_PARAMS_414	dddd dddd dddd dddd	0 (0x0000)
R0xF43E	CSS_PARAMS_415	dddd dddd dddd dddd	0 (0x0000)
R0xF440	CSS_PARAMS_416	dddd dddd dddd dddd	0 (0x0000)
R0xF442	CSS_PARAMS_417	dddd dddd dddd dddd	0 (0x0000)
R0xF444	CSS_PARAMS_418	dddd dddd dddd dddd	0 (0x0000)
R0xF446	CSS_PARAMS_419	dddd dddd dddd dddd	0 (0x0000)
R0xF448	CSS_PARAMS_420	dddd dddd dddd dddd	0 (0x0000)
R0xF44A	CSS_PARAMS_421	dddd dddd dddd dddd	0 (0x0000)
R0xF44C	CSS_PARAMS_422	dddd dddd dddd dddd	0 (0x0000)
R0xF44E	CSS_PARAMS_423	dddd dddd dddd dddd	0 (0x0000)
R0xF450	CSS_PARAMS_424	dddd dddd dddd dddd	0 (0x0000)
R0xF452	CSS_PARAMS_425	dddd dddd dddd dddd	0 (0x0000)
R0xF454	CSS_PARAMS_426	dddd dddd dddd dddd	0 (0x0000)
R0xF456	CSS_PARAMS_427	dddd dddd dddd dddd	0 (0x0000)
R0xF458	CSS_PARAMS_428	dddd dddd dddd dddd	0 (0x0000)
R0xF45A	CSS_PARAMS_429	dddd dddd dddd dddd	0 (0x0000)
R0xF45C	CSS_PARAMS_430	dddd dddd dddd dddd	0 (0x0000)
R0xF45E	CSS_PARAMS_431	dddd dddd dddd dddd	0 (0x0000)
R0xF460	CSS_PARAMS_432	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF462	CSS_PARAMS_433	dddd dddd dddd dddd	0 (0x0000)
R0xF464	CSS_PARAMS_434	dddd dddd dddd dddd	0 (0x0000)
R0xF466	CSS_PARAMS_435	dddd dddd dddd dddd	0 (0x0000)
R0xF468	CSS_PARAMS_436	dddd dddd dddd dddd	0 (0x0000)
R0xF46A	CSS_PARAMS_437	dddd dddd dddd dddd	0 (0x0000)
R0xF46C	CSS_PARAMS_438	dddd dddd dddd dddd	0 (0x0000)
R0xF46E	CSS_PARAMS_439	dddd dddd dddd dddd	0 (0x0000)
R0xF470	CSS_PARAMS_440	dddd dddd dddd dddd	0 (0x0000)
R0xF472	CSS_PARAMS_441	dddd dddd dddd dddd	0 (0x0000)
R0xF474	CSS_PARAMS_442	dddd dddd dddd dddd	0 (0x0000)
R0xF476	CSS_PARAMS_443	dddd dddd dddd dddd	0 (0x0000)
R0xF478	CSS_PARAMS_444	dddd dddd dddd dddd	0 (0x0000)
R0xF47A	CSS_PARAMS_445	dddd dddd dddd dddd	0 (0x0000)
R0xF47C	CSS_PARAMS_446	dddd dddd dddd dddd	0 (0x0000)
R0xF47E	CSS_PARAMS_447	dddd dddd dddd dddd	0 (0x0000)
R0xF480	CSS_PARAMS_448	dddd dddd dddd dddd	0 (0x0000)
R0xF482	CSS_PARAMS_449	dddd dddd dddd dddd	0 (0x0000)
R0xF484	CSS_PARAMS_450	dddd dddd dddd dddd	0 (0x0000)
R0xF486	CSS_PARAMS_451	dddd dddd dddd dddd	0 (0x0000)
R0xF488	CSS_PARAMS_452	dddd dddd dddd dddd	0 (0x0000)
R0xF48A	CSS_PARAMS_453	dddd dddd dddd dddd	0 (0x0000)
R0xF48C	CSS_PARAMS_454	dddd dddd dddd dddd	0 (0x0000)
R0xF48E	CSS_PARAMS_455	dddd dddd dddd dddd	0 (0x0000)
R0xF490	CSS_PARAMS_456	dddd dddd dddd dddd	0 (0x0000)
R0xF492	CSS_PARAMS_457	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF494	CSS_PARAMS_458	dddd dddd dddd dddd	0 (0x0000)
R0xF496	CSS_PARAMS_459	dddd dddd dddd dddd	0 (0x0000)
R0xF498	CSS_PARAMS_460	dddd dddd dddd dddd	0 (0x0000)
R0xF49A	CSS_PARAMS_461	dddd dddd dddd dddd	0 (0x0000)
R0xF49C	CSS_PARAMS_462	dddd dddd dddd dddd	0 (0x0000)
R0xF49E	CSS_PARAMS_463	dddd dddd dddd dddd	0 (0x0000)
R0xF4A0	CSS_PARAMS_464	dddd dddd dddd dddd	0 (0x0000)
R0xF4A2	CSS_PARAMS_465	dddd dddd dddd dddd	0 (0x0000)
R0xF4A4	CSS_PARAMS_466	dddd dddd dddd dddd	0 (0x0000)
R0xF4A6	CSS_PARAMS_467	dddd dddd dddd dddd	0 (0x0000)
R0xF4A8	CSS_PARAMS_468	dddd dddd dddd dddd	0 (0x0000)
R0xF4AA	CSS_PARAMS_469	dddd dddd dddd dddd	0 (0x0000)
R0xF4AC	CSS_PARAMS_470	dddd dddd dddd dddd	0 (0x0000)
R0xF4AE	CSS_PARAMS_471	dddd dddd dddd dddd	0 (0x0000)
R0xF4B0	CSS_PARAMS_472	dddd dddd dddd dddd	0 (0x0000)
R0xF4B2	CSS_PARAMS_473	dddd dddd dddd dddd	0 (0x0000)
R0xF4B4	CSS_PARAMS_474	dddd dddd dddd dddd	0 (0x0000)
R0xF4B6	CSS_PARAMS_475	dddd dddd dddd dddd	0 (0x0000)
R0xF4B8	CSS_PARAMS_476	dddd dddd dddd dddd	0 (0x0000)
R0xF4BA	CSS_PARAMS_477	dddd dddd dddd dddd	0 (0x0000)
R0xF4BC	CSS_PARAMS_478	dddd dddd dddd dddd	0 (0x0000)
R0xF4BE	CSS_PARAMS_479	dddd dddd dddd dddd	0 (0x0000)
R0xF4C0	CSS_PARAMS_480	dddd dddd dddd dddd	0 (0x0000)
R0xF4C2	CSS_PARAMS_481	dddd dddd dddd dddd	0 (0x0000)
R0xF4C4	CSS_PARAMS_482	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF4C6	CSS_PARAMS_483	dddd dddd dddd dddd	0 (0x0000)
R0xF4C8	CSS_PARAMS_484	dddd dddd dddd dddd	0 (0x0000)
R0xF4CA	CSS_PARAMS_485	dddd dddd dddd dddd	0 (0x0000)
R0xF4CC	CSS_PARAMS_486	dddd dddd dddd dddd	0 (0x0000)
R0xF4CE	CSS_PARAMS_487	dddd dddd dddd dddd	0 (0x0000)
R0xF4D0	CSS_PARAMS_488	dddd dddd dddd dddd	0 (0x0000)
R0xF4D2	CSS_PARAMS_489	dddd dddd dddd dddd	0 (0x0000)
R0xF4D4	CSS_PARAMS_490	dddd dddd dddd dddd	0 (0x0000)
R0xF4D6	CSS_PARAMS_491	dddd dddd dddd dddd	0 (0x0000)
R0xF4D8	CSS_PARAMS_492	dddd dddd dddd dddd	0 (0x0000)
R0xF4DA	CSS_PARAMS_493	dddd dddd dddd dddd	0 (0x0000)
R0xF4DC	CSS_PARAMS_494	dddd dddd dddd dddd	0 (0x0000)
R0xF4DE	CSS_PARAMS_495	dddd dddd dddd dddd	0 (0x0000)
R0xF4E0	CSS_PARAMS_496	dddd dddd dddd dddd	0 (0x0000)
R0xF4E2	CSS_PARAMS_497	dddd dddd dddd dddd	0 (0x0000)
R0xF4E4	CSS_PARAMS_498	dddd dddd dddd dddd	0 (0x0000)
R0xF4E6	CSS_PARAMS_499	dddd dddd dddd dddd	0 (0x0000)
R0xF4E8	CSS_PARAMS_500	dddd dddd dddd dddd	0 (0x0000)
R0xF4EA	CSS_PARAMS_501	dddd dddd dddd dddd	0 (0x0000)
R0xF4EC	CSS_PARAMS_502	dddd dddd dddd dddd	0 (0x0000)
R0xF4EE	CSS_PARAMS_503	dddd dddd dddd dddd	0 (0x0000)
R0xF4F0	CSS_PARAMS_504	dddd dddd dddd dddd	0 (0x0000)
R0xF4F2	CSS_PARAMS_505	dddd dddd dddd dddd	0 (0x0000)
R0xF4F4	CSS_PARAMS_506	dddd dddd dddd dddd	0 (0x0000)
R0xF4F6	CSS_PARAMS_507	dddd dddd dddd dddd	0 (0x0000)

Table 4. MANUFACTURER−SPECIFIC REGISTER LIST

1 = read−only, always 1; 0 = read−only, always 0; d = programmable; ? = read−only, dynamic

Register Hex	Name	Data Format (Binary)	Default Value Dec (Hex)
R0xF4F8	CSS_PARAMS_508	dddd dddd dddd dddd	0 (0x0000)
R0xF4FA	CSS_PARAMS_509	dddd dddd dddd dddd	0 (0x0000)
R0xF4FC	CSS_PARAMS_510	dddd dddd dddd dddd	0 (0x0000)
R0xF4FE	CSS_PARAMS_511	dddd dddd dddd dddd	0 (0x0000)

REGISTER DESCRIPTIONS

Attributes Columns; Usage and Values, left to right

Column 1; Buffering <blank> = Unbuffered S = Single Frame Synced D = Double Frame Synced	Column 2; Bad Frame <blank> = No bad frame Y = Causes a bad frame YM = Maskable bad frame	Column 3; Embedded <blank> = Not embedded E = embedded	Column 4; Locked <blank> = Not locked L = locked

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2000	**15:0**	**0xFFFF**	**FRAME_COUNT2_ (RO)**	**S**		**E**		**unsigned**
	Counts the number of processed frames. At the startup is initialized to 0xFFFF. Upper bits, [31:16]							
R0x2002	**15:0**	**0xFFFF**	**FRAME_COUNT_ (RO)**	**S**		**E**		**unsigned**
	Counts the number of processed frames. At the startup is initialized to 0xFFFF. Lower bits, [15:0]							
R0x2004	**15:0**	**0x0000**	**OTPM_STATUS (RO)**			**E**		**unsigned**
	15:12	RO	SEC_CNT Accumulation of Single Error Correction (SEC) errors for all reads (except invalidation). A SEC error is a single bit error that has been corrected by CRC code. SEC errors are non fatal and provide some status as to the state of the OTPM device. This register is reset at start of a command.			**E**		unsigned
	11	X	Undefined					
	10	RO	OTPM_INSUFFICIENT Insufficient OTPM space to include a record.			**E**		unsigned
	9	X	Undefined					
	8	RO	DED_PARITY_FAILURE Double error-detect parity failure and data is bad.			**E**		unsigned
	7	X	Undefined					
	6:1	RO	Reserved					
	0	RO	OTPM_DONE OTPM Read/Write Operation complete.			**E**		unsigned
	See otpm documentation							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2006	**15:0**	**0x0000**	**GPI_STATUS (RO)**			**E**		**unsigned**
	15:11	X	Undefined					
	10	RO	STANDBY_PIN_STATUS This bit reflects the state of the standby pin function if R0x301a[8] is enabled and one of the GPIO pins is programmed for that function.			**E**		unsigned
	9	RO	TRIGGER_PIN_STATUS This bit reflects the state of the trigger pin function if R0x301a[8] is enabled and one of the GPIO pins is programmed for that function.			**E**		unsigned
	8:7	X	Undefined					
	6	RO	SADDR2_PIN_STATUS This bit reflects the state of the SADDR2 pin.			**E**		unsigned
	5	RO	SADDR1_PIN_STATUS This bit reflects the state of the SADDR1 pin.			**E**		unsigned
	4	RO	SADDR0_PIN_STATUS This bit reflects the state of the SADDR0 pin.			**E**		unsigned
	3	RO	GPIO3_PIN_STATUS This bit reflects the state of the GPIO3 pin if the gpio3 input is not disabled in R0x340a. It shows the value being input or output depending of the gpio3 output enable setting in R0x340a.			**E**		unsigned
	2	RO	GPIO2_PIN_STATUS This bit reflects the state of the GPIO2 pin if the gpio2 input is not disabled in R0x340a. It shows the value being input or output depending of the gpio2 output enable setting in R0x340a.			**E**		unsigned
	1	RO	GPIO1_PIN_STATUS This bit reflects the state of the GPIO1 pin if the gpio1 input is not disabled in R0x340a. It shows the value being input or output depending of the gpio1 output enable setting in R0x340a.			**E**		unsigned
	0	RO	GPIO0_PIN_STATUS This bit reflects the state of the GPIO0 pin if the gpio0 input is not disabled in R0x340a. It shows the value being input or output depending of the gpio0 output enable setting in R0x340a.			**E**		unsigned
	Status of gpi and gpio pins							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2008	**15:0**	**0x0000**	**FRAME_STATUS (RO)**			**E**		**unsigned**
	15:4	X	Undefined					
	3	RO	FRAME_STATUS_PLL_LOCKED This bit indicates that the sensor is in streaming state and the PLL is locked. The sensor is now ready to output frames.			**E**		unsigned
	2	RO	FRAME_STATUS_FRAME_START_DURING_GPH This bit indicates that a new frame started while GROUPED_PARAMETER_HOLD is high. This tells the user if the sensor frame-sync start event has been missed, and therefore gain/integration time changes will take effect with a delayed of 1 frame time.			**E**		unsigned
	1	RO	FRAME_STATUS_STANDBY This bit indicates that the sensor is in standby state. It can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit R0x301A[4].			**E**		unsigned
	0	RO	FRAME_STATUS_FRAMESYNC Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.			**E**		unsigned
	Bitfields associated with frame status							
R0x200A	**15:0**	**0x0000**	**DATAPATH_STATUS (RO)**			**E**		**unsigned**
	15:6	X	Undefined					
	5	RO	Reserved					
	4	RO	Reserved					
	3:2	X	Undefined					
	1	RO	Reserved					
	0	RO	Reserved					
	Status bits associated with the final stages of the output datapath.							
R0x2020	**15:0**	**0x0000**	**EXPOSURE_T1_ROW (RO)**			**E**		**unsigned**
	T1 exposure in number of rows. It does not include sub-row time.							
R0x2022	**15:0**	**0x0000**	**EXPOSURE_T2_ROW (RO)**			**E**		**unsigned**
	T2 exposure in number of rows. It does not include sub-row time.							
R0x2024	**15:0**	**0x0000**	**EXPOSURE_T3_ROW (RO)**			**E**		**unsigned**
	T3 exposure in number of rows. It does not include sub-row time.							
R0x2026	**15:0**	**0x0000**	**EXPOSURE_T4_ROW (RO)**			**E**		**unsigned**
	T4 exposure in number of rows. It does not include sub-row time.							
R0x2028	**10:0**	**0x0000**	**EXPOSURE_T1_CLK_U (RO)**			**E**		**unsigned**
	T1 exposure in number of pixel clocks (upper bits). This value does not include any scaling for the effect of DCG_TRIM.							
R0x202A	**15:0**	**0x0000**	**EXPOSURE_T1_CLK_L (RO)**			**E**		**unsigned**
	T1 exposure in number of pixel clocks (lower bits). This value does not include any scaling for the effect of DCG_TRIM.							
R0x202C	**10:0**	**0x0000**	**EXPOSURE_T2_CLK_U (RO)**			**E**		**unsigned**
	T2 exposure in number of pixel clocks (upper bits). This value does not include any scaling for the effect of DCG_TRIM.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x202E	15:0	0x0000	EXPOSURE_T2_CLK_L (RO)			E		unsigned
	T2 exposure in number of pixel clocks (lower bits). This value does not include any scaling for the effect of DCG_TRIM.							
R0x2030	10:0	0x0000	EXPOSURE_T3_CLK_U (RO)			E		unsigned
	T3 exposure in number of pixel clocks (upper bits). This value does not include any scaling for the effect of DCG_TRIM.							
R0x2032	15:0	0x0000	EXPOSURE_T3_CLK_L (RO)			E		unsigned
	T3 exposure in number of pixel clocks (lower bits). This value does not include any scaling for the effect of DCG_TRIM.							
R0x2034	10:0	0x0000	EXPOSURE_T4_CLK_U (RO)			E		unsigned
	T4 exposure in number of pixel clocks (upper bits). This value does not include any scaling for the effect of DCG_TRIM.							
R0x2036	15:0	0x0000	EXPOSURE_T4_CLK_L (RO)			E		unsigned
	T4 exposure in number of pixel clocks (lower bits). This value does not include any scaling for the effect of DCG_TRIM.							
R0x2040	11:0	0x0020	RATIO_ACTUAL_T1_T2 (RO)			E		unsigned
	Actual T1 to T2 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX12,5 (NNNNNNN.MMMMM).							
R0x2042	11:0	0x0020	RATIO_ACTUAL_T2_T3 (RO)			E		unsigned
	Actual T2 to T3 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX12,5 (NNNNNNN.MMMMM).							
R0x2044	11:0	0x0020	RATIO_ACTUAL_T3_T4 (RO)			E		unsigned
	Actual T3 to T4 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX12,5 (NNNNNNN.MMMMM).							
R0x2046	15:0	0x0400	RATIO_ACTUAL_T2_T1 (RO)			E		unsigned
	Actual T2 to T1 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX16,10 (NNNNNN.MMMMMMMMMM).							
R0x2048	0:0	0x0000	RATIO_ACTUAL_T1_T3_MSB (RO)			E		unsigned
	MSB of 17-bit value for actual T1 to T3 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x204A	15:0	0x0020	RATIO_ACTUAL_T1_T3 (RO)			E		unsigned
	Actual T1 to T3 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x204C	0:0	0x0000	RATIO_ACTUAL_T1_T4_MSB (RO)			E		unsigned
	MSB of 17-bit value for actual T1 to T4 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x204E	15:0	0x0020	RATIO_ACTUAL_T1_T4 (RO)			E		unsigned
	Actual T1 to T4 exposure ratio. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x2050	11:0	0x0020	RATIO_ACTUAL_GAIN1 (RO)			E		unsigned
	Actual Gain 1 Exposure Ratio. 2 exposure mode: (T1+T2)/T2 3 exposure mode: (T1+T2+T3)/(T2+T3) 4 exposure mode: (T1+T2+T3+T4)/(T2+T3+T4). Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX12,5 (NNNNNNN.MMMMM).							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2054	**0:0**	**0x0000**	**RATIO_ACTUAL_GAIN2_MSB (RO)**			**E**		**unsigned**
	MSB of 17-bit value for actual Gain 2 Exposure Ratio. 3 exposure mode: (T1+T2+T3)/(T3) 4 exposure mode: (T1+T2+T3+T4)/(T3+T4). Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x2056	**15:0**	**0x0020**	**RATIO_ACTUAL_GAIN2 (RO)**			**E**		**unsigned**
	Actual Gain 2 Exposure Ratio. 3 exposure mode: (T1+T2+T3)/(T3) 4 exposure mode: (T1+T2+T3+T4)/(T3+T4). Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x2058	**0:0**	**0x0000**	**RATIO_ACTUAL_GAIN3_MSB (RO)**			**E**		**unsigned**
	MSB of 17-bit value for actual Gain 3 Exposure Ratio. 4 exposure mode: (T1+T2+T3+T4)/T4. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x205A	**15:0**	**0x0020**	**RATIO_ACTUAL_GAIN3 (RO)**			**E**		**unsigned**
	Actual Gain 3 Exposure Ratio. 4 exposure mode: (T1+T2+T3+T4)/T4. Any exposures affected by DC_GAIN bits are scaled by DCG_TRIM before calculation of the exposure ratio. Format is UFIX17,5 (NNNNNNNNNNNN.MMMMM).							
R0x205C	**15:0**	**0x140C**	**DATA_FORMAT_ACTUAL (RO)**			**E**		**unsigned**
	15:13	X	Undefined					
	12:8	RO	RAW_SIZE_ACTUAL The actual raw data size in use (different from the programmed value if the programmed value is illegal).	**S**		**E**		unsigned
	7:5	X	Undefined					
	4:0	RO	CCP_SIZE_ACTUAL The actual output (CCP) data size in use (different from the programmed value if the programmed value is illegal).	**S**		**E**		unsigned
	The actual values used for raw and output (CCP) data sizes. In normal operation these will match the values programmed in DATA_FORMAT_BITS (R0x31AC). If an illegal value is programmed,this register shows the actual values in use.							
R0x2060	**15:0**	**0x0000**	**ASIL_STATUS_00 (R/W)**			**E**		**unsigned**
	15	0x0000	ASIL_STATUS_CLK_REG_100_PARAM Status of clk_reg for 100 ext_clk check.			**E**		unsigned
	14	0x0000	ASIL_STATUS_CLK_OP_100_PARAM Status of clk_op for 100 ext_clk check.			**E**		unsigned
	13	0x0000	ASIL_STATUS_EXT_CLK_100_PARAM Status of ext_clk for 100 ext_clk check.			**E**		unsigned
	12	0x0000	ASIL_STATUS_CLK_REG_PARAM Status of clk_reg per frame check.			**E**		unsigned
	11	0x0000	ASIL_STATUS_CLK_OP_PARAM Status of clk_op per frame check.			**E**		unsigned
	10	0x0000	ASIL_STATUS_CLK_PIX_PARAM Status of clk_pix per frame check.			**E**		unsigned
	9	0x0000	ASIL_STATUS_EXT_CLK_PARAM Status of ext_clk per frame check.			**E**		unsigned
	8:1	X	Undefined					
	0	0x0000	Reserved					
	asil_status_00							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2062	**15:0**	**0x0000**	**ASIL_STATUS_01 (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	FAIL_RRC_ADDRESS Status of row ROM column sequence check - the calculated CRC did not match expected value. The CRC accumulation always includes the column address and optionally includes RST_L, DCG and TX* flags (enabled by ATR_CHECK_CONTROL).			**E**		unsigned
	13	0x0000	FAIL_RRC_LEGAL Status of row ROM column legal value check - one or more values was outside the programmed thresholds.			**E**		unsigned
	12	0x0000	FAIL_PT2_THRESHOLD Status of pixout 2 check, one or more pixels were below threshold programmed in ATR_CHECK_PT_HI_THRESH.			**E**		unsigned
	11	0x0000	FAIL_PT1_THRESHOLD Status of pixout 1 check, one or more pixels were above threshold programmed in ATR_CHECK_PT_LO_THRESH.			**E**		unsigned
	10	0x0000	FAIL_ZEBRA_BA_PIXEL_CORRECT Status of zebra BA correct value check, one or more pixels had an incorrect bright or dark value.			**E**		unsigned
	9	0x0000	FAIL_ZEBRA_BA_PIXEL_LEGAL Status of zebra BA legal value check, one or more pixels did not have a legal value.			**E**		unsigned
	8	0x0000	FAIL_ZEBRA_AB_PIXEL_CORRECT Status of zebra AB correct value check, one or more pixels had an incorrect bright or dark value.			**E**		unsigned
	7	0x0000	FAIL_ZEBRA_AB_PIXEL_LEGAL Status of zebra AB legal value check, one or more pixels did not have a legal value.			**E**		unsigned
	6	0x0000	FAIL_OT2_PIXEL_HIGH Status of pixel overdrive 2 high check: one or more pixels is above the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	5	0x0000	FAIL_OT2_PIXEL_LOW Status of pixel overdrive 2 low check: one or more pixels is below the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	4	0x0000	FAIL_OT1_PIXEL_HIGH Status of pixel overdrive 1 high check: one or more pixels is above the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	3	0x0000	FAIL_OT1_PIXEL_LOW Status of pixel overdrive 1 low check: one or more pixels is below the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	2	0x0000	FAIL_MT2 Status of column memory 2 check.			**E**		unsigned
	1	0x0000	FAIL_MT1 Status of column memory 1 check.			**E**		unsigned

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
	0	0x0000	FAIL_CRT Status of column ROM check.			**E**		unsigned
	Each bit of this register is automatically set if a corresponding check enable bit is set and the corresponding check fails during a frame time. See ASIL_CHECK_ENABLES_01 and ASIL_PIN_ENABLES_01.							
R0x2064	**15:0**	**0x0000**	**ASIL_STATUS_02 (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	ROW_FRAME_CRC_STATUS Status of the image row/frame CRC check.			**E**		unsigned
	13	0x0000	DTR_CRC_STATUS Status of the Digital Test Rows (DTR) CRC check.			**E**		unsigned
	12	0x0000	SEQUENCER_ECC_SEC_STATUS Status of the sequencer RAM ECC SEC check. A 1 indicates that the sequencer RAM has observed a single bit error in memory, corrected.			**E**		unsigned
	11	0x0000	SEQUENCER_ECC_DED_STATUS Status of the sequencer RAM DED ECC check. A 1 indicates that the sequencer RAM has observed a double error in memory.			**E**		unsigned
	10	0x0000	SHUTTER_CRC_STATUS Status of the shutter CRC check.			**E**		unsigned
	9	0x0000	TPG_RAM_ECC_DED Reserved. (Current TPG implementation does not contain RAM).			**E**		unsigned
	8:7	X	Undefined					
	6	0x0000	DBLC_FSM_PARITY Status of the DBLC state machine parity check.			**E**		unsigned
	5	0x0000	DBLC_RAM_ECC_SEC_STATUS Status of the DBLC RAM ECC single error correct.			**E**		unsigned
	4	0x0000	DBLC_RAM_ECC_DED_STATUS Status of the DBLC RAM ECC double error detect.			**E**		unsigned
	3:1	X	Undefined					
	0	0x0000	EMBEDDED_CRC_STATUS Status of embedded data CRC check.			**E**		unsigned
	Each bit of this register is automatically set if a corresponding check enable bit is set and the corresponding check fails during a frame time. See ASIL_CHECK_ENABLES_02 and ASIL_PIN_ENABLES_02.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2066	**15:0**	**0x0000**	**ASIL_STATUS_03 (R/W)**			**E**		**unsigned**
	15:8	X	Undefined					
	7	0x0000	SCALER_CRC_FAULT Status of the scaler RAM CRC check. Asserted when a CRC mismatch is detected. Configured by bits in ODP_CRC_FAULT_CONTROL. Error counts are reported in SCALER_CRC_FAULTS_PER_FRAME and SCALER_CRC_FAULT_FRAMES.			**E**		unsigned
	6	0x0000	ODP_BUF_CRC_FAULT Status of the ODP buffer RAM CRC check. Asserted when a CRC mismatch is detected. Configured by bits in ODP_CRC_FAULT_CONTROL. Error counts are reported in ODP_CRC_FAULTS_PER_FRAME and ODP_CRC_FAULT_FRAMES.			**E**		unsigned
	5:1	X	Undefined					
	0	0x0000	DELAY_BUFFER_CRC_FAULT Status of the delay buffer CRC check. Indicates a data or write/read pointer CRC fault has occurred. Configured by bits in DELAY_BUFFER_CRC_FAULT_CONTROL. Error counts are reported in DELAY_BUFFER_CRC_FAULTS_PER_FRAME and DELAY_BUFFER_CRC_FAULT_FRAMES.			**E**		unsigned
	Each bit of this register is automatically set if a corresponding check is enabled and the check fails during a frame time. There is no ASIL_CHECK_ENABLES_03 register or ASIL_PIN_ENABLES_03 register; refer to individual bit-fields for the associated enable bits for each check.							
R0x2068	**15:0**	**0x0000**	**ASIL_STARTUP_STATUS_00 (R/W)**			**E**		**unsigned**
	15:5	X	Undefined					
	4	0x0000	Reserved					
	3	0x0000	PDI_SCAN_STATUS If PDI startup scan has been enabled this shows the status; 0 if the computed value matched the expected value,1 if the computed value did not match the expected value.			**E**		unsigned
	2	0x0000	IREG_SCAN_STATUS If IREG startup scan has been enabled this shows the status; 0 if the computed value matched the expected value,1 if the computed value did not match the expected value.			**E**		unsigned
	1	0x0000	OTPM_SCAN_STATUS If OTPM startup scan has been enabled this shows the status; 0 if the computed value matched the expected value,1 if the computed value did not match the expected value.			**E**		unsigned
	0	0x0000	STARTUP_M3ROM_STATUS If M3ROM startup scan has been enabled this shows the status; 0 if the computed value matched the expected value,1 if the computed value did not match the expected value.			**E**		unsigned
	Collection of ASIL startup status flags.							
R0x206A	**15:0**	**0x0000**	**ATR_CHECK_CRT_CRC_VALUE (R/W)**			**E**		**unsigned**
	Value from CRC calculation from column ROM addresses.							
R0x206C	**15:0**	**0x0000**	**RRC_CHECK_ADDR_CRC_VALUE (R/W)**			**E**		**unsigned**
	Value from CRC calculation from row ROM addresses.							
R0x206E	**15:0**	**0x0000**	**DELAY_BUFFER_CRC_FAULTS_PER_FRAME (R/W)**			**E**		**unsigned**
	Number of delay buffer memories CRC faults in the current frame. Controlled by DELAY_BUFFER_CRC_FAULT_CONTROL (R0x3C0A).							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2070	**15:0**	**0x0000**	**DELAY_BUFFER_CRC_FAULT_FRAMES (R/W)**			**E**		**unsigned**
	Number of frames with delay buffer memories CRC faults. Controlled by DELAY_BUFFER_CRC_FAULT_CONTROL (R0x3C0A).							
R0x2072	**7:0**	**0x0000**	**FUSE_PIXEL_DEFECT_COUNT (RO)**			**E**		**unsigned**
	When enabled (See R0x31E0), this register is updated at the end of each frame to report the number of pixel defects that were tagged/ corrected in the frame. The candidates for correction can be unique per die and are loaded from OTPM after reset. The actual number of pixels corrected is dependent upon the readout mode and the field-of-view. For a particular die, readout mode and field of view, the number reported in this register should remain stable.							
R0x2076	**15:0**	**0x0000**	**ASIL_STATUS_04 (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13	0x0000	CTX_RAM_DED Status of the Context RAM DEC check. Asserted when has observed a double-bit error in memory has been detected.			**E**		unsigned
	12	0x0000	CTX_RAM_SEC Status of the Context RAM SEC check. Asserted when a single bit error in memory has been detected and corrected.			**E**		unsigned
	11:0	X	Undefined					
	ASIL flags for memory ECC.							
R0x207C	**15:0**	**0x0000**	**ASIL_STATUS_07 (R/W)**			**E**		**unsigned**
	15:1	X	Undefined					
	0	0x0000	ASIL_STATUS_LRE_CRC Status of the Line Reorder Engine CRC error check. Write-1-to-clear.			**E**		unsigned
	Each bit of this register is automatically set if a corresponding check enable bit is set and the corresponding check fails during a frame time. See ASIL_CHECK_ENABLES_07 and ASIL_PIN_ENABLES_07.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x207E	**15:0**	**0x0000**	**ASIL_STATUS_08 (R/W)**			**E**		**unsigned**
	15:8	X	Undefined					
	7	0x0000	FAIL_OT4_PIXEL_HIGH Failure of pixel overdrive test 4: one or more pixels is above the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	6	0x0000	FAIL_OT4_PIXEL_LOW Failure of pixel overdrive test 4: one or more pixels is below the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	5	0x0000	FAIL_OT3_PIXEL_HIGH Failure of pixel overdrive test 3: one or more pixels is above the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	4	0x0000	FAIL_OT3_PIXEL_LOW Failure of pixel overdrive test 3: one or more pixels is below the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	3	0x0000	FAIL_OT0_PIXEL_HIGH Failure of pixel overdrive test 0: one or more pixels is above the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	2	0x0000	FAIL_OT0_PIXEL_LOW Failure of pixel overdrive test 0: one or more pixels is below the value expected based on the programming of ATR_CHECK_OT_BASE, ATR_CHECK_OT_LO_OFFSET, ATR_CHECK_OT_HI_OFFSET.			**E**		unsigned
	1	0x0000	FAIL_GT2 Failure of column memory gray transfer test 2: one or more pixels did not match the value in ATR_CHECK_GT_EXPECT2.			**E**		unsigned
	0	0x0000	FAIL_GT1 Failure of column memory gray transfer test 1: one or more pixels did not match the value in ATR_CHECK_GT_EXPECT1.			**E**		unsigned
	Each bit of this register is automatically set if a corresponding check enable bit is set and the corresponding check fails during a frame time. See ASIL_CHECK_ENABLES_08 and ASIL_PIN_ENABLES_08.							
R0x2080	**5:0**	**0x0000**	**ASIL_EXT_CLK_COUNT_MSB (R/W)**			**E**		**unsigned**
	Actual ext_clk count per frame (MSB). When the associated bit in ASIL_CHECK_ENABLES_00 is 1, this counter will be active and will update each frame. The count value is compared against ASIL_EXT_CLK_COUNT_MSB_EXPECT. If the absolute difference is greater than the associated value in ASIL_CLK_COUNT_THRESHOLD (R0x34F2), an error will be flagged in the associated bit in ASIL_STATUS_00. The frame count (and associated _EXPECT) registers are 22-bit values and the count is measured modulo 2^22.							
R0x2082	**15:0**	**0x0000**	**ASIL_EXT_CLK_COUNT_LSB (R/W)**			**E**		**unsigned**
	Actual ext_clk count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x2084	**5:0**	**0x0000**	**ASIL_CLK_PIX_COUNT_MSB (R/W)**			**E**		**unsigned**
	Actual clk_pix count per frame (MSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2086	15:0	0x0000	ASIL_CLK_PIX_COUNT_LSB (R/W)			E		unsigned
	Actual clk_pix count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x2088	5:0	0x0000	ASIL_CLK_OP_COUNT_MSB (R/W)			E		unsigned
	Actual clk_op count per frame (MSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x208A	15:0	0x0000	ASIL_CLK_OP_COUNT_LSB (R/W)			E		unsigned
	Actual clk_op count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x208C	5:0	0x0000	ASIL_CLK_REG_COUNT_MSB (R/W)			E		unsigned
	Actual clk_reg count per frame (MSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x208E	15:0	0x0000	ASIL_CLK_REG_COUNT_LSB (R/W)			E		unsigned
	Actual clk_reg count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x2090	10:0	0x0000	ASIL_CLK_PIX_COUNT_100_EXT (R/W)			E		unsigned
	Actual clk_pix count for 100 ext_clk cycles. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x2092	10:0	0x0000	ASIL_CLK_OP_COUNT_100_EXT (R/W)			E		unsigned
	Actual clk_op count for 100 ext_clk cycles. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x2094	10:0	0x0000	ASIL_CLK_REG_COUNT_100_EXT (R/W)			E		unsigned
	Actual clk_reg count for 100 ext_clk cycles. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x209C	15:0	0x0000	I2C_WRT_COUNT (RO)			E		unsigned
	Each time a data value is applied to I2C_WRT_CHECKSUM (R0x31d6) this register is incremented by 1, modulo 2^16. This register is reset to 0 when I2C_WRT_CHECKSUM is re-initialised.							
R0x20B2	12:0	0x0000	TEMPSENS1_DATA_REG (RO)			E		unsigned
	Raw ADC temperature value from the temperature sensor selected by R0x3FC2.							
R0x20B4	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_0 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 0: Hi-boost TX_HI.							
R0x20B6	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_1 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 1: Hi-boost DCG_HI.							
R0x20B8	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_2 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 2: Hi-boost RST_HI.							
R0x20BA	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_3 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 3: Hi-boost RS_HI.							
R0x20BC	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_4 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 4: Lo-boost RS_LO.							
R0x20BE	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_5 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 5: Lo-boost RST_LO.							
R0x20C0	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_6 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 6: Lo-boost TX_X.							
R0x20C2	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_7 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 7: Lo-boost TX_RO.							
R0x20C4	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_8 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 8: Lo-boost TX_AB.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x20C6	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_9 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 9: Lo-boost SUB_LO.							
R0x20C8	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_10 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 10: Lo-boost DCG_X.							
R0x20CA	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_11 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 11: Lo-boost DCG_RO.							
R0x20CC	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_12 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 12: Med-boost VAAPIX.							
R0x20CE	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_13 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 13: Med-boost VAA.							
R0x20D0	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_14 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 14: Med-boost DVDD1V2_ANA.							
R0x20D2	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_15 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 15: Med-boost DVDD1V2.							
R0x20D4	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_16 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 16: Med-boost VDDIO.							
R0x20D6	15:0	0x0000	TEMPVSENS0_BOOST_MEAS_17 (RO)			E		unsigned
	Raw ADC voltage value from booster monitor at mux_address 17: VBG.							
R0x20EC	15:0	0x0000	TEMPVSENS1_VMON_MEAS_0 (RO)			E		unsigned
	Raw ADC voltage value from voltage monitor. The voltage monitor is enabled and configured by bits in TEMPVSENS1_TMG_CTRL.							
R0x20FE	12:0	0x0000	TEMPSENS1_DATA_K_REG (RO)			E		unsigned
	Temperature (in kelvin) measured on Temperature sensor selected by R0x3FC2. Resolution is in 1/4 kelvin. For example, a value of 1092 (0x444) represents a temperature of 1092/4=273k.							
R0x2150	15:0	0x0000	AE_MEAN_H (RO)					unsigned
	ROI-1: Return the true mean of all pixels of selected color (Higher bits). The value is updated at the end of every frame.							
R0x2152	15:0	0x0000	AE_MEAN_L (RO)					unsigned
	ROI-1: Return the true mean of all pixels of selected color (Lower bits). The value is updated at the end of every frame.							
R0x2154	15:0	0x0000	AE_HIST_BEGIN_H (RO)					unsigned
	ROI-1: Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (higher bits). The value is updated at the end of every frame.							
R0x2156	15:0	0x0000	AE_HIST_BEGIN_L (RO)					unsigned
	ROI-1: Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (lower bits). The value is updated at the end of every frame.							
R0x2158	15:0	0x0000	AE_HIST_END_H (RO)					unsigned
	ROI-1: Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (higher bits). The value is updated at the end of every frame.							
R0x215A	15:0	0x0000	AE_HIST_END_L (RO)					unsigned
	ROI-1: Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (lower 16 bits). The value is updated at the end of every frame.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x215C	15:0	0x0000	AE_LOW_END_MEAN_H (RO)					unsigned
	ROI-1: The true mean of all pixels of selected color in the ROI that fall into the low end of the histogram (where low end is defined by hist_div). (Higher bits). The value is updated at the end of every frame.							
R0x215E	15:0	0x0000	AE_LOW_END_MEAN_L (RO)					unsigned
	ROI-1: The true mean of all pixels of selected color in the ROI that fall into the low end of the histogram (where low end is defined by hist_div). (Lower 16 bits). The value is updated at the end of every frame.							
R0x2160	15:0	0x0000	AE_PERC_LOW_END (RO)					unsigned
	ROI-1: Percentage of pixels of selected color in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx. The value is updated at the end of every frame.							
R0x2162	15:0	0x0000	AE_NORM_ABS_DEV (RO)					unsigned
	ROI-1: Percentage of pixels of selected color in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx. The value is updated at the end of every frame.							
R0x2250	15:0	0x0000	AE_MEAN2_H (RO)					unsigned
	ROI-2: Return the true mean of all pixels of selected color (Higher bits). The value is updated at the end of every frame.							
R0x2252	15:0	0x0000	AE_MEAN2_L (RO)					unsigned
	ROI-2: Return the true mean of all pixels of selected color (Lower bits). The value is updated at the end of every frame.							
R0x2254	15:0	0x0000	AE_HIST2_BEGIN_H (RO)					unsigned
	ROI-2: Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (higher bits). The value is updated at the end of every frame.							
R0x2256	15:0	0x0000	AE_HIST2_BEGIN_L (RO)					unsigned
	ROI-2: Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (lower bits). The value is updated at the end of every frame.							
R0x2258	15:0	0x0000	AE_HIST2_END_H (RO)					unsigned
	ROI-2: Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (higher bits). The value is updated at the end of every frame.							
R0x225A	15:0	0x0000	AE_HIST2_END_L (RO)					unsigned
	ROI-2: Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (lower 16 bits). The value is updated at the end of every frame.							
R0x225C	15:0	0x0000	AE_LOW2_END_MEAN_H (RO)					unsigned
	ROI-2: The true mean of all pixels of selected color in the ROI that fall into the low end of the histogram (where low end is defined by hist_div). (Higher bits). The value is updated at the end of every frame.							
R0x225E	15:0	0x0000	AE_LOW2_END_MEAN_L (RO)					unsigned
	ROI-2: The true mean of all pixels of selected color in the ROI that fall into the low end of the histogram (where low end is defined by hist_div). (Lower 16 bits). The value is updated at the end of every frame.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2260	15:0	0x0000	AE_PERC2_LOW_END (RO)					unsigned
	ROI-2: Percentage of pixels of selected color in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx. The value is updated at the end of every frame.							
R0x2262	15:0	0x0000	AE_NORM2_ABS_DEV (RO)					unsigned
	ROI-2: Percentage of pixels of selected color in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx. The value is updated at the end of every frame.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x226E	**15:0**	**0x0000**	**AE_STATS_STATUS (RO)**					**unsigned**
	15:14	RO	Y_GRID_STATUS Number of regions in y-direction: 00: 1 region. 01: 2 regions. 10: 3 regions. 11: 4 regions.					unsigned
	13:12	RO	X_GRID_STATUS Number of regions in x-direction: 00: 1 region. 01: 2 regions. 10: 3 regions. 11: 4 regions.					unsigned
	11	RO	ROI3_STATS_DATA_VALID ROI-Stats data is valid and useable.					unsigned
	10	RO	ROI3_ROW_TYPE_EXP_INVALID Did not observe the selected row-type/exp-type in pixel data stream.					unsigned
	9	RO	ROI3_ROI_OUT_OF_BOUNDS Either (x-roi-size > x-actual-size) or (y-roi-size > y-actual-size). The stats module does not collect data for the exact configured ROI.					unsigned
	8	RO	ROI3_ROI_OFF_OUT_OF_IMG_WIN Either (x-roi-offset > x-actual-size) or (y-roi-offset > y-actual-size). The stats module collects no data. Stats data will be set to all zeros.					unsigned
	7	RO	ROI2_STATS_DATA_VALID ROI-Stats data is valid and useable.					unsigned
	6	RO	ROI2_ROW_TYPE_EXP_INVALID Did not observe the selected row-type/exp-type in pixel data stream.					unsigned
	5	RO	ROI2_ROI_OUT_OF_BOUNDS Either (x-roi-size > x-actual-size) or (y-roi-size > y-actual-size). The stats module does not collect data for the exact configured ROI.					unsigned
	4	RO	ROI2_ROI_OFF_OUT_OF_IMG_WIN Either (x-roi-offset > x-actual-size) or (y-roi-offset > y-actual-size). The stats module collects no data. Stats data will be set to all zeros.					unsigned
	3	RO	ROI1_STATS_DATA_VALID ROI-Stats data is valid and useable.					unsigned
	2	RO	ROI1_ROW_TYPE_EXP_INVALID Did not observe the selected row-type/exp-type in pixel data stream.					unsigned
	1	RO	ROI1_ROI_OUT_OF_BOUNDS Either (x-roi-size > x-actual-size) or (y-roi-size > y-actual-size). The stats module does not collect data for the exact configured ROI.					unsigned
	0	RO	ROI1_ROI_OFF_OUT_OF_IMG_WIN Either (x-roi-offset > x-actual-size) or (y-roi-offset > y-actual-size). The stats module collects no data. Stats data will be set to all zeros.					unsigned
	Flags that determine the status of the statistics modules and the correctness of their configuration.							
R0x2280	**15:0**	**0x0000**	**AE_X0_Y0_MEAN_H (RO)**					**unsigned**
	Stats mean for Grid ROI 0 (higher bits)							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2282	15:0	0x0000	AE_X0_Y0_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 0 (lower bits)							
R0x2284	15:0	0x0000	AE_X0_Y1_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 1 (higher bits)							
R0x2286	15:0	0x0000	AE_X0_Y1_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 1 (lower bits)							
R0x2288	15:0	0x0000	AE_X0_Y2_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 2 (higher bits)							
R0x228A	15:0	0x0000	AE_X0_Y2_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 2 (lower bits)							
R0x228C	15:0	0x0000	AE_X0_Y3_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 3 (higher bits)							
R0x228E	15:0	0x0000	AE_X0_Y3_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 3 (lower bits)							
R0x22A0	15:0	0x0000	AE_X1_Y0_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 4 (higher bits)							
R0x22A2	15:0	0x0000	AE_X1_Y0_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 4 (lower bits)							
R0x22A4	15:0	0x0000	AE_X1_Y1_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 5 (higher bits)							
R0x22A6	15:0	0x0000	AE_X1_Y1_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 5 (lower bits)							
R0x22A8	15:0	0x0000	AE_X1_Y2_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 6 (higher bits)							
R0x22AA	15:0	0x0000	AE_X1_Y2_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 6 (lower bits)							
R0x22AC	15:0	0x0000	AE_X1_Y3_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 7 (higher bits)							
R0x22AE	15:0	0x0000	AE_X1_Y3_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 7 (lower bits)							
R0x22B0	15:0	0x0000	AE_X2_Y0_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 8 (higher bits)							
R0x22B2	15:0	0x0000	AE_X2_Y0_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 8 (lower bits)							
R0x22B4	15:0	0x0000	AE_X2_Y1_MEAN_H (RO)					unsigned
	Stats mean for Grid ROI 9 (higher bits)							
R0x22B6	15:0	0x0000	AE_X2_Y1_MEAN_L (RO)					unsigned
	Stats mean for Grid ROI 9 (lower bits)							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x22B8	**15:0**	**0x0000**	**AE_X2_Y2_MEAN_H (RO)**					**unsigned**
	Stats mean for Grid ROI 10 (higher bits)							
R0x22BA	**15:0**	**0x0000**	**AE_X2_Y2_MEAN_L (RO)**					**unsigned**
	Stats mean for Grid ROI 10 (lower bits)							
R0x22BC	**15:0**	**0x0000**	**AE_X2_Y3_MEAN_H (RO)**					**unsigned**
	Stats mean for Grid ROI 11 (higher bits)							
R0x22BE	**15:0**	**0x0000**	**AE_X2_Y3_MEAN_L (RO)**					**unsigned**
	Stats mean for Grid ROI 11 (lower bits)							
R0x22C0	**15:0**	**0x0000**	**AE_X3_Y0_MEAN_H (RO)**					**unsigned**
	Stats mean for Grid ROI 12 (higher bits)							
R0x22C2	**15:0**	**0x0000**	**AE_X3_Y0_MEAN_L (RO)**					**unsigned**
	Stats mean for Grid ROI 12 (lower bits)							
R0x22C4	**15:0**	**0x0000**	**AE_X3_Y1_MEAN_H (RO)**					**unsigned**
	Stats mean for Grid ROI 13 (higher bits)							
R0x22C6	**15:0**	**0x0000**	**AE_X3_Y1_MEAN_L (RO)**					**unsigned**
	Stats mean for Grid ROI 13 (lower bits)							
R0x22C8	**15:0**	**0x0000**	**AE_X3_Y2_MEAN_H (RO)**					**unsigned**
	Stats mean for Grid ROI 14 (higher bits)							
R0x22CA	**15:0**	**0x0000**	**AE_X3_Y2_MEAN_L (RO)**					**unsigned**
	Stats mean for Grid ROI 14 (lower bits)							
R0x22CC	**15:0**	**0x0000**	**AE_X3_Y3_MEAN_H (RO)**					**unsigned**
	Stats mean for Grid ROI 15 (higher bits)							
R0x22CE	**15:0**	**0x0000**	**AE_X3_Y3_MEAN_L (RO)**					**unsigned**
	Stats mean for Grid ROI 15 (lower bits)							
R0x22F6	**15:0**	**0x0000**	**AE_MEAN3_H (RO)**					**unsigned**
	ROI-3: Return the true mean of all pixels of particular color (Higher bits). The value is updated at the end of every frame.							
R0x22F8	**15:0**	**0x0000**	**AE_MEAN3_L (RO)**					**unsigned**
	ROI-3: Return the true mean of all pixels of particular color (Lower bits). The value is updated at the end of every frame.							
R0x22FA	**15:0**	**0x0000**	**AE_HIST3_BEGIN_H (RO)**					**unsigned**
	ROI-3: Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (higher bits). The value is updated at the end of every frame.							
R0x22FC	**15:0**	**0x0000**	**AE_HIST3_BEGIN_L (RO)**					**unsigned**
	ROI-3: Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (lower bits). The value is updated at the end of every frame.							
R0x22FE	**15:0**	**0x0000**	**AE_HIST3_END_H (RO)**					**unsigned**
	ROI-3: Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (higher bits). The value is updated at the end of every frame.							

Table 5. MANUFACTURER−SPECIFIC 2 REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x2500	**15:0**	**0x0000**	**CTX_RD_DATA_REG (RO)**					**unsigned**
	Read from next address in context RAM and increment address. The address is reset by any write to CTX_CONTROL_REG (R0x3034). In order to read the context RAM using this register, start an I2C read from this register and continue with no STOP until all of the data has been read. An alternative way to read the context RAM is to use CTX_CONTROL_REG.CTX_I2C_ADDR_SEL to map the context RAM into the address space.							
R0x2510	**15:0**	**0x0000**	**SEQ_DATA_PORT (R/W)**					**unsigned**
	Register used for read/write access to the sequencer RAM. The sequencer RAM can only be accessed when the sequencer is stopped (i.e. when the sensor is in standby).							
R0x2512	**15:0**	**0x8000**	**SEQ_CTRL_PORT (R/W)**					**unsigned**
	15	RO	SEQUENCER_STOPPED Status for sequencer state. 1: Sequencer stopped 0: Sequencer running					unsigned
	14	0x0000	AUTO_INC_ON_READ Auto-increment address on read (from SEQ_DATA_PORT).					unsigned
	13	0x0000	SEQ_ECC_BYPASS Disable ECC generation during writes to sequencer memory. Provided as a simple mechanism to demostrate that the ECC generation and error-flagging is functioning correctly.					unsigned
	12:10	X	Undefined					
	9:0	0x0000	ACCESS_ADDR Sequencer memory address to access, write or read.					unsigned
	Control and status for read and write to sequencer RAM.							
R0x2F0A	**15:0**	**0x0000**	**AE_HIST3_END_L (RO)**					**unsigned**
	ROI-3: Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (lower 16 bits). The value is updated at the end of every frame.							
R0x2F0C	**15:0**	**0x0000**	**AE_LOW3_END_MEAN_H (RO)**					**unsigned**
	ROI-3: The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div). (Higher bits). The value is updated at the end of every frame.							
R0x2F0E	**15:0**	**0x0000**	**AE_LOW3_END_MEAN_L (RO)**					**unsigned**
	ROI-3: The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div). (Lower 16 bits). The value is updated at the end of every frame.							
R0x2F36	**7:0**	**0x0013**	**TEMPSENS_CLK_DIV (R/W)**			**E**		**unsigned**
	Clock divider for temperature sensor. A programmed value of N gives a clock frequency of clk_pix/(N+1). Values of N from 1-255 are legal.							
R0x2F48	**15:0**	**0x0000**	**AE_PERC3_LOW_END (RO)**					**unsigned**
	ROI-3: Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx. The value is updated at the end of every frame.							
R0x2F4E	**15:0**	**0x0000**	**AE_NORM3_ABS_DEV (RO)**					**unsigned**
	ROI-3: Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx. The value is updated at the end of every frame.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3000	15:0	0x1557	CHIP_VERSION_REG (RO)			E		unsigned
	Model ID.							
R0x3002	11:0	0x0000	Y_ADDR_START_ (R/W)	S		E		unsigned
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. This value must be a multiple of 8 (bits [2:0] must be 0)							
R0x3004	12:0	0x0000	X_ADDR_START_ (R/W)	S		E		unsigned
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. This value must be a multiple of 4 (bits [1:0] must be 0)							
R0x3006	11:0	0x0877	Y_ADDR_END_ (R/W)	S		E		unsigned
	The last row of visible pixels to be read out. The row region defined by Y_ADDR_START_, Y_ADDR_END_ must be a multiple of 8.							
R0x3008	12:0	0x0F07	X_ADDR_END_ (R/W)	S		E		unsigned
	The last column of visible pixels to be read out. The row region defined by X_ADDR_START_, X_ADDR_END_ must be a multiple of 4.							
R0x300A	15:0	0x0970	FRAME_LENGTH_LINES_ (R/W)	S		E		unsigned
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. Must be a multiple of 8 for correct operation.							
R0x300C	15:0	0x0434	LINE_LENGTH_PCK_ (R/W)	S		E		unsigned
	Controls the number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. The line time is given by ROPS*(NUM_EXP_MAX + 1)*LINE_LENGTH_PCK_. ROPS=2 when READ_MODE2 selects 3csum_ana or mono_ana, 4 otherwise. NUM_EXP_MAX is 0, 1, 2 or 3. LINE_LENGTH_PCK must be a multiple of 8 for correct operation.							
R0x300E	15:0	0x3126	REVISION_NUMBER (RO)			E		unsigned
	Revision number. See Developer's Guide for description. Example shown here is for AR0825AT3B18.							
R0x3010	15:0	0xBEEF	LOCK_CONTROL (R/W)			E		unsigned
	This register protects the mirror mode select (register READ_MODE). When set to value 0xBEEF, the horizontal and vertical mirror modes can be changed, otherwise these values are locked.							
R0x3012	15:0	0x0010	COARSE_INTEGRATION_TIME_ (R/W)	S		E		unsigned
	Integration time for T1. Coarse integration times are specified in multiples of ROPS*(NUM_EXP_MAX + 1)*LINE_LENGTH_PCK_. ROPS=2 when READ_MODE2 selects mono_ana, 4 otherwise. NUM_EXP_MAX is 0, 1, 2 or 3.							
R0x3014	15:0	0x0000	FINE_INTEGRATION_TIME_ (R/W)	S		E		unsigned
	Fine integration is used to delay the shutter (reset) operation so that the integration time is decreased. The resolution is 2 pixel clock time. Legal values are 0-15. Use of illegal values will disrupt normal operation of the sensor. The value programmed here affects all exposures (T1 - T4). The recommended value for this register is 0, which results in an actual fine integration time of 328 clk_pix cycles regardless of context and/or readout mode.							
R0x3016	15:0	0x0012	COARSE_INTEGRATION_TIME_CB (R/W)	S		E		unsigned
	Context B integration time for T1 exposure. See description of COARSE_INTEGRATION_TIME_ (R0x3012).							
	15:0	0x0058	RESET_REGISTER (R/W)			E		unsigned

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x301A	15	0x0000	RESET_REGISTER_GROUPED_PARAMETER_HOLD 0: Update of many of the registers is synchronized to frame start. 1: Inhibit register updates. Register changes will remain pending until this bit is returned to 0. When this bit is returned to 0, all pending register updates will be made on the next frame start. This bit cannot be used in conjunction with RAM-based context-switching because setting it also inhibits register updates from the context RAM.			**E**		unsigned
	14	X	Undefined					
	13	0x0000	RESET_LPF_ENABLE Enables a glitch filter for the RESET_BAR pin. 0: Reset LPF Disabled. 1: Reset LPF Enabled.			**E**		unsigned
	12	0x0000	RESET_REGISTER_SMIA_SERIALISER_DIS 0: Serial pixel data interface Enabled. 1: Serial pixel data interface Disabled.			**E**		unsigned
	11	0x0000	FORCED_PLL_ON 0: PLL will be powered down when the sensor is in standby (low power mode). 1: PLL will be enabled even when the sensor is in "standby."			**E**		unsigned
	10	0x0000	RESET_REGISTER_RESTART_BAD 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.			**E**		unsigned
	9	0x0000	RESET_REGISTER_MASK_BAD 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.			**E**		unsigned
	8	0x0000	RESET_REGISTER_GPI_EN 0: the GPIO input functions TRIGGER, and STANDBY are disabled. 1: the input functions are enabled. The GPIO pins must also be configured to map the input function(s) onto a particular GPIO pin(s) and to enable the respective pin(s) input buffer.			**E**		unsigned
	7:5	X	Undefined					
	4	0x0001	RESET_REGISTER_STANDBY_EOF 0 = Transition to standby is synchronized to the end of a sensor row readout (held-off until LINE_VALID has fallen). 1 = Transition to standby is synchronized to the end of a frame. ASIL implications: transition to standby at the end of a sensor row readout can truncate the current frame. This will cause frame-based ASIL checks to fail (including but not limited to the clocks-per-frame safety mechanisms).			**E**		unsigned
	3	0x0001	RESET_REGISTER_LOCK_REG Many parameter limit registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.			**E**		unsigned

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
	2	0x0000	RESET_REGISTER_STREAM 1: Places the sensor in streaming mode. 0: Places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.			**E**		unsigned
	1	0x0000	RESET_REGISTER_RESTART This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time. ASIL implications: truncating the current frame will cause frame-based ASIL checks to fail (including but not limited to the clocks-per-frame safety mechanisms).			**E**		unsigned
	0	0x0000	RESET_REGISTER_RESET This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.			**E**		unsigned
	Controls the operation of the sensor. For details see the bit field descriptions.							
R0x301C	**0:0**	**0x00**	**MODE_SELECT_ (R/W)**			**E**		**unsigned**
	This register is an alias of reset_register[2].							
R0x301D	**1:0**	**0x00**	**IMAGE_ORIENTATION_ (R/W)**			**E**		**unsigned**
	This register is an alias of read_mode[15:14].							
R0x301E	**15:0**	**0x00A8**	**DATA_PEDESTAL_ (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	DISABLE_DBLC_DATA_PEDESTAL When the bit is set, the data pedestal is disabled on the DBLC rows and ODC columns.			**E**		unsigned
	13	0x0000	PEDESTAL_ATR When enabled the data_pedestal is applied to the ATR rows.			**E**		unsigned
	12	0x0000	DISABLE_ACTIVE_DATA_PEDESTAL When enabled the data_pedestal is not applied to the imaging pixels.			**E**		unsigned
	11:0	0x00A8	DATA_PEDESTAL Constant offset that is added to pixel values at the end of datapath (after all corrections).			**E**		unsigned
	Constant offset that is added to pixel values at the end of datapath (after all corrections).							
R0x3021	**0:0**	**0x00**	**SOFTWARE_RESET_ (R/W)**			**E**		**unsigned**
	This register is an alias of RESET_REGISTER[0].							
R0x3022	**0:0**	**0x00**	**GROUPED_PARAMETER_HOLD_ (R/W)**			**E**		**unsigned**
	This register is an alias of RESET_REGISTER[15].							
R0x3023	**0:0**	**0x00**	**MASK_CORRUPTED_FRAMES_ (R/W)**			**E**		**unsigned**
	This register is an alias of RESET_REGISTER[9].							
R0x302A	**15:0**	**0x0006**	**VT_PIX_CLK_DIV (R/W)**			**E**		**unsigned**
	Set the ratio of the serial output clock and sensor operation clock (P2 clock divider in PLL). Legal values: [2-16]							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x302C	**15:0**	**0x0701**	**VT_SYS_CLK_DIV (R/W)**			**E**		**unsigned**
	15:5	X	Undefined					
	4:0	0x0001	VT_SYS_CLK_DIVIDER Set the ratio of the VCO clk and the serial output clock (P1 divider in PLL).			**E**		unsigned
	Sets the ratio of the VCO clk and the serial output clock (P1 divider in PLL). Legal values: [1,2,4,8]							
R0x302E	**15:0**	**0x0009**	**PRE_PLL_CLK_DIV (R/W)**			**E**		**unsigned**
	PLL input pre-divider value.							
R0x3030	**15:0**	**0x00E0**	**PLL_MULTIPLIER (R/W)**			**E**		**unsigned**
	PLL multiplier.							
R0x3032	**15:0**	**0x0000**	**SCALING_MODE (R/W)**			**E**		**unsigned**
	15:6	X	Undefined					
	5:4	0x0000	SCALING_CB 0: Disable scaler 2: Enable horizontal and vertical scaling. Other values are Reserved.			**E**		unsigned
	3:2	X	Undefined					
	1:0	0x0000	SCALING 0: Disable scaler 2: Enable horizontal and vertical scaling. Other values are Reserved.			**E**		unsigned
	Scaler control for Context A and Context B.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3034	**15:0**	**0x0800**	**CTX_CONTROL_REG (R/W)**			**E**		**unsigned**
	15	0x0000	CONTEXT_LOAD Load context immediately: context 0 (if CONTEXT_MULTI=1) or CONTEXT_SELECT (if CONTEXT_MULTI=0). This bit self-clears and so will always read as 0.			**E**		unsigned
	14:12	X	Undefined					
	11	0x0001	CTX_I2C_ADDR_SEL 0: The context RAM can only be accessed indirectly, using CTX_RD_DATA_REG (R0x2500) and CTX_WR_DATA_REG (R0x3066). 1: The context RAM can only be accessed directly, using the address range R0x3A00 - R0x3BFF.			**E**		unsigned
	10	0x0000	I2C_AUTO_INC_DISABLE Disable auto increment of addresses during I2C access. This is a test function.			**E**		unsigned
	9	0x0000	CONTEXT_MULTI_CYCLE_MODE Repeat multiple context readout.			**E**		unsigned
	8	0x0000	CONTEXT_MULTI_SYNC_MODE 1: The next context is loaded at the start of frame readout, 0: The next context is loaded at the start of frame integration. Ignored when CONTEXT_MULTI=0. For correct operation of frame-by-frame context switching this bit should always be set to 1.			**E**		unsigned
	7	0x0000	CONTEXT_MULTI Enable Multiple contexts to be read out. When CONTEXT_MULTI_CYCLE_MODE=0, load context 0 through CONTEXT_MULTI_NUM then clear CONTEXT_MULTI=0 and stop. When CONTEXT_MULTI_CYCLE_MODE=1, do not stop but repeat the context sequence forever. When this bit is cleared, any context load in progress will be completed. Each time this bit is set, context loading restarts at context 0.			**E**		unsigned
	6:4	0x0000	CONTEXT_MULTI_NUM Total number of (consecutive) contexts to read out when CONTEXT_MULTI=1.			**E**		unsigned
	3:0	0x0000	CONTEXT_SELECT When CONTEXT_MULTI=0, this field defines the context that will be loaded when CONTEXT_LOAD is set.			**E**		unsigned
	The programmable context engine allows a set of different contexts to be stored in on-chip RAM. A context is defined by a set of register writes. Any arbitrary set of registers can be used, but each context must supply a value for each of the registers in the set. The context RAM uses a record-based format (refer to the Developer Guide for details). When sequencing through multiple contexts (CONTEXT_MULTI=1) the load of the next context is synchronised to the start of readout or the start or integration. Set CONTEXT_LOAD=1 and CONTEXT_MULTI=1 to load the first context immediately.							
R0x3036	**15:0**	**0x000C**	**OP_WORD_CLK_DIV (R/W)**			**E**		**unsigned**
	Clock divisor applied to the output system clock to generate the output pixel clock. Legal values: [2-16]							
R0x3038	**15:0**	**0x0001**	**OP_SYS_CLK_DIV (R/W)**			**E**		**unsigned**
	Clock divisor applied to PLL output clock to generate output system clock. Legal values: [1,2,4,8]							
R0x303A	**11:0**	**0x0086**	**PLL_MULTIPLIER_ANA (R/W)**			**E**		**unsigned**
	pll_multiplier for PLL in analog core							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x303C	**15:0**	**0x0003**	**PRE_PLL_CLK_DIV_ANA (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13:12	0x0000	PLLANA_DIV_VCO VCO divider setting for PLL in analog core. 2'b00: divide-by-1 2'b01: divide-by-2 2'b10: divide-by-4 2'b11: divide-by-8.			**E**		unsigned
	11:10	X	Undefined					
	9:8	0x0000	PLLANA_P3 P3 divider setting for PLL in analog core. 2'b00: divide-by-1 2'b01: divide-by-2 2'b10: divide-by-4 2'b11: divide-by-8.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0003	PLLANA_N pre_pll_clk_div for PLL in analog core			**E**		unsigned
	contains bitfields for different digital functions							
R0x303E	**15:0**	**0x0434**	**LINE_LENGTH_PCK_CB (R/W)**			**E**		**unsigned**
	Line length in Context B. For correct operation of A/B context switching this must have the same value as LINE_LENGTH_PCK_ (R0x300C) and therefore must be a multiple of 8.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3040	**15:0**	**0x0000**	**READ_MODE (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	READ_MODE_VERT_FLIP 0: Normal readout. 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first. This register can only be changed when streaming is disabled.	**S**		**E**		unsigned
	14	0x0000	READ_MODE_HORIZ_MIRROR 0: Normal readout. 1: Readout is mirrored horizontally so that the column specified by x_addr_end_ (+1) is read out of the sensor first. This register can only be changed when streaming is disabled.	**S**		**E**		unsigned
	13:5	X	Undefined					
	4	0x0000	Reserved					
	3:2	0x0000	EMBED_ROWS_NR Number of embedded data rows. 00: 2 rows. 01: 4 rows. 10: 8 rows. 11: 16 rows. The number of embedded data rows required depends upon the width of the output image. Bits in R0x3064 control whether embedded data rows are transmitted as part of the output image.			**E**		unsigned
	1:0	0x0000	STATS_ROWS_NR Number of embedded statistics rows. 00: 2 rows. 01: 4 rows. 10: Reserved. 11: Reserved. Bits in R0x3064 control whether embedded statistics rows are transmitted as part of the output image. The embedded statistics rows are arranged as follows: Row1: ROI1 Row2: ROI2 Row3: ROI3 Row4: Grid statistics, DBLC and Statistics registers.			**E**		unsigned
	read mode control register							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3044	**15:0**	**0x0400**	**DARK_CONTROL (R/W)**	**S**		**E**		**unsigned**
	15:14	X	Undefined					
	13	0x0000	DARK_CONTROL_SHOW_DTR_ROWS If set the digital test rows (DTR) will be included in the output. PROCESS_DTR (R0x3F70) controls the processing that is applied to the DTR data.	**S**		**E**		unsigned
	12	0x0000	DARK_CONTROL_SHOW_ATR_ROWS If set the analog test rows (ATR) will be output. No correction will be applied to the data.	**S**		**E**		unsigned
	11	0x0000	DARK_CONTROL_SHOW_DARK_EXTRA_ROWS 1: The delta dark rows (including guard rows) will be included in FV and output. Row noise correction and dblc_pedestal will be applied to the data. By default the guard rows will be turned into padding data. See DISABLE_BORDER_PADDING (bit 7).	**S**		**E**		unsigned
	10	0x0001	DARK_CONTROL_ROW_NOISE_CORRECTION_EN 0: Row-noise correction (RNC) algorithm is disabled. 1: Row-noise correction algorithm is enabled.	**S**		**E**		unsigned
	9:8	0x0000	DARK_CONTROL_SHOW_DARK_COLS 00: No dark columns or row ROM columns (RRC) are included in the LV output. 01: Row ROM columns (RRC) are included in the LV and output. 10: Dark columns (tied) used for row noise correction and row ROM columns (RRC) are included in the LV and output. 11: RESERVED.	**S**		**E**		unsigned
	7	0x0000	DARK_CONTROL_DISABLE_BORDER_PADDING 1: Border Rows are not padded with fixed value. 0: Border Rows are padded with fixed value.	**S**		**E**		unsigned
	6	0x0000	Reserved					
	5:2	X	Undefined					
	1	0x0000	DARK_CONTROL_SHOW_OVERSCAN_ROWS If set the overscan rows (rows above and below the active region) will be included in the output.	**S**		**E**		unsigned
	0	0x0000	Reserved					
	dark algorithm and display control							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3046	**15:0**	**0x0000**	**FLASH (R/W)**	**S**		**E**		**unsigned**
	15:9	X	Undefined					
	8	0x0000	Reserved					
	7	0x0000	INVERT_FLASH Invert polarity of FLASH output. 0: FLASH is low when idle, high when active. 1: FLASH is high when idle, low when active.			**E**		unsigned
	6	X	Undefined					
	5:3	0x0000	XENON_FRAMES_ENABLE 0: Xenon flash disabled. 1-6: Number of frames with Xenon flash. 7: Xenon flash enabled for all frames.	**S**		**E**		unsigned
	2:0	0x0000	XENON_FRAMES_DELAY Number of the frames to wait before starting the sequence defined by XENON_FRAMES_ENABLE.	**S**		**E**		unsigned
	Control bits for FLASH output. The FLASH output is a strobe with programmable width and polarity, synchronised to the electronic rolling shutter (ERS). It can only be used when the sensor is operating in 1-exposure mode. When configured correctly the strobe asserts and negates while all rows of the visible image are integrating (it asserts after integration has started for the last visible image row and negates before readout starts for the first visible image row). This timing behavior is referred to as "Xenon flash". For a visible image of R rows in width and a maximum strobe assertion time of W (expressed in row rimes), COARSE_INTEGRATION_TIME_ must be set to at least R+W row times. If this constraint is not met, upper rows in the visible image will be read out before the strobe has asserted.					
R0x3048	**15:0**	**0x0100**	**FLASH2 (R/W)**			**E**		**unsigned**
	Width (assertion time) of Xenon flash strobe. For a programmed value of n, the strobe width is 2 * N/CLK_PIX_frequency.							
R0x3056	**10:0**	**0x0080**	**GREEN1_GAIN (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Green1 (Gr) pixels in Context A, in the format xxxx.yyyyyyy.							
R0x3058	**10:0**	**0x0080**	**BLUE_GAIN (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Blue pixels in Context A, in the format xxxx.yyyyyyy.							
R0x305A	**10:0**	**0x0080**	**RED_GAIN (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Red pixels in Context A, in the format xxxx.yyyyyyy.							
R0x305C	**10:0**	**0x0080**	**GREEN2_GAIN (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Green2 (Gb) pixels in Context A, in the format xxxx.yyyyyyy.							
R0x305E	**10:0**	**0x0080**	**GLOBAL_GAIN (R/W)**			**E**		**unsigned**
	Writes to this register write the same value to all 16 Context A color gain registers (GREEN1_GAIN, BLUE_GAIN, RED_GAIN, GREEN2_GAIN, GREEN1_GAIN_T2, BLUE_GAIN_T2, RED_GAIN_T2, GREEN2_GAIN_T2, GREEN1_GAIN_T3, BLUE_GAIN_T3, RED_GAIN_T3, GREEN2_GAIN_T3, GREEN1_GAIN_T4, BLUE_GAIN_T4, RED_GAIN_T4, GREEN2_GAIN_T4). Reading this register will return the value of the GREEN1_GAIN register.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3064	**15:0**	**0x0100**	**SMIA_TEST (R/W)**			**E**		**unsigned**
	15:14	0x0000	Reserved					
	13	0x0000	FORCE_SYS_CORE_RDY When bit is set, the sys_core_rdy port of the MIPI/HISPI TX block is forced high.			**E**		unsigned
	12:10	X	Undefined					
	9	0x0000	SMIA_TEST_PLL_BYPASS 0: Normal operation 1: Bypass the PLL VCO so that EXTCLK drives the PLL output clock divisors. In order to perform any repeatable phase-accurate testing, the PLL must be bypassed: either implicitly (by remaining in standby mode) or explicitly by setting this bit.			**E**		unsigned
	8	0x0001	SMIA_TEST_EMBEDDED_DATA_EN 0: No embedded data is transmitted. 1: Frames of data out of the sensor include embedded data rows before the image data. The number of embedded statistics rows is controlled by EMBED_ROWS_NR (R0x3040). This register field should only be changed while the sensor is in software standby.			**E**		unsigned
	7	0x0000	SMIA_TEST_EMBEDDED_STATS_EN 0: The statistics engines are disabled: no statistics data is calculated and no embedded statistics data is transmitted. 1: If SMIA_TEST_EMBEDDED_DATA_EN is also set to 1, Frames out of the sensor include embedded statistics data rows after the frame pixel data. The number of embedded statistics rows is controlled by STATS_ROWS_NR (R0x3040).			**E**		unsigned
	6	0x0000	STATS_ALIGN When 1, use the setting of RAW_DATA_FORMAT to control alignment of the stats data.			**E**		unsigned
	5	0x0000	Reserved					
	4	0x0000	SMIA_TEST_STATS_ROW_START_GB Enables statistics collection from Green/Blue row.			**E**		unsigned
	3:0	X	Undefined					
	smia test							
R0x3066	**15:0**	**0x0000**	**CTX_WR_DATA_REG (WO)**			**E**		**unsigned**
	Write to the next address in context RAM and increment address. The address is reset by any write to CTX_CONTROL_REG (R0x3034). This register is write-only (always reads as 0).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x306E	**15:0**	**0x9010**	**DATAPATH_SELECT (R/W)**			**E**		**unsigned**
	15:10	X	Undefined					
	9	0x0000	Reserved					
	8	X	Undefined					
	7	0x0000	AE_HIST_LOG_BINS_ENABLE enables logarithmic histograms			**E**		unsigned
	6	X	Undefined					
	5	0x0000	SCALER_WEIGHT2110 When SCALER_TRUE_BAYER=0, controls weighted binning mode. 0: Weighting 9:3:3:1, 1: Weighting 2:1:1:0.			**E**		unsigned
	4	0x0001	SCALER_TRUE_BAYER Enables true Bayer scaling mode.			**E**		unsigned
	3:0	X	Undefined					
	Bit-fields that affects the data path.							
R0x3070	**15:0**	**0x0000**	**TEST_PATTERN_MODE_ (R/W)**			**E**		**unsigned**
	15:9	X	Undefined					
	8	0x0000	WALKING_1_MODE 256: Marching 1 test pattern (12 bit)	**S**		**E**		unsigned
	7:3	X	Undefined					
	2:0	0x0000	MODE 0: Normal operation. Generate output data from pixel array 1: Solid color test pattern. 2: Full color bar test pattern. 3: Fade to grey color bar test pattern 4: PN9 test pattern Other: Reserved.	**S**		**E**		unsigned
	When enabled, test patterns are inserted in the active rows and columns of the T4 exposure only; ATR and DTR rows are forced to 0 and the active rows and columns of other exposures are forced to maximum value. Test patterns are not supported when READ_MODE_VERT_FLIP=1.							
R0x3072	**14:0**	**0x0000**	**TEST_DATA_RED_ (R/W)**			**E**		**unsigned**
	The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors.							
R0x3074	**14:0**	**0x0000**	**TEST_DATA_GREENR_ (R/W)**			**E**		**unsigned**
	The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors.							
R0x3076	**14:0**	**0x0000**	**TEST_DATA_BLUE_ (R/W)**			**E**		**unsigned**
	The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors.							
R0x3078	**14:0**	**0x0000**	**TEST_DATA_GREENB_ (R/W)**			**E**		**unsigned**
	The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x307A	**15:0**	**0x0000**	**TEST_RAW_MODE (R/W)**			**E**		**unsigned**
	15:2	X	Undefined					
	1	0x0000	TEST_PATTERN_OVERRIDE Prevents test_pattern from turning off corrections. By default the test patterns will disable corrections and pedestals. If set, the corrections will be enabled.			**E**		unsigned
	0	0x0000	RAW_DATA 0: Normal operation. 1: Turn off all corrections including output data companding.			**E**		unsigned
	Contains bitfields for controlling RAW data mode where corrections and pedestal are turned off							
R0x3082	**15:0**	**0x0004**	**OPERATION_MODE_CTRL (R/W)**	**S**		**E**		**unsigned**
	15:12	X	Undefined					
	11	0x0000	Reserved					
	10	0x0000	Reserved					
	9:5	X	Undefined					
	4	0x0000	OPERATION_MODE_CTRL_LIM_MODE Enable Line Interleave Mode (LIM).	**S**		**E**		unsigned
	3:2	0x0001	OPERATION_MODE_CTRL_NUM_EXP Set the number of exposures to num_exp + 1. 0: 1-exposure. 1: 2-exposure. 2: 3-exposure. 3: 4-exposure.	**S**		**E**		unsigned
	1:0	0x0000	OPERATION_MODE_CTRL_SEQUENCE_CODE Should always be 00 to select the HDR sequencer.	**S**		**E**		unsigned
	operation mode control							
R0x3084	**15:0**	**0x0004**	**OPERATION_MODE_CTRL_CB (R/W)**	**S**		**E**		**unsigned**
	15:12	X	Undefined					
	11	0x0000	Reserved					
	10	0x0000	Reserved					
	9:4	X	Undefined					
	3:2	0x0001	OPERATION_MODE_CTRL_NUM_EXP_CB When Context B is used, the value of this register must match the value of OPERATION_MODE_CTRL_NUM_EXP.	**S**		**E**		unsigned
	1:0	0x0000	OPERATION_MODE_CTRL_SEQUENCE_CODE_CB Should always be 00 to select the HDR sequencer.	**S**		**E**		unsigned
	Operation mode control bitfields for Context B							
R0x308A	**12:0**	**0x0000**	**X_ADDR_START_CB (R/W)**			**E**		**unsigned**
	X_ADDR_START for Context B. See R0x3004.							
R0x308C	**11:0**	**0x0000**	**Y_ADDR_START_CB (R/W)**			**E**		**unsigned**
	Y_ADDR_START for Context B. See R0x3002							
R0x308E	**12:0**	**0x0F07**	**X_ADDR_END_CB (R/W)**			**E**		**unsigned**
	X_ADDR_END for Context B. See R0x3008.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3090	**11:0**	**0x0877**	**Y_ADDR_END_CB (R/W)**			**E**		**unsigned**
	Y_ADDR_END for Context B. See R0x3006.							
R0x30AA	**15:0**	**0x04B8**	**FRAME_LENGTH_LINES_CB (R/W)**	**S**		**E**		**unsigned**
	FRAME_LENGTH_LINES for Context B. Must be a multiple of 8 for correct operation. See description of FRAME_LENGTH_LINES_ (R0x300A).							
R0x30B0	**15:0**	**0x0800**	**DIGITAL_TEST (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	PLL_COMPLETE_BYPASS 0: PLL is enabled 1: PLL is bypassed; EXTCLK will be used. Note that the serial interface does not function when the PLL is bypassed.			**E**		unsigned
	13	0x0000	CONTEXT_B Context Select. 0: Use Context A 1: Use Context B			**E**		unsigned
	12	X	Undefined					
	11	0x0001	Reserved					
	10	0x0000	Reserved					
	9	0x0000	Reserved					
	8	X	Undefined					
	7	0x0000	T1_DIGITAL_GAIN_REG_EN When bit is 1, the fine digital gain registers are used for a T1 only coarse digital gain setting in the format of xxxx.yyyyyyy. The fine digital gain stage is set to unity and can not be used. The coarse digital gain registers will only affect T2, T3 and T4. When using T1 digital gain enable, DCG_TRIM (R0x3364) must be updated so that the linearization block can compensate for the difference between the digital gain of the exposure T1 and T2, T3, T4	**S**		**E**		unsigned
	6	0x0000	Reserved					
	5	0x0000	Reserved					
	4	0x0000	Reserved					
	3	0x0000	Reserved					
	2	0x0000	Reserved					
	1	0x0000	Reserved					
	0	X	Undefined					
	Contains bit-fields for different digital functions.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x30B8	**15:0**	**0x0000**	**TEMPSENS1_CTRL_REG (R/W)**			**E**		**unsigned**
	15:6	0x0000	RETRIGGER1_THRSHOLD Temperature sensor temperature threshold that will trigger DBLC (if R0x3370[5]=1). The threshold is a 13-bit value formed by 10 bits here and 3 bits in R0x3EE2. When the temperature sensor is enabled or the CLEAR_VALUE bit is toggled, the next temperature conversion becomes the 'reference value'. When a subsequent temperature conversion differs from this 'reference value' (higher or lower) by more than the programmed temperature threshold, the current temperature value becomes the new 'reference value' and (if R0x3370[5]=1), DBLC is triggered.			**E**		unsigned
	5	0x0000	TEMP1_RED_FLAG_EN Set to enable red flag in tempvsens1_status register.			**E**		unsigned
	4	0x0000	TEMP1_YELLOW_FLAG_EN Set to enable yellow flag in tempvsens1_status register.			**E**		unsigned
	3	0x0000	TEMP1_CLEAR_VALUE 0: TEMPSENS1_DATA_REG (if enabled) is updated. 1: TEMPSENS1_DATA_REG is set to 0, clearing the last captured temperature value.			**E**		unsigned
	2	0x0000	TEMP1_START_CONV_STBY Set to enable conversions in standby mode in temperature sensor.			**E**		unsigned
	1	0x0000	TEMP1_START_CONV_STRM Set to enable conversions in streaming mode in temperature sensor.			**E**		unsigned
	0	0x0000	TEMP1_POWER_ON Set to enable temperature sensor.			**E**		unsigned
	Temperature sensor control register.							
R0x30BA	**15:0**	**0x1101**	**DIGITAL_CTRL (R/W)**			**E**		**unsigned**
	15	0x0000	Reserved					
	14	X	Undefined					
	13	0x0000	Reserved					
	12	0x0001	Reserved					
	11	X	Undefined					
	10	0x0000	Reserved					
	9	0x0000	Reserved					
	8	0x0001	Reserved					
	7:6	X	Undefined					
	5	0x0000	Reserved					
	4	0x0000	Reserved					
	3:2	X	Undefined					
	1:0	0x0001	NUM_EXP_MAX The value of this register must match the value of OPERATION_MODE_CTRL_NUM_EXP_.	**S**		**E**		unsigned
	digital control							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x30BC	**10:0**	**0x0080**	**GREEN1_GAIN_CB (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Green1 (Gr) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x30BE	**10:0**	**0x0080**	**BLUE_GAIN_CB (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Blue pixels in Context B, in the format xxxx.yyyyyyy.							
R0x30C0	**10:0**	**0x0080**	**RED_GAIN_CB (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Red pixels in Context B, in the format xxxx.yyyyyyy.							
R0x30C2	**10:0**	**0x0080**	**GREEN2_GAIN_CB (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T1 exposure of Green2 (Gb) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x30C4	**10:0**	**0x0080**	**GLOBAL_GAIN_CB (R/W)**			**E**		**unsigned**
	Writes to this register write the same value to all 16 Context B color gain registers (GREEN1_GAIN_CB, BLUE_GAIN_CB, RED_GAIN_CB, GREEN2_GAIN_CB, GREEN1_GAIN_T2_CB, BLUE_GAIN_T2_CB, RED_GAIN_T2_CB, GREEN2_GAIN_T2_CB, GREEN1_GAIN_T3_CB, BLUE_GAIN_T3_CB, RED_GAIN_T3_CB, GREEN2_GAIN_T3_CB, GREEN1_GAIN_T4_CB, BLUE_GAIN_T4_CB, RED_GAIN_T4_CB, GREEN2_GAIN_T4_CB). Reading this register will return the value of the GREEN1_GAIN_CB register.							
R0x30CA	**15:0**	**0x0000**	**TEMPSENS1_CALIB1 (R/W)**			**E**		**unsigned**
	Temperature sensor calibrated temperature code.							
R0x30CC	**15:0**	**0x0000**	**TEMPSENS1_CALIB2 (R/W)**			**E**		**unsigned**
	Temperature sensor calibrated temperature code.							
R0x30DC	**15:0**	**0x0020**	**TRIGGER_DELAY (R/W)**			**E**		**unsigned**
	15:1	0x0010	TRIGGER_DELAY_TRIGGER_DELAY Delay trigger pulse by number of clk_pix clocks when trigger delay mode is set. High-order bits of this delay are in SCALE_M (R0x3400).			**E**		unsigned
	0	0x0000	TRIGGER_DELAY_TRIGGER_DELAY_MODE trigger delay mode			**E**		unsigned
	trigger delay register							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3100	**15:0**	**0x0000**	**DLO_CONTROL0 (R/W)**			**E**		**unsigned**
	15	0x0000	NOISE_FILTER_DLO_QUAD Use quadratic function instead of linear function in DLO noise filter.	**S**		**E**		unsigned
	14	0x0000	NOISE_FILTER_DLO_EN Enable noise filtering in DLO.	**S**		**E**		unsigned
	13	0x0000	NOISE_DLO_DIS_PER_EXP If low noise filter disable threshold is backwards compatible. If high there are noise filter disable thresholds for each exposure.	**S**		**E**		unsigned
	12	X	Undefined					
	11:10	0x0000	DLO_BARRIER_DITHER_SPAN Set the span of barrier dither (if enabled). 0: Zero to 63*2 in steps of 2. 1: Zero to 63*4 in steps of 4. 2: Zero to 63*8 in steps of 8. Zero to 63*16 in steps of 16.	**S**		**E**		unsigned
	9:8	0x0000	DLO_BARRIER_DITHER_SELECT Before barriers are applied in the DLO algorithm they can optionally be dithered to smooth the SNR drops and to reduce the histogram spike that appears at each barrier. Dither is enabled by this field and adjusted using dlo_barrier_dither_span. 0: Barrier dither disabled. 1: Barrier dither enabled with flat distribution. 2: Barrier dither enabled with triangular distribution. 3: Reserved.	**S**		**E**		unsigned
	7:1	X	Undefined					
	0	0x0000	NCC_ENABLE Enable noise coring correction for DLO.	**S**		**E**		unsigned
	Contains bitfields for the control of DLO function							
R0x3102	**15:0**	**0x5040**	**DLO_CONTROL1 (R/W)**			**E**		**unsigned**
	15:12	0x0005	S12_DLO_RANGE_T2 Range of weighting transfer function defined by s2_dlo - s1_dlo	**S**		**E**		unsigned
	11:0	0x0040	S2_DLO_THRESHOLD_T2 Threshold level for end point of noise suppression applied to T2	**S**		**E**		unsigned
	Contains bitfields for the DLO threshold and range of T2							
R0x3104	**15:0**	**0x5040**	**DLO_CONTROL2 (R/W)**			**E**		**unsigned**
	15:12	0x0005	S12_DLO_RANGE_T3 Range of weighting transfer function defined by s2_dlo - s1_dlo	**S**		**E**		unsigned
	11:0	0x0040	S2_DLO_THRESHOLD_T3 Threshold level for end point of noise suppression applied to T3	**S**		**E**		unsigned
	Contains bitfields for the DLO threshold and range of T3							
R0x3106	**15:0**	**0x5040**	**DLO_CONTROL3 (R/W)**			**E**		**unsigned**
	15:12	0x0005	S12_DLO_RANGE_T4 Range of weighting transfer function defined by s2_dlo - s1_dlo	**S**		**E**		unsigned
	11:0	0x0040	S2_DLO_THRESHOLD_T4 Threshold level for end point of noise suppression applied to T4	**S**		**E**		unsigned
	Contains bitfields for the DLO threshold and range of T3							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3108	**15:0**	**0x0BB8**	**DLO_CONTROL4 (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11:0	0x0BB8	NOISE_DLO_DIS_THRESHOLD Threshold to disable noise filter (no noise filtering, if any of T1/T2/T3/T4 is over the threshold)	**S**		**E**		unsigned
	Contains bitfields for threshold to disable DLO noise filter							
R0x310A	**15:0**	**0x0BB8**	**DLO_CONTROL5 (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11:0	0x0BB8	NOISE_DLO_DIS_THRESHOLD_T2 Threshold to disable noise filter in T2 (no noise filtering, if any of T1/T2/T3/T4 is over the threshold)	**S**		**E**		unsigned
	Contains bitfields for threshold to disable DLO noise filter							
R0x310C	**15:0**	**0x0BB8**	**DLO_CONTROL6 (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11:0	0x0BB8	NOISE_DLO_DIS_THRESHOLD_T3 Threshold to disable noise filter in T3 (no noise filtering, if any of T1/T2/T3/T4 is over the threshold)	**S**		**E**		unsigned
	Contains bitfields for threshold to disable DLO noise filter							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3110	**15:0**	**0x0001**	**HDR_CONTROL0 (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14:12	0x0000	BYPASS_PIX_COMB_CB 3'b0xx: linearize (normal mode). 3'b100: bypass T1. 3'b101: bypass T2; valid for 3 exposure and 4 exposure HDR. Use bypass T4 setting to output T2 for 2 exposure HDR. 3'b110: bypass T3; valid for 4 exposure HDR. Use bypass T4 setting to output T3 for 3 exposure HDR. 3'b111: bypass T4; use to bypass the last exposure in 2, 3 or 4 exposure HDR.	**S**		**E**		unsigned
	11	X	Undefined					
	10:8	0x0000	BYPASS_PIX_COMB 3'b0xx: linearize (normal mode). 3'b100: bypass T1. 3'b101: bypass T2; valid for 3 exposure and 4 exposure HDR. Use bypass T4 setting to output T2 for 2 exposure HDR. 3'b110: bypass T3; valid for 4 exposure HDR. Use bypass T4 setting to output T3 for 3 exposure HDR. 3'b111: bypass T4; use to bypass the last exposure in 2, 3 or 4 exposure HDR.	**S**		**E**		unsigned
	7:5	X	Undefined					
	4	0x0000	PRE_HDR_GAIN_ENABLE Per-colour, per-exposure, per-context digital gain can be applied. 0: gain is applied after HDR reconstruct (linearization). 1: gain is applied before HDR reconstruct (linearization). The gain is controlled by the following registers: GREEN1_GAIN, BLUE_GAIN, RED_GAIN, GREEN2_GAIN, GREEN1_GAIN_T2, BLUE_GAIN_T2, RED_GAIN_T2, GREEN2_GAIN_T2, GREEN1_GAIN_T3, BLUE_GAIN_T3, RED_GAIN_T3, GREEN2_GAIN_T3, GREEN1_GAIN_T4, BLUE_GAIN_T4, RED_GAIN_T4, GREEN2_GAIN_T4, GLOBAL_GAIN, GREEN1_GAIN_CB, BLUE_GAIN_CB, RED_GAIN_CB, GREEN2_GAIN_CB, GREEN1_GAIN_T2_CB, BLUE_GAIN_T2_CB, RED_GAIN_T2_CB, GREEN2_GAIN_T2_CB, GREEN1_GAIN_T3_CB, BLUE_GAIN_T3_CB, RED_GAIN_T3_CB, GREEN2_GAIN_T3_CB, GREEN1_GAIN_T4_CB, BLUE_GAIN_T4_CB, RED_GAIN_T4_CB, GREEN2_GAIN_T4_CB, GLOBAL_GAIN_CB.	**S**		**E**		unsigned
	3:1	X	Undefined					
	0	0x0001	Reserved					
	Contains bitfields for the control of HDR reconstruct							
R0x3140	**12:0**	**0x0000**	**AE_ROI_X_START_OFFSET (R/W)**	**S**		**E**		**unsigned**
	ROI-1: Number of pixels skipped in each row before the ROI starts							
R0x3142	**11:0**	**0x0000**	**AE_ROI_Y_START_OFFSET (R/W)**	**S**		**E**		**unsigned**
	ROI-1: Number of pixels skipped in each frame before the ROI starts							
R0x3144	**12:0**	**0x0804**	**AE_ROI_X_SIZE (R/W)**	**S**		**E**		**unsigned**
	ROI-1: Number of columns in the ROI							
R0x3146	**11:0**	**0x0614**	**AE_ROI_Y_SIZE (R/W)**	**S**		**E**		**unsigned**
	ROI-1: Number of rows in the ROI							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3148	**15:0**	**0x0000**	**AE_HIST_BEGIN_PERC (R/W)**	**S**		**E**		**unsigned**
	ROI-1: Defines the percentage of Gr pixels that must have values below hist_begin. Specified as a number < 1 = 0.xx...xx							
R0x314A	**15:0**	**0xFFFF**	**AE_HIST_END_PERC (R/W)**	**S**		**E**		**unsigned**
	ROI-1: Defines the percentage of Gr pixels that must have values below hist_end. Specified as a number < 1 = 0.xx...xx. A value of all 1s is treated as a special case and equates to 1.0 (100%)							
R0x314C	**15:0**	**0x0100**	**AE_HIST_DIV (R/W)**			**E**		**unsigned**
	ROI-1: Defines the point at which the histogram is divided into the low and high end. Boundary value = hist_div*16							
R0x314E	**15:0**	**0x0020**	**AE_NORM_WIDTH_MIN (R/W)**			**E**		**unsigned**
	ROI-1: Defines the minimum histogram width normalization factor (=norm_width_min*16), for norm_abs_dev calculation. A value of all 1s turns off the norm_width_min option ie. all absolute deviation is normalized by hist_end - hist_begin							
R0x31AC	**15:0**	**0x140C**	**DATA_FORMAT_BITS (R/W)**			**E**		**unsigned**
	15:13	X	Undefined					
	12:8	0x0014	DATA_FORMAT_RAW Set the ADC or HDR data size. Legal values are 12, 14, 16, 18, 20 and 24 bit.			**E**		unsigned
	7:5	X	Undefined					
	4:0	0x000C	DATA_FORMAT_OUTPUT Set the output data size. Legal values are 10, 12, 14, 16, 20 and 24 bit.			**E**		unsigned
	Set the data format widths. The actual values used are reported in DATA_FORMAT_ACTUAL (R0x205C).							
R0x31AE	**15:0**	**0x0204**	**SERIAL_FORMAT (R/W)**			**E**		**unsigned**
	15:10	X	Undefined					
	9:8	0x0002	SERIAL_FORMAT_TYPE 2: MIPI. 0, 1, or 3: HiSpi.			**E**		unsigned
	7:3	X	Undefined					
	2:0	0x0004	SERIAL_FORMAT_LANES The number of active serial lanes: 1, 2, or 4.			**E**		unsigned
	Sets the serial format and the number of lanes.							
R0x31B0	**7:0**	**0x0053**	**FRAME_PREAMBLE (R/W)**			**E**		**unsigned**
	The frame preamble, expressed in op_pix_clk periods, must be large enough to allow the MIPI wakeup and start-of-frame short packet to be transmitted prior to the start of a frame of pixel data. The default value should be correct for most applications. Too small a value will result in a MIPI_PREAMBLE_ERROR being flagged in the DATAPATH_STATUS register. Legal values: [0, 255].							
R0x31B2	**7:0**	**0x003B**	**LINE_PREAMBLE (R/W)**			**E**		**unsigned**
	The line preamble, expressed in op_pix_clk periods, must be large enough to allow the MIPI long packet header to be transmitted prior to the start of a line of pixel data. The default value should be correct for most applications. Too small a value will result in a MIPI_PREAMBLE_ERROR being flagged in the DATAPATH_STATUS register. Legal values: [0, 255].							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x31BC	**15:0**	**0x1706**	**MIPI_TIMING_4 (R/W)**			**E**		**unsigned**
	15	0x0000	CONT_TX_CLK Set this bit when connecting the sensor to a SerDes component that requires the MIPI to operate in continuous mode. This register field should only be changed while the sensor is in software standby.			**E**		unsigned
	14	0x0000	Reserved					
	13:7	0x002E	Reserved					
	6:0	0x0006	Reserved					
	MIPI timing parameters							
R0x31BE	**15:0**	**0x0023**	**MIPI_CONFIG_STATUS (R/W)**			**E**		**unsigned**
	15	0x0000	LP11_ON_STANDBY 0: When the sensor is in standby, the MIPI interface will enter the Ultra low-power mode (ULPM). 1: When the sensor is in standby, the MIPI clock and data lanes will remain in the STOP state. Exit from ULPM takes at least 1.1ms; setting this bit allows sensor mode changes to be performed with low latency (for example, when using external trigger modes).			**E**		unsigned
	14	0x0000	Reserved					
	13	0x0000	TEST_MODE_0 MIPI PHY test mode. 0: normal operation. 1: scan mode.	**S**		**E**		unsigned
	12	0x0000	HRES Trim bit to reduce the driver output impedance	**S**		**E**		unsigned
	11	0x0000	Reserved					
	10	0x0000	Reserved					
	9	0x0000	Reserved					
	8:4	0x0002	Reserved					
	3:2	0x0000	HISPI_PHY_MODE Set the HiSpi signalling mode: 00: Hi-VCM. 01: SLVS with external regulator. 10: SubLVDS.			**E**		unsigned
	1	0x0001	FRAME_CNT_RST Reset the MIPI frame counting function.			**E**		unsigned
	0	0x0001	FRAME_CNT_EN Enable MIPI frame counting function.			**E**		unsigned
	Serial configuration and status							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x31C6	**15:0**	**0x0000**	**HISPI_CONTROL (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	EN_DESKEW_PAT Enable Deskew Pattern Insertion when operating PHY >1.5Gbps			**E**		unsigned
	13	0x0000	MASK_FRAMER_STANDBY When asserted, prevents the phy from going to a standby state.			**E**		unsigned
	12	0x0000	TRANSMIT_CHECKSUM When asserted, a checksum is appended to each line of HiSpi data except in 8-bit mode.			**E**		unsigned
	11:10	0x0000	Reserved					
	9	0x0000	Reserved					
	8	0x0000	Reserved					
	7	0x0000	Reserved					
	6:4	0x0000	Reserved					
	3	0x0000	BLANKING_DATA_EN 0: blanking data is set to the default value specified by the selected protocol. 1: For HiSpiSP and ActiveStart-SP8, use the HISPI_BLANKING register.			**E**		unsigned
	2	0x0000	STREAMING_MODE_EN For hispiSP and ActiveStart-SP8 and SP8+: 0 - packetized format, 1 - streaming format			**E**		unsigned
	1	0x0000	MSB_FIRST Enables MSB to be placed first in the data stream. This applies to data only and not sync codes.			**E**		unsigned
	0	0x0000	VERT_LEFT_BAR_EN When asserted one word of 0x0001 is transmitted between the last word of the SO* sync code and the first image data word in each lane			**E**		unsigned
	Contains bitfields for the HiSpi controls							
R0x31C8	**15:0**	**0x0000**	**MIPI_DESKEW_PAT_WIDTH (R/W)**			**E**		**unsigned**
	Programmable timer for width of Deskew Pattern Insertion							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x31CE	**15:0**	**0x0000**	**MIPI_CMOS_TOGGLE_TEST (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	MIPI_CMOS_TOGGLE_TEST_ENABLE When 1, the pads of the MIPI PHY are re-configured as CMOS outputs and the data value programmed into bits[9:0] of this register are driven on the associated output.	**S**		**E**		unsigned
	14:10	X	Undefined					
	9	0x0000	MIPI_CMOS_TOGGLE_TEST_DP3 Data value driven on DP3 pad in test mode.	**S**		**E**		unsigned
	8	0x0000	MIPI_CMOS_TOGGLE_TEST_DN3 Data value driven on DN3 pad in test mode.	**S**		**E**		unsigned
	7	0x0000	MIPI_CMOS_TOGGLE_TEST_DP2 Data value driven on DP2 pad in test mode.	**S**		**E**		unsigned
	6	0x0000	MIPI_CMOS_TOGGLE_TEST_DN2 Data value driven on DN2 pad in test mode.	**S**		**E**		unsigned
	5	0x0000	MIPI_CMOS_TOGGLE_TEST_DP1 Data value driven on DP1 pad in test mode.	**S**		**E**		unsigned
	4	0x0000	MIPI_CMOS_TOGGLE_TEST_DN1 Data value driven on DN1 pad in test mode.	**S**		**E**		unsigned
	3	0x0000	MIPI_CMOS_TOGGLE_TEST_DP0 Data value driven on DP0 pad in test mode.	**S**		**E**		unsigned
	2	0x0000	MIPI_CMOS_TOGGLE_TEST_DN0 Data value driven on DN0 pad in test mode.	**S**		**E**		unsigned
	1	0x0000	MIPI_CMOS_TOGGLE_TEST_CP Data value driven on CP pad in test mode.	**S**		**E**		unsigned
	0	0x0000	MIPI_CMOS_TOGGLE_TEST_CN Data value driven on CN pad in test mode.	**S**		**E**		unsigned
	mipi_cmos_toggle_test							
R0x31D0	**15:0**	**0x0000**	**COMPANDING (R/W)**			**E**		**unsigned**
	15:1	X	Undefined					
	0	0x0000	COMPAND_EN 0: Output companding disabled. 1: Output companding enabled.			**E**		unsigned
	Companding controls							
R0x31D2	**15:0**	**0x0000**	**STAT_FRAME_ID (R/W)**	**S**		**E**		**unsigned**
	User-programmable Stats Frame ID. Transferred in the first line of stats along with frame-count.							
R0x31D6	**15:0**	**0xFFFF**	**I2C_WRT_CHECKSUM (R/W)**			**E**		**unsigned**
	On every I2C write operation, the I2C address and write data are applied to a CRC generator. This register returns the current CRC. The CRC generator is initialised to 0xFFFF at reset. A write (any data) re-initialises the CRC generator to 0xFFFF. I2C writes are treated as a series of aligned 16-bit writes for the purpose of CRC accumulation.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x31E0	**15:0**	**0x0000**	**PIX_DEF_ID (R/W)**			**E**		**unsigned**
	15	0x0000	Reserved					
	14:3	X	Undefined					
	2	0x0000	Reserved					
	1	0x0000	PIX_DEF_ID_MODE Mode of pixel defect correction. 0: Tags bad pixels with the reserved value 0. 1: Corrects bad pixels using the traditional 1D correction scheme.			**E**		unsigned
	0	0x0000	PIX_DEF_ID_EN Enable pixel defect correction.			**E**		unsigned
	contains bitfield associated with pixel defect correction							
R0x31F8	**15:0**	**0x0000**	**MIPI_CONFIG_2 (R/W)**	**S**		**E**		**unsigned**
	15:2	X	Undefined					
	1	0x0000	MIPI_VALIDS_EN Controls which versions of FRAME_VALID, LINE_VALID and PIXCLK are observable on GPIO outputs. See description of GPIO_SELECT (R0x340E).	**S**		**E**		unsigned
	0	0x0000	ADT_EN When 1, the ATR, DTR, Dark and Overscan rows are output with the MIPI data-type codes specified by MIPI_F1_F2_ADT/ MIPI_F3_F4_ADT.	**S**		**E**		unsigned
	mipi_config_2							
R0x31FA	**15:0**	**0x3030**	**MIPI_F1_F2_ADT (R/W)**	**S**		**E**		**unsigned**
	15:14	X	Undefined					
	13:8	0x0030	MIPI_T1_DATA_TYPE MIPI data-type used in the packet header of T1-exposure ATR, DTR, Dark and Overscan rows, if MIPI_CONFIG_2[0]=1.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0030	MIPI_T2_DATA_TYPE MIPI data-type used in the packet header of T2-exposure ATR, DTR, Dark and Overscan rows, if MIPI_CONFIG_2[0]=1.			**E**		unsigned
	mipi_f1_f2_adt							
R0x31FC	**15:0**	**0x3030**	**MIPI_F3_F4_ADT (R/W)**	**S**		**E**		**unsigned**
	15:14	X	Undefined					
	13:8	0x0030	MIPI_T3_DATA_TYPE MIPI data-type used in the packet header of T3-exposure ATR, DTR, Dark and Overscan rows, if MIPI_CONFIG_2[0]=1.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0030	MIPI_T4_DATA_TYPE MIPI data-type used in the packet header of T4-exposure ATR, DTR, Dark and Overscan rows, if MIPI_CONFIG_2[0]=1.			**E**		unsigned
	mipi_f3_f4_adt							
R0x31FE	**15:0**	**0x0032**	**CUSTOMER_REV (RO)**			**E**		**unsigned**
	Customer revision register. See Developer's Guide for description. Example shown here is for AR0825AT3B18.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3212	**15:0**	**0x0002**	**COARSE_INTEGRATION_TIME2 (R/W)**	**S**		**E**		**unsigned**
	Integration time for T2 exposure when R0x3238[15]=1. See description of COARSE_INTEGRATION_TIME_ (R0x3012).							
R0x3214	**15:0**	**0x0002**	**COARSE_INTEGRATION_TIME2_CB (R/W)**	**S**		**E**		**unsigned**
	Context B integration time for T2 exposure R0x3238[15]=1. See description of COARSE_INTEGRATION_TIME_ (R0x3012).							
R0x3216	**15:0**	**0x0001**	**COARSE_INTEGRATION_TIME3 (R/W)**	**S**		**E**		**unsigned**
	Integration time for T3 exposure when R0x3238[15]=1. See description of COARSE_INTEGRATION_TIME_ (R0x3012).							
R0x3218	**15:0**	**0x0001**	**COARSE_INTEGRATION_TIME3_CB (R/W)**	**S**		**E**		**unsigned**
	Context B integration time for T3 exposure when R0x3238[15]=1. See description of COARSE_INTEGRATION_TIME_ (R0x3012).							
R0x321A	**15:0**	**0x0000**	**COARSE_INTEGRATION_TIME4 (R/W)**	**S**		**E**		**unsigned**
	Integration time for T4 exposure when R0x3238[15]=1. See description of COARSE_INTEGRATION_TIME_ (R0x3012).							
R0x321C	**15:0**	**0x0000**	**COARSE_INTEGRATION_TIME4_CB (R/W)**	**S**		**E**		**unsigned**
	Context B integration time for T4 exposure when R0x3238[15]=1. See description of COARSE_INTEGRATION_TIME_ (R0x3012).							
R0x3238	**15:0**	**0x0222**	**EXPOSURE_RATIO (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	EXPOSURE_RATIO_USE_REG Controls how integration times are set for Context A. The state of USE_REG_ must match USE_REG_CB.	**S**		**E**		unsigned
	14:11	X	Undefined					
	10:8	0x0002	EXPOSURE_RATIO_RATIO_T3_T4 Context A. Set T4 exposure based on T3 exposure and this ratio when USE_REG_=0.	**S**		**E**		unsigned
	7	X	Undefined					
	6:4	0x0002	EXPOSURE_RATIO_RATIO_T2_T3 Context A. Set T3 exposure based on T2 exposure and this ratio when USE_REG_=0.	**S**		**E**		unsigned
	3	X	Undefined					
	2:0	0x0002	EXPOSURE_RATIO_RATIO_T1_T2 Context A. Set T2 exposure based on T1 exposure and this ratio when USE_REG_=0.	**S**		**E**		unsigned
	Exposure ratio register for Context A. T1 integration is always set from COARSE_INTEGRATION_TIME. When USE_REG_=0, T2=COARSE_INTEGRATION_TIME_ / 2^RATIO_T1_T2, T3 = T2 / 2^RATIO_T2_T3, and T4 = T3 / 2^RATIO_T3_T4. With USE_REG_=1 (flexible exposures), T2=COARSE_INTEGRATION_TIME2, T3=COARSE_INTEGRATION_TIME_T3, T4=COARSE_INTEGRATION_TIME4.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x323A	**15:0**	**0x0222**	**EXPOSURE_RATIO_CB (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	EXPOSURE_RATIO_USE_REG_CB Controls how integration times are set for Context B. The state of USE_REG_CB must match USE_REG_.	**S**		**E**		unsigned
	14:11	X	Undefined					
	10:8	0x0002	EXPOSURE_RATIO_RATIO_T3_T4_CB Context B. Set T4 exposure based on T3 exposure and this ratio when USE_REG_CB=0.	**S**		**E**		unsigned
	7	X	Undefined					
	6:4	0x0002	EXPOSURE_RATIO_RATIO_T2_T3_CB Context B. Set T3 exposure based on T2 exposure and this ratio when USE_REG_CB=0.	**S**		**E**		unsigned
	3	X	Undefined					
	2:0	0x0002	EXPOSURE_RATIO_RATIO_T1_T2_CB Context B. Set T2 exposure based on T1 exposure and this ratio when USE_REG_CB=0.	**S**		**E**		unsigned
	Exposure ratio register for Context B. T1 integration is always set from COARSE_INTEGRATION_TIME_CB. When USE_REG_CB=0, T2=COARSE_INTEGRATION_TIME_CB / 2^RATIO_T1_T2_CB, T3 = T2 / 2^RATIO_T2_T3_CB, and T4 = T3 / 2^RATIO_T3_T4_CB. With USE_REG_CB=1 (flexible exposures), T2=COARSE_INTEGRATION_TIME2_CB, T3=COARSE_INTEGRATION_TIME_T3_CB, T4=COARSE_INTEGRATION_TIME4_CB.					
R0x323C	**15:0**	**0x8421**	**ROW_TX_ENABLE (R/W)**	**S**		**E**		**unsigned**
	15:12	0x0008	ROPD Bitmask to select TX pulses during ROPD. Bit [0] enables TXA, [1] enables TXB, [2] enables TXC and [3] enables TXD.	**S**		**E**		unsigned
	11:8	0x0004	ROPC Bitmask to select TX pulses during ROPC. Bit [0] enables TXA, [1] enables TXB, [2] enables TXC and [3] enables TXD.	**S**		**E**		unsigned
	7:4	0x0002	ROPB Bitmask to select TX pulses during ROPB. Bit [0] enables TXA, [1] enables TXB, [2] enables TXC and [3] enables TXD.	**S**		**E**		unsigned
	3:0	0x0001	ROPA Bitmask to select TX pulses during ROPA. Bit [0] enables TXA, [1] enables TXB, [2] enables TXC and [3] enables TXD.	**S**		**E**		unsigned
	Context A control of TX pulses during integration. The setting must correspond to the analog readout mode set in READ_MODE2 as follows normal (RGGB): 0x8421 ggbin_ana: 0x0429 mono_ana: 0x000f							
R0x323E	**15:0**	**0x000F**	**ROW_TX_ENABLE_CB (R/W)**	**S**		**E**		**unsigned**
	Context B control. See description of ROW_TX_ENABLE.							
R0x3240	**12:0**	**0x0000**	**AE_ROI2_X_START_OFFSET (R/W)**	**S**		**E**		**unsigned**
	ROI-2: Number of pixels dropped in each row before the ROI starts							
R0x3242	**11:0**	**0x0000**	**AE_ROI2_Y_START_OFFSET (R/W)**	**S**		**E**		**unsigned**
	ROI-2: Number of pixel rows dropped in each frame before the ROI starts							
R0x3244	**12:0**	**0x0804**	**AE_ROI2_X_SIZE (R/W)**	**S**		**E**		**unsigned**
	ROI-2: Number of columns in the ROI							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3246	11:0	0x0614	AE_ROI2_Y_SIZE (R/W)	S		E		unsigned
	ROI-2: Number of rows in the ROI							
R0x3248	15:0	0x0000	AE_HIST2_BEGIN_PERC (R/W)	S		E		unsigned
	ROI-2: Defines the percentage of Gr pixels that must have values below hist_begin. Specified as a number < 1 = 0.xx...xx							
R0x324A	15:0	0xFFFF	AE_HIST2_END_PERC (R/W)	S		E		unsigned
	ROI-2: Defines the percentage of Gr pixels that must have values below hist_end. Specified as a number < 1 = 0.xx...xx. A value of all 1s is treated as a special case and equates to 1.0 (100%)							
R0x324C	15:0	0x0100	AE_HIST2_DIV (R/W)			E		unsigned
	ROI-2: Defines the point at which the histogram is divided into the low and high end. Boundary value = hist_div*16							
R0x324E	15:0	0x0020	AE_NORM2_WIDTH_MIN (R/W)			E		unsigned
	ROI-2: Defines the minimum histogram width normalization factor (=norm_width_min*16), for norm_abs_dev calculation. A value of all 1s turns off the norm_width_min option ie. all absolute deviation is normalized by hist_end - hist_begin							
R0x3264	12:0	0x0000	AE_ROI3_X_START_OFFSET (R/W)			E		unsigned
	ROI-3: Number of pixels dropped in each row before the ROI starts							
R0x3266	11:0	0x0000	AE_ROI3_Y_START_OFFSET (R/W)			E		unsigned
	ROI-3: Number of pixel rows dropped in each frame before the ROI starts							
R0x3268	12:0	0x0804	AE_ROI3_X_SIZE (R/W)			E		unsigned
	ROI-3: Number of columns in the ROI							
R0x326A	11:0	0x0614	AE_ROI3_Y_SIZE (R/W)			E		unsigned
	ROI-3: Number of rows in the ROI							
R0x326C	15:0	0x0000	AE_HIST3_BEGIN_PERC (R/W)			E		unsigned
	ROI-3: Defines the percentage of Gr pixels that must have values below hist_begin. Specified as a number < 1 = 0.xx...xx							
R0x3270	12:0	0x0000	AE_X1_START_OFFSET (R/W)	S		E		unsigned
	Grid-stats: Marks the start of second grid ROI in x-direction. Selects region x-start to (x-start+x1_offset) for Grid ROI 0/4/8/12							
R0x3272	12:0	0x0000	AE_X2_START_OFFSET (R/W)	S		E		unsigned
	Grid-stats: Marks the start of third grid ROI in x-direction. Selects region (x-start+x1_offset) to (x-start+x1_offset+x2_offset)for Grid ROI 1/5/9/13							
R0x3274	12:0	0x0000	AE_X3_START_OFFSET (R/W)	S		E		unsigned
	Grid-stats: Marks the start of fourth grid ROI in x-direction. Selects region (x-start+x1_offset+x2_offset) to (x-start+x1_offset+x2_offset+x3_offset)for Grid ROI 2/6/10/14. Also sets the region (x-start+x1_offset+x2_offset+x3_offset) to x-end for Grid ROI 3/7/11/15.							
R0x3276	11:0	0x0000	AE_Y1_START_OFFSET (R/W)	S		E		unsigned
	Grid-stats: Marks the start of second grid ROI in y-direction. Selects region y-start to (y-start+y1_offset) for Grid ROI 0/1/2/3							
R0x3278	11:0	0x0000	AE_Y2_START_OFFSET (R/W)	S		E		unsigned
	Grid-stats: Marks the start of third grid ROI in y-direction. Selects region (y-start+y1_offset) to (y-start+y1_offset+y2_offset)for Grid ROI 4/5/6/7							
R0x327A	11:0	0x0000	AE_Y3_START_OFFSET (R/W)	S		E		unsigned
	Grid-stats: Marks the start of fourth grid ROI in y-direction. Selects region (y-start+y1_offset+y2_offset) to (y-start+y1_offset+y2_offset+y3_offset)for Grid ROI 8/9/10/11. Also sets the region (y-start+y1_offset+y2_offset+y3_offset) to y-end for Grid ROI 12/13/14/15.							

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R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x327C	**15:0**	**0x7070**	**AE_STATS_CONTROL (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	Reserved					
	14:12	0x0007	ROW_TYPE_ROI2 Select the Row type DTR/ATR/DeltaDk/Active to be sampled.	**S**		**E**		unsigned
	11:10	0x0000	EXP_SEL_ROI2 Select the exposure T1/T2/T3/T4 to be sampled.	**S**		**E**		unsigned
	9:8	0x0000	AE_COLOR_SEL_ROI2 Select the pixel R/Gr/Gb/B to be sampled.	**S**		**E**		unsigned
	7	0x0000	Reserved					
	6:4	0x0007	ROW_TYPE_ROI1 Select the Row type DTR/ATR/DeltaDk/Active to be sampled.	**S**		**E**		unsigned
	3:2	0x0000	EXP_SEL_ROI1 Select the exposure T1/T2/T3/T4 to be sampled.	**S**		**E**		unsigned
	1:0	0x0000	AE_COLOR_SEL_ROI1 Select the pixel R/Gr/Gb/B to be sampled.	**S**		**E**		unsigned
	This register along with other registers configures the stats module for operation.							
R0x327E	**15:0**	**0x7070**	**AE_STATS_CONTROL2 (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	Reserved					
	14:12	0x0007	ROW_TYPE_GRID Select the Row type DTR/ATR/DeltaDk/Active to be sampled.	**S**		**E**		unsigned
	11:10	0x0000	EXP_SEL_GRID Select the exposure T1/T2/T3/T4 to be sampled.	**S**		**E**		unsigned
	9:8	0x0000	AE_COLOR_SEL_GRID Select the pixel R/Gr/Gb/B to be sampled.	**S**		**E**		unsigned
	7	0x0000	Reserved					
	6:4	0x0007	ROW_TYPE_ROI3 Select the Row type DTR/ATR/DeltaDk/Active to be sampled.			**E**		unsigned
	3:2	0x0000	EXP_SEL_ROI3 Select the exposure T1/T2/T3/T4 to be sampled.			**E**		unsigned
	1:0	0x0000	AE_COLOR_SEL_ROI3 Select the pixel R/Gr/Gb/B to be sampled.			**E**		unsigned
	This register along with other registers configures the stats module for operation.							
R0x3280	**11:0**	**0x0BB8**	**T1_BARRIER_C0 (R/W)**	**S**		**E**		**unsigned**
	DLO clipping barrier for T1 color 0. When the DLO output transitions from the noise situation of a longer exposure to the noise situation of a shorter exposure it is possible to get noise halos in the image. Per-color barriers are one approach for removing color artefacts from the noise halos. An alternative (preferred) approach is to use per-color pre-HDR (digital) gain to adjust the white-balance of the image.							
R0x3282	**11:0**	**0x0BB8**	**T1_BARRIER_C1 (R/W)**	**S**		**E**		**unsigned**
	DLO clipping barrier for T1 color 1. See description of T1_BARRIER_C0.							
R0x3284	**11:0**	**0x0BB8**	**T1_BARRIER_C2 (R/W)**	**S**		**E**		**unsigned**
	DLO clipping barrier for T1 color 2. See description of T1_BARRIER_C0.							
R0x3286	**11:0**	**0x0BB8**	**T1_BARRIER_C3 (R/W)**	**S**		**E**		**unsigned**
	DLO clipping barrier for T1 color 3. See description of T1_BARRIER_C0.							

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R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3288	11:0	0x0DAC	T2_BARRIER_C0 (R/W)	S		E		unsigned
	DLO clipping barrier for T2 color 0. See description of T1_BARRIER_C0.							
R0x328A	11:0	0x0DAC	T2_BARRIER_C1 (R/W)	S		E		unsigned
	DLO clipping barrier for T2 color 1. See description of T1_BARRIER_C0.							
R0x328C	11:0	0x0DAC	T2_BARRIER_C2 (R/W)	S		E		unsigned
	DLO clipping barrier for T2 color 2. See description of T1_BARRIER_C0.							
R0x328E	11:0	0x0DAC	T2_BARRIER_C3 (R/W)	S		E		unsigned
	DLO clipping barrier for T2 color 3. See description of T1_BARRIER_C0.							
R0x3290	11:0	0x0DAC	T3_BARRIER_C0 (R/W)	S		E		unsigned
	DLO clipping barrier for T3 color 0. See description of T1_BARRIER_C0.							
R0x3292	11:0	0x0DAC	T3_BARRIER_C1 (R/W)	S		E		unsigned
	DLO clipping barrier for T3 color 1. See description of T1_BARRIER_C0.							
R0x3294	11:0	0x0DAC	T3_BARRIER_C2 (R/W)	S		E		unsigned
	DLO clipping barrier for T3 color 2. See description of T1_BARRIER_C0.							
R0x3296	11:0	0x0DAC	T3_BARRIER_C3 (R/W)	S		E		unsigned
	DLO clipping barrier for T3 color 3. See description of T1_BARRIER_C0.							
R0x3298	11:0	0x0DAC	T4_BARRIER_C0 (R/W)	S		E		unsigned
	DLO clipping barrier for T4 color 0. See description of T1_BARRIER_C0.							
R0x329A	11:0	0x0DAC	T4_BARRIER_C1 (R/W)	S		E		unsigned
	DLO clipping barrier for T4 color 1. See description of T1_BARRIER_C0.							
R0x329C	11:0	0x0DAC	T4_BARRIER_C2 (R/W)	S		E		unsigned
	DLO clipping barrier for T4 color 2. See description of T1_BARRIER_C0.							
R0x329E	11:0	0x0DAC	T4_BARRIER_C3 (R/W)	S		E		unsigned
	DLO clipping barrier for T4 color 3. See description of T1_BARRIER_C0.							

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R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x32A8	**15:0**	**0x0000**	**ATR_CHECK_CONTROL (R/W)**			**E**		**unsigned**
	15	0x0000	RRC_RST_CHECK Row ROM fields check: include RST L signal values in CRC calculation.			**E**		unsigned
	14	0x0000	RRC_CG_CHECK Row ROM fields check: include DCG mode signal values in CRC calculation.			**E**		unsigned
	13	0x0000	RRC_AB_CHECK Row ROM fields check: include TX* check signal values in CRC calculation.			**E**		unsigned
	12	0x0000	Reserved					
	11	0x0000	ATR_ZT_FIRSTVIS This bit is the expected bright or dark zebra AB pixel value in the Active imaging pixels.			**E**		unsigned
	10	0x0000	ATR_MT_ALTROWS This bit causes the memory column test check to alternate the expected value between rows.			**E**		unsigned
	9	0x0000	ATR_MT_ALTCOLS This bit causes the memory column test check to alternate the expected value between columns.			**E**		unsigned
	8	0x0000	Reserved					
	7:4	0x0000	CHECK_EXP_RRC 4 bits control which exposures of RRC are checked, in the order {T4,T3,T2,T1}.			**E**		unsigned
	3:0	0x0000	CHECK_EXP_ATR 4 bits control which exposures of ATR are checked, in the order {T4,T3,T2,T1}. A value of 8 (check T4 exposure) is supported; all other values are Reserved.			**E**		unsigned
	ATR check control register							

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Register Hex	Bits	Default	Name	Attributes				Data Type
R0x32AA	**15:0**	**0x3210**	**ATR_CHECK_ROWTYPES0 (R/W)**			**E**		**unsigned**
	15:12	0x0003	ATR_ROWTYPE_03 ATR test to run on ATR row 3			**E**		unsigned
	11:8	0x0002	ATR_ROWTYPE_02 ATR test to run on ATR row 2			**E**		unsigned
	7:4	0x0001	ATR_ROWTYPE_01 ATR test to run on ATR row 1			**E**		unsigned
	3:0	0x0000	ATR_ROWTYPE_00 ATR test to run on ATR row 0			**E**		unsigned
	4 RW registers with 4, 4-bit fields each which determine which tests to run on up to 16 ATR rows. ATR_ROWTYPE_00 determines which (if any) check to run on the first ATR row, etc. The rowtype fields have the following meanings: 0000: column ROM row. 0001: Gray transfer test 2 0010: Gray transfer test 1 0011: Column memory test 2 0100: Column memory test 1 0101: Overdrive test 0 0110: Overdrive test 1. 0111: Overdrive test 2. 1000: Overdrive test 3. 1001: Overdrive test 4. 1010: Zebra AB test 1011: Zebra BA test 1100: off (reserved for Frame Counter test) 1101: off (reserved for Gradient test) 1101: Vertical Pixout test 1 1111: Vertical Pixout test 2.							
R0x32AC	**15:0**	**0x7654**	**ATR_CHECK_ROWTYPES1 (R/W)**			**E**		**unsigned**
	15:12	0x0007	ATR_ROWTYPE_07 ATR test to run on ATR row 7			**E**		unsigned
	11:8	0x0006	ATR_ROWTYPE_06 ATR test to run on ATR row 6			**E**		unsigned
	7:4	0x0005	ATR_ROWTYPE_05 ATR test to run on ATR row 5			**E**		unsigned
	3:0	0x0004	ATR_ROWTYPE_04 ATR test to run on ATR row 4			**E**		unsigned
	See description of ATR_CHECK_ROWTYPES0.							
R0x32AE	**15:0**	**0xBA98**	**ATR_CHECK_ROWTYPES2 (R/W)**			**E**		**unsigned**
	15:12	0x000B	ATR_ROWTYPE_11 ATR test to run on ATR row 11			**E**		unsigned
	11:8	0x000A	ATR_ROWTYPE_10 ATR test to run on ATR row 10			**E**		unsigned
	7:4	0x0009	ATR_ROWTYPE_09 ATR test to run on ATR row 9			**E**		unsigned
	3:0	0x0008	ATR_ROWTYPE_08 ATR test to run on ATR row 8			**E**		unsigned
	See description of ATR_CHECK_ROWTYPES0.							

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R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x32B0	**15:0**	**0xFEDC**	**ATR_CHECK_ROWTYPES3 (R/W)**			**E**		**unsigned**
	15:12	0x000F	ATR_ROWTYPE_15 ATR test to run on ATR row 15			**E**		unsigned
	11:8	0x000E	ATR_ROWTYPE_14 ATR test to run on ATR row 14			**E**		unsigned
	7:4	0x000D	ATR_ROWTYPE_13 ATR test to run on ATR row 13			**E**		unsigned
	3:0	0x000C	ATR_ROWTYPE_12 ATR test to run on ATR row 12			**E**		unsigned
	See description of ATR_CHECK_ROWTYPES0.							
R0x32BA	**13:0**	**0x0000**	**ATR_CHECK_ZT_LO_THRESH (R/W)**			**E**		**unsigned**
	ATR pixels for zebra tests AB and BA are expected to be lower than this threshold or higher than ATR_CHECK_ZT_HI_THRESH according to the zebra pattern. Value is in s14 format but guaranteed to be in the range -2048..+6143.							
R0x32BC	**13:0**	**0x0000**	**ATR_CHECK_ZT_HI_THRESH (R/W)**			**E**		**unsigned**
	ATR pixels for zebra tests AB and BA are expected to be higher than this threshold or lower than ATR_CHECK_ZT_LO_THRESH according to the zebra pattern. Value is in s14 format but guaranteed to be in the range -2048..+6143.							
R0x32BE	**13:0**	**0x0000**	**ATR_CHECK_MT_EXPECT1 (R/W)**			**E**		**unsigned**
	One of two expected value registers used for ADC memory tests 1 and 2, in s14 format. Should be set to 0x0555.							
R0x32C0	**13:0**	**0x0000**	**ATR_CHECK_MT_EXPECT2 (R/W)**			**E**		**unsigned**
	One of two expected value registers used for ADC memory tests 1 and 2, in s14 format. Should be set to 0x3aab.							
R0x32C2	**13:0**	**0x0000**	**ATR_CHECK_PT_LO_THRESH (R/W)**			**E**		**unsigned**
	ATR pixels for pixout test 1 are expected to be lower than this threshold. Value is in s14 format but guaranteed to be in the range -2048..+6143.							
R0x32C4	**13:0**	**0x0000**	**ATR_CHECK_PT_HI_THRESH (R/W)**			**E**		**unsigned**
	ATR pixels for pixout test 2 are expected to be higher than this threshold. Value is in s14 format but guaranteed to be in the range -2048..+6143.							
R0x32C6	**13:0**	**0x0000**	**RRC_CHECK_LO_THRESH (R/W)**			**E**		**unsigned**
	RRC pixels for the DCG Mode and RST-L checks are deemed dark if lower than this threshold. Value is in s14 format but guaranteed to be in the range -2048..+6143.							
R0x32C8	**13:0**	**0x0000**	**RRC_CHECK_HI_THRESH (R/W)**			**E**		**unsigned**
	RRC pixels for the DCG Mode, TX* and row ROM address checks are deemed light if higher than this threshold. Value is in s14 format but guaranteed to be in the range -2048..+6143.							
R0x32CA	**15:0**	**0x0000**	**ATR_CHECK_CRT_CRC_EXPECT (R/W)**			**E**		**unsigned**
	Expected CRC value from column ROM addresses.							
R0x32CC	**15:0**	**0x0000**	**RRC_CHECK_ADDR_CRC_EXPECT (R/W)**			**E**		**unsigned**
	Expected CRC value from row ROM addresses.							
R0x32F0	**15:0**	**0xFFFF**	**AE_HIST3_END_PERC (R/W)**			**E**		**unsigned**
	ROI-3: Defines the percentage of Gr pixels that must have values below hist_end. Specified as a number < 1 = 0.xx...xx. A value of all 1s is treated as a special case and equates to 1.0 (100%)							
R0x32F2	**15:0**	**0x0200**	**AE_HIST3_DIV (R/W)**			**E**		**unsigned**
	ROI-3: Defines the point at which the histogram is divided into the low and high end. Boundary value = hist_div*16							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

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Register Hex	Bits	Default	Name	Attributes				Data Type
R0x32F4	**15:0**	**0x0020**	**AE_NORM3_WIDTH_MIN (R/W)**			**E**		**unsigned**
	ROI-3: Defines the minimum histogram width normalization factor (=norm_width_min*16), for norm_abs_dev calculation. A value of all 1s turns off the norm_width_min option ie. all absolute deviation is normalized by hist_end - hist_begin							
R0x32F6	**15:0**	**0x0000**	**MIDDLE_INTEGRATION_CTRL (R/W)**	**S**		**E**		**unsigned**
	15:13	X	Undefined					
	12	0x0000	T2_T3_SWAP_CB	**S**		**E**		unsigned
	11:8	0x0000	MIDDLE_INTEGRATION_TIME_CB	**S**		**E**		unsigned
	7:5	X	Undefined					
	4	0x0000	T2_T3_SWAP Swap the readout slot used for T2 readout and the readout slot used for T3 readout. This function is only available when the number of exposures is set to 4.	**S**		**E**		unsigned
	3:0	0x0000	MIDDLE_INTEGRATION_TIME Change the readout slot relationship so that the integration time for all exposures is increased by an integer number of ROP times. The range of values available depends upon the number of exposures and the number of conversions. In full resolution mode (4 conversions), 4 values are available for each exposure in use. Therefore, values of 0-3 can be used in 1-exposure mode and values of 0-15 can be used in 4-exposure mode. In mono mode (2 conversions), 2 values are available for each exposure in use. Therefore, values of 0-1 can be used in 1-exposure mode and values of 0-7 can be used in 4-exposure mode. Behaviour is UNDEFINED if the value is too large for the operating mode.	**S**		**E**		unsigned
	Each exposure provides a time-slot for pixel array reset and a time-slot for pixel array readout. Each time slot is 1 ROP in duration. By default, the time-slot used for readout is the same as the time slot used for reset, so that the integration time for every exposure is an integer number of row-times. This register allows small adjustments to the integration time by changing the readout slot order, and therefore changing the relationship between the reset slot for an exposure and its readout slot. Increasing the middle integration time makes the integration start earlier and therefore increases the integration time. Changing the MIT value within a single context during frame N will result in a ‘bad’ frame N+1 (frame with uneven integration). When writing to this register you should only change one MIT value (either MIDDLE_INTEGRATION_TIME or MIDDLE_INTEGRATION_TIME_CB) in each frame time; this ensures a clean switch from one MIT setting to another when the context changes.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x32FC	**15:0**	**0x0900**	**READ_MODE2 (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	CONTEXT_SW_MODE 0: Context B cannot be used. Both shutters are used for Context A. Context changes can only be achieved by reprogramming Context A registers. 1: Frame-by-frame context switching between Context A and ContextB can be achieved by toggling DIGITAL_TEST.CONTEXT_B (R0x30B0). One shutter is assigned to each context. For AR0825 REV2 this bit is removed and shutter assignment is performed automatically.			**E**		unsigned
	14	X	Undefined					
	13:8	0x0009	READOUT_CB Set readout for Context B. See description of readout.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0000	READOUT The following readout modes are supported: 0: Normal readout (no binning) 1: hbin_dig - digital same-color horizontal binning 2: vbin_dig - digital same-color vertical binning 3: hvbin_dig - digital same-color horizontal and vertical binning 5: hvbin_mono_dig - digital horizontal and vertical adjacent pixel (monochrome) binning 6: vbin_ana - analog SF same-color vertical binning 7: analog FD green/green diagonal binning 9: mono_ana - analog FD adjacent pixel (monochrome) binning 10: vbin_ana_hbin_dig - analog SF same-color vertical and digital same-color horizontal binning All other values are RESERVED.			**E**		unsigned
	Enable frame-by-frame context switching and select readout mode for contexts A and B.							
R0x3300	**10:0**	**0x0200**	**GREEN1_GAIN2_ (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain for Green1 (Gr) pixels in Context A, in format of xx.yyyyyyyyy.							
R0x3302	**10:0**	**0x0200**	**BLUE_GAIN2_ (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain for Blue pixels in Context A, in format of xx.yyyyyyyyy.							
R0x3304	**10:0**	**0x0200**	**RED_GAIN2_ (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain for Red pixels in Context A, in format of xx.yyyyyyyyy.							
R0x3306	**10:0**	**0x0200**	**GREEN2_GAIN2_ (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain for Green2 (Gb) pixels in Context A,in format of xx.yyyyyyyyy.							
R0x3308	**10:0**	**0x0200**	**GLOBAL_GAIN2_ (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain in format of xx.yyyyyyyyy. Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain2 registers. Reading from this register returns the value most recently written to the green1_gain2 register.							
R0x330A	**10:0**	**0x0200**	**GREEN1_GAIN2_CB (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain for Green1 (Gr) pixels in Context B, in format of xx.yyyyyyyyy.							
R0x330C	**10:0**	**0x0200**	**BLUE_GAIN2_CB (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain for Blue pixels in Context B, in format of xx.yyyyyyyyy.							
R0x330E	**10:0**	**0x0200**	**RED_GAIN2_CB (R/W)**	**S**		**E**		**unsigned**
	Post DLO 2nd stage fine digital gain for Red pixels in Context B, in format of xx.yyyyyyyyy.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3310	10:0	0x0200	GREEN2_GAIN2_CB (R/W)	S		E		unsigned
	Post DLO 2nd stage fine digital gain for Green2 (Gb) pixels in Context B,in format of xx.yyyyyyyyy.							
R0x3312	10:0	0x0200	GLOBAL_GAIN2_CB (R/W)	S		E		unsigned
	Post DLO 2nd stage fine digital gain in format of xx.yyyyyyyyy. Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain2 registers. Reading from this register returns the value most recently written to the green1_gain2 register.							
R0x3316	15:0	0x0000	OTPM_WRT_CHECKSUM (R/W)			E		unsigned
	Holds the expected 16-bit OTPM CRC value							
R0x3318	15:0	0x0000	IREG_WRT_CHECKSUM (R/W)			E		unsigned
	Holds the expected 16-bit startup register scan CRC value							
R0x331A	15:0	0x0000	PDIM_WRT_CHECKSUM (R/W)			E		unsigned
	Holds the expected 16-bit PDI memory CRC value							
R0x331C	15:0	0x0000	M3ROM_CALC_CHECKSUM (R/W)			E		unsigned
	Holds the calculated 16-bit M3ROM startup CRC value. Enabled by ASIL_STARTUP_ENABLES_00.							
R0x331E	15:0	0x0000	OTPM_CALC_CHECKSUM (R/W)			E		unsigned
	Holds the calculated-16 bit OTPM CRC value. Enabled by ASIL_STARTUP_ENABLES_00.							
R0x3320	15:0	0x0000	IREG_CALC_CHECKSUM (R/W)			E		unsigned
	Holds the calculated 16-bit startup register scan CRC value. Enabled by ASIL_STARTUP_ENABLES_00. The startup register scan is performed when the sensor is in standby. R0x3324[10] and R0x5100-R0x517E control which registers are included in the calculation. See also R0x332A CRC_EMB_CALC_CHECKSUM.							
R0x3322	15:0	0x0000	PDIM_CALC_CHECKSUM (R/W)			E		unsigned
	Holds the calculated 16-bit PDI memory CRC value. Enabled by ASIL_STARTUP_ENABLES_00.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3324	**15:0**	**0x8000**	**CRC_CONTROL_REG (R/W)**			**E**		**unsigned**
	15	0x0001	CRC_EMBED_ADDR_MAP 0: all embedded registers are included in the embedded data CRC and the startup register scan CRC, 1: The EMBED_CRC_MAP registers form a bit-map which identifies embedded registers that are EXCLUDED from the embedded data CRC and the startup register scan CRC.	**S**		**E**		unsigned
	14	0x0000	CRC_LINE_BITSWAP 1: Reverse bit-order of the values applied to the line CRC generator.	**S**		**E**		unsigned
	13	0x0000	CRC_FRAME_BITSWAP 1: Reverse bit-order of the values applied to the frame CRC generator.	**S**		**E**		unsigned
	12	0x0000	CRC_DTR_BITSWAP 1: Reverse bit-order of the values applied to the DTR CRC generator.	**S**		**E**		unsigned
	11	0x0000	CRC_EMBED_BITSWAP 1: Reverse bit-order of the values applied to the embedded CRC and the PDI startup scan CRC generators.	**S**		**E**		unsigned
	10:9	0x0000	CRC_COL_REGIONS Reserved.	**S**		**E**		unsigned
	8:4	0x0000	CRC_ROW_REGIONS Control which row regions are included in the frame CRC calculation. [8]: Include embedded data rows, [7]: Include statistics rows, [6]: Include ATR rows, [5]: Include active rows, [4]: Include dark data rows.	**S**		**E**		unsigned
	3:1	0x0000	CRC_EXPOSURE In LIM mode, control which exposures contribute to CRC generation. 000: T1,001: T2,010: T3, 011: T4, 1xx: Combined exposures.	**S**		**E**		unsigned
	0	0x0000	CRC_PER_FRAME 0: Enable per-line row CRC (parallel interface only). 1: Enable frame CRC. Must be 1 for AR0825.	**S**		**E**		unsigned
	Control for the streaming CRC generators and the embedded data CRC generator.							
R0x3326	**15:0**	**0x0000**	**CRC_EMB_WRT_CHECKSUM (R/W)**			**E**		**unsigned**
	Holds the expected 16-bit embedded CRC value.							
R0x332A	**15:0**	**0x0000**	**CRC_EMB_CALC_CHECKSUM (R/W)**			**E**		**unsigned**
	Holds the calculated 16-bit embedded CRC value. When enabled by ASIL_CHECK_ENABLES_02, the embedded CRC value is calculated for each frame. R0x3324[10] and R0x5100-R0x517E control which registers are included in the calculation. See also R0x3320 IREG_CALC_CHECKSUM.							
R0x332C	**15:0**	**0x0000**	**CRC_FR_WRT_CHECKSUM_LOW (R/W)**			**E**		**unsigned**
	Holds the low 16 bits of the expected 24-bit Frame/Row CRC.							
R0x332E	**15:0**	**0x0000**	**CRC_FR_CALC_CHECKSUM_LOW (R/W)**			**E**		**unsigned**
	Holds the low 16 bits of the calculated 24-bit Frame/Row CRC. Enabled by ASIL_CHECK_ENABLES_02 and CRC_CONTROL_REG.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3342	**15:0**	**0x122C**	**MIPI_F1_PDT_EDT (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13:8	0x0012	MIPI_F1_EDT MIPI data type for embedded data in exposure 1.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x002C	MIPI_F1_PDT MIPI data type for pixels in exposure 1.			**E**		unsigned
	Sets pixel and embedded mipi data type for exposure 1.							
R0x3344	**15:0**	**0x0011**	**MIPI_F1_VDT_VC (R/W)**			**E**		**unsigned**
	15:10	X	Undefined					
	9:8	0x0000	MIPI_F1_VC MIPI virtual channel for exposure 1.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0011	MIPI_F1_VDT MIPI data type for vertical blanking data in exposure 1.			**E**		unsigned
	Sets blanking mipi data type and the virtual channel for exposure 1.							
R0x3346	**15:0**	**0x122C**	**MIPI_F2_PDT_EDT (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13:8	0x0012	MIPI_F2_EDT MIPI data type for embedded data in exposure 2.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x002C	MIPI_F2_PDT MIPI data type for pixels in exposure 2.			**E**		unsigned
	Sets pixel and embedded mipi data type for exposure 2.							
R0x3348	**15:0**	**0x0111**	**MIPI_F2_VDT_VC (R/W)**			**E**		**unsigned**
	15:10	X	Undefined					
	9:8	0x0001	MIPI_F2_VC MIPI virtual channel for exposure 2.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0011	MIPI_F2_VDT MIPI data type for vertical blanking data in exposure 2.			**E**		unsigned
	Sets blanking mipi data type and the virtual channel for exposure 2.							
R0x334A	**15:0**	**0x122C**	**MIPI_F3_PDT_EDT (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13:8	0x0012	MIPI_F3_EDT MIPI data type for embedded data in exposure 3.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x002C	MIPI_F3_PDT MIPI data type for pixels in exposure 3.			**E**		unsigned
	Sets pixel and embedded mipi data type for exposure 3.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x334C	**15:0**	**0x0211**	**MIPI_F3_VDT_VC (R/W)**			**E**		**unsigned**
	15:10	X	Undefined					
	9:8	0x0002	MIPI_F3_VC MIPI virtual channel for exposure 3.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0011	MIPI_F3_VDT MIPI data type for vertical blanking data in exposure 3.			**E**		unsigned
	Sets blanking mipi data type and the virtual channel for exposure 3.							
R0x334E	**15:0**	**0x122C**	**MIPI_F4_PDT_EDT (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13:8	0x0012	MIPI_F4_EDT MIPI data type for embedded data in exposure 4.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x002C	MIPI_F4_PDT MIPI data type for pixels in exposure 4.			**E**		unsigned
	Sets pixel and embedded mipi data type for exposure 4.							
R0x3350	**15:0**	**0x0311**	**MIPI_F4_VDT_VC (R/W)**			**E**		**unsigned**
	15:10	X	Undefined					
	9:8	0x0003	MIPI_F4_VC MIPI virtual channel for exposure 4.			**E**		unsigned
	7:6	X	Undefined					
	5:0	0x0011	MIPI_F4_VDT MIPI data type for vertical blanking data in exposure 4.			**E**		unsigned
	Sets blanking mipi data type and the virtual channel for exposure 4.							
R0x3352	**15:0**	**0x0000**	**MIPI_DT_VC_CONFIG (R/W)**			**E**		**unsigned**
	15	0x0000	ENABLE_VB_LINES Enable vertical blanking lines in line interleave mode (LIM) and for lines that are present internally but not enabled at the sensor output (for example, DTR rows when DARK_CONTROL[13] is 0).			**E**		unsigned
	14	0x0000	ENABLE_DT_INTERLEAVING Enable data type and virtual channel interleaving in line interleave mode.			**E**		unsigned
	13:4	X	Undefined					
	3	0x0000	F4_VC_EN Enable f4 virtual channel's FS and FE packets.			**E**		unsigned
	2	0x0000	F3_VC_EN Enable f3 virtual channel's FS and FE packets.			**E**		unsigned
	1	0x0000	F2_VC_EN Enable f2 virtual channel's FS and FE packets.			**E**		unsigned
	0	X	Undefined					
	MIPI data type and virtual channel interleaving configuration. See DUMMY_PIXEL_VALUE (R0x33F2).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3354	**15:0**	**0xFFFF**	**I2C_RD_CHECKSUM (R/W)**			**E**		**unsigned**
	On every I2C read operation, the I2C address and read data are applied to a CRC generator. This register returns the current CRC. A read of this register is accumulated in the CRC generator after the read has completed. The CRC generator is initialised to 0xFFFF at reset. A write (any data) re-initialises the CRC generator to 0xFFFF. I2C reads are treated as a series of aligned 16-bit reads for the purpose of CRC accumulation.							
R0x3356	**15:0**	**0x0000**	**CRC_DTR_WRT_CHECKSUM_LOW (R/W)**			**E**		**unsigned**
	Holds the low part (bits [15:0]) of the expected 24-bit DTR CRC.							
R0x3358	**15:0**	**0x0000**	**CRC_DTR_CALC_CHECKSUM_LOW (R/W)**			**E**		**unsigned**
	Holds the low part (bits [15:0]) of the calculated 24-bit DTR CRC.							
R0x335C	**15:0**	**0x0000**	**CRC_FR_DTR_CALC_CHECKSUM_HIGH (R/W)**			**E**		**unsigned**
	15:8	0x0000	CRC_DTR_CALC_CHECKSUM_HIGH Holds the high part (bits [23:16]) of the calculated 24-bit DTR CRC.	**S**		**E**		unsigned
	7:0	0x0000	CRC_FR_CALC_CHECKSUM_HIGH Holds the high part (bits [23:16]) of the calculated 24-bit frame/row CRC.	**S**		**E**		unsigned
	Holds the high parts (bits [23:16]) of the calculated 24-bit DTR and frame/row CRCs.							
R0x335E	**15:0**	**0x0000**	**CRC_FR_DTR_WRT_CHECKSUM_HIGH (R/W)**			**E**		**unsigned**
	15:8	0x0000	CRC_DTR_WRT_CHECKSUM_HIGH Holds the high part (bits [20:16]) of the expected 24-bit DTR CRC.	**S**		**E**		unsigned
	7:0	0x0000	CRC_FR_WRT_CHECKSUM_HIGH Holds the high part (bits [20:16]) of the expected 24-bit Frame/Row CRC.	**S**		**E**		unsigned
	Holds the high parts (bits [24:16]) of the expected 24-bit DTR and Frame/Row CRCs.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3362	**15:0**	**0x0001**	**DC_GAIN (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	GCF_T4_CB Select pixel conversion gain as LCG/HCG -Context-B, T4 exposure.	**S**		**E**		unsigned
	14	0x0000	GCF_T3_CB Select pixel conversion gain as LCG/HCG -Context-B, T3 exposure.	**S**		**E**		unsigned
	13	0x0000	GCF_T2_CB Select pixel conversion gain as LCG/HCG -Context-B, T2 exposure.	**S**		**E**		unsigned
	12	0x0000	GCF_T1_CB Select pixel conversion gain as LCG/HCG -Context-B, T1 exposure.	**S**		**E**		unsigned
	11	0x0000	GCF_T4 Select pixel conversion gain as LCG/HCG -Context-A, T4 exposure.	**S**		**E**		unsigned
	10	0x0000	GCF_T3 Select pixel conversion gain as LCG/HCG -Context-A, T3 exposure.	**S**		**E**		unsigned
	9	0x0000	GCF_T2 Select pixel conversion gain as LCG/HCG -Context-A, T2 exposure.	**S**		**E**		unsigned
	8	0x0000	GCF_T1 Select pixel conversion gain as LCG/HCG -Context-A, T1 exposure.	**S**		**E**		unsigned
	7	0x0000	DC_GAIN_T4_CB Context B Conversion gain for exposure T4.	**S**		**E**		unsigned
	6	0x0000	DC_GAIN_T3_CB Context B Conversion gain for exposure T3.	**S**		**E**		unsigned
	5	0x0000	DC_GAIN_T2_CB Context B Conversion gain for exposure T2.	**S**		**E**		unsigned
	4	0x0000	DC_GAIN_T1_CB Context B Conversion gain for exposure T1.	**S**		**E**		unsigned
	3	0x0000	DC_GAIN_T4 Conversion gain for exposure T4.	**S**		**E**		unsigned
	2	0x0000	DC_GAIN_T3 Conversion gain for exposure T3.	**S**		**E**		unsigned
	1	0x0000	DC_GAIN_T2 Conversion gain for exposure T2.	**S**		**E**		unsigned
	0	0x0001	DC_GAIN_T1 Conversion gain for exposure T1.	**S**		**E**		unsigned
	Conversion gain application register. The DC_GAIN bits control the conversion gain for both contexts of each exposure (0: Low conversion gain, 1: High conversion gain). The GCF (gain correction factor) bits allow the actual exposure/gain ratios to be adjusted for particular exposures in each contect. The GCF bits are used with DCG_TRIM (R0x3364) and the _BYP bits in SAMPLE_CTRL (R0x33E2).							
R0x3364	**10:0**	**0x002A**	**DCG_TRIM (R/W)**	**S**		**E**		**unsigned**
	DCG gain trimming value, format NNNN.MMMMMMM. See description of DC_GAIN (R0x3362).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3366	**15:0**	**0x0000**	**ANALOG_GAIN (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	Reserved					
	14:12	0x0000	ANALOG_GAIN_T4 T4 analog_coarse_gain. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	11	0x0000	Reserved					
	10:8	0x0000	ANALOG_GAIN_T3 T3 analog_coarse_gain. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	7	0x0000	Reserved					
	6:4	0x0000	ANALOG_GAIN_T2 T2 analog_coarse_gain. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	3	0x0000	Reserved					
	2:0	0x0000	ANALOG_GAIN_T1 T1 analog_coarse_gain. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	The analogue gain is controlled separately for each exposure in Context A. It is controlled by analog_coarse_gain[2:0] bits in ANALOG_GAIN (R0x3366), analog_fine_gain[3:0] bits in ANALOG_GAIN2 (R0x336A) and an analog_low_gain bit in ANALOG_LOW_GAIN (R0x33BE). Actual gain = 2^(analog_coarse_gain[2:0]-analog_low_gain)*(1+(analog_fine_gain[3:0]/16)). Correct operation of DLO requires the analogue gain to be set to the same value for each exposure in a context, with two exceptions. Exception 1: DLO allows a mixture of LCG and HCG exposures, enabled by the DC_GAIN bits in R0x3362. Exception 2: Alternatively, DLO allows two values of analogue gain to be used, enabled by the GCF bits in R0x3362. For either exception, DCG_TRIM (R0x3364) must be programmed with a value representing the analogue gain ratio between the exposures.							
R0x3368	**15:0**	**0x0000**	**ANALOG_GAIN_CB (R/W)**	**S**		**E**		**unsigned**
	15	X	Undefined					
	14:12	0x0000	ANALOG_GAIN_T4_CB T4 analog_coarse_gain for CB. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	11	X	Undefined					
	10:8	0x0000	ANALOG_GAIN_T3_CB T3 analog_coarse_gain for CB. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	7	X	Undefined					
	6:4	0x0000	ANALOG_GAIN_T2_CB T2 analog_coarse_gain for CB. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	3	X	Undefined					
	2:0	0x0000	ANALOG_GAIN_T1_CB T1 analog_coarse_gain for CB. 000: 1x, 001: 2x, 010: 4x, 011: 8x	**S**		**E**		unsigned
	The analogue gain is controlled separately for each exposure in Context B. It is controlled by analog_coarse_gain[2:0] bits in ANALOG_GAIN_CB (R0x3368), analog_fine_gain[3:0] bits in ANALOG_GAIN2_CB (R0x336C) and an analog_low_gain bit in ANALOG_LOW_GAIN (R0x33BE). Actual gain = 2^(analog_coarse_gain[2:0]-analog_low_gain)*(1+(analog_fine_gain[3:0]/16)). Correct operation of DLO requires the analogue gain to be set to the same value for each exposure in a context, with two exceptions. Exception 1: DLO allows a mixture of LCG and HCG exposures, enabled by the DC_GAIN bits in R0x3362. Exception 2: Alternatively, DLO allows two values of analogue gain to be used, enabled by the GCF bits in R0x3362. For either exception, DCG_TRIM (R0x3364) must be programmed with a value representing the analogue gain ratio between the exposures.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x336A	**15:0**	**0x0000**	**ANALOG_GAIN2 (R/W)**	**S**		**E**		**unsigned**
	15:12	0x0000	COL_FINE_GAIN_T4 T4 analog_fine_gain. 1x~2x(1/16 step)	**S**		**E**		unsigned
	11:8	0x0000	COL_FINE_GAIN_T3 T3 analog_fine_gain. 1x~2x(1/16 step)	**S**		**E**		unsigned
	7:4	0x0000	COL_FINE_GAIN_T2 T2 analog_fine_gain. 1x~2x(1/16 step)	**S**		**E**		unsigned
	3:0	0x0000	COL_FINE_GAIN_T1 T1 analog_fine_gain. 1x~2x(1/16 step)	**S**		**E**		unsigned
	Analog_fine_gain for each exposure in Context A. See ANALOG_GAIN (R0x3366) for the gain equation.							
R0x336C	**15:0**	**0x0000**	**ANALOG_GAIN2_CB (R/W)**	**S**		**E**		**unsigned**
	15:12	0x0000	COL_FINE_GAIN_T4_CB T4 analog_fine_gain for CB. 1x~2x(1/16 step)	**S**		**E**		unsigned
	11:8	0x0000	COL_FINE_GAIN_T3_CB T3 analog_fine_gain for CB. 1x~2x(1/16 step)	**S**		**E**		unsigned
	7:4	0x0000	COL_FINE_GAIN_T2_CB T2 analog_fine_gain for CB. 1x~2x(1/16 step)	**S**		**E**		unsigned
	3:0	0x0000	COL_FINE_GAIN_T1_CB T1 analog_fine_gain for CB. 1x~2x(1/16 step)	**S**		**E**		unsigned
	Analog_fine_gain for each exposure in Context B. See ANALOG_GAIN_CB (R0x3368) for the gain equation.							
R0x336E	**15:0**	**0x0000**	**DATAPATH_SELECT2 (R/W)**	**S**		**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	Reserved					
	13:0	X	Undefined					
	data-path control switches for 16-bit mode.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3370	**15:0**	**0x0100**	**DBLC_CONTROL (R/W)**			**E**		**unsigned**
	15	0x0000	DBLC_FS_TRIG_T4 manual trigger for t4, self clearing	**S**		**E**		unsigned
	14	0x0000	DBLC_FS_TRIG_T3 manual trigger for t3, self clearing	**S**		**E**		unsigned
	13	0x0000	DBLC_FS_TRIG_T2 manual trigger for t2, self clearing. In AR0825 REV1, bits [13:12] are also used to control FRAME_STYLE_CB.	**S**		**E**		unsigned
	12	0x0000	DBLC_FS_TRIG_T1 manual trigger for t1, self clearing. In AR0825 REV1, bits [13:12] are also used to control FRAME_STYLE_CB.	**S**		**E**		unsigned
	11:10	0x0000	Reserved					
	9	X	Undefined					
	8	0x0001	DBLC_EN_TOP_ROWS enable top rows in calculation. If clear, the top DBLC calculation registers will not be transferred to the correction registers. If set the top DBLC calculations will be transferred but may be averaged with the bottom rows during the transfer if the bottom rows are enabled. It is assumed that at least one of the enable top rows or enable bottom rows bits are set.	**S**		**E**		unsigned
	7:6	X	Undefined					
	5	0x0000	DBLC_EN_TEMPTRIG Enable temperature triggering. The DBLC measurements and calculations can be enabled or disabled from being triggered by changes in temperature. See R0x30B8.	**S**		**E**		unsigned
	4	0x0000	DBLC_EN_GAINTRIG enable gain triggering. The DBLC measurements and calculations enabled or disabled from being triggered by changes in analog gain and exposures.	**S**		**E**		unsigned
	3:2	0x0000	DBLC_FRAME_STYLE frame style. This register determines which 16 register subgroup of the 64 register TopCalc, 64 BtmCalc, or Correction groups is the source of data for the DBLC calculation. See also DBLC_FRAME_STYLE_CB (R0x3c74).	**S**		**E**		unsigned
	1	0x0000	DBLC_EMBED_EN enable embedded data. The DBLC data registers are only available for read access to the I2C or to the embedded stats output, but not both. Enabling reads onto embedded data will disable read access from the I2C. Write access is not affected.	**S**		**E**		unsigned
	0	0x0000	DBLC_ENABLE main enable for DBLC calculations and corrections.	**S**		**E**		unsigned
	Digital black level correction (DBLC) control register.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3372	**15:0**	**0x700F**	**DBLC_FS0_CONTROL (R/W)**			**E**		**unsigned**
	15	0x0000	DBLC_FS0_EVERY_FRAME frame style performs calculation on every frame			**E**		unsigned
	14	0x0001	Reserved					
	13	0x0001	Reserved					
	12	0x0001	Reserved					
	11	0x0000	DBLC_FS0_OFFSET_SEL Offset register selection for fs0. 0: use DBLC_OFFSET0, 1: use DBLC_OFFSET1.			**E**		unsigned
	10	0x0000	DBLC_FS0_OFFSET_EN frame style enable for offset.			**E**		unsigned
	9	0x0000	DBLC_FS0_SCALE_SEL Scaling register selection for fs0. 0: use DBLC_SCALE0, 1: use DBLC_SCALE1.			**E**		unsigned
	8	0x0000	DBLC_FS0_SCALE_EN frame style enable for scaling			**E**		unsigned
	7	0x0000	DBLC_FS0_HIST_SEL History register selection for fs0. 0: use DBLC_WEIGHT0, 1: use DBLC_WEIGHT1			**E**		unsigned
	6	0x0000	DBLC_FS0_HIST_EN frame style enable for history weighting			**E**		unsigned
	5:4	0x0000	DBLC_FS0_COLOR_MODE frame style color mode			**E**		unsigned
	3	0x0001	Reserved					
	2	0x0001	Reserved					
	1	0x0001	Reserved					
	0	0x0001	Reserved					
	DBLC settings for frame style 0. These settings are used if the dblc_frame_style field is set to 0.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3374	**15:0**	**0x700F**	**DBLC_FS1_CONTROL (R/W)**			**E**		**unsigned**
	15	0x0000	DBLC_FS1_EVERY_FRAME frame style performs calculation on every frame			**E**		unsigned
	14	0x0001	Reserved					
	13	0x0001	Reserved					
	12	0x0001	Reserved					
	11	0x0000	DBLC_FS1_OFFSET_SEL Offset register selection for fs1. 0: use DBLC_OFFSET0, 1: use DBLC_OFFSET1.			**E**		unsigned
	10	0x0000	DBLC_FS1_OFFSET_EN frame style enable for offset.			**E**		unsigned
	9	0x0000	DBLC_FS1_SCALE_SEL Scaling register selection for fs1. 0: use DBLC_SCALE0, 1: use DBLC_SCALE1.			**E**		unsigned
	8	0x0000	DBLC_FS1_SCALE_EN frame style enable for scaling			**E**		unsigned
	7	0x0000	DBLC_FS1_HIST_SEL History register selection for fs1. 0: use DBLC_WEIGHT0, 1: use DBLC_WEIGHT1			**E**		unsigned
	6	0x0000	DBLC_FS1_HIST_EN frame style enable for history weighting			**E**		unsigned
	5:4	0x0000	DBLC_FS1_COLOR_MODE frame style color mode			**E**		unsigned
	3	0x0001	Reserved					
	2	0x0001	Reserved					
	1	0x0001	Reserved					
	0	0x0001	Reserved					
	DBLC settings for frame style 1. These settings are used if the dblc_frame_style field is set to 1.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3376	**15:0**	**0x700F**	**DBLC_FS2_CONTROL (R/W)**			**E**		**unsigned**
	15	0x0000	DBLC_FS2_EVERY_FRAME frame style performs calculation on every frame			**E**		unsigned
	14	0x0001	Reserved					
	13	0x0001	Reserved					
	12	0x0001	Reserved					
	11	0x0000	DBLC_FS2_OFFSET_SEL Offset register selection for fs2. 0: use DBLC_OFFSET0, 1: use DBLC_OFFSET1.			**E**		unsigned
	10	0x0000	DBLC_FS2_OFFSET_EN frame style enable for offset.			**E**		unsigned
	9	0x0000	DBLC_FS2_SCALE_SEL Scaling register selection for fs2. 0: use DBLC_SCALE0, 1: use DBLC_SCALE1.			**E**		unsigned
	8	0x0000	DBLC_FS2_SCALE_EN frame style enable for scaling			**E**		unsigned
	7	0x0000	DBLC_FS2_HIST_SEL History register selection for fs2. 0: use DBLC_WEIGHT0, 1: use DBLC_WEIGHT1			**E**		unsigned
	6	0x0000	DBLC_FS2_HIST_EN frame style enable for history weighting			**E**		unsigned
	5:4	0x0000	DBLC_FS2_COLOR_MODE frame style color mode			**E**		unsigned
	3	0x0001	Reserved					
	2	0x0001	Reserved					
	1	0x0001	Reserved					
	0	0x0001	Reserved					
	DBLC settings for frame style 2. These settings are used if the dblc_frame_style field is set to 2.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3378	**15:0**	**0x700F**	**DBLC_FS3_CONTROL (R/W)**			**E**		**unsigned**
	15	0x0000	DBLC_FS3_EVERY_FRAME frame style performs calculation on every frame			**E**		unsigned
	14	0x0001	Reserved					
	13	0x0001	Reserved					
	12	0x0001	Reserved					
	11	0x0000	DBLC_FS3_OFFSET_SEL Offset register selection for fs3. 0: use DBLC_OFFSET0, 1: use DBLC_OFFSET1.			**E**		unsigned
	10	0x0000	DBLC_FS3_OFFSET_EN frame style enable for offset.			**E**		unsigned
	9	0x0000	DBLC_FS3_SCALE_SEL Scaling register selection for fs3. 0: use DBLC_SCALE0, 1: use DBLC_SCALE1.			**E**		unsigned
	8	0x0000	DBLC_FS3_SCALE_EN frame style enable for scaling			**E**		unsigned
	7	0x0000	DBLC_FS3_HIST_SEL History register selection for fs3. 0: use DBLC_WEIGHT0, 1: use DBLC_WEIGHT1			**E**		unsigned
	6	0x0000	DBLC_FS3_HIST_EN frame style enable for history weighting			**E**		unsigned
	5:4	0x0000	DBLC_FS3_COLOR_MODE frame style color mode			**E**		unsigned
	3	0x0001	Reserved					
	2	0x0001	Reserved					
	1	0x0001	Reserved					
	0	0x0001	Reserved					
	dblc settings for frame style 3. These settings are used if the dblc_frame_style field is set to three.							
R0x337E	**15:0**	**0x0000**	**DBLC_OFFSET0 (R/W)**			**E**		**unsigned**
	DBLC offset 0, format is s15.4							
R0x3380	**15:0**	**0x0000**	**DBLC_OFFSET1 (R/W)**			**E**		**unsigned**
	DBLC offset 1, format is s15.4							
R0x3382	**7:0**	**0x00FF**	**DBLC_WEIGHT0 (R/W)**			**E**		**unsigned**
	DBLC weight 0. weight0/256 is the weight give to history, (256-weight0)/256 is given to the current calculation.							
R0x3384	**7:0**	**0x00FF**	**DBLC_WEIGHT1 (R/W)**			**E**		**unsigned**
	DBLC weight 1. weight1/256 is the weight give to history, (256-weight1)/256 is given to the current calculation.							
R0x3386	**13:0**	**0x0000**	**DBLC_PEDESTAL (R/W)**			**E**		**unsigned**
	DBLC pedestal value to add to OB pixels. This addition can help keep these pixels from being clipped.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3388	**15:0**	**0x0000**	**TPG_CONTROL (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11:8	0x0000	TPG_NOISE1_AMPLITUDE Amplitude for noise1 generator. The amplitude is 2^tgp_noise1_amplitude.			**E**		unsigned
	7	0x0000	TPG_NOISE2_EN Enable noise2, noise generators for each exposure. These values are summed in after HDR decomposition. The amplitudes are given in tpg_nois2_amplitude.			**E**		unsigned
	6	0x0000	TPG_NOISE1_EN Enable noise1, the HDR noise generator. This signed generator is summed with the standard pattern before HDR decomposition. The amplitude is given by tpg_noise1_amplitude.			**E**		unsigned
	5:4	0x0000	TPG_MERGE_MODE 00: Replace data from the ADC in enabled regions. 01 : Add pattern data to data from the ADC in enabled regions. 1x: Overlay ADC data with rectangular blob data.			**E**		unsigned
	3:2	0x0000	TPG_MODE 00: Off; the standard pattern data and regions are zero. 01: Solid color; Color0 registers are used in stdpat region 1 and Color1 registers are used in stdpat region 2. 10: linearly increasing values (all codes); Color0 registers define the initial values and Color1 registers define the increment values. Values increment throughout the union of stdpat region 1 and stdpat region 2. The 24-bit counters used to implement this pattern will overflow when they reach their maximum value. 11: Rectangular area (blob); the color1 registers define the background color and the color0 registers define the blob color. The corners of the rectangular area are defined by (blob_x1, blob_y1) to (blob_x2, blob_y2). The counters used to define the rectangle update on any valid row type and any valid column type.			**E**		unsigned
	1	X	Undefined					
	0	0x0000	TPG_ENABLE Main enable for all functions			**E**		unsigned
	Test Pattern Generator (TPG) control register							
R0x338A	**7:0**	**0x0000**	**TPG_COLOR0_GR1_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit green1 value of color0.							
R0x338C	**15:0**	**0x0100**	**TPG_COLOR0_GR1_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit green1 value of color0.							
R0x338E	**7:0**	**0x0000**	**TPG_COLOR0_RED_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit red value of color0.							
R0x3390	**15:0**	**0x0200**	**TPG_COLOR0_RED_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit red value of color0.							
R0x3392	**7:0**	**0x0000**	**TPG_COLOR0_BLU_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit blue value of color0.							
R0x3394	**15:0**	**0x0300**	**TPG_COLOR0_BLU_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit blue value of color0.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3396	**7:0**	**0x0000**	**TPG_COLOR0_GR2_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit green2 value of color0.							
R0x3398	**15:0**	**0x0400**	**TPG_COLOR0_GR2_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit green2 value of color0.							
R0x339A	**7:0**	**0x0000**	**TPG_COLOR1_GR1_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit green1 value of color1.							
R0x339C	**15:0**	**0x0500**	**TPG_COLOR1_GR1_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit green1 value of color1.							
R0x339E	**7:0**	**0x0000**	**TPG_COLOR1_RED_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit red value of color1.							
R0x33A0	**15:0**	**0x0600**	**TPG_COLOR1_RED_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit red value of color1.							
R0x33A2	**7:0**	**0x0000**	**TPG_COLOR1_BLU_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit blue value of color1.							
R0x33A4	**15:0**	**0x0700**	**TPG_COLOR1_BLU_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit blue value of color1.							
R0x33A6	**7:0**	**0x0000**	**TPG_COLOR1_GR2_HI (R/W)**			**E**		**unsigned**
	High portion of 24-bit green2 value of color1.							
R0x33A8	**15:0**	**0x0800**	**TPG_COLOR1_GR2_LO (R/W)**			**E**		**unsigned**
	Low portion of 24-bit green2 value of color1.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x33AA	**15:0**	**0x1F03**	**TPG_STDPAT_REGION1 (R/W)**			**E**		**unsigned**
	15:13	X	Undefined					
	12	0x0001	COLS_ACTIVE_EN Columns Region: Active Columns enabled for TPG region 1.			**E**		unsigned
	11	0x0001	COLS_RRC_EN Columns Region: Row ROM Columns enabled for TPG region 1.			**E**		unsigned
	10:9	X	Undefined					
	8	0x0001	COLS_RNC_EN Columns Region: Row noise columns enabled for TPG region 1.			**E**		unsigned
	7	X	Undefined					
	6	0x0000	ROWS_ATR_BTM_EN Row Region: ATR bottom rows enabled for TPG region 1.			**E**		unsigned
	5	X	Undefined					
	4	0x0000	ROWS_ACTIVE_EN Row Region: Active rows enabled for TPG region 1.			**E**		unsigned
	3	X	Undefined					
	2	0x0000	ROWS_DDK_TOP_EN Row Region: DBLC top rows enabled for TPG region 1.			**E**		unsigned
	1	X	Undefined					
	0	0x0001	ROWS_DTR_TOP_EN Row Region: DTR top rows enabled for TPG region 1.			**E**		unsigned
	Region enables for standard pattern region 1. Region 1 is the intersection of the union of selected rows and selected columns. Where a sensor does not implement a particular row or column type, the enable bit has no effect.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x33AC	**15:0**	**0x0800**	**TPG_STDPAT_REGION2 (R/W)**			**E**		**unsigned**
	15:13	X	Undefined					
	12	0x0000	COLS_ACTIVE_EN Columns Region: Active Columns enabled for TPG region 2.			**E**		unsigned
	11	0x0001	COLS_RRC_EN Columns Region: Row Row Columns enabled for TPG region 2.			**E**		unsigned
	10:9	X	Undefined					
	8	0x0000	COLS_RNC_EN Columns Region: Row noise columns enabled for TPG region 2.			**E**		unsigned
	7	X	Undefined					
	6	0x0000	ROWS_ATR_BTM_EN Row Region: ATR bottom rows enabled for TPG region 2.			**E**		unsigned
	5	X	Undefined					
	4	0x0000	ROWS_ACTIVE_EN Row Region: Active rows enabled for TPG region 2.			**E**		unsigned
	3	X	Undefined					
	2	0x0000	ROWS_DDK_TOP_EN Row Region: DBLC top rows enabled for TPG region 2.			**E**		unsigned
	1	X	Undefined					
	0	0x0000	ROWS_DTR_TOP_EN Row Region: DTR top rows enabled for TPG region 2.			**E**		unsigned
	Region enables for standard pattern region 2. Region 2 is the intersection of the union of selected rows and selected columns. Where a sensor does not implement a particular row or column type, the enable bit has no effect.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x33AE	**15:0**	**0x1003**	**TPG_NOISE1_REGION (R/W)**			**E**		**unsigned**
	15:13	X	Undefined					
	12	0x0001	COLS_ACTIVE_EN Columns Region: Active Columns enabled for TPG region 1.			**E**		unsigned
	11	0x0000	COLS_RRC_EN Columns Region: Row Row Columns enabled for TPG region 1.			**E**		unsigned
	10:9	X	Undefined					
	8	0x0000	COLS_RNC_EN Columns Region: Row noise columns enabled for TPG region 1.			**E**		unsigned
	7	X	Undefined					
	6	0x0000	ROWS_ATR_BTM_EN Row Region: ATR bottom rows enabled for TPG region 1.			**E**		unsigned
	5	X	Undefined					
	4	0x0000	ROWS_ACTIVE_EN Row Region: Active rows enabled for TPG region 1.			**E**		unsigned
	3	X	Undefined					
	2	0x0000	ROWS_DDK_TOP_EN Row Region: DBLC top rows enabled for TPG region 1.			**E**		unsigned
	1	X	Undefined					
	0	0x0001	ROWS_DTR_TOP_EN Row Region: DTR top rows enabled for TPG region 1.			**E**		unsigned
	Region enables for noise generator 1.							
R0x33B0	**15:0**	**0x0000**	**TPG_NOISE2_REGION (R/W)**			**E**		**unsigned**
	15:13	X	Undefined					
	12	0x0000	COLS_ACTIVE_EN Columns Region: Active Columns enabled for TPG region 2.			**E**		unsigned
	11	0x0000	COLS_RRC_EN Columns Region: Row Row Columns enabled for TPG region 2.			**E**		unsigned
	10:9	X	Undefined					
	8	0x0000	COLS_RNC_EN Columns Region: Row noise columns enabled for TPG region 2.			**E**		unsigned
	7	X	Undefined					
	6	0x0000	ROWS_ATR_BTM_EN Row Region: ATR bottom rows enabled for TPG region 2.			**E**		unsigned
	5	X	Undefined					
	4	0x0000	ROWS_ACTIVE_EN Row Region: Active rows enabled for TPG region 2.			**E**		unsigned
	3	X	Undefined					
	2	0x0000	ROWS_DDK_TOP_EN Row Region: DBLC top rows enabled for TPG region 2.			**E**		unsigned
	1	X	Undefined					
	0	0x0000	ROWS_DTR_TOP_EN Row Region: DTR top rows enabled for TPG region 2.			**E**		unsigned
	Region enables for noise generator 2.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x33B2	**15:0**	**0x0000**	**TPG_NOISE2_AMPLITUDE (R/W)**			**E**		**unsigned**
	15:12	0x0000	TPG_NOISE2_T4_AMPLITUD T4 noise amplitude for noise generator 2. The amplitude is 2^tpg_noise2_t4_amplitude.			**E**		unsigned
	11:8	0x0000	TPG_NOISE2_T3_AMPLITUD T3 noise amplitude for noise generator 2. The amplitude is 2^tpg_noise2_t3_amplitude.			**E**		unsigned
	7:4	0x0000	TPG_NOISE2_T2_AMPLITUD T2 noise amplitude for noise generator 2. The amplitude is 2^tpg_noise2_t2_amplitude.			**E**		unsigned
	3:0	0x0000	TPG_NOISE2_T1_AMPLITUD T1 noise amplitude for noise generator 2. The amplitude is 2^tpg_noise2_t1_amplitude.			**E**		unsigned
	Per exposure mask to limit the noise generated from the LFSR.							
R0x33B4	**12:0**	**0x0000**	**TPG_BLOB_X1 (R/W)**			**E**		**unsigned**
	X value for upper left corner of blob.							
R0x33B6	**11:0**	**0x0000**	**TPG_BLOB_Y1 (R/W)**			**E**		**unsigned**
	Y value for upper left corner of blob.							
R0x33B8	**12:0**	**0x0000**	**TPG_BLOB_X2 (R/W)**			**E**		**unsigned**
	X value for lower right corner of blob.							
R0x33BA	**11:0**	**0x0000**	**TPG_BLOB_Y2 (R/W)**			**E**		**unsigned**
	Y value for lower right corner of blob.							
R0x33BC	**15:0**	**0x2000**	**TPG_HDR_RATIOS (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13	0x0001	TPG_HDR_SATURATE If set, saturate any exposure if the next shorter exposure is non zero.			**E**		unsigned
	12	0x0000	TPG_HDR_DECOMPOSE If set, standard patterns decompose the 24-bit pattern onto each exposure using the ratio fields. If clear, only 13-bits of the pattern are put onto all exposures.			**E**		unsigned
	11	X	Undefined					
	10:8	0x0000	TPG_T3_T4_RATIO Value to right shift exposure 3 by to get exposure 4.			**E**		unsigned
	7	X	Undefined					
	6:4	0x0000	TPG_T2_T3_RATIO Value to right shift exposure 2 by to get exposure 3.			**E**		unsigned
	3	X	Undefined					
	2:0	0x0000	TPG_T1_T2_RATIO Value to right shift exposure 1 by to get exposure 2.			**E**		unsigned
	HDR decomposition ratios and style. The 24-bit standard pattern, after adding noise 1, is right shifted by these ratios to extract values to place on each exposure. The value is then saturated if tpg_hdr_saturate is set and the next shorter exposure is not zero.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x33BE	**15:0**	**0x0000**	**ANALOG_LOW_GAIN (R/W)**	**S**		**E**		**unsigned**
	15:8	X	Undefined					
	7	0x0000	ANA_LO_GAIN_T4_CB T4 analog_low_gain for CB. 0: 1x, 1: 0.5x			**E**		unsigned
	6	0x0000	ANA_LO_GAIN_T3_CB T3 analog_low_gain for CB. 0: 1x, 1: 0.5x			**E**		unsigned
	5	0x0000	ANA_LO_GAIN_T2_CB T2 analog_low_gain for CB. 0: 1x, 1: 0.5x			**E**		unsigned
	4	0x0000	ANA_LO_GAIN_T1_CB T1 analog_low_gain for CB. 0: 1x, 1: 0.5x			**E**		unsigned
	3	0x0000	ANA_LO_GAIN_T4 T4 analog_low_gain. 0: 1x, 1: 0.5x			**E**		unsigned
	2	0x0000	ANA_LO_GAIN_T3 T3 analog_low_gain. 0: 1x, 1: 0.5x			**E**		unsigned
	1	0x0000	ANA_LO_GAIN_T2 T2 analog_low_gain. 0: 1x, 1: 0.5x			**E**		unsigned
	0	0x0000	ANA_LO_GAIN_T1 T1 analog_low_gain. 0: 1x, 1: 0.5x			**E**		unsigned
	Analog low gain. See ANALOG_GAIN (R0x3366) and ANALOG_GAIN_CB (R0x3368) for the gain equation.							
R0x33C0	**15:0**	**0x2000**	**OC_LUT_00 (R/W)**			**E**		**unsigned**
	Output compander knee point 0. All of the knee point registers are msb-aligned. For example, a programmed value of 0x2000 acts as 0x200 when the output is 12-bit data and acts as 0x2000 when the output is 16-bit data.							
R0x33C2	**15:0**	**0x4000**	**OC_LUT_01 (R/W)**			**E**		**unsigned**
	Output compander knee point 1							
R0x33C4	**15:0**	**0x8000**	**OC_LUT_02 (R/W)**			**E**		**unsigned**
	Output compander knee point 2							
R0x33C6	**15:0**	**0x8200**	**OC_LUT_03 (R/W)**			**E**		**unsigned**
	Output compander knee point 3							
R0x33C8	**15:0**	**0x8600**	**OC_LUT_04 (R/W)**			**E**		**unsigned**
	Output compander knee point 4							
R0x33CA	**15:0**	**0x8E00**	**OC_LUT_05 (R/W)**			**E**		**unsigned**
	Output compander knee point 5							
R0x33CC	**15:0**	**0x9E00**	**OC_LUT_06 (R/W)**			**E**		**unsigned**
	Output compander knee point 6							
R0x33CE	**15:0**	**0xBE00**	**OC_LUT_07 (R/W)**			**E**		**unsigned**
	Output compander knee point 7							
R0x33D0	**15:0**	**0xC200**	**OC_LUT_08 (R/W)**			**E**		**unsigned**
	Output compander knee point 8							
R0x33D2	**15:0**	**0xCA00**	**OC_LUT_09 (R/W)**			**E**		**unsigned**
	Output compander knee point 9							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x33D4	**15:0**	**0xDA00**	**OC_LUT_10 (R/W)**			**E**		**unsigned**
	Output compander knee point 10							
R0x33D6	**15:0**	**0xFA00**	**OC_LUT_11 (R/W)**			**E**		**unsigned**
	Output compander knee point 11							
R0x33D8	**15:0**	**0xFA00**	**OC_LUT_12 (R/W)**			**E**		**unsigned**
	Output compander knee point 12							
R0x33DA	**15:0**	**0xFA00**	**OC_LUT_13 (R/W)**			**E**		**unsigned**
	Output compander knee point 13							
R0x33DC	**15:0**	**0xFA00**	**OC_LUT_14 (R/W)**			**E**		**unsigned**
	Output compander knee point 14							
R0x33DE	**15:0**	**0xFA00**	**OC_LUT_15 (R/W)**			**E**		**unsigned**
	Output compander knee point 15							
R0x33E0	**15:0**	**0x0110**	**TEST_ASIL_ROWS (R/W)**			**E**		**unsigned**
	15:12	0x0000	TEST_ASIL_ROWS_ANALOG_TEST_TOP_ROWS_NR Number of ATR at the top of the image.			**E**		unsigned
	11:8	0x0001	TEST_ASIL_ROWS_ANALOG_TEST_BTM_ROWS_NR Number of ATR at the bottom of the image.			**E**		unsigned
	7:4	0x0001	TEST_ASIL_ROWS_DIGITAL_TEST_TOP_ROWS_NR Number of DTR at the top of the image.			**E**		unsigned
	3:0	0x0000	TEST_ASIL_ROWS_DIGITAL_TEST_BTM_ROWS_NR Number of DTR at the bottom of the image.			**E**		unsigned
	Configure the number of analog test rows (ATR) and digital test rows (DTR) at the top and the bottom of the output image. The number of top and bottom ATR is (ANALOG_TEST_TOP_ROWS_NR*2*8) and (ANALOG_TEST_BTM_ROWS_NR*2*8) respectively. The number of top and bottom ATR is also affected by the state of TEST_CTRL[0] (R0x33EE) . For other fields, number of rows is programmed value*8.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x33EE	**15:0**	**0x0F40**	**TEST_CTRL (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11:8	0x000F	Reserved					
	7	X	Undefined					
	6	0x0001	Reserved					
	5	0x0000	Reserved					
	4	0x0000	Reserved					
	3:1	0x0000	Reserved					
	0	0x0000	TEST_CTRL_TAR_ADDR_MODE For some values of READ_MODE2, setting this bit causes ATR value to change at the ROP rate. This allows the whole set of ATR to be sequenced using fewer output rows. Using this bit imposes the constraint that ANA-LOG_TEST_BTM_ROWS_NR is programmed with an even value. For example, with ANA-LOG_TEST_BTM_ROWS_NR=8 and this bit set to 0, each of the 16 ATRs would be sequenced 4 times generating 16*8=128 rows in the output image. With this bit set to 1, each of the 16 ATRs would be sequenced 1 time generating 16*8/4=32 rows in the output image. When READ_MODE2 for the current context is 7 or 9, the state of this bit is ignored and ATR value changes at the row rate.			**E**		unsigned
	Miscellaneous tests.							
R0x33F2	**11:0**	**0x0004**	**DUMMY_PIXEL_VALUE (R/W)**			**E**		**unsigned**
	Sets dummy pixel value to use in data type or virtual channel interleaving.							
R0x33F6	**15:0**	**0x0000**	**OC_LUT_CONTROL (R/W)**			**E**		**unsigned**
	15:3	X	Undefined					
	2	0x0000	OC_STOCHASTIC_RND_EN When asserted stochastic rounding (dithering) is enabled			**E**		unsigned
	1	0x0000	OC_SET_LUT_DEFAULT 0: The OC_LUT registers R0x33C0-R0x33DE must be programmed manually. 1: The OC_LUT registers are automatically programmed depending upon the setting of DATA_FORMAT_ACTUAL (R0x205c). The automatically-programmed values can be read back from the OC_LUT registers but cannot be changed (writes to the OC_LUT registers will be ignored).			**E**		unsigned
	0	X	Undefined					
	compand control register							
R0x3402	**15:0**	**0x0F08**	**X_OUTPUT_CONTROL (R/W)**			**E**		**unsigned**
	15	0x0000	X_OUTPUT_SIZE_EN 0: The X output size of the image is auto-calculated. 1: The X output size of the image is set by X_OUTPUT_SIZE.			**E**		unsigned
	14:13	X	Undefined					
	12:1	0x0784	X_OUTPUT_SIZE X Output size control for Context A.			**E**		unsigned
	0	X	Undefined					
	MIPI header frame X-size.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3406	**15:0**	**0x0F08**	**X_OUTPUT_CONTROL_CB (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	X_OUTPUT_CONTROL_EN_CB 0: The X output size of the image is auto-calculated. 1: The X output size of the image is set by X_OUTPUT_SIZE_B.	**S**		**E**		unsigned
	14:13	X	Undefined					
	12:1	0x0784	X_OUTPUT_SIZE_CB X Output size control for Context B.	**S**		**E**		unsigned
	0	X	Undefined					
	Context-B: MIPI header frame X-size.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x340A	**15:0**	**0x00F7**	**GPIO_CONTROL1 (R/W)**			**E**		**unsigned**
	15	0x0000	Reserved					
	14	0x0000	Reserved					
	13	0x0000	Reserved					
	12	0x0000	Reserved					
	11	0x0000	Reserved					
	10	0x0000	Reserved					
	9	0x0000	Reserved					
	8	0x0000	Reserved					
	7	0x0001	GPIO3_INPUT_DISABLE gpio3 ippd 0 - enable input buffer 1 - power down input buffer			**E**		unsigned
	6	0x0001	GPIO2_INPUT_DISABLE gpio2 ippd 0 - enable input buffer 1 - power down input buffer			**E**		unsigned
	5	0x0001	GPIO1_INPUT_DISABLE gpio1 ippd 0 - enable input buffer 1 - power down input buffer			**E**		unsigned
	4	0x0001	GPIO0_INPUT_DISABLE gpio0 ippd 0 - enable input buffer 1 - power down input buffer			**E**		unsigned
	3	0x0000	GPIO3_OUTPUT_ENABLE gpio3 oe 0 - disable output 1 - enable output			**E**		unsigned
	2	0x0001	GPIO2_OUTPUT_ENABLE gpio2 oe 0 - disable output 1 - enable output			**E**		unsigned
	1	0x0001	GPIO1_OUTPUT_ENABLE gpio1 oe 0 - disable output 1 - enable output			**E**		unsigned
	0	0x0001	GPIO0_OUTPUT_ENABLE gpio0 oe 0 - disable output 1 - enable output			**E**		unsigned
	pad controls which directly control pins of the pad cell.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x340C	**15:0**	**0x0000**	**GPIO_CONTROL2 (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11	0x0000	GPIO_HIDRV_EN GPIO hidrv enable use 0 for 1.8v use 1 for 2.8v			**E**		unsigned
	10:8	0x0000	GPIO_SLEW GPIO slew control			**E**		unsigned
	7:6	0x0000	GPIO3_ISEL gpio3 input select 0 - no input function 1 - OUTPUT_ENABLE_N 2 - TRIGGER 3 - STANDBY			**E**		unsigned
	5:4	0x0000	GPIO2_ISEL gpio2 input select 0 - no input function 1 - OUTPUT_ENABLE_N 2 - TRIGGER 3 - STANDBY			**E**		unsigned
	3:2	0x0000	GPIO1_ISEL gpio1 input select 0 - no input function 1 - OUTPUT_ENABLE_N 2 - TRIGGER 3 - STANDBY			**E**		unsigned
	1:0	0x0000	GPIO0_ISEL gpio0 input select 0 - no input function 1 - OUTPUT_ENABLE_N 2 - TRIGGER 3 - STANDBY			**E**		unsigned
	gpio input mapping controls and shared padcell controls							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x340E	**15:0**	**0x0210**	**GPIO_SELECT (R/W)**			**E**		**unsigned**
	15:12	0x0000	GPIO3_OSEL gpio3 output function selection			**E**		unsigned
	11:8	0x0002	GPIO2_OSEL gpio2 output function selection			**E**		unsigned
	7:4	0x0001	GPIO1_OSEL gpio1 output function selection			**E**		unsigned
	3:0	0x0000	GPIO0_OSEL gpio0 output function selection			**E**		unsigned
	GPIO output selection. 0: BOOT_STATUS[0]. 1: BOOT_STATUS[1]. 2: BOOT_STATUS[2]. 3: SHUTTER_READOUT (0-1 transition at the start of the shutter sequence, 1-0 transition at the start of the readout sequence). 4: FLASH. 5: SHUTTER. 6: LINE_VALID. 7: FRAME_VALID. 8: PIXCLK. 9: Logic zero. 10: Logic one. 11: NEW_ROW pulse 12: NEW_FRAME pulse 13,14,15: Reserved. The 3-bit BOOT_STATUS bus shows sensor internal state as follows: 0 and hard reset: EXTCLK is toggling SYS_CHECK. 0 and reset released: M3ROM upload in progress. 1: Critical OTPM upload in progress. 2: Non-critical OTPM upload in progress. 3: Register scan in progress. 4: Startup MBIST in progress (if implemented). 5: Test frame in progress. 6: Sensor in standby. 7: Sensor streaming. For GPIO output selection 6, 7, 8 the source is controlled by MIPI_VALIDS_EN (R0x31F8[1]) as follows: 0: Early (ODP) versions of signals. 1: Late (MIPI framer) versions of signals.								
R0x3410	**15:0**	**0x0010**	**LOW_POWER_CONTROL (R/W)**			**E**		**unsigned**
	15:5	X	Undefined					
	4	0x0001	Reserved					
	3:1	X	Undefined					
	0	0x0000	ENABLE Set chip to low power mode. This bit is read-only and can be made read/write by clearing R0x301A[3].			**E**		unsigned
	Low-power and safe-state control.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3418	**15:0**	**0x0000**	**LRE_GAIN_GRR_RED (R/W)**	**S**		**E**		**unsigned**
	15:8	0x0000	GREENR_LRE_GAIN	**S**		**E**		unsigned
	7:0	0x0000	RED_LRE_GAIN	**S**		**E**		unsigned
	Per-color gain for digital binning in Context A. When READ_MODE2 is used to select a digital binning mode, The per-color gain should be adjusted to avoid saturation. Each 8-bit value 0-0xFF corresponds to a digital gain of 256/256, 1/256, ..255/256. Suggested values for each digital binning mode are shown below: normal (RGGB): set all gains to 0 (256/256 - unity gain) hbin_dig, vbin_dig: set all gains to 128 (128/256) hvbin_dig, mono_dig: set all gains to 64 (64/128).							
R0x341A	**15:0**	**0x0000**	**LRE_GAIN_BLU_GRB (R/W)**	**S**		**E**		**unsigned**
	15:8	0x0000	BLUE_LRE_GAIN	**S**		**E**		unsigned
	7:0	0x0000	GREENB_LRE_GAIN	**S**		**E**		unsigned
	Per-colour gain for digital binning in Context B. See description of LRE_GAIN_GRR_RED.							
R0x341C	**15:0**	**0x0000**	**LRE_GAIN_GRR_RED_CB (R/W)**	**S**		**E**		**unsigned**
	15:8	0x0000	GREENR_LRE_GAIN_CB	**S**		**E**		unsigned
	7:0	0x0000	RED_LRE_GAIN_CB	**S**		**E**		unsigned
	Per-colour gain for digital binning in Context A. See description of LRE_GAIN_GRR_RED.							
R0x341E	**15:0**	**0x0000**	**LRE_GAIN_BLU_GRB_CB (R/W)**	**S**		**E**		**unsigned**
	15:8	0x0000	BLUE_LRE_GAIN_CB	**S**		**E**		unsigned
	7:0	0x0000	GREENB_LRE_GAIN_CB	**S**		**E**		unsigned
	Per-colour gain for digital binning in Context B. See description of LRE_GAIN_GRR_RED.							
R0x3420	**15:0**	**0x3020**	**I2CIDS0 (R/W)**			**E**		**unsigned**
	15:8	0x0030	I2CIDS_001 I2C addresses for SADDR[2:0]=1. Default is 0x30/0x31. Bit 0 is ignored.			**E**		unsigned
	7:0	0x0020	I2CIDS_000 I2C addresses for SADDR[2:0]=0. Default is 0x20/0x21. Bit 0 is ignored.			**E**		unsigned
	I2C addresses for SADDR[2:0]=0 and 1							
R0x3422	**15:0**	**0x6E6C**	**I2CIDS1 (R/W)**			**E**		**unsigned**
	15:8	0x006E	I2CIDS_011 I2C addresses for SADDR[2:0]=3. Default is 0x6e/0x6f. Bit 0 is ignored.			**E**		unsigned
	7:0	0x006C	I2CIDS_010 I2C addresses for SADDR[2:0]=2. Default is 0x6c/0x6d. Bit 0 is ignored.			**E**		unsigned
	I2C addresses for SADDR[2:0]=2 and 3							
R0x3424	**15:0**	**0x5040**	**I2CIDS2 (R/W)**			**E**		**unsigned**
	15:8	0x0050	I2CIDS_101 I2C addresses for SADDR[2:0]=5. Default is 0x50/0x51. Bit 0 is ignored.			**E**		unsigned
	7:0	0x0040	I2CIDS_100 I2C addresses for SADDR[2:0]=4. Default is 0x40/0x41. Bit 0 is ignored.			**E**		unsigned
	I2C addresses for SADDR[2:0]=4 and 5							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3426	**15:0**	**0x7060**	**I2CIDS3 (RO)**			**E**		**unsigned**
	15:8	RO	I2CIDS_111 I2C addresses for SADDR[2:0]=7. Hard coded to 0x70/0x71. Bit 0 is ignored.			**E**		unsigned
	7:0	RO	I2CIDS_110 I2C addresses for SADDR[2:0]=6. Hard coded to 0x60/0x61. Bit 0 is ignored.			**E**		unsigned
	I2C addresses for SADDR[2:0]=6 and 7							
R0x34C0	**15:0**	**0x0000**	**FUSE_ID1 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34C2	**15:0**	**0x0000**	**FUSE_ID2 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34C4	**15:0**	**0x0000**	**FUSE_ID3 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34C6	**15:0**	**0x0000**	**FUSE_ID4 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34C8	**15:0**	**0x0000**	**FUSE_ID5 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34CA	**15:0**	**0x0000**	**FUSE_ID6 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34CC	**15:0**	**0x0000**	**FUSE_ID7 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34CE	**15:0**	**0x0000**	**FUSE_ID8 (RO)**			**E**		**unsigned**
	Manufacturing ID							
R0x34DC	**5:0**	**0x0000**	**ASIL_EXT_CLK_COUNT_MSB_EXPECT (R/W)**			**E**		**unsigned**
	Target ext_clk count per frame (MSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34DE	**15:0**	**0x0000**	**ASIL_EXT_CLK_COUNT_LSB_EXPECT (R/W)**			**E**		**unsigned**
	Target ext_clk count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34E0	**5:0**	**0x0000**	**ASIL_CLK_PIX_COUNT_MSB_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_pix count per frame (MSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34E2	**15:0**	**0x0000**	**ASIL_CLK_PIX_COUNT_LSB_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_pix count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34E4	**5:0**	**0x0000**	**ASIL_CLK_OP_COUNT_MSB_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_op count per frame (MSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34E6	**15:0**	**0x0000**	**ASIL_CLK_OP_COUNT_LSB_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_op count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34E8	**5:0**	**0x0000**	**ASIL_CLK_REG_COUNT_MSB_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_reg count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34EA	**15:0**	**0x0000**	**ASIL_CLK_REG_COUNT_LSB_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_reg count per frame (LSB). See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x34EC	**10:0**	**0x0000**	**ASIL_CLK_PIX_COUNT_100_EXT_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_pix count for 100 ext_clk cycles. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34EE	**10:0**	**0x0000**	**ASIL_CLK_OP_COUNT_100_EXT_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_op count for 100 ext_clk cycles. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34F0	**10:0**	**0x0000**	**ASIL_CLK_REG_COUNT_100_EXT_EXPECT (R/W)**			**E**		**unsigned**
	Target clk_reg count for 100 ext_clk cycles. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34F2	**15:0**	**0x0000**	**ASIL_CLK_COUNT_THRESHOLD (R/W)**			**E**		**unsigned**
	15:12	0x0000	ASIL_CLK_REG_COUNT_THRESHOLD Clock count threshold per frame for clk_reg			**E**		unsigned
	11:8	0x0000	ASIL_CLK_OP_COUNT_THRESHOLD Clock count threshold per frame for clk_op			**E**		unsigned
	7:4	0x0000	ASIL_CLK_PIX_COUNT_THRESHOLD Clock count threshold per frame for clk_pix			**E**		unsigned
	3:0	0x0000	ASIL_EXT_CLK_COUNT_THRESHOLD Clock count threshold per frame for ext_clk			**E**		unsigned
	Clock count thresholds per frame. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x34F4	**15:0**	**0x0000**	**ASIL_CLK_COUNT_100_THRESHOLD (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11:8	0x0000	ASIL_CLK_REG_COUNT_100_THRESHOLD Clock count threshold per 100 ext_clk duration for clk_reg			**E**		unsigned
	7:4	0x0000	ASIL_CLK_OP_COUNT_100_THRESHOLD Clock count threshold per 100 ext_clk duration for clk_op			**E**		unsigned
	3:0	0x0000	ASIL_CLK_PIX_COUNT_100_THRESHOLD Clock count threshold per 100 ext_clk duration for clk_pix			**E**		unsigned
	Clock count threshold per 100 ext_clk cycles. See description of ASIL_EXT_CLK_COUNT_MSB (R0x2080).							
R0x35A0	**10:0**	**0x0080**	**GREEN1_GAIN_T2 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T2 exposure of Green1 (Gr) pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35A2	**10:0**	**0x0080**	**BLUE_GAIN_T2 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T2 exposure of Blue pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35A4	**10:0**	**0x0080**	**RED_GAIN_T2 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T2 exposure of Red pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35A6	**10:0**	**0x0080**	**GREEN2_GAIN_T2 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T2 exposure of Green2 (Gb) pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35A8	**10:0**	**0x0080**	**GREEN1_GAIN_T3 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T3 exposure of Green1 (Gr) pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35AA	**10:0**	**0x0080**	**BLUE_GAIN_T3 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T3 exposure of Blue pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35AC	**10:0**	**0x0080**	**RED_GAIN_T3 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T3 exposure of Red pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35AE	**10:0**	**0x0080**	**GREEN2_GAIN_T3 (R/W)**	**S**		**E**		**unsigned**
	Digital gain for T3 exposure of Green2 (Gb) pixels in Context A, in the format xxxx.yyyyyyy.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x35B0	10:0	0x0080	GREEN1_GAIN_T4 (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Green1 (Gr) pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35B2	10:0	0x0080	BLUE_GAIN_T4 (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Blue pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35B4	10:0	0x0080	RED_GAIN_T4 (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Red pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35B6	10:0	0x0080	GREEN2_GAIN_T4 (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Green2 (Gb) pixels in Context A, in the format xxxx.yyyyyyy.							
R0x35C0	10:0	0x0080	GREEN1_GAIN_T2_CB (R/W)	S		E		unsigned
	Digital gain for T2 exposure of Green1 (Gr) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35C2	10:0	0x0080	BLUE_GAIN_T2_CB (R/W)	S		E		unsigned
	Digital gain for T2 exposure of Blue pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35C4	10:0	0x0080	RED_GAIN_T2_CB (R/W)	S		E		unsigned
	Digital gain for T2 exposure of Red pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35C6	10:0	0x0080	GREEN2_GAIN_T2_CB (R/W)	S		E		unsigned
	Digital gain for T2 exposure of Green2 (Gb) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35C8	10:0	0x0080	GREEN1_GAIN_T3_CB (R/W)	S		E		unsigned
	Digital gain for T3 exposure of Green1 (Gr) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35CA	10:0	0x0080	BLUE_GAIN_T3_CB (R/W)	S		E		unsigned
	Digital gain for T3 exposure of Blue pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35CC	10:0	0x0080	RED_GAIN_T3_CB (R/W)	S		E		unsigned
	Digital gain for T3 exposure of Red pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35CE	10:0	0x0080	GREEN2_GAIN_T3_CB (R/W)	S		E		unsigned
	Digital gain for T3 exposure of Green2 (Gb) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35D0	10:0	0x0080	GREEN1_GAIN_T4_CB (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Green1 (Gr) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35D2	10:0	0x0080	BLUE_GAIN_T4_CB (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Blue pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35D4	10:0	0x0080	RED_GAIN_T4_CB (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Red pixels in Context B, in the format xxxx.yyyyyyy.							
R0x35D6	10:0	0x0080	GREEN2_GAIN_T4_CB (R/W)	S		E		unsigned
	Digital gain for T4 exposure of Green2 (Gb) pixels in Context B, in the format xxxx.yyyyyyy.							
R0x37A0	15:0	0x0001	COARSE_INTEGRATION_AD_TIME (R/W)	S		E		unsigned
	Coarse integration advance time for T1 exposure, Context A. The minimum value is 1. The maximum value is 15.							
R0x37A2	15:0	0x0001	COARSE_INTEGRATION_AD_TIME_CB (R/W)	S		E		unsigned
	Coarse integration advance time for T1 exposure, Context B. See description of COARSE_INTEGRATION_AD_TIME.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x37A4	**15:0**	**0x0000**	**COARSE_INTEGRATION_AD_TIME2 (R/W)**	**S**		**E**		**unsigned**
	Coarse integration advance time for T2 exposure, Context A. The minimum value is 0 or 1, depending upon the number of exposures in use, the analogue readout mode in use and the value of middle_integration. The maximum value is 15.							
R0x37A6	**15:0**	**0x0000**	**COARSE_INTEGRATION_AD_TIME2_CB (R/W)**	**S**		**E**		**unsigned**
	Coarse integration advance time for T2 exposure, Context B. See description of COARSE_INTEGRATION_AD_TIME2.							
R0x37A8	**15:0**	**0x0000**	**COARSE_INTEGRATION_AD_TIME3 (R/W)**	**S**		**E**		**unsigned**
	Coarse integration advance time for T3 exposure, Context A. The minimum value is 0 or 1, depending upon the number of exposures in use, the analogue readout mode in use and the value of middle_integration. The maximum value is 15.							
R0x37AA	**15:0**	**0x0000**	**COARSE_INTEGRATION_AD_TIME3_CB (R/W)**	**S**		**E**		**unsigned**
	Coarse integration advance time for T3 exposure, Context B. See description of COARSE_INTEGRATION_AD_TIME3.							
R0x37AC	**15:0**	**0x0000**	**COARSE_INTEGRATION_AD_TIME4 (R/W)**	**S**		**E**		**unsigned**
	Coarse integration advance time for T4 exposure, Context A. The minimum value is 0 or 1, depending upon the number of exposures in use, the analogue readout mode in use and the value of middle_integration. The maximum value is 15.							
R0x37AE	**15:0**	**0x0000**	**COARSE_INTEGRATION_AD_TIME4_CB (R/W)**	**S**		**E**		**unsigned**
	Coarse integration advance time for T4 exposure, Context B. See description of COARSE_INTEGRATION_AD_TIME4.							
R0x37E0	**15:0**	**0x8421**	**ROW_TX_RO_ENABLE (R/W)**	**S**		**E**		**unsigned**
	Context A control of TX pulses during READOUT. The setting must correspond to the analog readout mode set in READ_MODE2 as follows normal (RGGB): 0x8421 ggbin_ana: 0x0429 mono_ana: 0x000f							
R0x37E2	**15:0**	**0x000F**	**ROW_TX_RO_ENABLE_CB (R/W)**	**S**		**E**		**unsigned**
	Context B control. See description of ROW_TX_RO_ENABLE.							
R0x3C06	**15:0**	**0x1484**	**CONFIGURE_BUFFERS1 (R/W)**	**S**		**E**		**unsigned**
	15:8	0x0014	CONFIGURE_BUFFERS_T2 Number of delay buffers allocated to store the T2 exposure. Delay buffers are grouped by 4 per memory so configuration value must be divisible by 4.	**S**		**E**		unsigned
	7:0	0x0084	CONFIGURE_BUFFERS_T1 Number of delay buffers allocated to store the T1 exposure. Delay buffers are grouped by 4 per memory so configuration value must be divisible by 4.	**S**		**E**		unsigned
	Delay buffers memory configuration.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3C08	**15:0**	**0x000C**	**CONFIGURE_BUFFERS2 (R/W)**	**S**		**E**		**unsigned**
	15	0x0000	DB_DECOMPAND_TO_MIDDLE When bit is set, the dither if enabled is added/subtracted around the middle of the output code when decompanding.			**E**		unsigned
	14	0x0000	DB_EXPAND_KNEE_POINT unused.			**E**		unsigned
	13	0x0000	DB_MIN_EXP Control to adjust/correct delay buffer operation when the T1 and T2 data are read consecutively (equivalent to T2 integration time=0).			**E**		unsigned
	12	0x0000	DB_NOCOMPRESS unused.			**E**		unsigned
	11	0x0000	DB_MEM_PACK Doubles the amount of delay buffers available by writing 8 rows of data per memory. The bit is intended to be used when the column width has been reduced by half through digital binning or x-windowing.	**S**		**E**		unsigned
	10:9	X	Undefined					
	8	0x0000	CONFIGURE_BUFFERS_EN Use configure_buffers registers to assign number of delay buffers. Otherwise use hardcoded values (4-exposure: T1=132 rows, T2=20 rows, T3=12 rows. 3-exposure: T1=144 rows, T2=20 rows. 2-exposure: T1=164 rows).	**S**		**E**		unsigned
	7:0	0x000C	CONFIGURE_BUFFERS_T3 Number of delay buffers allocated to store the T3 exposure. Delay buffers are grouped by 4 per memory so configuration value must be divisible by 4.	**S**		**E**		unsigned
	Delay buffers memory configuration. A total of 164 lines of buffering are available.							
R0x3C0A	**15:0**	**0x0000**	**DELAY_BUFFER_CRC_FAULT_CONTROL (R/W)**			**E**		**unsigned**
	15:5	0x0000	DELAY_BUFFER_FAULT_PIXEL Defines the column/pixel number on which the fault is inserted during the test frame.			**E**		unsigned
	4	0x0000	DELAY_BUFFER_FAULT_INS Enable fault insertion on one pixel per line in the delay buffers. Enables delay buffer latent fault checking in Test Frame.			**E**		unsigned
	3	X	Undefined					
	2	0x0000	DELAY_BUFFER_SYS_CHECK_EN Enable delay buffers CRC fault check to be reported on the SYS_CHECK pin			**E**		unsigned
	1	0x0000	DELAY_BUFFER_CRC_FAULT_EN Enable delay buffers CRC fault check			**E**		unsigned
	0	0x0000	DELAY_BUFFER_CRC_FAULT_RESET Reset delay buffers CRC fault counters and flag. DELAY_BUFFER_CRC_FAULT_EN must be 1 in order to use this reset.			**E**		unsigned
	Delay buffers data and write/read pointer CRC fault check control. Faults are reported in DELAY_BUFFER_CRC_FAULTS_PER_FRAME (R0x206E) and DELAY_BUFFER_CRC_FAULT_FRAMES (R0x2070) and ASIL_STATUS_03 (R0x2066).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3C0E	15:0	0xFFFF	NOISE_LIMIT_LEVEL (R/W)	S		E		unsigned
	This setting is used when the digital black-level control (DBCL) row(s) of pixels are accumulated and averaged. If a pixel value is greater than or equal to the programmed value of NOISE_LIMIT_LEVEL then it is not included in the accumulation/average. NOISE_LIMIT_LEVEL is an unsigned value. This register has 16bit but only 14bit is used in RNC.							
R0x3C10	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_00 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_0. 0 if uncalibrated.							
R0x3C12	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_01 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_1. 0 if uncalibrated.							
R0x3C14	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_02 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_2. 0 if uncalibrated.							
R0x3C16	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_03 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_3. 0 if uncalibrated.							
R0x3C18	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_04 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_4. 0 if uncalibrated.							
R0x3C1A	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_05 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_5. 0 if uncalibrated.							
R0x3C1C	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_06 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_6. 0 if uncalibrated.							
R0x3C1E	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_07 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_7. 0 if uncalibrated.							
R0x3C20	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_08 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_8. 0 if uncalibrated.							
R0x3C22	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_09 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_9. 0 if uncalibrated.							
R0x3C24	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_10 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_20. 0 if uncalibrated.							
R0x3C26	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_11 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_11. 0 if uncalibrated.							
R0x3C28	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_12 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_12. 0 if uncalibrated.							
R0x3C2A	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_13 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_13. 0 if uncalibrated.							
R0x3C2C	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_14 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_14. 0 if uncalibrated.							
R0x3C2E	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_15 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_15. 0 if uncalibrated.							
R0x3C30	11:0	0x0000	TEMPVSENS_BOOST_CAL_SLOPE_16 (R/W)			E		unsigned
	Calibration slope for TEMPVSENS0_BOOST_MEAS_16. 0 if uncalibrated.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3C32	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_SLOPE_17 (R/W)**			**E**		**unsigned**
	Calibration slope for TEMPVSENS0_BOOST_MEAS_17. 0 if uncalibrated.							
R0x3C34	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_SLOPE_18 (R/W)**			**E**		**unsigned**
	Unused.							
R0x3C36	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_SLOPE_19 (R/W)**			**E**		**unsigned**
	Unused.							
R0x3C38	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_SLOPE_20 (R/W)**			**E**		**unsigned**
	Unused.							
R0x3C40	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_12 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_4. 0 if uncalibrated.							
R0x3C42	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_14 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_5. 0 if uncalibrated.							
R0x3C44	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_15 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_6. 0 if uncalibrated.							
R0x3C46	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_16 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_7. 0 if uncalibrated.							
R0x3C48	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_17 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_8. 0 if uncalibrated.							
R0x3C4A	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_18 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_9. 0 if uncalibrated.							
R0x3C4C	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_19 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_10. 0 if uncalibrated.							
R0x3C4E	**11:0**	**0x0000**	**TEMPVSENS_BOOST_CAL_OFFSET_20 (R/W)**			**E**		**unsigned**
	Calibration offset for TEMPVSENS0_BOOST_MEAS_11. 0 if uncalibrated.							
R0x3C60	**11:0**	**0x0000**	**TEMPVSENS1_VMON_CAL_SLOPE_0 (R/W)**			**E**		**unsigned**
	Calibration slope for TEMPVSENS1_VMON_MEAS_0. 0 if uncalibrated.							
R0x3C70	**0:0**	**0x0000**	**DBLC_SEPARATE_DISABLE (R/W)**	**S**		**E**		**unsigned**
	0: Digital black-level correction (DBLC) average calculation and correction is applied per-color. 1: All colors are averaged together to calculate a single DBLC value which is applied to applied to all pixels.							
R0x3C72	**15:0**	**0x0001**	**TEMP_FLAG_CONTROL (R/W)**			**E**		**unsigned**
	15:1	X	Undefined					
	0	0x0001	TEMP_FLAG_ENABLE	**S**		**E**		unsigned
	Controls OE of TEMP_FLAG port .							
R0x3C74	**15:0**	**0x0000**	**DBLC_CONTROL_CB (R/W)**			**E**		**unsigned**
	15:2	X	Undefined					
	1:0	0x0000	DBLC_FRAME_STYLE_CB frame style, Context B. This register determines which 16 register sub-group of the 64 register TopCalc, 64 BtmCalc, or Correction groups is the source of data for the DBLC calculation.	**S**		**E**		unsigned
	Digital black level correction (DBLC) control register, Context B.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3E6E	**15:0**	**0x1F40**	**TEMPVSENS1_TMG_CTRL_K0 (R/W)**			**E**		**unsigned**
	15:13	0x0000	Reserved					
	12:0	0x1F40	TEMPSENS1_RED_TEMP_CODE_K Temperature compare value in kelvin			**E**		unsigned
	Temperature compare value in kelvin							
R0x3E70	**15:0**	**0x0110**	**TEMPVSENS1_TMG_CTRL_K1 (R/W)**			**E**		**unsigned**
	15:10	X	Undefined					
	9:8	0x0001	TEMPSENS1_YELLOW_HYST_K Temperature compare hysterisis in kelvin			**E**		unsigned
	7	X	Undefined					
	6:0	0x0010	TEMPSENS1_YELLOW_OFF_RED_K Temperature compare offset in kelvin			**E**		unsigned
	When TEMPVSENS1_EN_CTRL[8]=1, the comparators that generate the Red and Yellow flags perform comparisons on temperature values in kelvin. This register controls the thresholds for generating the Red and Yellow flags. See also R0x3E6E.							
R0x3E98	**15:0**	**0x4000**	**TEMPVSENS1_EN_CTRL (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14:12	0x0004	Reserved					
	11:10	X	Undefined					
	9	0x0000	TEMPSENS1_TEST_CTRL_MODE test control setting. Used in conjunction with TEST_CTRL[3:0] in R0x3F92.			**E**		unsigned
	8	0x0000	TEMPSENS1_TEMP_COMP_EN_K 0: Yellow and Red flag generation uses comparison of raw ADC temperature codes. 1: Yellow and Red flag generation uses comparison of temperatures in kelvin.			**E**		unsigned
	7:5	X	Undefined					
	4	0x0000	Reserved					
	3	0x0000	Reserved					
	2	0x0000	Reserved					
	1	0x0000	Reserved					
	0	0x0000	Reserved					
	TempVolt Sensor control							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3EE0	**15:0**	**0x0700**	**TEMPVSENS1_FLAG_CTRL_EXT (R/W)**			**E**		**unsigned**
	15:11	X	Undefined					
	10:8	0x0007	TEMPVSENS1_RED_TEMP_CODE Upper 3 bits of temp compare/red_temp_code from R0x3F96; Compare against temp value, if temp_comp > temp value then the red flag is set.			**E**		unsigned
	7	X	Undefined					
	6:3	0x0000	TEMPVSENS1_YELLOW_OFF_RED Upper 4 bits of temp compare offset/yellow_off_red from R0x3F96.			**E**		unsigned
	2:0	0x0000	TEMPVSENS1_YELLOW_HYST Upper 3 bits of yellow flag hysteresis from R0x3F96.			**E**		unsigned
	Extended tempsensor flag control register							
R0x3EE2	**15:0**	**0x0000**	**TEMPSENS1_CTRL_REG_EXT (R/W)**			**E**		**unsigned**
	15:3	X	Undefined					
	2:0	0x0000	RETRIGGER1_THRESHOLD Upper 3 bits of retrigger threshold from R0x30B8.			**E**		unsigned
	Extended tempsensor control register							
R0x3EE4	**2:0**	**0x0007**	**TEMPVSENS0_SHUTTER_RESET_EN (R/W)**			**E**		**unsigned**
	Indicates whether pre_cond and tempsense0_sample_* signals have to be generated during Shutter (integration) or Readout phase for the current MUX address(corresponding to the bit position). 0: shutter phase ; 1: readout phase							
R0x3F60	**15:0**	**0x0000**	**ASIL_CHECK_ENABLES_00 (R/W)**			**E**		**unsigned**
	15	0x0000	ASIL_CHK_CLK_REG_100_PARAM Enable clk_reg for 100 ext_clk check.	**S**		**E**		unsigned
	14	0x0000	ASIL_CHK_CLK_OP_100_PARAM Enable clk_op for 100 ext_clk check.	**S**		**E**		unsigned
	13	0x0000	ASIL_CHK_CLK_PIX_100_PARAM Enable clk_pix for 100 ext_clk check.	**S**		**E**		unsigned
	12	0x0000	ASIL_CHK_CLK_REG_PARAM Enable clk_reg per frame check.	**S**		**E**		unsigned
	11	0x0000	ASIL_CHK_CLK_OP_PARAM Enable clk_op per frame check.	**S**		**E**		unsigned
	10	0x0000	ASIL_CHK_CLK_PIX_PARAM Enable clk_pix per frame check.	**S**		**E**		unsigned
	9	0x0000	ASIL_CHK_EXT_CLK_PARAM Enable ext_clk per frame check.	**S**		**E**		unsigned
	8:1	X	Undefined					
	0	0x0000	Reserved					
	Each bit of this register enables a particular ASIL check. See ASIL_PIN_ENABLES_00 and ASIL_STATUS_00.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F62	**15:0**	**0x0000**	**ASIL_CHECK_ENABLES_01 (R/W)**	**S**		**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	CHECK_RRC_ADDR Enable row ROM address sequence (enable CRC generation on row ROM address sequence) check. R0x32A8[15:12] selects the fields to be included in the row ROM CRC. The calculated CRC in RRC_CHECK_ADDR_CRC_VALUE is compared against the expected value programmed into RRC_CHECK_ADDR_CRC_EXPECT.	**S**		**E**		unsigned
	13	0x0000	CHECK_RRC_LEGAL Enable RRC columns legal pixel values (not between thresholds) check.	**S**		**E**		unsigned
	12	0x0000	CHECK_PT2 Enable pixout test 2 (pixels must be above a threshold) check.	**S**		**E**		unsigned
	11	0x0000	CHECK_PT1 Enable pixout test 1 (pixels must be below a threshold) check.	**S**		**E**		unsigned
	10	0x0000	CHECK_ZT_BA_VALUE Enable zebra BA rows correct values (high enough or low enough) check.	**S**		**E**		unsigned
	9	0x0000	CHECK_ZT_BA_LEGAL Enable zebra BA rows legal pixel values (not between thresholds) check.	**S**		**E**		unsigned
	8	0x0000	CHECK_ZT_AB_VALUE Enable zebra AB rows correct values (high enough or low enough) check.	**S**		**E**		unsigned
	7	0x0000	CHECK_ZT_AB_LEGAL Enable zebra AB rows legal pixel values (not between thresholds) check.	**S**		**E**		unsigned
	6	0x0000	CHECK_OT2_HIGH Enable overdrive 2 rows high pixel value check.	**S**		**E**		unsigned
	5	0x0000	CHECK_OT2_LOW Enable overdrive 2 rows low pixel value check.	**S**		**E**		unsigned
	4	0x0000	CHECK_OT1_HIGH Enable overdrive 1 rows high pixel value check.	**S**		**E**		unsigned
	3	0x0000	CHECK_OT1_LOW Enable overdrive 1 rows low pixel value check.	**S**		**E**		unsigned
	2	0x0000	CHECK_MT2 Enable ADC memory test 2 check.	**S**		**E**		unsigned
	1	0x0000	CHECK_MT1 Enable ADC memory test 1 check.	**S**		**E**		unsigned
	0	0x0000	CHECK_CRT Enable column ROM CRC check. The calculated CRC in ATR_CHECK_CRT_CRC_VALUE is compared against the expected value programmed into ATR_CHECK_CRT_CRC_EXPECT.	**S**		**E**		unsigned
	Each bit of this register enables a particular ASIL check. See ASIL_PIN_ENABLES_01 and ASIL_STATUS_01.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F64	**15:0**	**0x0000**	**ASIL_CHECK_ENABLES_02 (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	ROW_FRAME_CRC_ENABLE Enable image row or frame CRC generation and check, configured by CRC_CONTROL_REG. The calculated CRC in CRC_FR_DTR_CALC_CHECKSUM_HIGH/ CRC_FR_CALC_CHECKSUM_LOW is compared against the expected value programmed into CRC_FR_DTR_WRT_CHECKSUM_HIGH/ CRC_FR_WRT_CHECKSUM_LOW.			**E**		unsigned
	13	0x0000	DTR_CRC_ENABLE Enable DTR region CRC calculation and check. The calculated CRC in CRC_FR_DTR_CALC_CHECKSUM_HIGH/ CRC_DTR_CALC_CHECKSUM_LOW is compared against the expected value programmed into CRC_FR_DTR_WRT_CHECKSUM_HIGH/ CRC_DTR_WRT_CHECKSUM_LOW.			**E**		unsigned
	12	0x0000	SEQUENCER_ECC_SEC_ENABLE Enable sequencer RAM ECC SEC check.			**E**		unsigned
	11	0x0000	SEQUENCER_ECC_DED_ENABLE Enable sequencer RAM ECC DED check.			**E**		unsigned
	10	0x0000	SHUTTER_CRC_ENABLE Enable shutter state machine CRC check.			**E**		unsigned
	9:7	X	Undefined					
	6	0x0000	Reserved					
	5	0x0000	DBLC_RAM_ECC_SEC_ENABLE Enable DBLC RAM SEC ECC check.			**E**		unsigned
	4	0x0000	DBLC_RAM_ECC_DED_ENABLE Enable DBLC RAM DED ECC check.			**E**		unsigned
	3:1	X	Undefined					
	0	0x0000	EMBEDDED_CRC_ENABLE Enable embedded CRC calculation and check, configured by CRC_CONTROL_REG. The calculated CRC in CRC_EMB_CALC_CHECKSUM is compared against the expected value programmed into CRC_EMB_WRT_CHECKSUM.			**E**		unsigned
	Each bit of this register enables a particular ASIL check. See ASIL_PIN_ENABLES_02 and ASIL_STATUS_02.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F66	**15:0**	**0x0003**	**ASIL_STARTUP_ENABLES_00 (R/W)**			**E**		**unsigned**
	15:8	X	Undefined					
	7	0x0000	MASK_TEST_FRAME Mask output of test frame (prevent it from propagating off-chip). This bit is write-only due to an AR0825 REV2 design bug.			**E**		unsigned
	6	0x0000	EN_TEST_FRAME Enable test frame for startup checks. After writing 1, this bit remains set until the test frame completes and then self-clears. This bit should only be set when the sensor is in standby.			**E**		unsigned
	5	X	Undefined					
	4	0x0000	Reserved					
	3	0x0000	EN_PDI_SCAN Enable PDI cache scan. The results are recorded in PDIM_CALC_CHECKSUM (R0x3322) and checked against the value in PDIM_WRT_CHECKSUM (R0x331A). The PDI cache scan can be run automatically after reset or can be triggered manually. After writing 1, this bit remains set until the PDI cache scan completes and then self-clears.			**E**		unsigned
	2	0x0000	EN_IREG_SCAN Enable register scan. The results are recorded in IREG_CALC_CHECKSUM (R0x3320) and checked against the value in IREG_WRT_CHECKSUM (R0x3318). This register scan can be run automatically after reset or can be triggered manually when the sensor is in standby. After writing 1, this bit remains set until the register scan completes and then self-clears.			**E**		unsigned
	1	0x0001	EN_OTPM_SCAN Enable OTPM cache scan. The results are recorded in OTPM_CALC_CHECKSUM (R0x331E) and checked against the value in OTPM_WRT_CHECKSUM (R0x3316). This bit is set at reset and cleared when the scan has completed. The OTPM cache scan runs as part of the internal startup sequence. Therefore, the bit will always read back as zero, but the non-zero value in OTPM_CALC_CHECKSUM shows that the scan has been performed. Writing a 1 to this bit has no effect because the scan can only be re-run by performing a hard or soft reset.			**E**		unsigned
	0	0x0001	EN_M3ROM_SCAN Enable M3 ROM scan. The results are recorded in M3ROM_CALC_CHECKSUM (R0x331C) and checked against the value in M3ROM_WRT_CHECKSUM (R0x31D8). This bit is set at reset and cleared when the scan has completed. The M3 ROM scan runs as part of the internal startup sequence. Therefore, the bit will always read back as zero, but the non-zero value in M3ROM_CALC_CHECKSUM shows that the scan has been performed. Writing a 1 to this bit has no effect because the scan can only be re-run by performing a hard or soft reset.			**E**		unsigned
	Each bit of this register enables a particular ASIL startup check. See ASIL_STARTUP_PIN_ENABLES_00 and ASIL_STARTUP_STATUS_00.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F68	**15:0**	**0x0000**	**ASIL_PIN_ENABLES_00 (R/W)**			**E**		**unsigned**
	15	0x0000	ASIL_PIN_CLK_REG_100_PARAM Enable result of the clk_reg for 100 ext_clk check onto the SYS_CHECK pin.			**E**		unsigned
	14	0x0000	ASIL_PIN_CLK_OP_100_PARAM Enable result of the clk_op for 100 ext_clk check onto the SYS_CHECK pin.			**E**		unsigned
	13	0x0000	ASIL_PIN_CLK_PIX_100_PARAM Enable result of the clk_pix for 100 ext_clk check onto the SYS_CHECK pin.			**E**		unsigned
	12	0x0000	ASIL_PIN_CLK_REG_PARAM Enable result of clk_reg per frame check onto the SYS_CHECK pin.			**E**		unsigned
	11	0x0000	ASIL_PIN_CLK_OP_PARAM Enable result of the clk_op per frame check onto the SYS_CHECK pin.			**E**		unsigned
	10	0x0000	ASIL_PIN_CLK_PIX_PARAM Enable result of clk_pix per frame check onto the SYS_CHECK pin.			**E**		unsigned
	9	0x0000	ASIL_PIN_EXT_CLK_PARAM Enable result of ext_clk per frame check onto the SYS_CHECK pin.			**E**		unsigned
	8:1	X	Undefined					
	0	0x0000	Reserved					
	Each bit enables a failure of the corresponding check to assert the SYS_CHECK pin.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F6A	**15:0**	**0x0000**	**ASIL_PIN_ENABLES_01 (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	EN_PIN_RRC_ADDR Enable result of the row ROM address sequence check onto the SYS_CHECK pin.			**E**		unsigned
	13	0x0000	EN_PIN_RRC_LEGAL Enable result of the row ROM legal pixel value check onto the SYS_CHECK pin.			**E**		unsigned
	12	0x0000	EN_PIN_PT2 Enable result of the pixout 2 check onto the SYS_CHECK pin.			**E**		unsigned
	11	0x0000	EN_PIN_PT1 Enable result of the pixout 1 check onto the SYS_CHECK pin.			**E**		unsigned
	10	0x0000	EN_PIN_ZT_BA_VALUE Enable result of the zebra BA correct value check onto the SYS_CHECK pin.			**E**		unsigned
	9	0x0000	EN_PIN_ZT_BA_LEGAL Enable result of the zebra BA legal check onto the SYS_CHECK pin.			**E**		unsigned
	8	0x0000	EN_PIN_ZT_AB_VALUE Enable result of the zebra AB correct value check onto the SYS_CHECK pin.			**E**		unsigned
	7	0x0000	EN_PIN_ZT_AB_LEGAL Enable result of the zebra AB legal check onto the SYS_CHECK pin.			**E**		unsigned
	6	0x0000	EN_PIN_OT2_HIGH Enable result of the OT2 high check onto the SYS_CHECK pin.			**E**		unsigned
	5	0x0000	EN_PIN_OT2_LOW Enable result of the OT2 low check onto the SYS_CHECK pin.			**E**		unsigned
	4	0x0000	EN_PIN_OT1_HIGH Enable result of the OT1 high result onto the SYS_CHECK pin.			**E**		unsigned
	3	0x0000	EN_PIN_OT1_LOW Enable result of the OT1 low check onto the SYS_CHECK pin.			**E**		unsigned
	2	0x0000	EN_PIN_MT2 Enable result of the MT2 check onto the SYS_CHECK pin.			**E**		unsigned
	1	0x0000	EN_PIN_MT1 Enable result of the MT1 check onto the SYS_CHECK pin.			**E**		unsigned
	0	0x0000	EN_PIN_CRT Enable result of the CRT (column ROM) check onto the SYS_CHECK pin.			**E**		unsigned
	Each bit enables a failure of the corresponding check to assert the SYS_CHECK pin.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F6C	**15:0**	**0x0000**	**ASIL_PIN_ENABLES_02 (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14	0x0000	ROW_FRAME_CRC_PIN_ENABLE Enables the result of the image frame/row CRC check onto the SYS_CHECK pin.			**E**		unsigned
	13	0x0000	DTR_CRC_PIN_ENABLE Enable the result of the DTR CRC check onto the SYS_CHECK pin.			**E**		unsigned
	12	0x0000	SEQUENCER_ECC_SEC_PIN_ENABLE Enable the result of the sequencer RAM SEC ECC check onto the SYS_CHECK pin.			**E**		unsigned
	11	0x0000	SEQUENCER_ECC_DED_PIN_ENABLE Enable the result of the sequencer RAM DED ECC check onto the SYS_CHECK pin.			**E**		unsigned
	10	0x0000	SHUTTER_CRC_PIN_ENABLE Enable the result of the shutter state machine CRC check onto the SYS_CHECK pin.			**E**		unsigned
	9:7	X	Undefined					
	6	0x0000	DBLC_STATE_PARITY_PIN_ENABLE Enable result of the DBLC state machine parity check onto the SYS_CHECK pin.			**E**		unsigned
	5	0x0000	DBLC_RAM_ECC_SEC_PIN_ENABLE Enable result of the DBLC RAM ECC SEC check onto the SYS_CHECK pin.			**E**		unsigned
	4	0x0000	DBLC_RAM_ECC_DED_PIN_ENABLE Enable result of the DBLC RAM ECC DED check onto the SYS_CHECK pin.			**E**		unsigned
	3:1	X	Undefined					
	0	0x0000	EMBEDDED_CRC_PIN_ENABLE Enables result of the embedded CRC check onto the SYS_CHECK pin.			**E**		unsigned
	Each bit enables a failure of the corresponding check to assert the SYS_CHECK pin.							
R0x3F6E	**15:0**	**0x0000**	**ASIL_STARTUP_PIN_ENABLES_00 (R/W)**			**E**		**unsigned**
	15:4	X	Undefined					
	3	0x0000	PIN_ENABLE_PDI_CACHE_SCAN Enable result of the PDI cache scan check onto the SYS_CHECK pin.			**E**		unsigned
	2	0x0000	PIN_ENABLE_REGISTER_SCAN Enable result of the register scan check onto the SYS_CHECK pin.			**E**		unsigned
	1	0x0000	PIN_ENABLE_OTPM_CACHE_SCAN Enable result of the OTPM cache scan check onto the SYS_CHECK pin.			**E**		unsigned
	0	0x0000	PIN_ENABLE_M3_ROM_SCAN Enable result of the M3 ROM scan check on the SYS_CHECK pin.			**E**		unsigned
	Each bit enables a failure of the corresponding check to assert the SYS_CHECK pin.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F70	**15:0**	**0x0000**	**PROCESS_DTR (R/W)**			**E**		**unsigned**
	15:12	X	Undefined					
	11	0x0000	Reserved					
	10	0x0000	Reserved					
	9	0x0000	DTR_PEDESTAL Enable pedestal on DTR rows			**E**		unsigned
	8	0x0000	DTR_POST_HDR_GAIN_DITHER Enable post-HDR gain dither on DTR rows			**E**		unsigned
	7	0x0000	DTR_POST_HDR_GAIN Enable post-HDR gain on DTR rows			**E**		unsigned
	6	0x0000	DTR_PRE_HDR_GAIN_DITHER Enable pre-HDR gain dither on DTR rows			**E**		unsigned
	5	0x0000	DTR_PRE_HDR_GAIN Enable pre-HDR gain on DTR rows			**E**		unsigned
	4	0x0000	DTR_DEF_CORR Enable defect correction on DTR rows. When this bit is set, addition and subtraction of noise pedestal is also enabled; the state of the DTR_NOISE_PEDESTAL bit is ignored.			**E**		unsigned
	3:2	X	Undefined					
	1	0x0000	DTR_RNC Enable RNC on DTR rows			**E**		unsigned
	0	X	Undefined					
	Control the way in which DTR rows are processed.							
R0x3F72	**0:0**	**0x0000**	**ASIL_CRC_ENABLES (R/W)**					**unsigned**
	Embedded CRC calculation enable							
R0x3F74	**15:0**	**0x0000**	**ASIL_CHECK_ENABLES_04 (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13	0x0000	CTX_ECC_2BIT_CHECK_EN Enable Context RAM ECC check to flag DED (2-bit) error.			**E**		unsigned
	12	0x0000	CTX_ECC_1BIT_CHECK_EN Enable Context RAM ECC to flag SEC (1-bit) error. A 1-bit error is corrected but can also be flagged when the event happens.			**E**		unsigned
	11:0	X	Undefined					
	Each bit of this register enables a particular ASIL check. See ASIL_PIN_ENABLES_04 and ASIL_STATUS_04.							
R0x3F76	**15:0**	**0x0000**	**ASIL_PIN_ENABLES_04 (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13	0x0000	CTX_ECC_2BIT_PIN_EN Enable result of the Context RAM ECC DED check onto the SYS_CHECK pin.			**E**		unsigned
	12	0x0000	CTX_ECC_1BIT_PIN_EN Enable result of the Context RAM ECC SEC check onto the SYS_CHECK pin.			**E**		unsigned
	11:0	X	Undefined					
	Each bit enables a failure of the corresponding check to assert the SYS_CHECK pin.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F7C	**15:0**	**0x0000**	**ASIL_CHECK_ENABLES_07 (R/W)**			**E**		**unsigned**
	15:1	X	Undefined					
	0	0x0000	ASIL_CHK_LRE_CRC Enable Line Reorder Engine CRC error check.			**E**		unsigned
	Each bit of this register enables a particular ASIL check. See ASIL_PIN_ENABLES_07 and ASIL_STATUS_07.							
R0x3F7E	**15:0**	**0x0000**	**ASIL_PIN_ENABLES_07 (R/W)**			**E**		**unsigned**
	15:1	X	Undefined					
	0	0x0000	ASIL_PIN_LRE_CRC Enable result of the Reorder Engine CRC error check onto the SYS_CHECK pin.			**E**		unsigned
	Each bit enables a failure of the corresponding check to assert the SYS_CHECK pin.							
R0x3F92	**15:0**	**0x1400**	**TEMPVSENS1_TMG_CTRL (R/W)**			**E**		**unsigned**
	15	0x0000	TEMP1_ADDR_LOCK set to ensure bottom temperature conversions are doing temperature only			**E**		unsigned
	14	0x0000	Reserved					
	13	0x0000	Reserved					
	12:8	0x0014	TEMPSENS1_DIV_BY_N Divides temperature sensor clock vt_pixel_clock by n-value. This is the low 5 bits. The high bits are in R0x3FC2.			**E**		unsigned
	7:4	0x0000	Reserved					
	3	0x0000	Reserved					
	2	X	Undefined					
	1	0x0000	Reserved					
	0	0x0000	Reserved					
	Temperature sensor voltage monitoring and timing control							
R0x3F96	**15:0**	**0xD03E**	**TEMPVSENS1_FLAG_CTRL (R/W)**			**E**		**unsigned**
	15:6	0x0340	TEMPSENS1_RED_TEMP_CODE raw ADC temperature code where the temperature sensor and TEMP_FLAG pin report only temperature until the part is reset. This is a 13-bit value formed by 10 bits here and 3 high-order bits in R0x3EE0.			**E**		unsigned
	5:3	0x0007	TEMPSENS1_YELLOW_OFF_RED yellow flag trip point as number of raw ADC temperature code values below the red flag code trip point. This is a 7-bit value formed by 3 bits here and 4 high-order bits in R0x3EE0.			**E**		unsigned
	2:1	0x0003	TEMPSENS1_YELLOW_HYST hysteresis in raw ADC temperature codes around the yellow flag code trip point. This is a 5-bit value formed by 2 bits here and 3 high-order bits in R0x3EE0.			**E**		unsigned
	0	X	Undefined					
	When TEMPVSENS1_EN_CTRL[8]=0, the comparators that generate the Red and Yellow flags perform comparisons on raw ADC temperature codes. This register controls the thresholds for generating the Red and Yellow flags. See also R0x3EE0 which contains high-order bits for some of the fields here.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3F9A	**15:0**	**0x0000**	**TEMPVSENS0_BOOST_SAMP_CTRL (R/W)**			**E**		**unsigned**
	15	0x0000	SAMP_ADDR_CONT 0: The booster monitor cycles through the addresses set by the bit-mask formed from TEMPVSENS0_MUX_ADDR_EN_HI and TEMPVSENS0_MUX_ADDR_EN_LO. 1: The booster monitor uses the fixed address set by BSAMP_MUX_ADDR_I.			**E**		unsigned
	14	0x0000	SAMP_TRIG_CONT set to trigger booster sampling continuously unless temperature or voltage is set to trigger continuously			**E**		unsigned
	13	0x0000	SAMP_NO_PRECONDITION set to defeat pre-condition voltage on analog bandgap and analog booster voltage sampling capacitors			**E**		unsigned
	12	0x0000	SAMP_AGND set to measure AGND node instead of bandgap or booster voltage			**E**		unsigned
	11:9	X	Undefined					
	8:4	0x0000	BSAMP_MUX_ADDR_I Select booster monitor sample MUX address, when SAMP_ADDR_CONT=1.			**E**		unsigned
	3	0x0000	SAMP_CLEAR_VALUES 0: TEMPVSENS0_BOOST_MEAS_* (if enabled) are updated. 1: TEMPVSENS1_BOOST_MEAS_* are set to 0, clearing the last captured booster monitor value.			**E**		unsigned
	2:1	X	Undefined					
	0	0x0000	Reserved					
	Booster monitor analog bandbap and sampling control							
R0x3F9C	**15:0**	**0xF850**	**TEMPVSENS1_AUTO_VREF4_PULSE (R/W)**			**E**		**unsigned**
	15:12	0x000F	S2_PULSE_CNT s2_pulse_cnt			**E**		unsigned
	11:7	0x0010	SREG_VREF4_TRIM sreg_vref4_trim			**E**		unsigned
	6:0	0x0050	AUTO_ZERO_CNT auto_zero_cnt			**E**		unsigned
	tempvsens1_auto_vref4_pulse							
R0x3F9E	**15:0**	**0x4086**	**TEMPVSENS1_PEDESTAL_VREF16 (R/W)**			**E**		**unsigned**
	15	X	Undefined					
	14:10	0x0010	SREG_VREF16_TRIM sreg_vref16_trim			**E**		unsigned
	9:0	0x0086	PEDESTAL_CNT pedestal_cnt			**E**		unsigned
	tempvsens1_pedestal_vref16							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x3FC2	**15:0**	**0x0000**	**TEMPVSENS1_TMG_CTRL_EX (R/W)**			**E**		**unsigned**
	15:6	X	Undefined					
	5:3	0x0000	TEMPVSENS1_DIODE_EN Select diode for temperature sensor measurement. 0: Temperature diode in temperature sensor, located at die top-left. 1: Temperature diode, located at die centre. 2: Temperature diode, located at die centre-right. 3-7: Reserved.			**E**		unsigned
	2:0	0x0000	TEMPVSENS1_DIV_BY_N Bits [7:5] of clock divider. Low-order bits are in R0x3F92.			**E**		unsigned
	Control of Temperature/voltage sensor 1.							
R0x5100	**15:0**	**0x0003**	**EMBED_CRC_MAP00 (R/W)**					**unsigned**
	Bit-mapped CRC exclusion registers for embedded data and startup register scan. EMBED_CRC_MAP0[0] is the first entry and EMBED_CRC_MAP63[15] is the last. When a bit is set, the 16-bit register corresponding to that bit is excluded from the embedded data CRC. The relationship between a register address and a bit in this map is as follows: the first embedded register is associated with bit 0 in the map, the second embedded register is associated with bit 1 in the map, and so on.							
R0x5102	**15:0**	**0x0006**	**EMBED_CRC_MAP01 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5104	**15:0**	**0x1000**	**EMBED_CRC_MAP02 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5106	**15:0**	**0x0000**	**EMBED_CRC_MAP03 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5108	**15:0**	**0x0002**	**EMBED_CRC_MAP04 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x510A	**15:0**	**0x0000**	**EMBED_CRC_MAP05 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x510C	**15:0**	**0x0000**	**EMBED_CRC_MAP06 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x510E	**15:0**	**0x0000**	**EMBED_CRC_MAP07 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5110	**15:0**	**0x0000**	**EMBED_CRC_MAP08 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5112	**15:0**	**0x0000**	**EMBED_CRC_MAP09 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5114	**15:0**	**0x0040**	**EMBED_CRC_MAP10 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5116	**15:0**	**0x0000**	**EMBED_CRC_MAP11 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5118	**15:0**	**0x0000**	**EMBED_CRC_MAP12 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x511A	**15:0**	**0x0000**	**EMBED_CRC_MAP13 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x511C	15:0	0x0000	EMBED_CRC_MAP14 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x511E	15:0	0x0000	EMBED_CRC_MAP15 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5120	15:0	0x0002	EMBED_CRC_MAP16 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5122	15:0	0x4000	EMBED_CRC_MAP17 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5124	15:0	0x0000	EMBED_CRC_MAP18 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5126	15:0	0x0000	EMBED_CRC_MAP19 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5128	15:0	0x0000	EMBED_CRC_MAP20 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x512A	15:0	0x0000	EMBED_CRC_MAP21 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x512C	15:0	0x0000	EMBED_CRC_MAP22 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x512E	15:0	0x0000	EMBED_CRC_MAP23 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5130	15:0	0x0000	EMBED_CRC_MAP24 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5132	15:0	0x05C0	EMBED_CRC_MAP25 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5134	15:0	0x0000	EMBED_CRC_MAP26 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5136	15:0	0x0010	EMBED_CRC_MAP27 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5138	15:0	0x0000	EMBED_CRC_MAP28 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x513A	15:0	0x0000	EMBED_CRC_MAP29 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x513C	15:0	0x0000	EMBED_CRC_MAP30 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x513E	15:0	0x0000	EMBED_CRC_MAP31 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5140	15:0	0x0000	EMBED_CRC_MAP32 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x5142	15:0	0x0000	EMBED_CRC_MAP33 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5144	15:0	0x0000	EMBED_CRC_MAP34 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5146	15:0	0x0000	EMBED_CRC_MAP35 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5148	15:0	0x0000	EMBED_CRC_MAP36 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x514A	15:0	0x0000	EMBED_CRC_MAP37 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x514C	15:0	0x0000	EMBED_CRC_MAP38 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x514E	15:0	0x0000	EMBED_CRC_MAP39 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5150	15:0	0x0000	EMBED_CRC_MAP40 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5152	15:0	0x0000	EMBED_CRC_MAP41 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5154	15:0	0x0000	EMBED_CRC_MAP42 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5156	15:0	0x0000	EMBED_CRC_MAP43 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5158	15:0	0x4000	EMBED_CRC_MAP44 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x515A	15:0	0x0000	EMBED_CRC_MAP45 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x515C	15:0	0x0000	EMBED_CRC_MAP46 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x515E	15:0	0x0008	EMBED_CRC_MAP47 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5160	15:0	0x0000	EMBED_CRC_MAP48 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5162	15:0	0x4000	EMBED_CRC_MAP49 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5164	15:0	0x0000	EMBED_CRC_MAP50 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x5166	15:0	0x0000	EMBED_CRC_MAP51 (R/W)					unsigned
	See description of EMBED_CRC_MAP00 (R0x5100).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x5168	**15:0**	**0x0000**	**EMBED_CRC_MAP52 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100).							
R0x516A	**15:0**	**0x0000**	**EMBED_CRC_MAP53 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x516C	**15:0**	**0x0000**	**EMBED_CRC_MAP54 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x516E	**15:0**	**0x0000**	**EMBED_CRC_MAP55 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x5170	**15:0**	**0x0000**	**EMBED_CRC_MAP56 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x5172	**15:0**	**0x0000**	**EMBED_CRC_MAP57 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x5174	**15:0**	**0x0000**	**EMBED_CRC_MAP58 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x5176	**15:0**	**0x0000**	**EMBED_CRC_MAP59 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x5178	**15:0**	**0x0000**	**EMBED_CRC_MAP60 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x517A	**15:0**	**0x0000**	**EMBED_CRC_MAP61 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x517C	**15:0**	**0x0000**	**EMBED_CRC_MAP62 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							
R0x517E	**15:0**	**0x0000**	**EMBED_CRC_MAP63 (R/W)**					**unsigned**
	See description of EMBED_CRC_MAP00 (R0x5100). There are no embedded registers associated with this map register.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x559E	**15:0**	**0x0000**	**ODP_CRC_FAULT_CONTROL (R/W)**			**E**		**unsigned**
	15:14	X	Undefined					
	13:12	0x0000	SCALER_CRC_FAULT_INJECT Force error in scaler RAM for test purposes (should trigger CRC errors). 0: Off, 1: Memory fault, 2: Register fault, 3: Reserved.			**E**		unsigned
	11	X	Undefined					
	10	0x0000	SCALER_CRC_SYS_CHECK_EN Enable scaler RAM CRC errors to cause the SYS_CHECK pin to go high.			**E**		unsigned
	9	0x0000	SCALER_CRC_FAULT_EN Enable CRC checking for the scaler RAM			**E**		unsigned
	8	0x0000	SCALER_CRC_FAULT_RESET Reset error and error counters for scaler CRC.			**E**		unsigned
	7:6	X	Undefined					
	5:4	0x0000	ODP_CRC_ERROR_INJECT Force error in ODP buffer RAM for test purposes (should trigger CRC error). 0: Off, 1: Memory fault, 2: Register fault, 3: Reserved.			**E**		unsigned
	3	X	Undefined					
	2	0x0000	SYS_CHECK_EN Enable ODP buffer RAM CRC errors to cause the SYS_CHECK pin to go high.			**E**		unsigned
	1	0x0000	CRC_FAULT_EN Enable CRC checking for the ODP buffer RAM.			**E**		unsigned
	0	0x0000	CRC_FAULT_RESET Reset error and error counters for ODP buffer RAM CRC.			**E**		unsigned
	Control for ODP buffer RAM CRC check and Scaler RAM CRC check. Both CRC checks work in a similar way: as a row of image data is written sequentially to a RAM-based buffer, a CRC is accumulated and stored. When the row of image data is read out again (also sequentially) the CRC is re-computed. At the end of row readout, the re-computed CRC should match the value that was stored when the row was written. A miscompare causes an error to be counted and (optionally) SYS_CHECK to be asserted. The _INJECT bits provide methods for forcing an error for test purposes. The "memory fault" bit corrupts the CRC that is accumulated/stored during the write to the RAM. The "register fault" bit forces a mis-compare when the read and write CRCs are compared at the end of the row read.							
R0x55A0	**15:0**	**0x0000**	**ODP_CRC_FAULTS_PER_FRAME (RO)**			**E**		**unsigned**
	Number of ODP buffer RAM CRC faults in the previous frame. Cleared at start of frame or by CRC_FAULT_RESET (in R0x559E).							
R0x55A2	**15:0**	**0x0000**	**ODP_CRC_FAULT_FRAMES (RO)**			**E**		**unsigned**
	Number of frames with at least 1 ODP buffer CRC fault. Cleared by CRC_FAULT_RESET (in R0x559E).							
R0x55A4	**15:0**	**0x0000**	**SCALER_CRC_FAULTS_PER_FRAME (RO)**			**E**		**unsigned**
	Number of scaler RAM CRC faults in the previous frame. Cleared at the start of frame or by SCALER_RAM_CRC_FAULT_RESET (in R0x559E).							
R0x55A6	**15:0**	**0x0000**	**SCALER_CRC_FAULT_FRAMES (RO)**			**E**		**unsigned**
	Number of frames with at least 1 scaler RAM CRC fault. Cleared by SCALER_RAM_CRC_FAULT_RESET (in R0x559E).							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x5800	**15:0**	**0x0000**	**ASIL_CHECK_ENABLES_08 (R/W)**	**S**		**E**		**unsigned**
	15:8	X	Undefined					
	7	0x0000	CHECK_OT4_HIGH Enable pixel overdrive test 4 high check.	**S**		**E**		unsigned
	6	0x0000	CHECK_OT4_LOW Enable pixel overdrive 4 low check.	**S**		**E**		unsigned
	5	0x0000	CHECK_OT3_HIGH Enable pixel overdrive 3 high check.	**S**		**E**		unsigned
	4	0x0000	CHECK_OT3_LOW Enable pixel overdrive 3 low check.	**S**		**E**		unsigned
	3	0x0000	CHECK_OT0_HIGH Enable pixel overdrive 0 high check.	**S**		**E**		unsigned
	2	0x0000	CHECK_OT0_LOW Enable pixel overdrive 0 low check.	**S**		**E**		unsigned
	1	0x0000	CHECK_GT2 Enable column memory gray transfer 2 check.	**S**		**E**		unsigned
	0	0x0000	CHECK_GT1 Enable column memory gray transfer 1 check.	**S**		**E**		unsigned
	Each bit of this register enables a particular check. See ASIL_STATUS_08 and ASIL_PIN_ENABLES_08.							
R0x5802	**15:0**	**0x0000**	**ASIL_PIN_ENABLES_08 (R/W)**			**E**		**unsigned**
	15:8	X	Undefined					
	7	0x0000	EN_PIN_OT4_HIGH Enable result of the OT3 high check onto the SYS_CHECK pin.			**E**		unsigned
	6	0x0000	EN_PIN_OT4_LOW Enable result of the OT3 low check onto the SYS_CHECK pin.			**E**		unsigned
	5	0x0000	EN_PIN_OT3_HIGH Enable result of the OT3 high check onto the SYS_CHECK pin.			**E**		unsigned
	4	0x0000	EN_PIN_OT3_LOW Enable result of the OT3 low check onto the SYS_CHECK pin.			**E**		unsigned
	3	0x0000	EN_PIN_OT0_HIGH Enable result of the OT0 high check onto the SYS_CHECK pin.			**E**		unsigned
	2	0x0000	EN_PIN_OT0_LOW Enable result of the OT0 low check onto the SYS_CHECK pin.			**E**		unsigned
	1	0x0000	EN_PIN_GT2 Enable result of the GT2 check onto the SYS_CHECK pin.			**E**		unsigned
	0	0x0000	EN_PIN_GT1 Enable result of the GT1 check onto the SYS_CHECK pin.			**E**		unsigned
	Each bit of this register controls whether a detected error in the associated check is flagged on the SYS_CHECK pin. See ASIL_CHECK_ENABLES_08 and ASIL_STATUS_08.							
R0x5900	**13:0**	**0x0000**	**ATR_CHECK_OT_BASE (R/W)**			**E**		**unsigned**
	Used with ATR_CHECK_OT_LO_OFFSET and ATR_CHECK_OT_HI_OFFSET to compute low and high thresholds for OT tests 0, 1, 2, 3, and 4. A low check fails if any pixel is below the computed low threshold. A high check fails if any pixel is above the computed high threshold. All values are in s14 format. The base is given by ATR_CHECK_OT_BASE multiplied by the analogue gain value used for the OT test. The pass window extends up from the base (to a value given by ATR_CHECK_OT_HI_OFFSET multiplied by the analogue gain value used for the OT test) and down from the base (to a value given by ATR_CHECK_OT_LO_OFFSET multiplied by the analogue gain value used for the OT test). ATR_CHECK_OT_BASE + ATR_CHECK_OT_HI_OFFSET must be <= 511.							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0x5902	**13:0**	**0x0000**	**ATR_CHECK_OT_LO_OFFSET (R/W)**			**E**		**unsigned**
	See ATR_CHECK_OT_LO_OFFSET (R0x590).							
R0x5904	**13:0**	**0x0000**	**ATR_CHECK_OT_HI_OFFSET (R/W)**			**E**		**unsigned**
	See ATR_CHECK_OT_LO_OFFSET (R0x590).							
R0x5906	**13:0**	**0x0000**	**ATR_CHECK_GT_EXPECT1 (R/W)**			**E**		**unsigned**
	Expected value for gray transfer test 1, in s14 format. Should be set to 0x0CCC.							
R0x5908	**13:0**	**0x0000**	**ATR_CHECK_GT_EXPECT2 (R/W)**			**E**		**unsigned**
	Expected value for gray transfer test 2, in s14 format. Should be set to 0x3999.							
R0x590A	**13:0**	**0x0000**	**RRC_CHECK_LO_THRESH2 (R/W)**			**E**		**unsigned**
	RRC pixels for the TX* and row ROM address checks are deemed dark if lower than this threshold. Value is in s14 format but guaranteed to be in the range -2048..+6143.							
R0x590C	**15:0**	**0x0000**	**ATR_PEDESTAL_SELECT0 (R/W)**					**unsigned**
	Allows a pedestal value to be added to the ATR so that it can be passed through the data-path to the output without clipping. The pedestal is applied in a circular number space (no attempt is made to clamp a value that underflows or overflows as a result of applying the pedestal). Internal ATR checking is performed before the pedestal is applied. Four pedestal values are available, and a 2-bit field for each of the 16 ATRs selects which pedestal to apply. Bits[1:0] select pedestal for ATR0, Bits[3:2] select pedestal for ATR1 etc.							
R0x590E	**15:0**	**0x0000**	**ATR_PEDESTAL_SELECT1 (R/W)**					**unsigned**
	Used in conjunction with ATR_PEDESTAL_SELECT1. Bits[1:0] select pedestal for ATR8, Bits[3:2] select pedestal for ATR9 etc.							
R0x5910	**13:0**	**0x0000**	**ATR_PEDESTAL0 (R/W)**					**unsigned**
	ATR pedestal value (14-bit, 2s complement) used if select=0.							
R0x5912	**13:0**	**0x3800**	**ATR_PEDESTAL1 (R/W)**					**unsigned**
	ATR pedestal value (14-bit, 2s complement) used if select=1. The default value of 0x3800 corresponds to a value of -2048.							
R0x5914	**13:0**	**0x0800**	**ATR_PEDESTAL2 (R/W)**					**unsigned**
	ATR pedestal value (14-bit, 2s complement) used if select=2. The default value of 0x0800 corresponds to a value of 2048.							
R0x5916	**13:0**	**0x0FFF**	**ATR_PEDESTAL3 (R/W)**					**unsigned**
	ATR pedestal value (14-bit, 2s complement) used if select=3. The default value of 0x0fff corresponds to a value of 4095.							
R0x5918	**15:0**	**0x0078**	**ATC_PEDESTAL (R/W)**					**unsigned**
	Allows a pedestal value to be added to the ATC so that they can be passed through the data-path to the output without clipping. The pedestal is applied in a circular number space (no attempt is made to clamp a value that underflows or overflows as a result of applying the pedestal). Internal ATC checking is performed before the pedestal is applied.							
R0xF000	**15:0**	**0x8000**	**CSS_COMMAND (R/W)**					**unsigned**
	15	0x0001	DOORBELL doorbell 0 : Host has access rights to the command interface 1: Firmware has access rights to the command interface					unsigned
	14:0	0x0000	RESULT host command and security command result					unsigned
	Cryptographic susbsystem host command interface							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF008	**15:0**	**0x0000**	**CSS_ERROR (RO)**					**unsigned**
	15:10	RO	FAULTCODE Error condition fault code					unsigned
	9:0	RO	FAULTCONTEXT Error condition context					unsigned
	Cryptographic subsystem error condition							
R0xF00A	**15:0**	**0x0000**	**CSS_INFO (RO)**					**unsigned**
	Cryptographic subsystem information							
R0xF00C	**1:0**	**0x0000**	**CSS_PAGE (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory page. 00: page 0 01: page 1 10: page 2 11: page 3							
R0xF100	**15:0**	**0x0000**	**CSS_PARAMS_0 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 0							
R0xF102	**15:0**	**0x0000**	**CSS_PARAMS_1 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 1							
R0xF104	**15:0**	**0x0000**	**CSS_PARAMS_2 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 2							
R0xF106	**15:0**	**0x0000**	**CSS_PARAMS_3 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 3							
R0xF108	**15:0**	**0x0000**	**CSS_PARAMS_4 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 4							
R0xF10A	**15:0**	**0x0000**	**CSS_PARAMS_5 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 5							
R0xF10C	**15:0**	**0x0000**	**CSS_PARAMS_6 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 6							
R0xF10E	**15:0**	**0x0000**	**CSS_PARAMS_7 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 7							
R0xF110	**15:0**	**0x0000**	**CSS_PARAMS_8 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 8							
R0xF112	**15:0**	**0x0000**	**CSS_PARAMS_9 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 9							
R0xF114	**15:0**	**0x0000**	**CSS_PARAMS_10 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 10							
R0xF116	**15:0**	**0x0000**	**CSS_PARAMS_11 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 11							
R0xF118	**15:0**	**0x0000**	**CSS_PARAMS_12 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 12							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF11A	15:0	0x0000	CSS_PARAMS_13 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 13							
R0xF11C	15:0	0x0000	CSS_PARAMS_14 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 14							
R0xF11E	15:0	0x0000	CSS_PARAMS_15 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 15							
R0xF120	15:0	0x0000	CSS_PARAMS_16 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 16							
R0xF122	15:0	0x0000	CSS_PARAMS_17 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 17							
R0xF124	15:0	0x0000	CSS_PARAMS_18 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 18							
R0xF126	15:0	0x0000	CSS_PARAMS_19 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 19							
R0xF128	15:0	0x0000	CSS_PARAMS_20 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 20							
R0xF12A	15:0	0x0000	CSS_PARAMS_21 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 21							
R0xF12C	15:0	0x0000	CSS_PARAMS_22 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 22							
R0xF12E	15:0	0x0000	CSS_PARAMS_23 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 23							
R0xF130	15:0	0x0000	CSS_PARAMS_24 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 24							
R0xF132	15:0	0x0000	CSS_PARAMS_25 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 25							
R0xF134	15:0	0x0000	CSS_PARAMS_26 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 26							
R0xF136	15:0	0x0000	CSS_PARAMS_27 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 27							
R0xF138	15:0	0x0000	CSS_PARAMS_28 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 28							
R0xF13A	15:0	0x0000	CSS_PARAMS_29 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 29							
R0xF13C	15:0	0x0000	CSS_PARAMS_30 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 30							
R0xF13E	15:0	0x0000	CSS_PARAMS_31 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 31							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF140	**15:0**	**0x0000**	**CSS_PARAMS_32 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 32							
R0xF142	**15:0**	**0x0000**	**CSS_PARAMS_33 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 33							
R0xF144	**15:0**	**0x0000**	**CSS_PARAMS_34 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 34							
R0xF146	**15:0**	**0x0000**	**CSS_PARAMS_35 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 35							
R0xF148	**15:0**	**0x0000**	**CSS_PARAMS_36 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 36							
R0xF14A	**15:0**	**0x0000**	**CSS_PARAMS_37 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 37							
R0xF14C	**15:0**	**0x0000**	**CSS_PARAMS_38 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 38							
R0xF14E	**15:0**	**0x0000**	**CSS_PARAMS_39 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 39							
R0xF150	**15:0**	**0x0000**	**CSS_PARAMS_40 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 40							
R0xF152	**15:0**	**0x0000**	**CSS_PARAMS_41 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 41							
R0xF154	**15:0**	**0x0000**	**CSS_PARAMS_42 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 42							
R0xF156	**15:0**	**0x0000**	**CSS_PARAMS_43 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 43							
R0xF158	**15:0**	**0x0000**	**CSS_PARAMS_44 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 44							
R0xF15A	**15:0**	**0x0000**	**CSS_PARAMS_45 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 45							
R0xF15C	**15:0**	**0x0000**	**CSS_PARAMS_46 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 46							
R0xF15E	**15:0**	**0x0000**	**CSS_PARAMS_47 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 47							
R0xF160	**15:0**	**0x0000**	**CSS_PARAMS_48 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 48							
R0xF162	**15:0**	**0x0000**	**CSS_PARAMS_49 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 49							
R0xF164	**15:0**	**0x0000**	**CSS_PARAMS_50 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 50							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF166	**15:0**	**0x0000**	**CSS_PARAMS_51 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 51							
R0xF168	**15:0**	**0x0000**	**CSS_PARAMS_52 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 52							
R0xF16A	**15:0**	**0x0000**	**CSS_PARAMS_53 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 53							
R0xF16C	**15:0**	**0x0000**	**CSS_PARAMS_54 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 54							
R0xF16E	**15:0**	**0x0000**	**CSS_PARAMS_55 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 55							
R0xF170	**15:0**	**0x0000**	**CSS_PARAMS_56 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 56							
R0xF172	**15:0**	**0x0000**	**CSS_PARAMS_57 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 57							
R0xF174	**15:0**	**0x0000**	**CSS_PARAMS_58 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 58							
R0xF176	**15:0**	**0x0000**	**CSS_PARAMS_59 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 59							
R0xF178	**15:0**	**0x0000**	**CSS_PARAMS_60 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 60							
R0xF17A	**15:0**	**0x0000**	**CSS_PARAMS_61 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 61							
R0xF17C	**15:0**	**0x0000**	**CSS_PARAMS_62 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 62							
R0xF17E	**15:0**	**0x0000**	**CSS_PARAMS_63 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 63							
R0xF180	**15:0**	**0x0000**	**CSS_PARAMS_64 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 64							
R0xF182	**15:0**	**0x0000**	**CSS_PARAMS_65 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 65							
R0xF184	**15:0**	**0x0000**	**CSS_PARAMS_66 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 66							
R0xF186	**15:0**	**0x0000**	**CSS_PARAMS_67 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 67							
R0xF188	**15:0**	**0x0000**	**CSS_PARAMS_68 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 68							
R0xF18A	**15:0**	**0x0000**	**CSS_PARAMS_69 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 69							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF18C	**15:0**	**0x0000**	**CSS_PARAMS_70 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 70							
R0xF18E	**15:0**	**0x0000**	**CSS_PARAMS_71 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 71							
R0xF190	**15:0**	**0x0000**	**CSS_PARAMS_72 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 72							
R0xF192	**15:0**	**0x0000**	**CSS_PARAMS_73 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 73							
R0xF194	**15:0**	**0x0000**	**CSS_PARAMS_74 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 74							
R0xF196	**15:0**	**0x0000**	**CSS_PARAMS_75 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 75							
R0xF198	**15:0**	**0x0000**	**CSS_PARAMS_76 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 76							
R0xF19A	**15:0**	**0x0000**	**CSS_PARAMS_77 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 77							
R0xF19C	**15:0**	**0x0000**	**CSS_PARAMS_78 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 78							
R0xF19E	**15:0**	**0x0000**	**CSS_PARAMS_79 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 79							
R0xF1A0	**15:0**	**0x0000**	**CSS_PARAMS_80 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 80							
R0xF1A2	**15:0**	**0x0000**	**CSS_PARAMS_81 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 81							
R0xF1A4	**15:0**	**0x0000**	**CSS_PARAMS_82 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 82							
R0xF1A6	**15:0**	**0x0000**	**CSS_PARAMS_83 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 83							
R0xF1A8	**15:0**	**0x0000**	**CSS_PARAMS_84 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 84							
R0xF1AA	**15:0**	**0x0000**	**CSS_PARAMS_85 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 85							
R0xF1AC	**15:0**	**0x0000**	**CSS_PARAMS_86 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 86							
R0xF1AE	**15:0**	**0x0000**	**CSS_PARAMS_87 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 87							
R0xF1B0	**15:0**	**0x0000**	**CSS_PARAMS_88 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 88							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF1B2	15:0	0x0000	CSS_PARAMS_89 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 89							
R0xF1B4	15:0	0x0000	CSS_PARAMS_90 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 90							
R0xF1B6	15:0	0x0000	CSS_PARAMS_91 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 91							
R0xF1B8	15:0	0x0000	CSS_PARAMS_92 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 92							
R0xF1BA	15:0	0x0000	CSS_PARAMS_93 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 93							
R0xF1BC	15:0	0x0000	CSS_PARAMS_94 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 94							
R0xF1BE	15:0	0x0000	CSS_PARAMS_95 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 95							
R0xF1C0	15:0	0x0000	CSS_PARAMS_96 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 96							
R0xF1C2	15:0	0x0000	CSS_PARAMS_97 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 97							
R0xF1C4	15:0	0x0000	CSS_PARAMS_98 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 98							
R0xF1C6	15:0	0x0000	CSS_PARAMS_99 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 99							
R0xF1C8	15:0	0x0000	CSS_PARAMS_100 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 100							
R0xF1CA	15:0	0x0000	CSS_PARAMS_101 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 101							
R0xF1CC	15:0	0x0000	CSS_PARAMS_102 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 102							
R0xF1CE	15:0	0x0000	CSS_PARAMS_103 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 103							
R0xF1D0	15:0	0x0000	CSS_PARAMS_104 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 104							
R0xF1D2	15:0	0x0000	CSS_PARAMS_105 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 105							
R0xF1D4	15:0	0x0000	CSS_PARAMS_106 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 106							
R0xF1D6	15:0	0x0000	CSS_PARAMS_107 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 107							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF1D8	**15:0**	**0x0000**	**CSS_PARAMS_108 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 108							
R0xF1DA	**15:0**	**0x0000**	**CSS_PARAMS_109 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 109							
R0xF1DC	**15:0**	**0x0000**	**CSS_PARAMS_110 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 110							
R0xF1DE	**15:0**	**0x0000**	**CSS_PARAMS_111 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 111							
R0xF1E0	**15:0**	**0x0000**	**CSS_PARAMS_112 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 112							
R0xF1E2	**15:0**	**0x0000**	**CSS_PARAMS_113 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 113							
R0xF1E4	**15:0**	**0x0000**	**CSS_PARAMS_114 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 114							
R0xF1E6	**15:0**	**0x0000**	**CSS_PARAMS_115 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 115							
R0xF1E8	**15:0**	**0x0000**	**CSS_PARAMS_116 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 116							
R0xF1EA	**15:0**	**0x0000**	**CSS_PARAMS_117 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 117							
R0xF1EC	**15:0**	**0x0000**	**CSS_PARAMS_118 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 118							
R0xF1EE	**15:0**	**0x0000**	**CSS_PARAMS_119 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 119							
R0xF1F0	**15:0**	**0x0000**	**CSS_PARAMS_120 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 120							
R0xF1F2	**15:0**	**0x0000**	**CSS_PARAMS_121 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 121							
R0xF1F4	**15:0**	**0x0000**	**CSS_PARAMS_122 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 122							
R0xF1F6	**15:0**	**0x0000**	**CSS_PARAMS_123 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 123							
R0xF1F8	**15:0**	**0x0000**	**CSS_PARAMS_124 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 124							
R0xF1FA	**15:0**	**0x0000**	**CSS_PARAMS_125 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 125							
R0xF1FC	**15:0**	**0x0000**	**CSS_PARAMS_126 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 126							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF1FE	**15:0**	**0x0000**	**CSS_PARAMS_127 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 127							
R0xF200	**15:0**	**0x0000**	**CSS_PARAMS_128 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 128							
R0xF202	**15:0**	**0x0000**	**CSS_PARAMS_129 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 129							
R0xF204	**15:0**	**0x0000**	**CSS_PARAMS_130 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 130							
R0xF206	**15:0**	**0x0000**	**CSS_PARAMS_131 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 131							
R0xF208	**15:0**	**0x0000**	**CSS_PARAMS_132 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 132							
R0xF20A	**15:0**	**0x0000**	**CSS_PARAMS_133 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 133							
R0xF20C	**15:0**	**0x0000**	**CSS_PARAMS_134 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 134							
R0xF20E	**15:0**	**0x0000**	**CSS_PARAMS_135 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 135							
R0xF210	**15:0**	**0x0000**	**CSS_PARAMS_136 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 136							
R0xF212	**15:0**	**0x0000**	**CSS_PARAMS_137 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 137							
R0xF214	**15:0**	**0x0000**	**CSS_PARAMS_138 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 138							
R0xF216	**15:0**	**0x0000**	**CSS_PARAMS_139 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 139							
R0xF218	**15:0**	**0x0000**	**CSS_PARAMS_140 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 140							
R0xF21A	**15:0**	**0x0000**	**CSS_PARAMS_141 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 141							
R0xF21C	**15:0**	**0x0000**	**CSS_PARAMS_142 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 142							
R0xF21E	**15:0**	**0x0000**	**CSS_PARAMS_143 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 143							
R0xF220	**15:0**	**0x0000**	**CSS_PARAMS_144 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 144							
R0xF222	**15:0**	**0x0000**	**CSS_PARAMS_145 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 145							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF224	**15:0**	**0x0000**	**CSS_PARAMS_146 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 146							
R0xF226	**15:0**	**0x0000**	**CSS_PARAMS_147 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 147							
R0xF228	**15:0**	**0x0000**	**CSS_PARAMS_148 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 148							
R0xF22A	**15:0**	**0x0000**	**CSS_PARAMS_149 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 149							
R0xF22C	**15:0**	**0x0000**	**CSS_PARAMS_150 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 150							
R0xF22E	**15:0**	**0x0000**	**CSS_PARAMS_151 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 151							
R0xF230	**15:0**	**0x0000**	**CSS_PARAMS_152 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 152							
R0xF232	**15:0**	**0x0000**	**CSS_PARAMS_153 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 153							
R0xF234	**15:0**	**0x0000**	**CSS_PARAMS_154 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 154							
R0xF236	**15:0**	**0x0000**	**CSS_PARAMS_155 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 155							
R0xF238	**15:0**	**0x0000**	**CSS_PARAMS_156 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 156							
R0xF23A	**15:0**	**0x0000**	**CSS_PARAMS_157 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 157							
R0xF23C	**15:0**	**0x0000**	**CSS_PARAMS_158 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 158							
R0xF23E	**15:0**	**0x0000**	**CSS_PARAMS_159 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 159							
R0xF240	**15:0**	**0x0000**	**CSS_PARAMS_160 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 160							
R0xF242	**15:0**	**0x0000**	**CSS_PARAMS_161 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 161							
R0xF244	**15:0**	**0x0000**	**CSS_PARAMS_162 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 162							
R0xF246	**15:0**	**0x0000**	**CSS_PARAMS_163 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 163							
R0xF248	**15:0**	**0x0000**	**CSS_PARAMS_164 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 164							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF24A	15:0	0x0000	CSS_PARAMS_165 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 165							
R0xF24C	15:0	0x0000	CSS_PARAMS_166 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 166							
R0xF24E	15:0	0x0000	CSS_PARAMS_167 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 167							
R0xF250	15:0	0x0000	CSS_PARAMS_168 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 168							
R0xF252	15:0	0x0000	CSS_PARAMS_169 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 169							
R0xF254	15:0	0x0000	CSS_PARAMS_170 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 170							
R0xF256	15:0	0x0000	CSS_PARAMS_171 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 171							
R0xF258	15:0	0x0000	CSS_PARAMS_172 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 172							
R0xF25A	15:0	0x0000	CSS_PARAMS_173 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 173							
R0xF25C	15:0	0x0000	CSS_PARAMS_174 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 174							
R0xF25E	15:0	0x0000	CSS_PARAMS_175 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 175							
R0xF260	15:0	0x0000	CSS_PARAMS_176 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 176							
R0xF262	15:0	0x0000	CSS_PARAMS_177 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 177							
R0xF264	15:0	0x0000	CSS_PARAMS_178 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 178							
R0xF266	15:0	0x0000	CSS_PARAMS_179 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 179							
R0xF268	15:0	0x0000	CSS_PARAMS_180 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 180							
R0xF26A	15:0	0x0000	CSS_PARAMS_181 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 181							
R0xF26C	15:0	0x0000	CSS_PARAMS_182 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 182							
R0xF26E	15:0	0x0000	CSS_PARAMS_183 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 183							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF270	**15:0**	**0x0000**	**CSS_PARAMS_184 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 184							
R0xF272	**15:0**	**0x0000**	**CSS_PARAMS_185 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 185							
R0xF274	**15:0**	**0x0000**	**CSS_PARAMS_186 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 186							
R0xF276	**15:0**	**0x0000**	**CSS_PARAMS_187 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 187							
R0xF278	**15:0**	**0x0000**	**CSS_PARAMS_188 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 188							
R0xF27A	**15:0**	**0x0000**	**CSS_PARAMS_189 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 189							
R0xF27C	**15:0**	**0x0000**	**CSS_PARAMS_190 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 190							
R0xF27E	**15:0**	**0x0000**	**CSS_PARAMS_191 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 191							
R0xF280	**15:0**	**0x0000**	**CSS_PARAMS_192 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 192							
R0xF282	**15:0**	**0x0000**	**CSS_PARAMS_193 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 193							
R0xF284	**15:0**	**0x0000**	**CSS_PARAMS_194 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 194							
R0xF286	**15:0**	**0x0000**	**CSS_PARAMS_195 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 195							
R0xF288	**15:0**	**0x0000**	**CSS_PARAMS_196 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 196							
R0xF28A	**15:0**	**0x0000**	**CSS_PARAMS_197 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 197							
R0xF28C	**15:0**	**0x0000**	**CSS_PARAMS_198 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 198							
R0xF28E	**15:0**	**0x0000**	**CSS_PARAMS_199 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 199							
R0xF290	**15:0**	**0x0000**	**CSS_PARAMS_200 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 200							
R0xF292	**15:0**	**0x0000**	**CSS_PARAMS_201 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 201							
R0xF294	**15:0**	**0x0000**	**CSS_PARAMS_202 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 202							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF296	**15:0**	**0x0000**	**CSS_PARAMS_203 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 203							
R0xF298	**15:0**	**0x0000**	**CSS_PARAMS_204 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 204							
R0xF29A	**15:0**	**0x0000**	**CSS_PARAMS_205 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 205							
R0xF29C	**15:0**	**0x0000**	**CSS_PARAMS_206 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 206							
R0xF29E	**15:0**	**0x0000**	**CSS_PARAMS_207 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 207							
R0xF2A0	**15:0**	**0x0000**	**CSS_PARAMS_208 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 208							
R0xF2A2	**15:0**	**0x0000**	**CSS_PARAMS_209 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 209							
R0xF2A4	**15:0**	**0x0000**	**CSS_PARAMS_210 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 210							
R0xF2A6	**15:0**	**0x0000**	**CSS_PARAMS_211 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 211							
R0xF2A8	**15:0**	**0x0000**	**CSS_PARAMS_212 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 212							
R0xF2AA	**15:0**	**0x0000**	**CSS_PARAMS_213 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 213							
R0xF2AC	**15:0**	**0x0000**	**CSS_PARAMS_214 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 214							
R0xF2AE	**15:0**	**0x0000**	**CSS_PARAMS_215 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 215							
R0xF2B0	**15:0**	**0x0000**	**CSS_PARAMS_216 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 216							
R0xF2B2	**15:0**	**0x0000**	**CSS_PARAMS_217 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 217							
R0xF2B4	**15:0**	**0x0000**	**CSS_PARAMS_218 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 218							
R0xF2B6	**15:0**	**0x0000**	**CSS_PARAMS_219 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 219							
R0xF2B8	**15:0**	**0x0000**	**CSS_PARAMS_220 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 220							
R0xF2BA	**15:0**	**0x0000**	**CSS_PARAMS_221 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 221							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF2BC	**15:0**	**0x0000**	**CSS_PARAMS_222 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 222							
R0xF2BE	**15:0**	**0x0000**	**CSS_PARAMS_223 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 223							
R0xF2C0	**15:0**	**0x0000**	**CSS_PARAMS_224 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 224							
R0xF2C2	**15:0**	**0x0000**	**CSS_PARAMS_225 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 225							
R0xF2C4	**15:0**	**0x0000**	**CSS_PARAMS_226 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 226							
R0xF2C6	**15:0**	**0x0000**	**CSS_PARAMS_227 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 227							
R0xF2C8	**15:0**	**0x0000**	**CSS_PARAMS_228 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 228							
R0xF2CA	**15:0**	**0x0000**	**CSS_PARAMS_229 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 229							
R0xF2CC	**15:0**	**0x0000**	**CSS_PARAMS_230 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 230							
R0xF2CE	**15:0**	**0x0000**	**CSS_PARAMS_231 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 231							
R0xF2D0	**15:0**	**0x0000**	**CSS_PARAMS_232 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 232							
R0xF2D2	**15:0**	**0x0000**	**CSS_PARAMS_233 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 233							
R0xF2D4	**15:0**	**0x0000**	**CSS_PARAMS_234 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 234							
R0xF2D6	**15:0**	**0x0000**	**CSS_PARAMS_235 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 235							
R0xF2D8	**15:0**	**0x0000**	**CSS_PARAMS_236 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 236							
R0xF2DA	**15:0**	**0x0000**	**CSS_PARAMS_237 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 237							
R0xF2DC	**15:0**	**0x0000**	**CSS_PARAMS_238 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 238							
R0xF2DE	**15:0**	**0x0000**	**CSS_PARAMS_239 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 239							
R0xF2E0	**15:0**	**0x0000**	**CSS_PARAMS_240 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 240							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF2E2	**15:0**	**0x0000**	**CSS_PARAMS_241 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 241							
R0xF2E4	**15:0**	**0x0000**	**CSS_PARAMS_242 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 242							
R0xF2E6	**15:0**	**0x0000**	**CSS_PARAMS_243 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 243							
R0xF2E8	**15:0**	**0x0000**	**CSS_PARAMS_244 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 244							
R0xF2EA	**15:0**	**0x0000**	**CSS_PARAMS_245 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 245							
R0xF2EC	**15:0**	**0x0000**	**CSS_PARAMS_246 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 246							
R0xF2EE	**15:0**	**0x0000**	**CSS_PARAMS_247 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 247							
R0xF2F0	**15:0**	**0x0000**	**CSS_PARAMS_248 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 248							
R0xF2F2	**15:0**	**0x0000**	**CSS_PARAMS_249 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 249							
R0xF2F4	**15:0**	**0x0000**	**CSS_PARAMS_250 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 250							
R0xF2F6	**15:0**	**0x0000**	**CSS_PARAMS_251 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 251							
R0xF2F8	**15:0**	**0x0000**	**CSS_PARAMS_252 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 252							
R0xF2FA	**15:0**	**0x0000**	**CSS_PARAMS_253 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 253							
R0xF2FC	**15:0**	**0x0000**	**CSS_PARAMS_254 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 254							
R0xF2FE	**15:0**	**0x0000**	**CSS_PARAMS_255 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 255							
R0xF300	**15:0**	**0x0000**	**CSS_PARAMS_256 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 256							
R0xF302	**15:0**	**0x0000**	**CSS_PARAMS_257 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 257							
R0xF304	**15:0**	**0x0000**	**CSS_PARAMS_258 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 258							
R0xF306	**15:0**	**0x0000**	**CSS_PARAMS_259 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 259							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF308	**15:0**	**0x0000**	**CSS_PARAMS_260 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 260							
R0xF30A	**15:0**	**0x0000**	**CSS_PARAMS_261 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 261							
R0xF30C	**15:0**	**0x0000**	**CSS_PARAMS_262 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 262							
R0xF30E	**15:0**	**0x0000**	**CSS_PARAMS_263 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 263							
R0xF310	**15:0**	**0x0000**	**CSS_PARAMS_264 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 264							
R0xF312	**15:0**	**0x0000**	**CSS_PARAMS_265 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 265							
R0xF314	**15:0**	**0x0000**	**CSS_PARAMS_266 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 266							
R0xF316	**15:0**	**0x0000**	**CSS_PARAMS_267 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 267							
R0xF318	**15:0**	**0x0000**	**CSS_PARAMS_268 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 268							
R0xF31A	**15:0**	**0x0000**	**CSS_PARAMS_269 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 269							
R0xF31C	**15:0**	**0x0000**	**CSS_PARAMS_270 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 270							
R0xF31E	**15:0**	**0x0000**	**CSS_PARAMS_271 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 271							
R0xF320	**15:0**	**0x0000**	**CSS_PARAMS_272 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 272							
R0xF322	**15:0**	**0x0000**	**CSS_PARAMS_273 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 273							
R0xF324	**15:0**	**0x0000**	**CSS_PARAMS_274 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 274							
R0xF326	**15:0**	**0x0000**	**CSS_PARAMS_275 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 275							
R0xF328	**15:0**	**0x0000**	**CSS_PARAMS_276 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 276							
R0xF32A	**15:0**	**0x0000**	**CSS_PARAMS_277 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 277							
R0xF32C	**15:0**	**0x0000**	**CSS_PARAMS_278 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 278							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF32E	**15:0**	**0x0000**	**CSS_PARAMS_279 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 279							
R0xF330	**15:0**	**0x0000**	**CSS_PARAMS_280 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 280							
R0xF332	**15:0**	**0x0000**	**CSS_PARAMS_281 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 281							
R0xF334	**15:0**	**0x0000**	**CSS_PARAMS_282 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 282							
R0xF336	**15:0**	**0x0000**	**CSS_PARAMS_283 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 283							
R0xF338	**15:0**	**0x0000**	**CSS_PARAMS_284 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 284							
R0xF33A	**15:0**	**0x0000**	**CSS_PARAMS_285 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 285							
R0xF33C	**15:0**	**0x0000**	**CSS_PARAMS_286 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 286							
R0xF33E	**15:0**	**0x0000**	**CSS_PARAMS_287 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 287							
R0xF340	**15:0**	**0x0000**	**CSS_PARAMS_288 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 288							
R0xF342	**15:0**	**0x0000**	**CSS_PARAMS_289 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 289							
R0xF344	**15:0**	**0x0000**	**CSS_PARAMS_290 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 290							
R0xF346	**15:0**	**0x0000**	**CSS_PARAMS_291 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 291							
R0xF348	**15:0**	**0x0000**	**CSS_PARAMS_292 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 292							
R0xF34A	**15:0**	**0x0000**	**CSS_PARAMS_293 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 293							
R0xF34C	**15:0**	**0x0000**	**CSS_PARAMS_294 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 294							
R0xF34E	**15:0**	**0x0000**	**CSS_PARAMS_295 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 295							
R0xF350	**15:0**	**0x0000**	**CSS_PARAMS_296 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 296							
R0xF352	**15:0**	**0x0000**	**CSS_PARAMS_297 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 297							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF354	**15:0**	**0x0000**	**CSS_PARAMS_298 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 298							
R0xF356	**15:0**	**0x0000**	**CSS_PARAMS_299 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 299							
R0xF358	**15:0**	**0x0000**	**CSS_PARAMS_300 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 300							
R0xF35A	**15:0**	**0x0000**	**CSS_PARAMS_301 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 301							
R0xF35C	**15:0**	**0x0000**	**CSS_PARAMS_302 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 302							
R0xF35E	**15:0**	**0x0000**	**CSS_PARAMS_303 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 303							
R0xF360	**15:0**	**0x0000**	**CSS_PARAMS_304 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 304							
R0xF362	**15:0**	**0x0000**	**CSS_PARAMS_305 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 305							
R0xF364	**15:0**	**0x0000**	**CSS_PARAMS_306 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 306							
R0xF366	**15:0**	**0x0000**	**CSS_PARAMS_307 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 307							
R0xF368	**15:0**	**0x0000**	**CSS_PARAMS_308 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 308							
R0xF36A	**15:0**	**0x0000**	**CSS_PARAMS_309 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 309							
R0xF36C	**15:0**	**0x0000**	**CSS_PARAMS_310 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 310							
R0xF36E	**15:0**	**0x0000**	**CSS_PARAMS_311 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 311							
R0xF370	**15:0**	**0x0000**	**CSS_PARAMS_312 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 312							
R0xF372	**15:0**	**0x0000**	**CSS_PARAMS_313 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 313							
R0xF374	**15:0**	**0x0000**	**CSS_PARAMS_314 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 314							
R0xF376	**15:0**	**0x0000**	**CSS_PARAMS_315 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 315							
R0xF378	**15:0**	**0x0000**	**CSS_PARAMS_316 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 316							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF37A	**15:0**	**0x0000**	**CSS_PARAMS_317 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 317							
R0xF37C	**15:0**	**0x0000**	**CSS_PARAMS_318 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 318							
R0xF37E	**15:0**	**0x0000**	**CSS_PARAMS_319 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 319							
R0xF380	**15:0**	**0x0000**	**CSS_PARAMS_320 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 320							
R0xF382	**15:0**	**0x0000**	**CSS_PARAMS_321 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 321							
R0xF384	**15:0**	**0x0000**	**CSS_PARAMS_322 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 322							
R0xF386	**15:0**	**0x0000**	**CSS_PARAMS_323 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 323							
R0xF388	**15:0**	**0x0000**	**CSS_PARAMS_324 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 324							
R0xF38A	**15:0**	**0x0000**	**CSS_PARAMS_325 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 325							
R0xF38C	**15:0**	**0x0000**	**CSS_PARAMS_326 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 326							
R0xF38E	**15:0**	**0x0000**	**CSS_PARAMS_327 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 327							
R0xF390	**15:0**	**0x0000**	**CSS_PARAMS_328 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 328							
R0xF392	**15:0**	**0x0000**	**CSS_PARAMS_329 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 329							
R0xF394	**15:0**	**0x0000**	**CSS_PARAMS_330 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 330							
R0xF396	**15:0**	**0x0000**	**CSS_PARAMS_331 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 331							
R0xF398	**15:0**	**0x0000**	**CSS_PARAMS_332 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 332							
R0xF39A	**15:0**	**0x0000**	**CSS_PARAMS_333 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 333							
R0xF39C	**15:0**	**0x0000**	**CSS_PARAMS_334 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 334							
R0xF39E	**15:0**	**0x0000**	**CSS_PARAMS_335 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 335							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF3A0	15:0	0x0000	CSS_PARAMS_336 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 336							
R0xF3A2	15:0	0x0000	CSS_PARAMS_337 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 337							
R0xF3A4	15:0	0x0000	CSS_PARAMS_338 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 338							
R0xF3A6	15:0	0x0000	CSS_PARAMS_339 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 339							
R0xF3A8	15:0	0x0000	CSS_PARAMS_340 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 340							
R0xF3AA	15:0	0x0000	CSS_PARAMS_341 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 341							
R0xF3AC	15:0	0x0000	CSS_PARAMS_342 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 342							
R0xF3AE	15:0	0x0000	CSS_PARAMS_343 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 343							
R0xF3B0	15:0	0x0000	CSS_PARAMS_344 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 344							
R0xF3B2	15:0	0x0000	CSS_PARAMS_345 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 345							
R0xF3B4	15:0	0x0000	CSS_PARAMS_346 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 346							
R0xF3B6	15:0	0x0000	CSS_PARAMS_347 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 347							
R0xF3B8	15:0	0x0000	CSS_PARAMS_348 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 348							
R0xF3BA	15:0	0x0000	CSS_PARAMS_349 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 349							
R0xF3BC	15:0	0x0000	CSS_PARAMS_350 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 350							
R0xF3BE	15:0	0x0000	CSS_PARAMS_351 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 351							
R0xF3C0	15:0	0x0000	CSS_PARAMS_352 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 352							
R0xF3C2	15:0	0x0000	CSS_PARAMS_353 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 353							
R0xF3C4	15:0	0x0000	CSS_PARAMS_354 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 354							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF3C6	15:0	0x0000	CSS_PARAMS_355 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 355							
R0xF3C8	15:0	0x0000	CSS_PARAMS_356 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 356							
R0xF3CA	15:0	0x0000	CSS_PARAMS_357 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 357							
R0xF3CC	15:0	0x0000	CSS_PARAMS_358 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 358							
R0xF3CE	15:0	0x0000	CSS_PARAMS_359 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 359							
R0xF3D0	15:0	0x0000	CSS_PARAMS_360 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 360							
R0xF3D2	15:0	0x0000	CSS_PARAMS_361 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 361							
R0xF3D4	15:0	0x0000	CSS_PARAMS_362 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 362							
R0xF3D6	15:0	0x0000	CSS_PARAMS_363 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 363							
R0xF3D8	15:0	0x0000	CSS_PARAMS_364 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 364							
R0xF3DA	15:0	0x0000	CSS_PARAMS_365 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 365							
R0xF3DC	15:0	0x0000	CSS_PARAMS_366 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 366							
R0xF3DE	15:0	0x0000	CSS_PARAMS_367 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 367							
R0xF3E0	15:0	0x0000	CSS_PARAMS_368 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 368							
R0xF3E2	15:0	0x0000	CSS_PARAMS_369 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 369							
R0xF3E4	15:0	0x0000	CSS_PARAMS_370 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 370							
R0xF3E6	15:0	0x0000	CSS_PARAMS_371 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 371							
R0xF3E8	15:0	0x0000	CSS_PARAMS_372 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 372							
R0xF3EA	15:0	0x0000	CSS_PARAMS_373 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 373							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF3EC	**15:0**	**0x0000**	**CSS_PARAMS_374 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 374							
R0xF3EE	**15:0**	**0x0000**	**CSS_PARAMS_375 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 375							
R0xF3F0	**15:0**	**0x0000**	**CSS_PARAMS_376 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 376							
R0xF3F2	**15:0**	**0x0000**	**CSS_PARAMS_377 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 377							
R0xF3F4	**15:0**	**0x0000**	**CSS_PARAMS_378 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 378							
R0xF3F6	**15:0**	**0x0000**	**CSS_PARAMS_379 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 379							
R0xF3F8	**15:0**	**0x0000**	**CSS_PARAMS_380 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 380							
R0xF3FA	**15:0**	**0x0000**	**CSS_PARAMS_381 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 381							
R0xF3FC	**15:0**	**0x0000**	**CSS_PARAMS_382 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 382							
R0xF3FE	**15:0**	**0x0000**	**CSS_PARAMS_383 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 383							
R0xF400	**15:0**	**0x0000**	**CSS_PARAMS_384 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 384							
R0xF402	**15:0**	**0x0000**	**CSS_PARAMS_385 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 385							
R0xF404	**15:0**	**0x0000**	**CSS_PARAMS_386 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 386							
R0xF406	**15:0**	**0x0000**	**CSS_PARAMS_387 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 387							
R0xF408	**15:0**	**0x0000**	**CSS_PARAMS_388 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 388							
R0xF40A	**15:0**	**0x0000**	**CSS_PARAMS_389 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 389							
R0xF40C	**15:0**	**0x0000**	**CSS_PARAMS_390 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 390							
R0xF40E	**15:0**	**0x0000**	**CSS_PARAMS_391 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 391							
R0xF410	**15:0**	**0x0000**	**CSS_PARAMS_392 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 392							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF412	**15:0**	**0x0000**	**CSS_PARAMS_393 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 393							
R0xF414	**15:0**	**0x0000**	**CSS_PARAMS_394 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 394							
R0xF416	**15:0**	**0x0000**	**CSS_PARAMS_395 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 395							
R0xF418	**15:0**	**0x0000**	**CSS_PARAMS_396 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 396							
R0xF41A	**15:0**	**0x0000**	**CSS_PARAMS_397 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 397							
R0xF41C	**15:0**	**0x0000**	**CSS_PARAMS_398 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 398							
R0xF41E	**15:0**	**0x0000**	**CSS_PARAMS_399 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 399							
R0xF420	**15:0**	**0x0000**	**CSS_PARAMS_400 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 400							
R0xF422	**15:0**	**0x0000**	**CSS_PARAMS_401 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 401							
R0xF424	**15:0**	**0x0000**	**CSS_PARAMS_402 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 402							
R0xF426	**15:0**	**0x0000**	**CSS_PARAMS_403 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 403							
R0xF428	**15:0**	**0x0000**	**CSS_PARAMS_404 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 404							
R0xF42A	**15:0**	**0x0000**	**CSS_PARAMS_405 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 405							
R0xF42C	**15:0**	**0x0000**	**CSS_PARAMS_406 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 406							
R0xF42E	**15:0**	**0x0000**	**CSS_PARAMS_407 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 407							
R0xF430	**15:0**	**0x0000**	**CSS_PARAMS_408 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 408							
R0xF432	**15:0**	**0x0000**	**CSS_PARAMS_409 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 409							
R0xF434	**15:0**	**0x0000**	**CSS_PARAMS_410 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 410							
R0xF436	**15:0**	**0x0000**	**CSS_PARAMS_411 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 411							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF438	**15:0**	**0x0000**	**CSS_PARAMS_412 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 412							
R0xF43A	**15:0**	**0x0000**	**CSS_PARAMS_413 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 413							
R0xF43C	**15:0**	**0x0000**	**CSS_PARAMS_414 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 414							
R0xF43E	**15:0**	**0x0000**	**CSS_PARAMS_415 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 415							
R0xF440	**15:0**	**0x0000**	**CSS_PARAMS_416 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 416							
R0xF442	**15:0**	**0x0000**	**CSS_PARAMS_417 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 417							
R0xF444	**15:0**	**0x0000**	**CSS_PARAMS_418 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 418							
R0xF446	**15:0**	**0x0000**	**CSS_PARAMS_419 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 419							
R0xF448	**15:0**	**0x0000**	**CSS_PARAMS_420 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 420							
R0xF44A	**15:0**	**0x0000**	**CSS_PARAMS_421 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 421							
R0xF44C	**15:0**	**0x0000**	**CSS_PARAMS_422 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 422							
R0xF44E	**15:0**	**0x0000**	**CSS_PARAMS_423 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 423							
R0xF450	**15:0**	**0x0000**	**CSS_PARAMS_424 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 424							
R0xF452	**15:0**	**0x0000**	**CSS_PARAMS_425 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 425							
R0xF454	**15:0**	**0x0000**	**CSS_PARAMS_426 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 426							
R0xF456	**15:0**	**0x0000**	**CSS_PARAMS_427 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 427							
R0xF458	**15:0**	**0x0000**	**CSS_PARAMS_428 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 428							
R0xF45A	**15:0**	**0x0000**	**CSS_PARAMS_429 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 429							
R0xF45C	**15:0**	**0x0000**	**CSS_PARAMS_430 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 430							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF45E	**15:0**	**0x0000**	**CSS_PARAMS_431 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 431							
R0xF460	**15:0**	**0x0000**	**CSS_PARAMS_432 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 432							
R0xF462	**15:0**	**0x0000**	**CSS_PARAMS_433 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 433							
R0xF464	**15:0**	**0x0000**	**CSS_PARAMS_434 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 434							
R0xF466	**15:0**	**0x0000**	**CSS_PARAMS_435 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 435							
R0xF468	**15:0**	**0x0000**	**CSS_PARAMS_436 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 436							
R0xF46A	**15:0**	**0x0000**	**CSS_PARAMS_437 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 437							
R0xF46C	**15:0**	**0x0000**	**CSS_PARAMS_438 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 438							
R0xF46E	**15:0**	**0x0000**	**CSS_PARAMS_439 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 439							
R0xF470	**15:0**	**0x0000**	**CSS_PARAMS_440 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 440							
R0xF472	**15:0**	**0x0000**	**CSS_PARAMS_441 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 441							
R0xF474	**15:0**	**0x0000**	**CSS_PARAMS_442 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 442							
R0xF476	**15:0**	**0x0000**	**CSS_PARAMS_443 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 443							
R0xF478	**15:0**	**0x0000**	**CSS_PARAMS_444 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 444							
R0xF47A	**15:0**	**0x0000**	**CSS_PARAMS_445 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 445							
R0xF47C	**15:0**	**0x0000**	**CSS_PARAMS_446 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 446							
R0xF47E	**15:0**	**0x0000**	**CSS_PARAMS_447 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 447							
R0xF480	**15:0**	**0x0000**	**CSS_PARAMS_448 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 448							
R0xF482	**15:0**	**0x0000**	**CSS_PARAMS_449 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 449							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF484	**15:0**	**0x0000**	**CSS_PARAMS_450 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 450							
R0xF486	**15:0**	**0x0000**	**CSS_PARAMS_451 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 451							
R0xF488	**15:0**	**0x0000**	**CSS_PARAMS_452 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 452							
R0xF48A	**15:0**	**0x0000**	**CSS_PARAMS_453 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 453							
R0xF48C	**15:0**	**0x0000**	**CSS_PARAMS_454 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 454							
R0xF48E	**15:0**	**0x0000**	**CSS_PARAMS_455 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 455							
R0xF490	**15:0**	**0x0000**	**CSS_PARAMS_456 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 456							
R0xF492	**15:0**	**0x0000**	**CSS_PARAMS_457 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 457							
R0xF494	**15:0**	**0x0000**	**CSS_PARAMS_458 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 458							
R0xF496	**15:0**	**0x0000**	**CSS_PARAMS_459 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 459							
R0xF498	**15:0**	**0x0000**	**CSS_PARAMS_460 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 460							
R0xF49A	**15:0**	**0x0000**	**CSS_PARAMS_461 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 461							
R0xF49C	**15:0**	**0x0000**	**CSS_PARAMS_462 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 462							
R0xF49E	**15:0**	**0x0000**	**CSS_PARAMS_463 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 463							
R0xF4A0	**15:0**	**0x0000**	**CSS_PARAMS_464 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 464							
R0xF4A2	**15:0**	**0x0000**	**CSS_PARAMS_465 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 465							
R0xF4A4	**15:0**	**0x0000**	**CSS_PARAMS_466 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 466							
R0xF4A6	**15:0**	**0x0000**	**CSS_PARAMS_467 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 467							
R0xF4A8	**15:0**	**0x0000**	**CSS_PARAMS_468 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 468							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF4AA	**15:0**	**0x0000**	**CSS_PARAMS_469 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 469							
R0xF4AC	**15:0**	**0x0000**	**CSS_PARAMS_470 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 470							
R0xF4AE	**15:0**	**0x0000**	**CSS_PARAMS_471 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 471							
R0xF4B0	**15:0**	**0x0000**	**CSS_PARAMS_472 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 472							
R0xF4B2	**15:0**	**0x0000**	**CSS_PARAMS_473 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 473							
R0xF4B4	**15:0**	**0x0000**	**CSS_PARAMS_474 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 474							
R0xF4B6	**15:0**	**0x0000**	**CSS_PARAMS_475 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 475							
R0xF4B8	**15:0**	**0x0000**	**CSS_PARAMS_476 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 476							
R0xF4BA	**15:0**	**0x0000**	**CSS_PARAMS_477 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 477							
R0xF4BC	**15:0**	**0x0000**	**CSS_PARAMS_478 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 478							
R0xF4BE	**15:0**	**0x0000**	**CSS_PARAMS_479 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 479							
R0xF4C0	**15:0**	**0x0000**	**CSS_PARAMS_480 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 480							
R0xF4C2	**15:0**	**0x0000**	**CSS_PARAMS_481 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 481							
R0xF4C4	**15:0**	**0x0000**	**CSS_PARAMS_482 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 482							
R0xF4C6	**15:0**	**0x0000**	**CSS_PARAMS_483 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 483							
R0xF4C8	**15:0**	**0x0000**	**CSS_PARAMS_484 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 484							
R0xF4CA	**15:0**	**0x0000**	**CSS_PARAMS_485 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 485							
R0xF4CC	**15:0**	**0x0000**	**CSS_PARAMS_486 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 486							
R0xF4CE	**15:0**	**0x0000**	**CSS_PARAMS_487 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 487							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS
R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF4D0	15:0	0x0000	CSS_PARAMS_488 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 488							
R0xF4D2	15:0	0x0000	CSS_PARAMS_489 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 489							
R0xF4D4	15:0	0x0000	CSS_PARAMS_490 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 490							
R0xF4D6	15:0	0x0000	CSS_PARAMS_491 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 491							
R0xF4D8	15:0	0x0000	CSS_PARAMS_492 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 492							
R0xF4DA	15:0	0x0000	CSS_PARAMS_493 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 493							
R0xF4DC	15:0	0x0000	CSS_PARAMS_494 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 494							
R0xF4DE	15:0	0x0000	CSS_PARAMS_495 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 495							
R0xF4E0	15:0	0x0000	CSS_PARAMS_496 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 496							
R0xF4E2	15:0	0x0000	CSS_PARAMS_497 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 497							
R0xF4E4	15:0	0x0000	CSS_PARAMS_498 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 498							
R0xF4E6	15:0	0x0000	CSS_PARAMS_499 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 499							
R0xF4E8	15:0	0x0000	CSS_PARAMS_500 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 500							
R0xF4EA	15:0	0x0000	CSS_PARAMS_501 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 501							
R0xF4EC	15:0	0x0000	CSS_PARAMS_502 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 502							
R0xF4EE	15:0	0x0000	CSS_PARAMS_503 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 503							
R0xF4F0	15:0	0x0000	CSS_PARAMS_504 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 504							
R0xF4F2	15:0	0x0000	CSS_PARAMS_505 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 505							
R0xF4F4	15:0	0x0000	CSS_PARAMS_506 (R/W)					unsigned
	Cryptographic subsystem parameter memory word 506							

Table 6. MANUFACTURER−SPECIFIC REGISTER DESCRIPTIONS

R/W (Read or Write) bit; RO (Read Only) bit; WO (Write Only) bit

Register Hex	Bits	Default	Name	Attributes				Data Type
R0xF4F6	**15:0**	**0x0000**	**CSS_PARAMS_507 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 507							
R0xF4F8	**15:0**	**0x0000**	**CSS_PARAMS_508 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 508							
R0xF4FA	**15:0**	**0x0000**	**CSS_PARAMS_509 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 509							
R0xF4FC	**15:0**	**0x0000**	**CSS_PARAMS_510 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 510							
R0xF4FE	**15:0**	**0x0000**	**CSS_PARAMS_511 (R/W)**					**unsigned**
	Cryptographic subsystem parameter memory word 511							

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