

## NCV7685 I<sup>2</sup>C Programming Guide



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### INTRODUCTION AND DOCUMENT SCOPE

This document deals with the recommendation how to control the NCV7685 devices using I<sup>2</sup>C protocol and how to configure OTPs.

### PREREQUISITES

The following guidelines are required:

- VDD supply has to be in range between 3.15 V to 5.5 V.
- Proper selection of the Pull-up resistors in respect with I<sup>2</sup>C speed, VDD supply voltage and bus capacitance.
- For Hard coding and OTP register access, the ISET pin has to be put to high.
- To Burn OTP, the VS supply has to be > 13 V.
- Every I<sup>2</sup>C message is protected by repeating address safety mechanism.
- Additional CRC may be activated based on the ERREN flag.

### PULL UP RESISTOR SELECTION

Open drain I<sup>2</sup>C communication protocol needs pull-up resistors for communication. The pull-up resistors keep the I<sup>2</sup>C pins in high while there is no communication on the bus. The selection of the resistor value depends on bus capacitance, VDD supply, I<sup>2</sup>C speed and power consumption.

The equations for 400 kbps:

$$R_{p(min)} = \frac{V_{DD} - 0.4}{0.003} \Omega \quad (\text{eq. 1})$$

$$R_{p(max)} = \frac{300ns}{0.8473 \cdot C_B} \Omega \quad (\text{eq. 2})$$

### APPLICATION NOTE

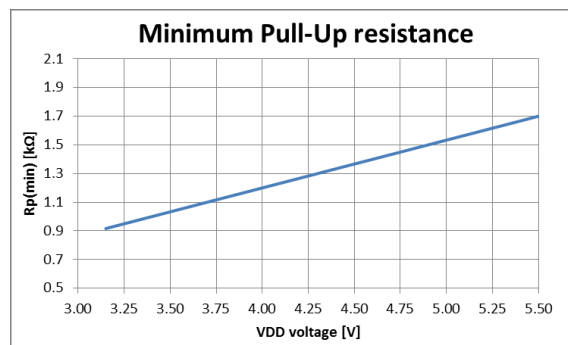


Figure 1. Rp(min) Versus VDD Voltage

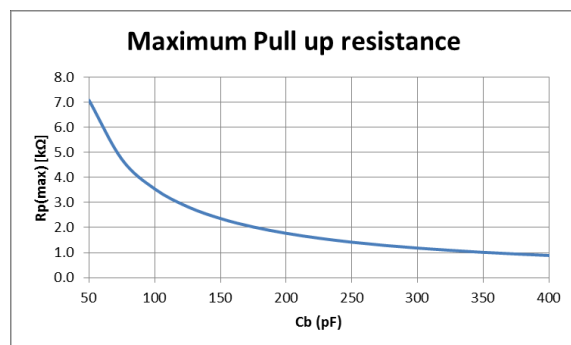


Figure 2. Rp (max) Versus Bus Capacity

For VDD = 3.3 V and bus capacity 100 pF the Pull-up resistors should be in range of 0.98 kΩ to 3.45 kΩ

## FORMAT OF THE I<sup>2</sup>C FRAMES

Writing and reading data to the NCV7685 drivers uses a simple protocol: the address is written, and then data are transferred until the end of the message.

A single message writes to the NCV7685 driver. After the START command, the master sends the chip's bus 7-bit address with the direction bit clear (write), then sends the repeated address data byte and then sends the message identifier (ID) followed with data bytes to be written followed by a STOP. Every transmitted byte is acknowledged by slave device.

To read the data from NCV7685 driver a combined message has to be used. After a START, the master first writes chip's bus 7-bit address with the direction bit clear (write) and then the repeated address 8-bit followed by ID message. Then the (repeated) START is send and the chip's bus 7-bit address with the direction bit set (read). The NCV7685 will then respond with the data bytes which are acknowledged except the last byte and then the stop condition terminate the communication.

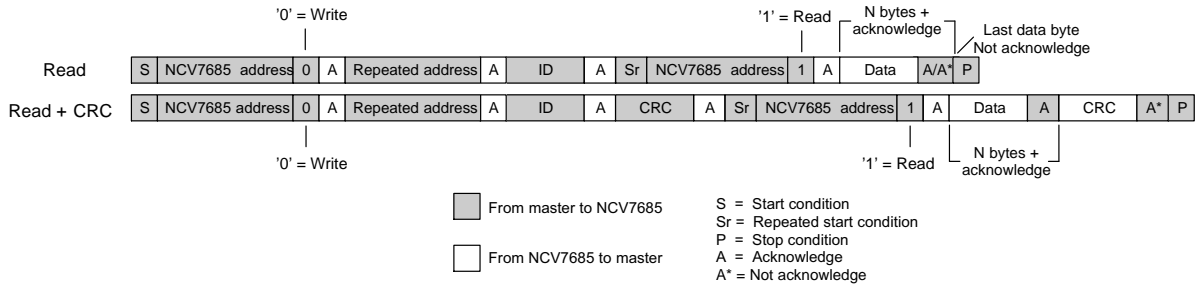


Figure 3. Format of the I<sup>2</sup>C Read Frames with Repeated Start Condition

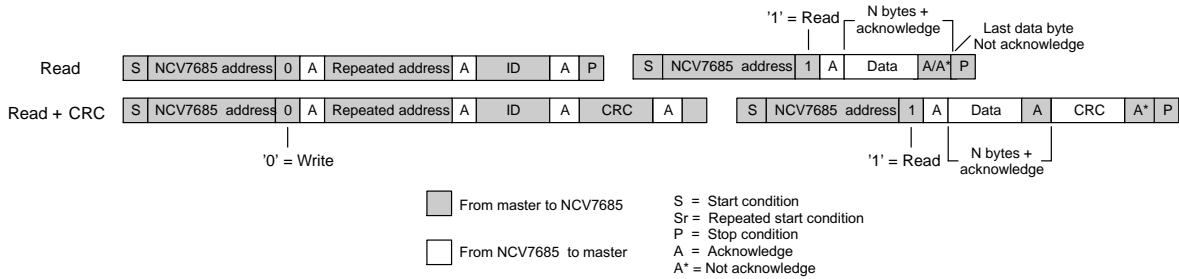


Figure 4. Format of the I<sup>2</sup>C Read Frames with Stop and Start Condition

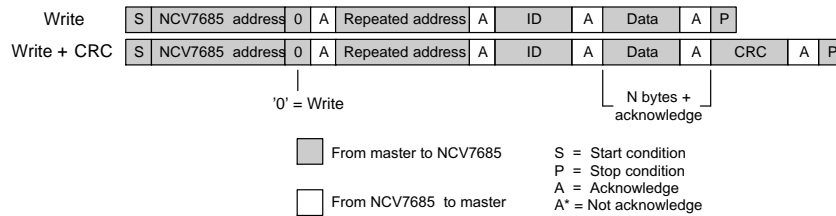


Figure 5. Format of the I<sup>2</sup>C Write Frames

## NCV7685 I<sup>2</sup>C ADDRESSING

The NCV7685 driver is using 7-bit I<sup>2</sup>C address. Up to 32 NCV7685 devices can be addressed using the 5-bits ADD[4:0] OTP register. The remaining two bits of the I<sup>2</sup>C address are fixed: ADD[6:5] = 11.

The default I<sup>2</sup>C address configuration of the non-zapped device is 0b1100000 = 0x60 + R/W flag which is automatically generated by  $\mu$ C.

**Table 1. THE 1<sup>ST</sup> BYTE STRUCTURE OF I<sup>2</sup>C DEVICE ADDRESS**

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	0	0	0	1/0

After first address byte which is automatically send by Master I<sup>2</sup>C device, the repeated address data byte has to be send. The second I<sup>2</sup>C address data byte is safety mechanism

to improve the immunity of the system. This byte contains 8-bits of the data where the address (ADD[4:0]) and W = 0 flag is included in the data byte.

**Table 2. THE 2<sup>ND</sup> BYTE STRUCTURE OF I<sup>2</sup>C DEVICE ADDRESS**

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	0	0

This second byte is send as regular data content. The default value for not zapped device is 0xC0. The list of the all possible combinations is mentioned in the Table 3.

**Table 3. LIST OF THE I<sup>2</sup>C DEVICE ADDRESS**

5-bit	7-bit	8-bit
ADD [4:0] Device#	1 <sup>st</sup> I <sup>2</sup> C Address byte	2 <sup>nd</sup> I <sup>2</sup> C Address byte
0	0x60	0xC0
1	0x61	0xC2
2	0x62	0xC4
3	0x63	0xC6
4	0x64	0xC8
5	0x65	0xCA
6	0x66	0xCC
7	0x67	0xCE
8	0x68	0xD0
9	0x69	0xD2
10	0x6A	0xD4
11	0x6B	0xD6
12	0x6C	0xD8
13	0x6D	0xDA
14	0x6E	0xDC
15	0x6F	0xDE
16	0x70	0xE0
17	0x71	0xE2
18	0x72	0xE4

Table 3. LIST OF THE I<sup>2</sup>C DEVICE ADDRESS

5-bit	7-bit	8-bit
19	0x73	0xE6
20	0x74	0xE8
21	0x75	0xEA
22	0x76	0xEC
23	0x77	0xEE
24	0x78	0xF0
25	0x79	0xF2
26	0x7A	0xF4
27	0x7B	0xF6
28	0x7C	0xF8
29	0x7D	0xFA
30	0x7E	0xFC
31	0x7F	0xFE

## I<sup>2</sup>C COMMUNICATION

This second byte is send as regular data content. The volatile registers can be accessed by sending appropriate ID message. The list of the addressing identifiers is described in the datasheet.

## I<sup>2</sup>C REGISTER READING

The volatile registers: I2C Status, Fault Status, and I2C Channel status can be read using dedicated ID messages. The Hard Coding and OTP registers can be read using ID\_READ\_OTP message.

To read the I<sup>2</sup>C data from the NCV7685, the 7-bit address has to be sent with Write Flag. After repeated address the ID\_STATUS, ID\_FAULT or ID\_READALL is send. Either repeated start or stop condition followed by start condition can be used for second part of the I<sup>2</sup>C communication. The 7-bit address with Read flag has to be transmitted before slave device transmit all requested data bytes. The graphic representation of the I<sup>2</sup>C reading is shown in Figure 3 and Figure 4.

## CRC ERROR DETECTION ALGORITHM

The CRC protection is turned off by default. It can be enabled by activation of the OTP ERREN bit (ERREN = 1). The every I<sup>2</sup>C byte including both addresses with R/W flag are calculated using CRC8 algorithms. The CRC polynomial is following:  $x^8 + x^5 + x^3 + x^2 + x + 1$ .

Table 4. CRC DETAILED PARAMETERS

Parameter	Value
CRC Width	CRC-8
Polynomial	0x2F
Initial Value	0xFF
Final Xor Value	0x00
Input Reflected	no
Result Reflected	no

CRC Calculation [Reference](#)

Example of the CRC used in the I<sup>2</sup>C message with I2C\_CONF byte = 0xCFFF and with I<sup>2</sup>C address 0x60 (0xC0) is 0x2E.

Table 5. EXAMPLE OF THE I<sup>2</sup>C MESSAGE WITH CRC8 PROTECTION

Device Address & R/W bit	Repeated address	ID	I2C CONF [15:8]	I2C CONF [7:0]	CRC
0xC0	0xC0	0x00	0xCF	0xFF	0x2E

**OTP PROGRAMMING**

To access the Hardcoding and OTP registers the ISET pin has to be put to high; otherwise the slave device will not respond on these three OTP I<sup>2</sup>C messages (ID\_SET\_OTP, ID\_LOCK\_OTP and ID\_READ\_OTP).

The I<sup>2</sup>C address, Open Load detection modes, CRC activation, silicon ID device and channel configuration can be read/(write) by OTP messages.

The ISET pin has to be externally pulled high to the voltage between 2.5 V and 3.3 V otherwise the driver will not accept the I<sup>2</sup>C message.

The main intention of forcing 2.5 V – 3.3 V to the ISET pin is protection against entering to the programming mode during the normal operation. And this technique is also used as chip select functionality for the End-Of-Line OTP programming procedure.

Three sets of the commands are available to access the OTP registers: ID\_SET\_OTP (W), ID\_LOCK\_OTP (W) and ID\_READ\_OTP(R).

The ID\_SET\_OTP message will write the information into shadow registers without affecting the OTP registers. The information in registers is lost when both power supplies (VDD and VS) are turned off.

The ID\_LOCK\_OTP message will zap the OTPs. No further change will be possible. It is necessary to have VS supply voltage higher than 13 V to ensure proper zapping procedure.

Please note that as soon as the ID\_SET\_OTP or ID\_LOCK\_OTP is processed, all other I<sup>2</sup>C messages have to be sent with respect to the new I<sup>2</sup>C address or CRC activation setting.

**REQUIRED TIME DELAY FOR OTP ZAPPING**

As soon as the ID\_LOCK\_OTP message is received, the I<sup>2</sup>C acknowledge is immediately sent out to the MCU. However, the internal circuitries still requires 500 µs time delay to complete the OTP zapping of one OTP bit. Therefore, no I<sup>2</sup>C confirmation is send. The number of OTP bits that are zapped corresponds with each change from the default values. It is needed 16.5 ms in total to successfully finish the zapping sequence of all 32 customer bits + one internal bit. The verification of the OTP banks can be done by readout of the ID\_READ\_OTP I<sup>2</sup>C message after zapping delay.

**CHANGING THE OTP ADDRESS ON THE SAME I<sup>2</sup>C BUS**

Every non-zapped device has the same I<sup>2</sup>C address. To change the address, the ID\_SET\_OTP or ID\_LOCK\_OTP message with appropriate content has to be sent. It is necessary to put the ISET pin to high, to address appropriate device. The graphic representation of the End-of-Line OTP programming is shown in Figure 6.

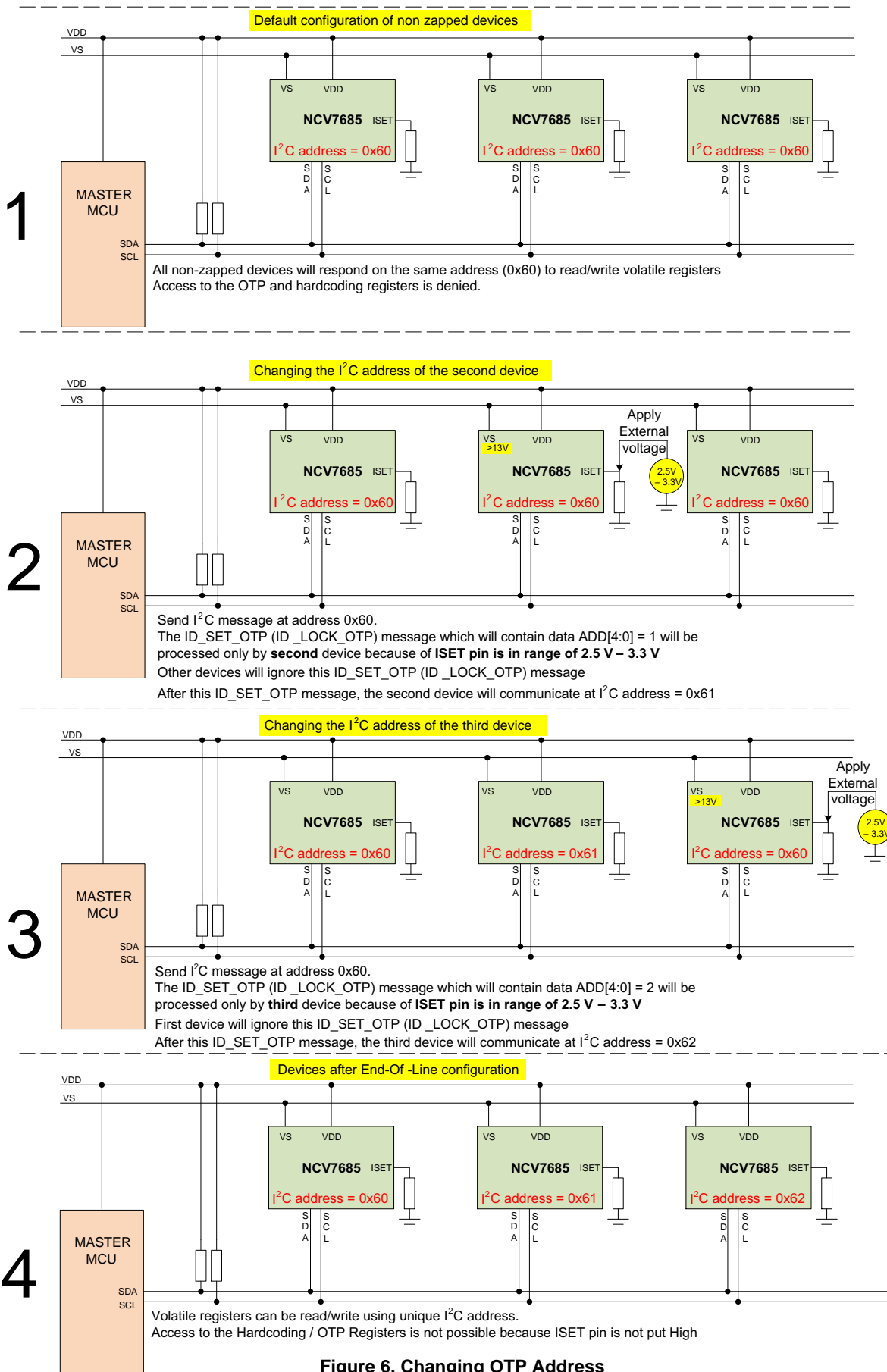



Figure 6. Changing OTP Address

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