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# AND9714/D

# Designing a LED Driver Controlled by the NCL30386/88

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**APPLICATION NOTE**

### Description

This paper describes the key steps to design a LED driver controlled by the NCL30386/88. It gives hints on the components selection to obtain a good constant−voltage and constant−current regulation.

The process is illustrated by a practical 20−W, universal main application:

- Maximum output power: 20 W
- Input voltage range: 90 to 265 V rms
- Output voltage range: 20 to 40 V dc
- Output current: 500 mA

### Introduction

The NCL30386 [1] and NCL30388 [2] are power−factor−corrected controllers with primary side constant voltage (CV) and constant current (CC) Control suitable for flyback, buck−boost or SEPIC. The NCL30386 is housed in an SOIC 10 package and provides analog dimming of the output current with two dedicated dimming control input pins ADIM and PDIM. The NCL30388 is housed in an SOIC 8 package and targets high−performance LED drivers. These controllers integrate a proprietary circuit for power factor correction and constant current control allowing achieving a power factor above 0.95 with a total harmonic distortion below 10% for universal mains input. The output current and the output voltage regulation are typically within ±2% for an input voltage varying from 85 V rms to 265 V rms. The current−mode, quasi−resonant architecture of these controllers optimizes the efficiency by turning on the MOSFET when the drain−source voltage is minimal (valley). The valley lockout and frequency foldback circuitry maintains high−efficiency performance in dimmed conditions or in light load during constant−voltage regulation.

In addition, the circuit contains a set of powerful protections to ensure a robust LED driver design [1]:

- Output Over Voltage Protection
- Cycle−by−cycle Peak Current Limit
- Winding and Output Diode Short Circuit Protection
- Output Short Circuit Protection
- $V_{CC}$ pin Over Voltage Protection
- Floating/Short Pin Detection: the circuit can detect most of these situations which is of great help to pass safety tests

## MAXIMUM DUTY−RATIO

The NCL30386 / 88 offer a board range of options. Among them, there are two selectable reference voltages for the constant current regulation: $V_{REF}$ = 333 mV or $V_{REF}$ = 250 mV. The reference voltage selection directly sets the duty−ratio limit.

For $V_{REF}$ = 333 mV, the duty−ratio is limited to 70% at the top of the lowest line sinusoid. For $V_{REF}$ = 250 mV, the duty−ratio is limited to 80% at the top of the lowest line sinusoid.

**Table 1. OUTPUT VOLTAGE RANGE OF CONVERTER**

| Controller Reference Voltagefor CC Mode | Maximum Duty−Ratio at $V_{inLL,rms}$ | Output Voltage Range for Non−isolated Converters (Note 1) | Output Voltage Range for Flyback Converters (Note 1) |
|---|---|---|---|
| $V_{REF}$ = 333 mV | 50% | $V_{out} + V_f \le \sqrt{2}\ V_{inLL,\,rms}$ | $V_{out} + V_f \le \frac{n_s}{n_p}\sqrt{2}\ V_{inLL,\,rms}$ |
| $V_{REF}$ = 250 mV | 63% | $V_{out} + V_f \le \frac{63}{37}\sqrt{2}\ V_{inLL,\,rms}$ | $V_{out} + V_f \le \frac{63}{37}\frac{n_s}{n_p}\sqrt{2}\ V_{inLL,\,rms}$ |

1. $V_{inLL,rms}$ is the lowest line rms voltage (e.g. 85 V rms), $V_f$ is the output diode forward voltage.

## PRIMARY SIDE CONSTANT VOLTAGE OPERATION

In primary−side constant−voltage regulation, the output voltage is sensed via the auxiliary winding. Indeed, the auxiliary winding provides an image of the output voltage during the off−time of the power MOSFET. By sampling the auxiliary voltage knee (which represents the end of the core demagnetization) the controller is able to accurately control the output voltage. Figure 1 illustrates the idealized waveforms of a flyback converter operated in discontinuous conduction mode (DCM). When the secondary current becomes null, the auxiliary winding voltage is sampled on ZCD pin:

$$V_{ZCD} = \frac{R_{ZCDL}}{R_{ZCDU} + R_{ZCDL}} \times \frac{N_{ap}}{N_{sp}} \times V_{out} \qquad \text{(eq. 1)}$$

Where:

- $N_{ap}$ is the auxiliary to primary turns ratio: $N_{ap} = N_a / N_p$ with $N_a$ and $N_p$ being respectively the auxiliary and primary turns
- $N_{sp}$ is the secondary to primary turns ratio: $N_{sp} = N_s / N_p$ with $N_s$ being respectively the secondary turns
- $R_{ZCDU}$ is the upper resistor of the voltage divider at ZCD pin
- $R_{ZCDL}$ is the lower resistor of the voltage divider at ZCD pin

The sampled voltage is applied to the negative input terminal of the operational transconductance amplifier (OTA) and compared to the internal precise reference voltage $V_{REF(CV)}$ ( Figure 2). A voltage feedback $V_{COMP}$ is then generated through the external components placed at the OTA output. This $V_{COMP}$ is then internally used to modulate the reference voltage of the PFC loop. The reference voltage is modulated from 0% to 100% of $V_{REF}$ to regulate the output voltage.

The resistor divider ($R_{ZCDU}$, $R_{ZCDL}$) from the auxiliary winding to the ZCD pin selects the output voltage nominal value:

$$V_{REF(CV)} = \frac{R_{ZCDL}}{R_{ZCDU} + R_{ZCDL}} \times \frac{N_{ap}}{N_{sp}} \times V_{out} \qquad \text{(eq. 2)}$$

There are several ways to calculate $R_{ZCDU}$ and $R_{ZCDL}$. To decrease the resistor divider current consumption and keep the $RC$ time constant at ZCD pin small, it is better to choose $R_{ZCDU}$ in the range of 10 kΩ to 82 kΩ..

Then $R_{ZCDL}$ value can be calculated with:

$$R_{ZCDL} = \frac{R_{ZCDU} \times V_{REF(CV)}}{\frac{N_{ap}}{N_{sp}} \times V_{out} - V_{REF(CV)}} \qquad \text{(eq. 3)}$$

For the 20−W LED driver board, a 43−kΩ $R_{ZCDU}$ resistance was chosen . Thus, $R_{ZCDL}$ value is:

$$R_{ZCDL} = \frac{43k \times 2.5}{\frac{0.183}{0.353}\ 40 - 2.5} = 5.9\ k\Omega \qquad \text{(eq. 4)}$$

Finally, two 12−kΩ resistors in parallel were chosen for $R_{ZCDL}$.

The power factor correction operation induces larges variations of the MOSFET off−time. Particularly around the input voltage zero crossing, the demagnetization time is very small and the auxiliary winding voltage cannot be sampled correctly. For this reason, the sampling is disabled whenever the input sine waveform is below 50 V with a 5 V hysteresis. In the same way, the sampling is disabled during the ZCD blanking to avoid false reading output voltage caused by the leakage inductance at the power switch turn off. Thus, the power supply designer must ensure that $t_{demag} > 2\,\mu s$ when $V_{in}$ is above 55 V for heavy to medium output load and $t_{demag} >$ 1.3 μs for light load conditions.

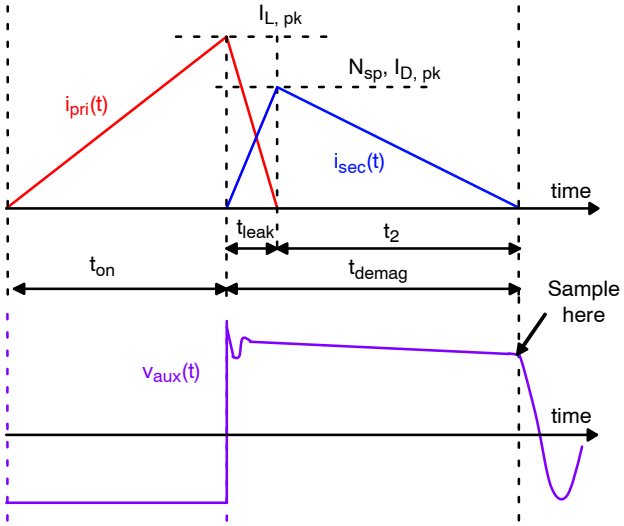


**Figure 1. Idealized Waveforms of a Flyback Converter in DCM**

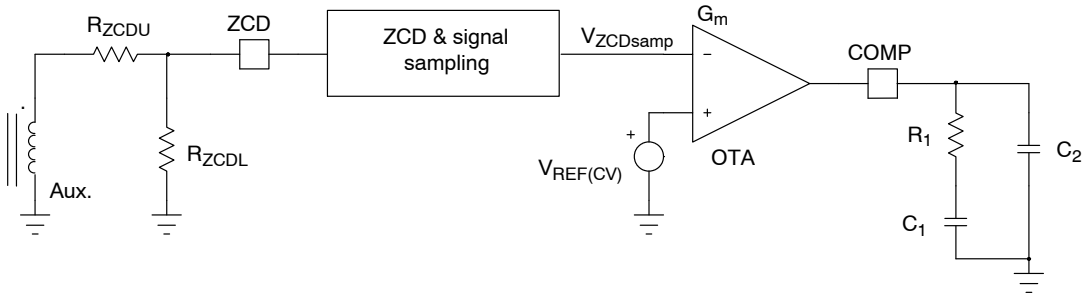


**Figure 2. Constant Voltage Feedback Circuit**

## TRANSFORMER SELECTION FOR GOOD CV REGULATION

The application note AND9200 [2] details how to select the turns ratio and primary inductance for the NCL3008X family of controller. The same method can be applied for the NCL30386/88 with some specificity concerning the constant voltage mode.

### Selecting the Secondary turns ratio

The secondary to primary turns ratio of the transformer called $N_{sp}$ in this document ($N_{sp} = n_s / n_p$) sets the reflected voltage during the off−time and thus, must be high enough to limit the voltage stress across the primary−side MOSFET. The maximum voltage to be sustained by the MOSFET is:

$$V_{DS, max} = \sqrt{2}\ V_{inHL, rms} + \frac{(1 + k_c)\ (V_{out(OVP)} + V_f)}{N_{sp}} \qquad \text{(eq. 5)}$$

Where:

- $k_c$ is the clamping coefficient of the RCD clamp network. The clamping network is generally designed so that the voltage overshoot on the MOSFET drain caused by the leakage inductance reset is between 50% and 100% of the reflected voltage: $0.5 \leq k_c \leq 1$
- $V_{inHL, rms}$ is the highest line voltage
- $V_{out(OVP)}$ is the output voltage at which the fast OVP will trigger:

$$V_{out(OVP)} = 1.3\ V_{out(nom)} \qquad \text{(eq. 6)}$$

- $V_{out(nom)}$ Is the output voltage setpoint for the constant voltage regulation

Some derating is requested to avoid exceeding the MOSFET breakdown voltage. If we apply a 15% safety factor, the MOSFET voltage, in a worst−case situation, must remain below 85% of its breakdown voltage. Finally, the turns ratio can be estimated with eq. 7.

$$N_{sp} \geq \frac{(1 + k_c)\ (1.3\ V_{out(nom)} + V_f)}{0.85\ V_{DSS} - \sqrt{2}\ V_{inHL, rms}} \qquad \text{(eq. 7)}$$

In our design, $V_{inHL, rms}$ is 265 V and $V_{out(nom)}$ is 40 V. With a 800−V MOSFET, we have:

$$N_{sp} \geq \frac{(1 + 0.8)\ (1.3 \times 40 + 0.6)}{0.85 \times 800 - \sqrt{2} \times 265} \cong 0.311 \qquad \text{(eq. 8)}$$

Finally, we chose $N_{sp}$ = 0.35.

Using Table 1, it can be checked that a controller with $V_{REF}$ = 333 mV is enough for our design.

### Selecting the Auxiliary turns ratio

The Auxiliary winding can be designed such that the controller is supplied by the auxiliary winding when there are few LEDs at the output, meaning the output voltage is at its minimum value $V_{out(min)}$. It is reasonable to target a 10−V value for $V_{CC}$ when $V_{out} = V_{out(min)}$. In this case, the auxiliary winding turns ratio can be calculated with:

$$N_{ap} = \frac{N_{sp}\,(V_{CC} + V_f)}{V_{out(min)} + V_f} \qquad \text{(eq. 9)}$$

Based on eq. 10, we selected $N_{ap}$ = 0.183 for our transformer.

$$N_{ap} = \frac{0.35\,(10 + 0.6)}{20 + 0.6} = 0.18 \qquad \text{(eq. 10)}$$

### Selecting the Primary Inductance

It is important to choose the primary inductance in order to provide a demagnetization time long enough for a correct sampling of the output voltage. As said above, ZCD sampling is not allowed if:

- $t_{demag} < t_{ZCD(blank)}$
- $V_{in} < 50$ V

For a correct voltage sampling, we need:

- $t_{demag} \geq 1.3$ μs when 0 V < $V_{REFX} \leq 25\%V_{REF}$ (light load)
- $t_{demag} \geq 2$ μs when $25\%V_{REF} < V_{REFX} \leq V_{REF}$

Practically, to avoid too big a $L_p$, we can decide to meet the above constraint when $v_{in}\,(t) \geq V_{in,\,pk} / 2$. Also, $t_{demag}$ tends to decrease as the output load decreases, thus, the primary inductance will be calculated when $V_{REFX} = 25\%V_{REF}$, which is the transition threshold for valley lockout to frequency foldback operation.

When designing the transformer, the Mathcad® spreadsheet can help to adjust the primary inductance in order to have $t_{demag}$ large enough for correct sampling. If you do not want to use Mathcad, the following equation can help choosing $L_p$:

$$L_p \geq \frac{R_{sense}(V_{out} + V_f) \times t_{demag}^{\,2}}{\frac{0.25\,V_{REF}}{2} \times N_{sp}\left[t_{demag} + t_v(2n_v - 1) + \frac{t_{demag}(V_{out} + V_f)}{N_{sp} \times \frac{\sqrt{2}\,V_{in,\,rms}}{2}}\right]} \qquad \text{(eq. 11)}$$

Where:

- $t_{demag}$ is the transformer targeted demagnetization duration and must be ≥ 2 μs
- $V_{REF}$ = 333 mV

$n_v$ is the operating valley number: $n_v$ = 5 if $V_{in,\,rms}$ < 200 V, $n_v$ = 6 if $V_{in,\,rms} \geq 200$ V

As a design example, we have chosen a turns ratio $N_{sp}$ = 0.35 for our transformer and we set the targeted demagnetization time at 2.1 μs for $V_{in}$ = 115 V rms. We obtain for $L_p$:

$$L_p \geq \frac{0.9 \times (40 + 0.6) \times 2.1\,\mu^2}{\frac{0.25 \times 0.333}{2} \times 0.35\left[2.1\,\mu + 0.9\,\mu(2 \times 5 - 1) + \frac{2.1\,\mu \times (40 + 0.6)}{0.35 \times \frac{\sqrt{2} \times 115}{2}}\right]} = 837\ \mu\text{H} \qquad \text{(eq. 12)}$$

In the end, we chose $L_p$ at 850 μH.

## COMP PIN

The COMP pin is the output of the OTA used for the constant voltage regulation. Figure 2 shows the recommended compensation scheme. The components $R_1$, $C_1$ and $C_2$ form a type 2 compensator (an origin pole plus a pole / zero pair) with the OTA. The transfer function of the compensator circuit can be expressed as [2]:

$$G(s) = -G_0 \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \quad \text{(eq. 13)}$$

Where:

- $G_0$ is the mid−band gain
- $\omega_z$ is the compensator zero
- $\omega_p$ is the compensator pole

If $C_2$ is much smaller than $C_1$ (at least 10 times smaller), a symbolic expression for $G(s)$ is:

$$G(s) = -\frac{R_1 R_{ZCDL} g_m}{R_{ZCDU} + R_{ZCDL}} \times \frac{1 + \frac{1}{sR_1C_1}}{sR_1C_2} \quad \text{(eq. 14)}$$

In order to select the right components for the loop, we need to find the worst−case operating point for the FB loop. Figure 3 shows the control to output stage bode plots at maximum output load and at light load. The control to output transfer function is the auxiliary winding voltage divided by the COMP pin voltage since this is a primary side regulated system:

$$H(s) = \frac{V_{aux}(s)}{V_{COMP}(s)} \quad \text{(eq. 15)}$$

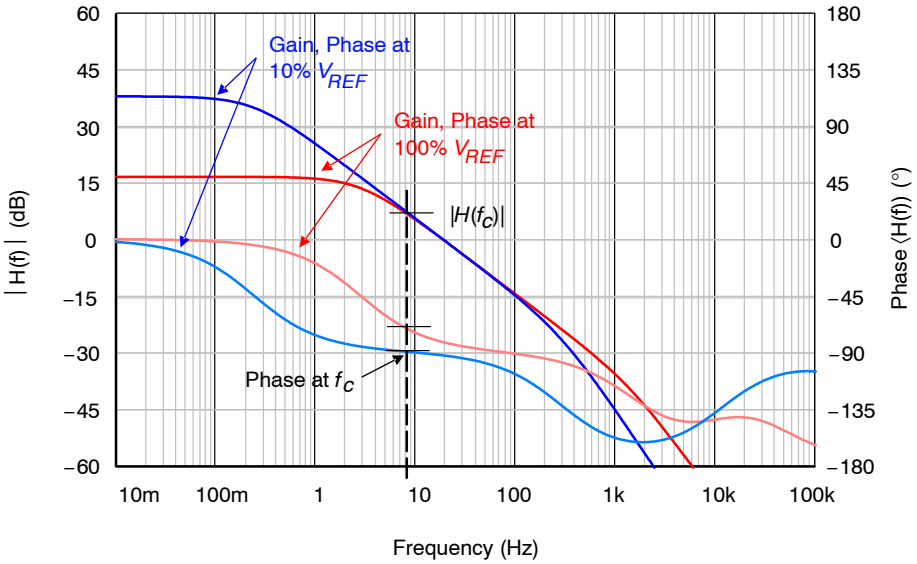


**Figure 3. Bode Plots of the Converter at Maximum Output Load and Light Load**

Because of the control algorithm, the power stage gain increases at light load and the low−frequency pole moves towards lower frequencies (Figure 3). Looking at the phase, the shift is less important at heavy load (−70° versus −90° at light load for the 20−W design example). If we do not take into account this phase shift at light load and consider only the phase at maximum output load to calculate the compensator, this could result in instabilities at light load. On another hand, if we calculate the compensator based only on the light load transfer function, the loop bandwidth would be very limited. For this design, we can see that, based on the light−load curves, the chosen crossover frequency could not be higher than 8 Hz because the power stage phase shift is already −90° at 8 Hz and the type compensator can only bring a phase boost up to 90°. Thus, compensating at light load only results in low bandwidth and sluggish transient output load response. To avoid this, the following compensation method is proposed:

$$f_{zC} = 2\pi\omega_{p1} \quad \text{(eq. 16)}$$

- Place the compensator pole $f_{pc}$ to bring enough phase boost ($PB$) to compensate the light load phase shift:

$$f_{pC} = \frac{f_{zC} f_c + \tan(PB) f_c^2}{f_c - f_{zC}\tan(PB)} \quad \text{(eq. 17)}$$

$$PB = PM - PS - 90 \quad \text{(eq. 18)}$$

Where:

- PB is the phase boost brought by the compensator
- PM is the targeted phase margin
- PS is the power stage phase shift at light load

As a guideline, in order to avoid calculating the phase at light load, consider a phase shift at light load of −90°: $PS$ = −90°.

Target a phase margin of 60° for a robust design: $PM$ = 60°.

- Calculate the mid−band gain of the corrector to cancel the power stage gain at the crossover frequency:

$$\frac{R_1 R_{ZCDL} g_m}{R_{ZCDU} + R_{ZCDL}} = |H(f_c)| \quad \text{(eq. 19)}$$

The control−to−output complete transfer function is not detailed in this application note because the expressions are too large. Everything has been properly entered and verified in the Mathcad spreadsheet (available from www.onsemi.com), so we recommend using the file to calculate the power stage pole, its phase shift at the selected crossover frequency, and the power stage gain $H_{PS}(f_c)$ at the crossover frequency. For people who do not have Mathcad, a simplified mathematical expression of the power stage transfer function is given at the end of this document (see Annexe I)

As an example, if we select a crossover frequency $f_c$ of 8 Hz:

- the power stage low frequency pole is: $f_{p1}$ = 3 Hz
- the phase shift at $f_c$ at light load is $PS$ = −89.7°
- the control−to−output gain at 10 Hz is $H(f_c)$ = 7.06 dB

If we target a phase margin of 60° at light load ($PM$ = 60°), then the phase boost ($PB$) that must be brought by the compensator is:

$$PB = PM - PS - 90 = 60 - (-89.7) - 90 = 59.7° \quad \text{(eq. 20)}$$

$R_1$ is calculated to set the necessary gain or attenuation at the crossover frequency $H(f_c)$.

$$R_1 = |H(f_c)| \frac{R_{ZCDU} + R_{ZCDL}}{R_{ZCDL} g_m} = 10^{\frac{-7.06}{20}} \left( \frac{43k + 6k}{6k \times 50\,\mu} \right) = 72.5\ k\Omega \quad \text{(eq. 21)}$$

A 68−kΩ resistor is chosen for $R_1$.

As said above, the compensator zero is placed at the power stage pole frequency:

$$C_1 = \frac{1}{2\pi f_{p1} R_1} = \frac{1}{2\pi \times 3 \times 68k} = 780\ nF \quad \text{(eq. 22)}$$

In the end, we chose a 1−μF capacitor for $C_1$.

$C_2$ is selected to have enough phase margin at $f_c$:

$$f_{pC} = \frac{f_{zC} f_c + \tan(PB) f_c^{\,2}}{f_c + f_{zC} \tan(PB)} = \frac{3 \times 8 + \tan(59.7) \times 8^2}{8 - 3 \times \tan(59.7)} = 49.8\ Hz \quad \text{(eq. 23)}$$

$$C_2 = \frac{1}{2\pi f_{pC} R_1} = \frac{1}{2\pi \times 49.8 \times 68k} = 47\ nF \quad \text{(eq. 24)}$$

Looking at eq. 23, we calculated a frequency around 50 Hz for the pole. In order to filter the line ripple, it is better to place the pole at a frequency lower than 50 Hz. For this reason, a 100−nF capacitor was chosen for $C_2$.

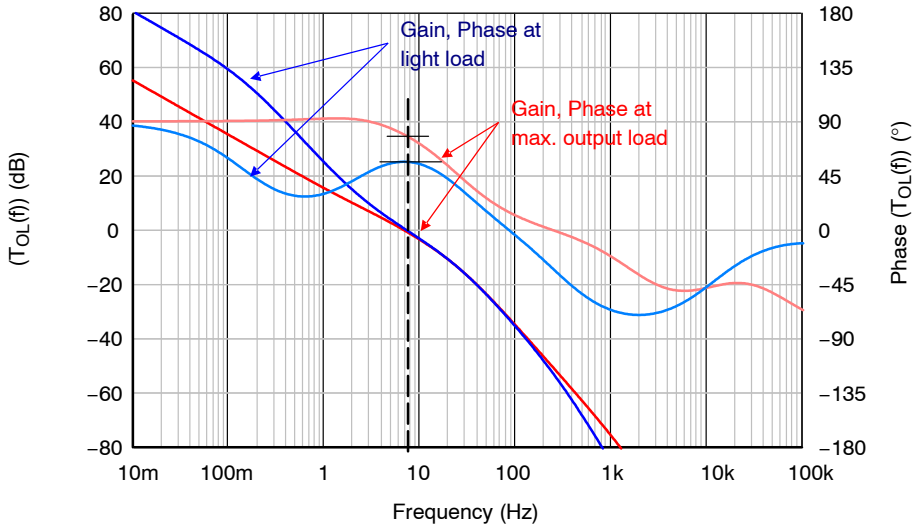


**Figure 4. Open Loop Gain / Phase at Max Output Load**

The open loop transfer function $T_{OL}$(s) gain and phase curves are plotted in Figure 4.

With the chosen compensation, we have a comfortable phase margin of 70° at maximum output load and 56° at light load.

The stability of the design is also confirmed by the transient load step response of the converter shown in Figure 5.

Looking at the transient load step response, we can see that the loop is slow to react, since we chose an 8−Hz crossover frequency. In order to have more bandwidth, we tried two other compensations scheme, setting a crossover frequency of 10 Hz and then 20 Hz. For the transient load step, the output load is varied from 83 Ω to 2 kΩ, resulting in an output current step of 480 mA to 20 mA.

**Table 2. OUTPUT VOLTAGE OVERSHOOT / UNDERSHOOT FOR DIFFERENT COMPENSATIONS**

| | $f_c$ = 8 Hz | $f_c$ = 10 Hz | $f_c$ = 20 Hz |
|---|---|---|---|
| COMP pin elements | $R_1$ = 68 kΩ, $C_1$ = 1 μF, $C_2$ = 100 nF | $R_1$ = 82 kΩ, $C_1$ = 660 nF, $C_2$ = 47 nF | $R_1$ = 150 kΩ, $C_1$ = 330 nF, $C_2$ = 22 nF |
| $V_{out}$ overshoot | 48 V | 46 V | 46 V |
| $V_{out}$ undershoot | 31 V | 32 V | 34 V |
| COMP pin voltage peak to peak ripple at 75% $P_{out,max}$ | 62 mV | 160 mV | 300 mV |
| THD at $V_{in}$ = 115 V rms and $P_{out}$ = 75% $P_{out,max}$ | 5% | 5% | 6.5% |
| THD at $V_{in}$ = 230 V rms and $P_{out}$ = 75% $P_{out,max}$ | 5.7% | 5.7% | 7.6% |

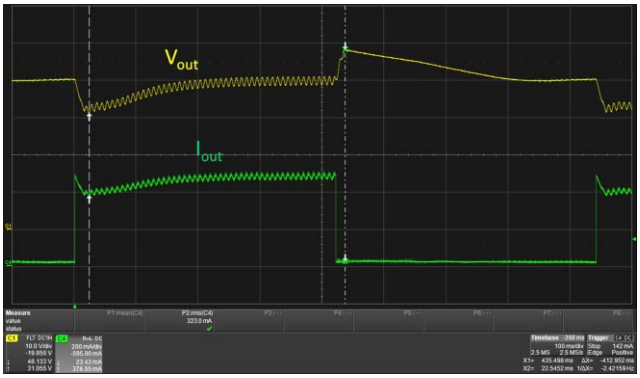


**Figure 5. Load Step for $f_c$ around 8 Hz**

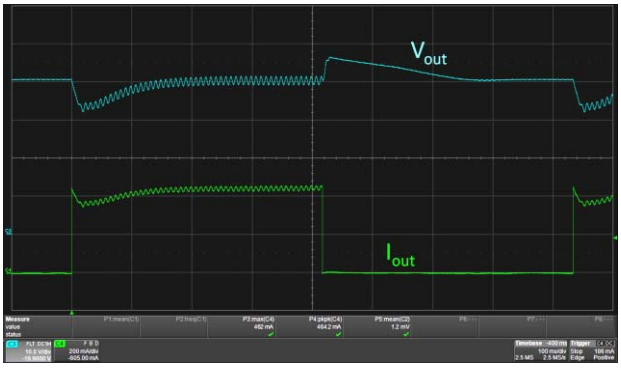


**Figure 6. Load Step for $f_c$ around 10 Hz**

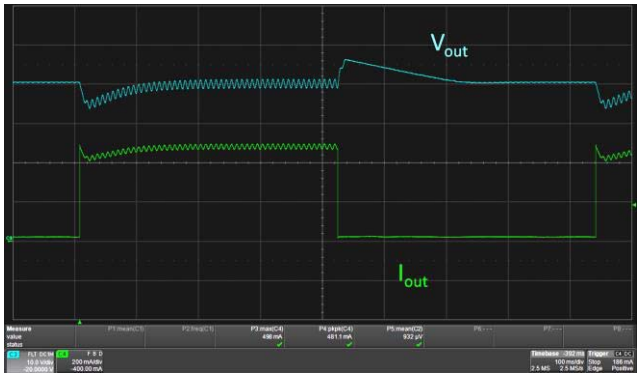


**Figure 7. Load Step for $f_c$ around 20 Hz**

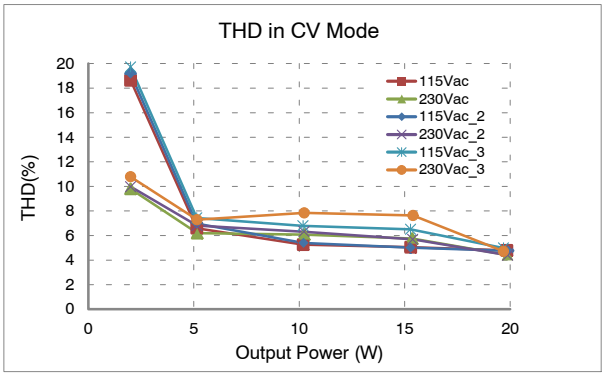


**Figure 8. THD in CV mode for $f_c$ = 8, 10 and 20 Hz**

Figure 8 plots the THD evolution with the output power in constant voltage mode for $f_c$ = 8 Hz (curves labeled 115 Vac and 230 Vac), for $f_c$ =10 Hz (115Vac_2 and 230Vac_2 curves) and for $f_c$ = 20 Hz (115Vac_3 and 230Vac_3 curves). For $f_c$ = 20 Hz, there is quite a lot of ripple on the COMP pin and this directly affects the current−sense voltage, resulting in more distortion. To avoid this, we could have set the compensator pole at a lower frequency (with $R_1$ = 150 kΩ and $C_2$ = 22 nF, the pole is at 48 Hz) but this would have decreased the phase margin.

As a conclusion for the compensation part, it is important to calculate properly the COMP pin elements according to the application. The validity of the compensator can be tested by doing transient load step.

## $V_{CC}$ CAPACITOR

The NCL30386/88 includes a high voltage start−up circuitry that derives current from the input line to charge the $V_{CC}$ capacitor. When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the $V_{CC}$ capacitor. When the voltage on this $V_{CC}$ capacitor reaches the $V_{CC(on)}$ level, the current source turns off, reducing the amount of power being dissipated. At this time, the controller is only supplied by the $V_{CC}$ capacitor, and the auxiliary supply should take over before $V_{CC}$ collapses below $V_{CC(off)}$. The $V_{CC}$ capacitor is calculated to provide the energy for the controller until the auxiliary winding voltage is high enough to supply the controller. If we call $t_{reg}$ the time needed by the converter to build a high enough voltage:

$$C_{Vcc} = \frac{(I_{CC2} + Q_g F_{sw}) t_{reg}}{V_{CC(on)} + V_{CC(of)}} \quad \text{(eq. 25)}$$

Where:

- $I_{CC2}$ is the controller consumption (see datasheet: 2.9 mA)
- $Q_g$ is the MOSFET total gate charge (22 nC)
- $F_{sw}$ is the switching frequency in maximum load, minimum input voltage

Now, we need to estimate $t_{reg}$. If LEDs are placed at the converter output, all the output current charges the output capacitor until the output voltage reaches the LED string forward voltage.

$$t_{reg} = \frac{C_{out} V_{out\_start}}{I_{out}} = \frac{C_{out} \times \frac{N_{sp}}{N_{ap}} \times V_{aux\_start}}{I_{out}} \quad \text{(eq. 26)}$$

Choose $V_{out\_start}$ high enough to have sufficient voltage on the aux. winding to bias the controller. Practically, targeting an auxiliary winding voltage around 15 V gives enough margins to properly bias the controller.

$$C_{Vcc} = \frac{(I_{CC2} + Q_g F_{sw}) t_{reg}}{V_{CC(on)} - V_{CC(off)}} = \frac{(2.9m + 22n \times 65k) \times 40m}{18 - 8.6} = 18.4\ \mu F \quad \text{(eq. 27)}$$

A 22−μF capacitor should be used.

### Total Startup Time

The high voltage start−up circuit features two start−up current levels, $I_{HV(start1)}$ and $I_{HV(start2)}$. At power−up, as long as $V_{CC}$ is below $V_{CC(TH)}$ (2 V typ.), the source delivers $I_{HV(start1)}$ (around 300 μA typical). The total start−up duration is:

$$t_{startup} = C_{Vcc}\left(\frac{V_{CC(TH)}}{I_{HV(start)}} + \frac{V_{CC(on)} - V_{CC(TH)}}{I_{HV(start2)}}\right) + t_{reg} \quad \text{(eq. 28)}$$

For our design, with a 22−μF capacitor, we should reach a start−up time of 226 ms.

$$t_{startup} = 22\ \mu\left(\frac{2}{300\ \mu} + \frac{18 - 2}{6\ m}\right) + 0.04 = 226\ ms \quad \text{(eq. 29)}$$

## DIMMING WITH THE NCL30386

The NCL30386 features 2 dimming pins for an improved dimming control: ADIM and PDIM pin.

### Dimming with ADIM

The ADIM pin receives an analog signal varying from $V_{ADIM100}$ to $V_{ADIM(MIN)}$ and translate this signal to vary the reference voltage for constant current regulation from 100 %$V_{REF}$ to 0% $V_{REF}$ or 0.5% $V_{REF}$ if the dimming clamp is activated. The NCL30386 features an option to select the dimming curve shape:

- For linear dimming, select L option
- For square dimming, select S option

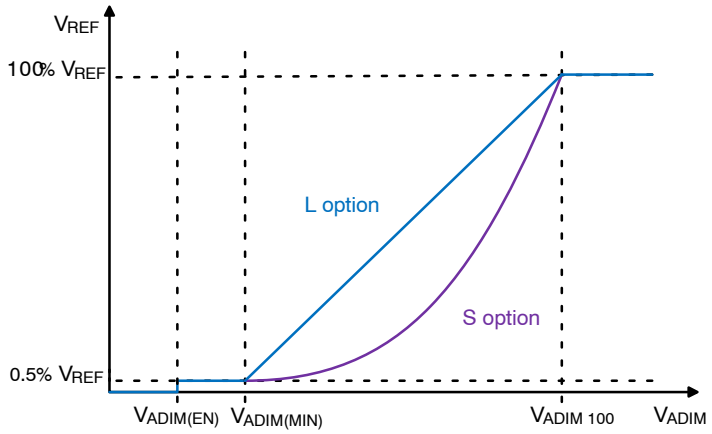


**Figure 9. NCL30386 Dimming Curves Options**

The following figures shows the output current of the 20−W board when a triangular dimming signal varying from 3.5 V to 0.6 V is applied to ADIM pin.

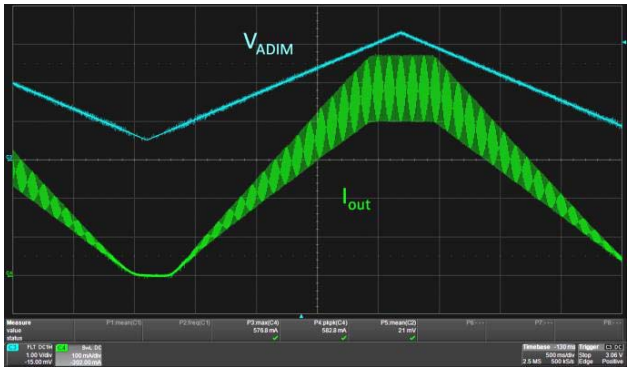


**Figure 10. Output Current with Linear Dimming**

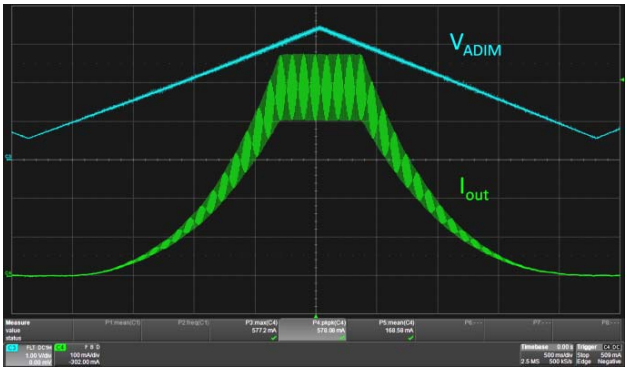


**Figure 11. Output Current with Square Dimming**

### Dimming with PDIM

The PDIM pin receives a pulse width modulated (PWM) signal and measures its duty ratio. The duty ratio is then directly applied as the output current setpoint. For example, if the duty ratio of the PWM signal is 10%, then we have $V_{REFX}$ = 10% $V_{REF}$. More precisely, the controller extracts the duty cycle by measuring the current inside PDIM pin which is directly the opto coupler collector current.

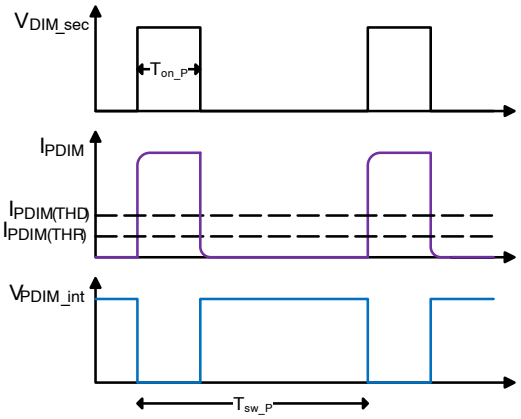


**Figure 12. PDIM Signals**

Figure 12 shows the signal applied on the optocoupler LED in black, the current in PDIM in purple and the internal dimming signal $V_{PDIM\_int}$. Practically, the internal dimming signal is inverted, with respect to the signal applied on the optocoupler LED, so the controller actually measures the off−time of the PWM signal. The internal $V_{REFX}$ setpoint is:

$$V_{REFX} = 1 - \frac{T_{on\_P}}{T_{sw\_P}} \quad \text{(eq. 30)}$$

### $R_{LED}$ Setting

For a correct detection of the rising edge and falling edge of the PWM dimming signal, the current drawn out of PDIM must be above $I_{PDIM(THD)}$. Given that the optocoupler current transfer ratio drops with temperature and aging, it is better to set the collector current high, such that at 25°C ambient temperature, the collector current is near the current capability limit of PDIM. PDIM pin feature a cascode circuit for connecting the optocoupler transistor. Its current capability is typically 600 μA.

If we set 500 μA as the target collector current at 25°C, we can calculate $R_{LED}$ with:

$$R_{LED} = CTR \times \frac{V_{DIM\_sec} - V_{opto\_LED}}{I_{opto\_C}} \quad \text{(eq. 31)}$$

At startup, if the PDIM pin is left open, the controller delivers 100% of $I_{out}$. If the pin is pulled down or if the low state of the PWM signal is less than 10 μs, the controller is disabled.

Please note that for the PDIM pin, the output current is varied in an analog way even if the dimming signal is digital.

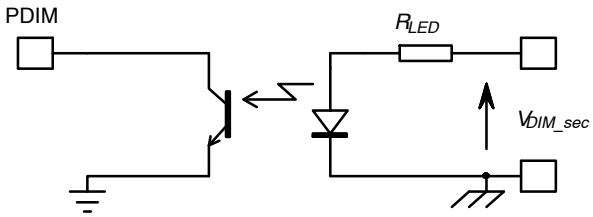


**Figure 13. Optocoupler on PDIM PIN**

- $I_{opto\_C}$ is the target collector current at 25°C: $I_{opto\_C}$ = 500 μA
- $V_{opto\_LED}$ is the forward drop voltage of the optocoupler LED: $V_{opto\_LED}$ ≈ 0.9 to 1 V
- CTR is the current transfer ratio of the optocoupler

### PDIM Pin Capacitor / Resistor

As the controller reads the optocoupler collector current through PDIM pin, adding a capacitor on this pin will divert a part of the optocoupler current. Thus, it is recommended to keep the capacitor on PDIM pin small (if the power supply designer really wants to use one). The PDIM capacitor must not exceed 100 pF.

In the same way, adding an *RC* filter on PDIM pin will delay the rising and falling edge detection of the dimming signal, resulting in a less−precise dimming setpoint, particularly at low dimming.

Thus, if a *RC* filter must be used on this pin, it is recommended to keep its time constant small (less than 1 μs).

## DYNAMIC SELF SUPPLY

As an option, the controller features a Dynamic Self Supply to keep the controller alive during dimming. Indeed, during dimming the forward voltage of the LED drops as the output current decreases; thus, the output voltage becomes very low and the auxiliary winding cannot supply the controller anymore. In this case, when $V_{CC}$ voltage reaches $V_{CC(off)}$, the controller turns on the HV current source to supply the controller. The HV current source stays on until $V_{CC}$ reaches $V_{CC(on2)}$ which is around 10.5 V. Figure 14 shows $V_{CC}$ waveforms when the DSS is activated. For this picture, the output current was dimmed at 1% ($I_{out}$ was around 4 mA).

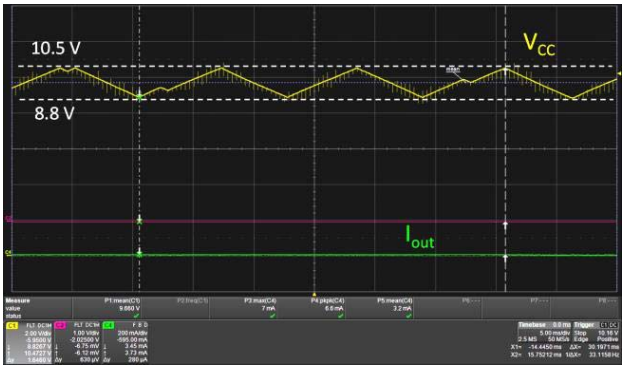


**Figure 14. DSS at Works during Dimming**

## PROTECTIONS

### Fast Over Voltage Protection

If ZCD voltage exceeds 130% of $V_{REF(CV)}$ (2.5 V) for 4 consecutive switching cycles (slow OVP not triggered) or for 2 switching cycles if the slow OVP has already been triggered, the controller detects a fault and shuts down. The controller initiates a new startup sequence after waiting for 4 seconds.

Figure 15 shows the fast OVP at work in the 20−W LED driver board. In order to trigger the fast OVP, the dummy load $R_{21}$ at the board output is removed at time $t_1$. The slow OVP is first triggered and the controller reduces its switching period around 1.4 ms. The output voltage continues increasing until the fast OVP triggers at $t_2$: $V_{out}$ = 58 V. The controller stops switching during 4 s and $V_{CC}$ hiccups. At $t_3$, the controller restarts switching ($V_{out}$ = 57.4 V). The output voltage increases and the fast OVP is triggered again at $t_4$.

For this design, when the fast OVP is triggered, the output voltage varies between 58 V and 57.4 V.

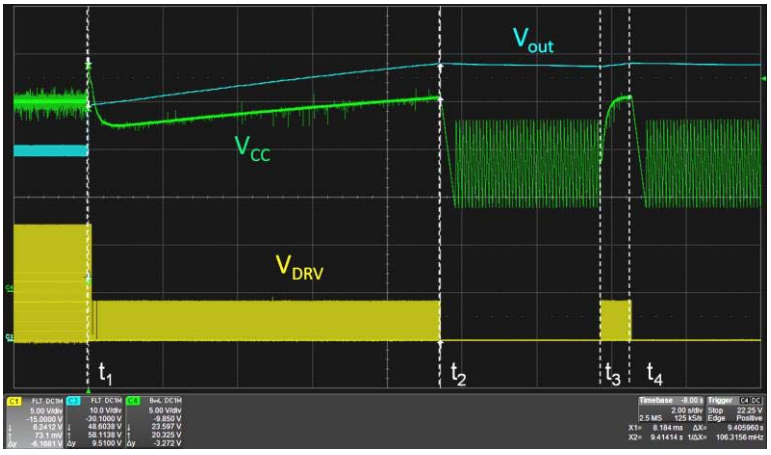


**Figure 15. Fast OVP at Works**

### Output Short Circuit Protection

Figure 16 illustrates the behavior of the short circuit protection (SCP). At $t_1$, the output is shorted. As a result, $V_{ZCD}$ < 1 V and the short circuit timer start counting. After 90 ms at $t_2$, the controller stops switching and $V_{CC}$ hiccups. When the 4−s auto−recovery timer elapses, the controller restarts switching at $t_3$.

If the output is shorted at startup, there is not enough reflected voltage on the auxiliary winding to keep the controller switching operating before the SCP triggers. In this case, the SCP timer is not reset when $V_{CC} < V_{CC(off)}$. The SCP timer keeps counting during the $V_{CC}$ hiccups and when it finally reaches 90 ms, the controller shuts down during 4 s. This behavior is illustrated by Figure 17 where the output of the 20−W converter is shorted prior to startup. We can see that the short−circuit protection is triggered after 5 bursts cycles, when the SCP timer has counted the equivalent of 90 ms of switching cycles with $V_{ZCD}$ below 1 V.

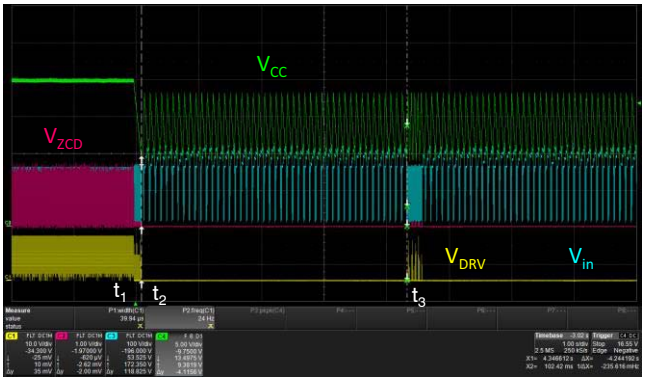


**Figure 16. Output Short Circuit Protection**

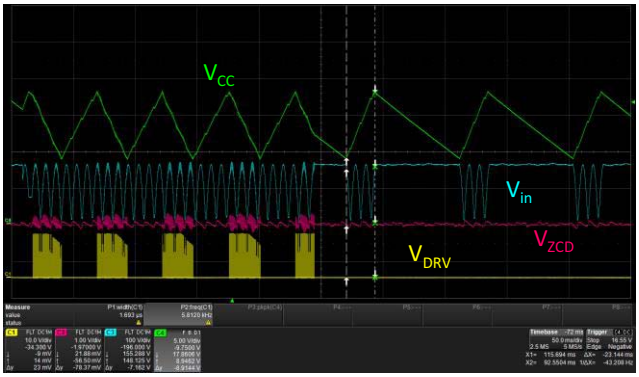


**Figure 17. Output Short before Startup**

### Output Diode Short protection

The LED driver stops operating as soon as $V_{CS}$ exceeds $V_{CS(stop)}$ (140% of maximum peak current limit) during 4 consecutives DRV pulses. The NCL30386/88 tries to resume operation when the 4−s auto−recovery delay is elapsed.

This is illustrated by Figure 17 where the output diode of the LED driver has been shorted.

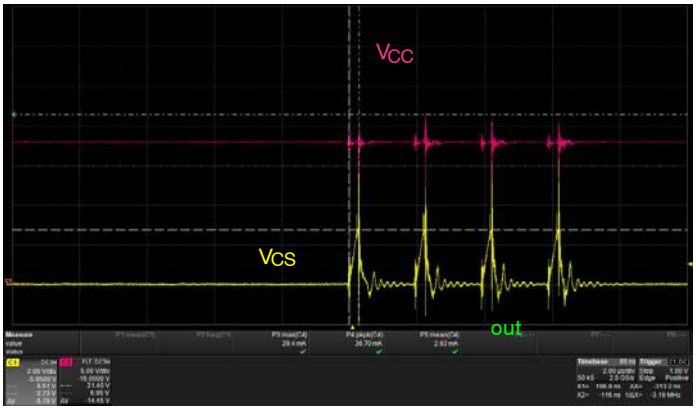


**Figure 18. The Winding or Output Diode Short Circuit Protection Triggers as soon as 4 Consecutive Faulty DRV Pulses are Detected**

### $V_{CC}$ OVP

When the voltage on $V_{CC}$ pin exceeds 26.5 V, the controller stops operating during 4 s. The controller re−starts switching after the 4−s timer has elapsed if $V_{CC}$ is below the OVP threshold. This behavior is illustrated by figure 19. The $V_{CC}$ pin voltage was increased to 27 V at $t_1$ with an external power supply. The external bias is removed at $t_2$. The controller restarts switching after the 4−s auto−recovery timer has elapsed at $t_3$.

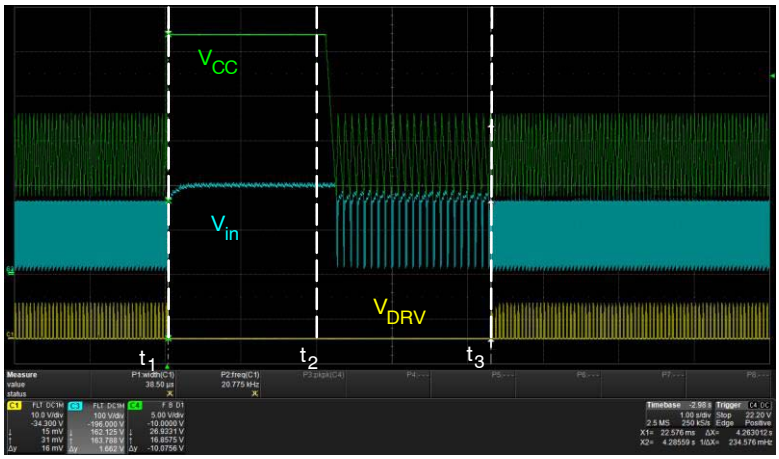


**Figure 19. $V_{CC}$ over Voltage Protection**

## CONCLUSION

This application note has shown the steps to design a LED driver controlled by the NCL30386 and the NCL30388.

This new family of controllers provides a very good regulation of the output current / voltage from the primary side of a flyback controller while maintaining a good power factor with low total harmonic distortion. For more information about the performances of these controllers, refer to [3] and [4].

## ANNEXE I

The power stage transfer function when the converter operates in the 1st valley is:

$$H_{PS}(s) = \frac{1}{3}\frac{N_{auxp}}{N_{sp}} k_{CV} \frac{1}{D2} \frac{H_0}{K_{v2}+1} \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1-\frac{s}{\omega_{z3}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \quad \text{(eq. 32)}$$

- $k_{CV}$ is the gain of the COMP pin voltage to the internal $V_{REFX}$ conversion: $k_{CV} = 0.3027$
- $D_2$ is the demagnetization duty−cycle:

$$D_2 = \frac{t_{demag}}{T_{sw}} \quad \text{(eq. 33)}$$

For 1st valley operation, if we neglect the valley duration, $D_2$ can be approximated with:

$$D_2 \approx \frac{N_{sp}V_{inLL}}{V_O + N_{sp}V_{inLL}} \quad \text{(eq. 34)}$$

Where:

- $V_O$ is the output voltage of the converter in CV mode plus the secondary rectifier forward voltage drop:

$$V_O = V_{out} + V_f \quad \text{(eq. 35)}$$

- $V_{inLL}$ is the low line rms voltage for calculating the transfer function of the power stage:

We recommend to select $V_{inLL}$ = 115 V rms

- $H_0$ is a constant:

$$H_0 = \frac{R_{load}V_{inLL}(V_O + N_{sp}V_{inLL})}{2R_{sense}(V_O + N_{sp}V_{inLL})^2 + V_{inLL}V_{CS}R_{load}} \quad \text{(eq. 36)}$$

$V_{CS}$ (the current−sense voltage at maximum output load) can be calculated with:

$$V_{CS} = V_{REF}\left(\frac{V_O + N_{sp}V_{inLL}}{N_{sp}V_{inLL}}\right) \quad \text{(eq. 37)}$$

NOTE: equation 37 is valid only if the valley duration is small with respect to the on−time plus the demagnetization time.

- $K_{v2}$ is a constant:

$$K_{v2} = H_0 \frac{V_{CS}}{D_2} \frac{N_{sp}}{V_O{}^2\left(\frac{N_{sp}}{V_O}+\frac{1}{V_{in}}\right)} \left[\frac{N_{sp}}{R_{sense}V_O\left(\frac{N_{sp}}{V_O}+\frac{1}{V_{in}}\right)} - 1\right] \quad \text{(eq. 38)}$$

- $\omega_{z1}$ is a zero formed by the output capacitor ESR and the output capacitance:

$$\omega_{z1} = \frac{1}{r_C C_{out}} \quad \text{(eq. 39)}$$

– $r_C$ is the ESR of the output capacitor $C_{out}$.

- $\omega_{z2}$ is a zero introduced by the CC/CV control algorithm
- $\omega_{z3}$ is a the right−half−plane zero of the flyback converter in discontinuous conduction mode:

$$\omega_{z3} = \frac{2R_{sense}V_{inLL}}{L_p V_{CS}} \quad \text{(eq. 40)}$$

- $\omega_{p1}$ is the low frequency pole of the power stage needed to calculate the compensation network:

$$\omega_{p1} = \frac{1}{b_1} \quad \text{(eq. 41)}$$

$$b_1 = \frac{1}{K_{v2} + 1}\left[\frac{1}{\omega_x} + \frac{40\ \mu s}{D_2} + \frac{K_{v2}}{\omega_{z1}} + 40\ \mu s\ (1 + K_{v2})\right] \quad \text{(eq. 42)}$$

$$\omega_x = \frac{1}{C_{out}\left[\frac{V_{CS}V_{inLL}R_{load}r_C + 2R_{sense}(V_O + N_{sp}V_{inLL})^2 \times (r_C + R_{load})}{V_{CS}V_{inLL}R_{load} + 2R_{sense}\ (V_O + N_{sp}V_{inLL})^2}\right]} \quad \text{(eq. 43)}$$

- $\omega_{p2}$ and $\omega_{p3}$ are the other poles of the power stage

**Design Example**

Calculate the low frequency pole value of the 20−W LED driver. First, start with $V_{CS}$:

$$V_{CS} = V_{REF}\left(\frac{V_O + N_{sp}V_{inLL}}{N_{sp}V_{inLL}}\right) = 0.333\ \frac{40.7 + 0.35 \times 115}{0.35 \times 115} = 0.67\ V \quad \text{(eq. 44)}$$

Calculate $D_2$:

$$D_2 \approx \frac{N_{sp}V_{inLL}}{V_O + N_{sp}V_{inLL}} = \frac{0.35 \times 115}{40.7 + 0.35 \times 115} = 0.497 \quad \text{(eq. 45)}$$

Calculate $H_0$:

$$H_0 = \frac{R_{load}V_{inLL}(V_O + N_{sp}V_{inLL})}{2R_{sense}(V_O + N_{sp}V_{inLL})^2 + V_{inLL}V_{CS}R_{load}} \quad \text{(eq. 46)}$$

$$= \frac{80 \times 115\ (40.7 + 0.35 \times 115)}{2 \times 0.9\ (40.7 + 0.35 \times 115)^2 + 115 \times 0.67 \times 80} = 41.47$$

Calculate $K_{v2}$:

$$K_{v2} = H_0\ \frac{V_{CS}}{D_2}\ \frac{N_{sp}}{V_O{}^2\left(\frac{N_{sp}}{V_O} + \frac{1}{V_{inLL}}\right)}\left[\frac{N_{sp}}{R_{sense}V_O\left(\frac{N_{sp}}{V_O} + \frac{1}{V_{inLL}}\right)} - 1\right] \quad \text{(eq. 47)}$$

$$= 41.47\ \frac{0.67}{0.497}\ \frac{0.35}{40.7^2\left(\frac{0.57}{40.7} + \frac{1}{115}\right)}\left[\frac{0.35}{0.9 \times 40.7\left(\frac{0.57}{40.7} + \frac{1}{115}\right)} - 1\right] = -0.343$$

Calculate $\omega_x$:

$$\omega_x = \frac{1}{C_{out}\left[\frac{V_{CS}V_{inLL}R_{load}r_C + 2R_{sense}(V_O + N_{sp}V_{inLL})^2 \times (r_C + R_{load})}{V_{CS}V_{inLL}R_{load} + 2R_{sense}\ (V_O + N_{sp}V_{inLL})^2}\right]} \quad \text{(eq. 48)}$$

$$= \frac{1}{660\ \mu\left[\frac{0.67 \times 115 \times 80 \times 20\ m + 2 \times 0.9(40.7 + 0.35 \times 115)^2 \times (20\ m + 80)}{0.67 \times 115 \times 80 + 2 \times 0.9\ (40.7 + 0.35 \times 115)^2}\right]} = 28.82\ rad.s^{-1}$$

Finally, we can calculate $\omega_{p1}$ and deduce the frequency to place the compensator zero:

$$\omega_{p1} = \frac{1}{\frac{1}{K_{v2}+1}\left[\frac{1}{\omega_x} + \frac{40\ \mu s}{D_2} + \frac{K_{v2}}{\omega_{z1}} + 40\ \mu s\ (1 + K_{v2})\right]} \quad \text{(eq. 49)}$$

$$= \frac{1}{\frac{1}{-0.343+1}\left[\frac{1}{28.82} + \frac{40\ \mu s}{0.497} + \frac{-0.343}{75.76\ k} + 40\ \mu s\ (1 - 0.343)\right]} = 18.87\ rad.s^{-1}$$

$$f_{zC} = f_{p1} = \frac{\omega_{p1}}{2\pi} = \frac{18.87}{2\pi} = 3\ Hz \quad \text{(eq. 50)}$$

## References

[1] NCL30386 Datasheet, NCL30388 Datasheet, http://www.onsemi.com/
[2] AND9200, 4 Key Steps to Design a NCL30088−Controlled LED Driver, Joel Turchi, http://www.onsemi.com/pub/Collateral/AND9200−D.PDF
[3] AND9715, Performance of a LED driver controlled by the NCL30386/88, Stéphanie Cannenterre
[4] EVBUMXXXX, 60W LED driver



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