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Key Steps to Design an Interleaved PFC Stage Driven by the NCP1632

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APPLICATION NOTE

Interleaved PFC is an efficient solution which is particularly popular in applications where a strict form factor has to be met like for instance, in slim notebook adapters or in LCD TVs. Interleaving consists of two paralleled “small” stages in lieu of a bigger single one, which may be more difficult to design. Practically, two 150−W PFC stages are combined to form a 300−W PFC pre−regulator. This approach offers several merits like the ease of implementation, the use of more but smaller components, a drastic reduction of the input and bulk rms currents or a better heat distribution [1].

This paper provides the main equations that are useful to design an interleaved PFC stage driven by the NCP1632. The process is illustrated by the following 300−W, universal mains application:

- Maximum Output Power: 300 W
- Input Voltage Range: from 90 V rms to 265 V rms
- Regulation Output Voltage: 390 V

AND8407/D [2] details the design procedure of an interleaved PFC stage controlled by the NCP1631. The same process is valid for the NCP1632 apart from a few peculiarities. This application note will particularly focus on them. Note that if given equations provide a good starting point, bench validation remains necessary!

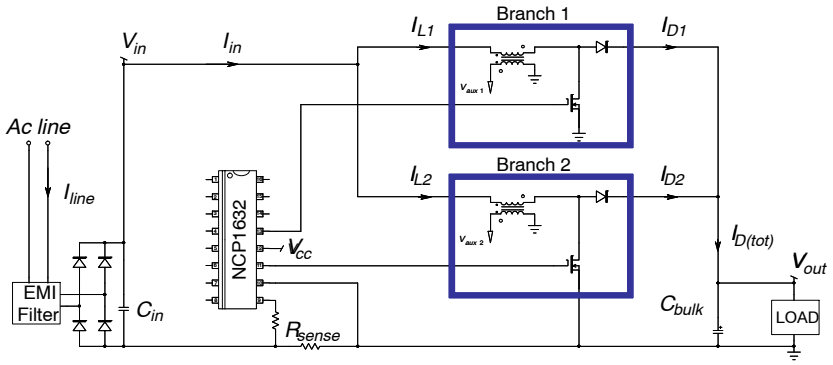


Figure 1. 2−Phase Interleaved PFC Stage

Introduction

As discussed in [3], the NCP1632 is derived from the NCP1631. It is worth noting that the NCP1632 has inherited the NCP1631 capability to limit the switching frequency range. Like the NCP1631, it is designed to operate in critical conduction mode (CrM) in heavy−load conditions and in discontinuous conduction mode (DCM) with frequency foldback in light load. This is to optimize efficiency over the whole power range. In no−load conditions, the two circuits further reduce operation losses by entering skip mode.

Note that the frequency−clamped mode of operation not only optimizes the efficiency but also provides a significant reduction of the boost inductors size. The switching frequency of pure CrM solutions becomes high as the load decays. It is then necessary to use high−value inductances for containing the medium− and light−load switching frequency to levels compatible with targeted efficiency ratios. By contrast, the frequency−clamped mode inherently forbids inefficient frequency levels. It lets you dimension the boost inductors for the only heavy load and as a result, authorizes the selection of smaller ones. As an example, the NCP1632 300−W evaluation board yields high−level performance with 165−μH boost inductors whereas a pure critical conduction mode solution would require about 250−μH to 350−μH ones.

In addition, the NCP1632 incorporates protection features for a rugged operation. More generally, the NCP1632 functions make it the ideal candidate in systems where cost−effectiveness, reliability, low stand−by power,

high−level efficiency over the load range and near−unity power factor are the key parameters:

- *Stable Phase Control between the two branches.*

Unlike master/slave controllers, the NCP1632 utilizes an interactive−phase approach where the two branches operate independently. More specifically, the two phases operate in ***F**requency−**C**lamped **Cr**itical conduction **M**ode* (**FCCrM**), preventing risks of undesired dead−times or continuous conduction mode sequences(1). In addition, the circuit makes them interact so that they run out−of−phase. The NCP1632 proprietary interleaving technique substantially maintains the wished 180° phase shift between the 2 branches, in all conditions, including start−up, fault or transient sequences.

1. The minimum switching period of a branch is the time interval between valley n and valley n+2 of the oscillator. The minimum switching period of the other branch is the time interval between valley n+1 and valley n+3 of the oscillator. See data sheet [1].

- *Optimized Efficiency Over The Full Power Range.*

The NCP1632 optimizes the efficiency of your PFC stage in the whole line/load range. Designed to operate in critical conduction mode at full load, the frequency can be clamped when the line current goes below a programmable level. In addition, the clamp frequency linearly decays as a function of the input current to maintain high efficiency levels even in very light load. The current threshold under which frequency reduces is programmed by the resistor placed between pin 6 and ground. To prevent any risk of regulation loss at no load, the circuit further skips cycles when the error amplifier reaches its low clamp level.

- *Fast Line / Load Transient Compensation.*

Characterized by the low bandwidth of their regulation loop, PFC stages exhibit large over− and under−shoots when abrupt load or line transients occur (e.g. at start−up). The NCP1632 dramatically narrows the output voltage range. First, the controller dedicates one pin to set an accurate Over−Voltage Protection level and interrupts the power delivery as long as the output voltage exceeds this threshold. Also, the NCP1632 ***dynamic response enhancer*** drastically speeds−up the regulation loop when the output voltage is 4.5% below its desired level. As a matter of fact, a PFC stage provides the downstream converter with a very narrow voltage range.

- *A "pfcOK" Signal.*

The circuit detects when the PFC stage is in steady state or if on the contrary, it is in a start−up or fault condition. In the first case, the "pfcOK" pin (pin15) is in high state and low otherwise. This signal is to disable the downstream converter until the bulk capacitor is charged and when the NCP1632 detects a major fault. Finally, the downstream converter can be optimally designed for the narrow voltage provided by the PFC stage in normal operation.

- *Safety Protections.*

The NCP1632 permanently monitors the input and output voltages, the input current and the die temperature to protect the system from possible over−stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:

- *Maximum Current Limit*: the circuit permanently senses the total input current and prevents it from exceeding the programmed current limit, still maintaining the out−of−phase operation.
- *In−rush detection*: the NCP1632 prevents the power switches from turning on in the presence of the large in−rush currents which typically take place when the power supply is plugged in.
- *Under−Voltage Protection*: this feature prevents operation in case of a failure in the OVP monitoring network (e.g., accidental grounding of the OVP pin).
- *Brown−Out Detection*: the circuit stops operating if the line magnitude is too low to protect the PFC stage from the excessive potentially−destructive stress occurring it in such conditions.
- *Thermal Shutdown*: the circuit stops pulsing when its junction temperature exceeds 140°C typically and resumes operation once it drops below about 90°C (50°C hysteresis).

DESIGN STEPS

Key Specifications

We must first identify the main specification points of the PFC stage:

- f_{line} : Line frequency. 50 Hz /60 Hz applications are targeted. Practically, they are often specified in a range of 47−63 Hz and for calculations such as hold−up time, one has to factor in the lowest specified value.
- $(V_{in,rms})_{LL}$: Lowest level of the line voltage. This is the minimum rms input voltage for which the PFC stage must operate nominally. Such a level is usually 10−12% below the minimum typical voltage which could be 100 V in many countries. We will take: $(V_{in,rms})_{LL} = 90\,V$.
- $(V_{in,rms})_{HL}$: Highest level for the line voltage. This is the maximum input rms voltage. It is usually 10% above the maximum typical voltage (240 V in many countries). We will use: $(V_{in,rms})_{HL} = 264\,V$.
- Brown−out line thresholds. The circuit prevents operation until the line rms voltage exceeds the upper

brown−out threshold $(V_{in,rms})_{boH}$ and stops operation when the line rms voltage goes below the lower brown−out threshold $(V_{in,rms})_{boL}$. The NCP1632 offers a programmable hysteresis. We will target:

- $(V_{in,rms})_{boH} = 90\% \cdot (V_{in,rms})_{LL} = 81V$
- $(V_{in,rms})_{boL} = 80\% \cdot (V_{in,rms})_{LL} = 72V$.

- $V_{out,nom}$: Nominal output voltage. This is the regulation level for the PFC output voltage (also designated as bulk voltage). $V_{out,nom}$ must be higher than $(\sqrt{2} \cdot (V_{line,rms})_{HL})$. 390 V is our target value.
- $(\Delta V_{out})_{pk-pk}$: Peak−to−peak output voltage ripple. This parameter is often specified in percentage of output voltage. It must be selected equal or lower than 8% to avoid triggering the Dynamic Response Enhancer (DRE) in normal operation.
- $t_{HOLD-UP}$: Hold−up time. This parameter specifies the amount of time the output will remain valid during a line drop−out event. One line cycle is typically specified. This requirement requires knowing the minimum voltage on the PFC stage output necessary for the proper operation in your application $(V_{out,min})$. No hold−up time will be considered here.
- P_{out} : Output power. This is the power consumed by the PFC load.
- $P_{out,max}$: Maximum output power. This is the maximum output power level, that is, 300 W in our application.
- $(P_{in,avg})_{max}$: Maximum input power. This is the maximum power that can be absorbed from the mains in normal operation. This level is obtained at full load, low line. The full−load efficiency of a NCP1632−driven interleaved PFC stage typically exceeds 95% over the line range. However, for margin considerations, we will assume an efficiency of 92% which leads to:

$$(P_{in,avg})_{max} = \frac{300}{92\%} \cong 325\,W$$

- $(I_{in,rms})_{max}$: Maximum value of the line rms current obtained at full load, low line.
- $(I_{in,rms})_{th}$: Line rms current threshold below which the circuit enters the frequency foldback mode (FFOLD) which forces a reduced frequency clamp to contain the switching losses. In our example, this threshold will be set to 25% of $(I_{in,rms})_{max}$ so that the PFC stage will enter the FFOLD mode:
  - At 25% of the load at the lowest line level $(V_{in,rms} = (V_{in,rms})_{LL})$
  - At 75% of the load at the highest line level $(V_{in,rms} = (V_{in,rms})_{HL})$

We can now compute the value of the components shown in the generic application schematic of Figure 2.

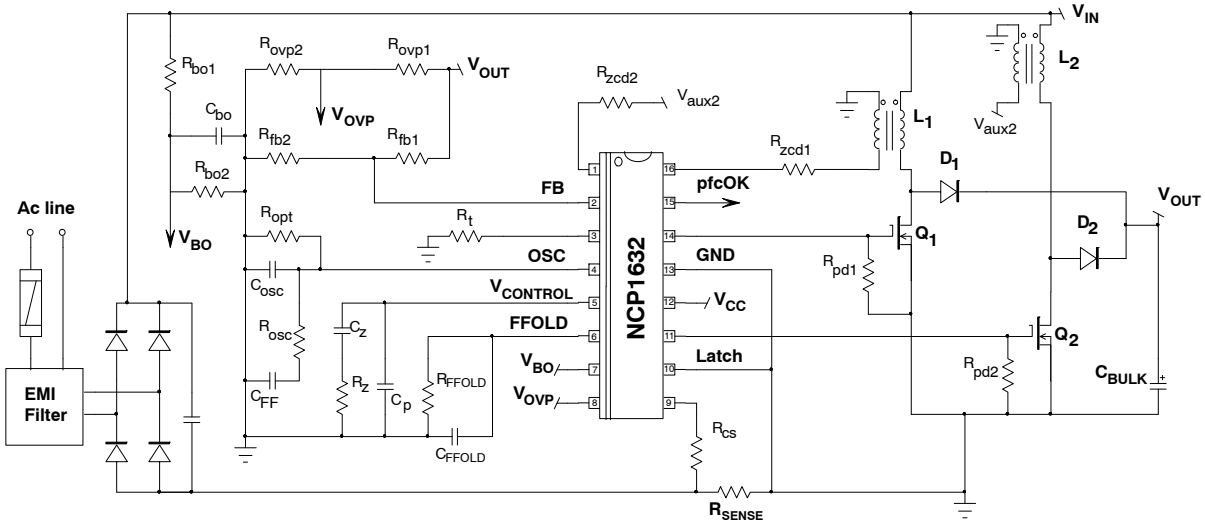


Figure 2. NCP1632 Generic Application Schematic

Power Components

- Inductor Selection

Assuming CrM operation at low line, full load, the (maximum) peak and rms inductor currents within one branch are:

$$\left(I_{L(pk)}\right)_{MAX} = \frac{2\sqrt{2}\cdot\left(\frac{\left(P_{in,avg}\right)_{max}}{2}\right)}{\left(V_{in(rms)}\right)_{LL}} = \frac{\sqrt{2}\cdot 325}{90} \cong 5.1A \quad \textit{(eq. 1)}$$

And:

$$\left(I_{L(rms)}\right)_{MAX} = \frac{\left(I_{L(pk)}\right)_{MAX}}{\sqrt{6}} \cong \frac{5.1}{\sqrt{6}} = 2.1A \quad \textit{(eq. 2)}$$

Where:

- $\left(V_{in,rms}\right)_{LL}$ is the lowest line rms voltage
- $\left(P_{in,avg}\right)_{max}$ is the maximum level of the input average power
- $V_{out,nom}$ is the nominal output voltage (regulation level)

In our application,

- $\left(V_{in,rms}\right)_{LL} = 90\,V$
- $V_{out,nom} = 390\,V$
- $\left(P_{in,avg}\right)_{max} = 325\,W$ (assuming a 92 % global efficiency which is a conservative value to offer a significant margin)

There is some flexibility in the inductors selection. In practice, the inductor value will set the switching frequency when in critical conduction mode operation. As the rule of the thumb, we can select L to limit this frequency to below 100 kHz in most severe conditions (top of the lowest−line sinusoid, full−load conditions). When f_{LLFL} is chosen, we can compute the inductor value as follows:

$$L \geq \frac{\left(V_{in,rms}\right)_{LL}^{2}\cdot\left(V_{out}-\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}\right)}{\left(P_{in,avg}\right)_{max}\cdot V_{out,nom}\cdot f_{LLFL}} \quad \textit{(eq. 3)}$$

In our application, this leads to:

$$L \geq \frac{90^2\cdot\left(390-\left(\sqrt{2}\cdot 90\right)\right)}{325\cdot 390\cdot 100\cdot 10^3} \cong 168\ \mu H \quad \textit{(eq. 4)}$$

Component 750316986 from Würth Elektronik (165 μH / 6 A pk / 2.5 A rms) was selected.

- Power Semiconductors

Diodes bridge

The diodes bridge is mainly selected based on the power it must dissipate, which is given by:

$$P_{bridge} = \frac{4\sqrt{2}}{\pi}\cdot V_f\cdot\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in(rms)}\right)_{LL}} \cong 1.8\cdot V_f\cdot\frac{325}{90} \cong 6.5\cdot V_f \quad \textit{(eq. 5)}$$

Assuming a 1−V forward voltage per diode $\left(V_f = 1V\right)$, the bridge approximately dissipates 6.5 W.

Boost diodes

Interleaved PFC requires two boost diodes (one per branch). No reverse recovery issues to worry about. Simply, they must meet the correct voltage rating ($V_{out(max)}$+margin) and exhibit a low forward voltage drop. Assuming a perfect current sharing, the average current of each individual diode is the half of the load one

$$\left(I_{D1(avg)} = I_{D2(avg)} = \frac{I_{D(tot)_{(avg)}}}{2} = \frac{I_{LOAD}}{2} = \frac{P_{out}}{2\cdot V_{out}} \cong 0.39\ A\right)$$

So, the losses are about $\left(\frac{I_{LOAD}\cdot V_f}{2}\right)$ per diode, i.e., less than 500 mW per diode using MUR550 rectifiers. For each phase, the peak current seen by the diode will be the same as the corresponding inductor peak current.

Two axial MUR550 are selected.

Power MOSFETs

The MOSFET of each branch is selected based on the peak voltage stress ($V_{out(max)}$+margin) and on the rms current flowing through it ($I_{Q(rms)}$):

$$I_{Q(rms)} = \frac{2}{\sqrt{3}}\cdot\frac{\left(\frac{\left(P_{in,avg}\right)_{max}}{2}\right)}{\left(V_{in(rms)}\right)_{LL}}\cdot\sqrt{1-\frac{8\cdot\sqrt{2}\cdot\left(V_{in(rms)}\right)_{LL}}{3\cdot\pi\cdot V_{out,nom}}} =$$

$$= \frac{325}{\sqrt{3}\cdot 90}\cdot\sqrt{1-\frac{8\cdot\sqrt{2}\cdot 90}{3\cdot\pi\cdot 390}} \cong 1.8\ A \quad \textit{(eq. 6)}$$

FCPF22N60 MOSFETs from ON Semiconductor are selected (1 per branch). They exhibit a maximum drain−to−source on−resistance ($r_{DS(on)}$) of 165 mΩ @ 25°C. Considering a 80% $r_{DS(on)}$ increase at high temperature, the maximum conduction losses are given by:

$$P_{cond} = I_{M(rms)}^{2}\cdot 180\%\cdot\left(r_{DS(on)}\right)_{25°C} =$$

$$= 1.8^2\cdot 1.8\cdot 0.165 \cong 1.0\ \ W \quad \textit{(eq. 7)}$$

This computation is valid for one branch. As there are two phases to consider, the total MOSFETs conduction losses are actually twice (2 W).

The MOSFETs switching losses are hard to predict. They highly depend on the diode choice, on the MOSFET drive speed and on the possible presence of some snubbering circuitry. Hence, their prediction is a tough and inaccurate exercise that will not be made in this paper. Instead, we will place the MOSFETs and the diodes bridge on the same heat−sink and consider that as a rule of the thumb, the total power to be dissipated by the heatsink is 5% of the output power [2].

Note that to further improve the efficiency, the MOSFET opening can be accelerated using the schematic of Figure 2, where $\boldsymbol{Q_1}$, a small pnp transistor, amplifies the MOSFET turn off gate current.

2. This is a conservative value which would mean that the PFC stage efficiency is less than 95%.

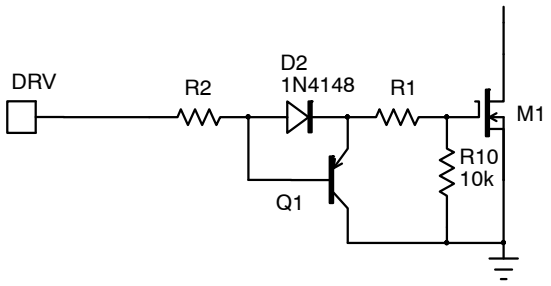


Figure 3. Q_1 Speeds Up the MOSFET Turn Off

Heatsink

The input bridge rectifying the line voltage and the MOSFETs of the two branches can share a common heat−sink. As discussed in the above lines, we can use 5% of P_{out} as a starting point for the power it must dissipate: $(5\% \cdot 300W \cong 15\ W)$. A 2.9°C/W heat−sink (ref. 437479 from AAVID THERMALLOY) is implemented. It limits the rise of the case temperature (of the input bridge and MOSFETs applied to it) to about 50°C compared to the ambient temperature.

- Bulk Capacitor Design

The output capacitor is generally designed considering 3 factors:

- The maximum permissible low−frequency ripple of the output voltage. The input current and voltage being both sinusoidal, PFC stages deliver a squared sinusoidal power that matches the load power demand in average only. As a consequence, the output voltage exhibits a low frequency ripple (e.g., 120 Hz in USA) that is inherent to the PFC function
- The rms current flowing through the bulk capacitor. Based on this computation, one must estimate the maximal permissible ESR for an adequate power dissipation.
- The hold−up time specification. The hold−up time is the time for which the power supply must keep providing the full power while the line is gone. The duration of the mains interruption (hold−up time) is generally in the range of 10 or 20 ms.

The output voltage ripple is given by:

$$\Delta V_{out(p-p)} = \frac{P_{out}}{2\pi \cdot f_{line} \cdot C_{bulk} \cdot V_{out,nom}} \qquad \textit{(eq. 8)}$$

The capacitor rms current is given by (assuming a resistive load):

$$I_{C(rms)} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot \left(V_{in(rms)}\right)_{LL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out,nom}}\right)^2} \qquad \textit{(eq. 9)}$$

Finally the following equation expresses the hold−up time:

$$t_{hold-up} = \frac{C_{bulk} \cdot \left(V_{out}{}^2 - V_{out(\min)}{}^2\right)}{2 \cdot P_{out}} \qquad \textit{(eq. 10)}$$

Where $\boldsymbol{V_{out(min)}}$ is the minimal bulk voltage necessary to the downstream converter to keep properly feeding the load.

The hold−time being not considered here, a 100−μF capacitor was chosen to satisfy the other above conditions. The peak−peak ripple is 25 V (±3% of $\boldsymbol{V_{out}}$) and the rms current is 1.4 A.

Brown−out Circuitry

The brown−out terminal (pin7) typically receives a portion of the PFC input voltage ($v_{in}(t)$). As during the PFC operation, $v_{in}(t)$ is a rectified sinusoid, a capacitor must integrate the ac line ripple so that a portion of the $v_{in}(t)$ average value is applied to the brown−out pin.

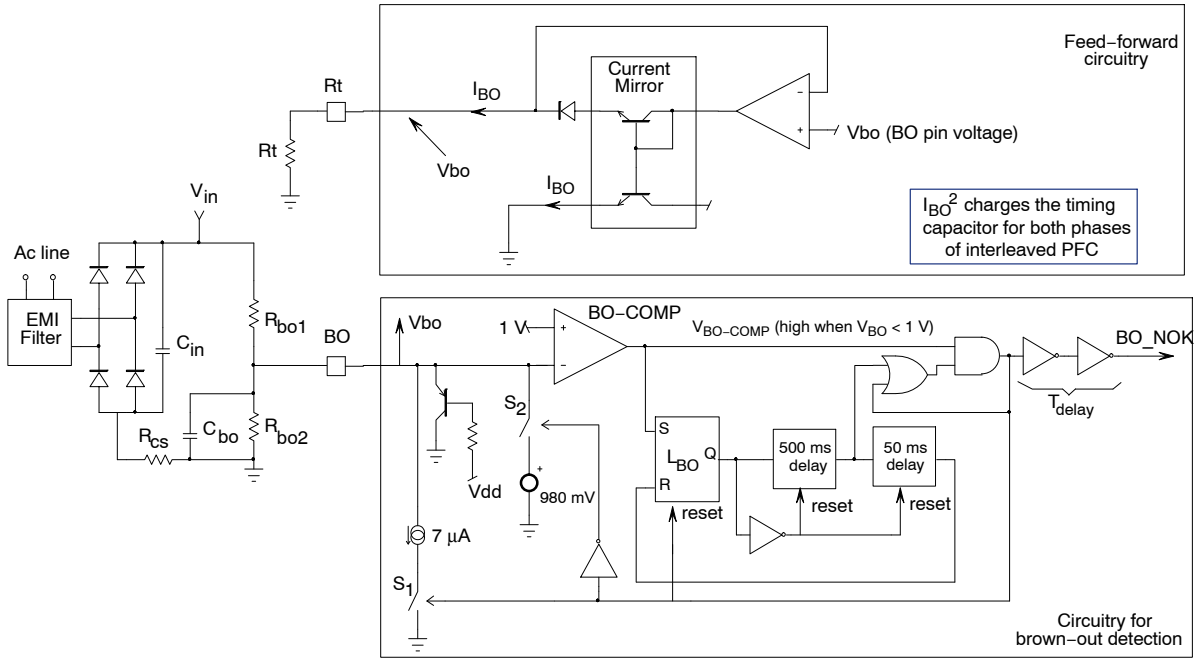


Figure 4. Brown−out Block

As sketched by Figure 4, the brown−out block performs two functions:

- Feed−forward: The brown−out pin voltage is buffered to generate an internal current I_{BO} proportional to the input voltage average value in conjunction with the pin3 resistor (R_t). This current is squared to form the current charging the internal timing capacitors which control the on−time in each individual branch. As a matter of fact, the on−time is inversely proportional to the square of the line magnitude. This feed−forward feature makes the transfer function and the power delivery independent of the ac line level.
- Detection of the line magnitude being too low. A 7−µA current source lowers the BO pin voltage when a brown−out condition is detected, for hysteresis purpose as required by this function. In traditional applications, the sensed voltage dramatically varies depending on the PFC stage state:
  - Before operation, the PFC stage is off and the input bridge acts as a peak detector (refer to Figure 5). As a consequence, the input voltage is approximately flat and nearly equates the ac line amplitude: $v_{in}(t) = \sqrt{2} \cdot V_{in,rms}$, where $V_{in,rms}$ is the rms voltage of the line. Hence, the voltage applied to pin7 is: $V_{pin7} = \sqrt{2} \cdot V_{in,rms} \cdot \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$.
  - After the PFC stage has started operation, the input voltage becomes a rectified sinusoid and the voltage applied to pin7 is: $V_{pin7} = \frac{2\sqrt{2}\, V_{in,rms}}{\pi} \frac{R_{bo2}}{R_{bo1} + R_{bo2}}$, i.e., about 64% of the previous value.

Therefore, in traditional applications, the same line magnitude leads to a BO pin voltage which is 36% lower when the PFC is working. That is why a large hysteresis is required.

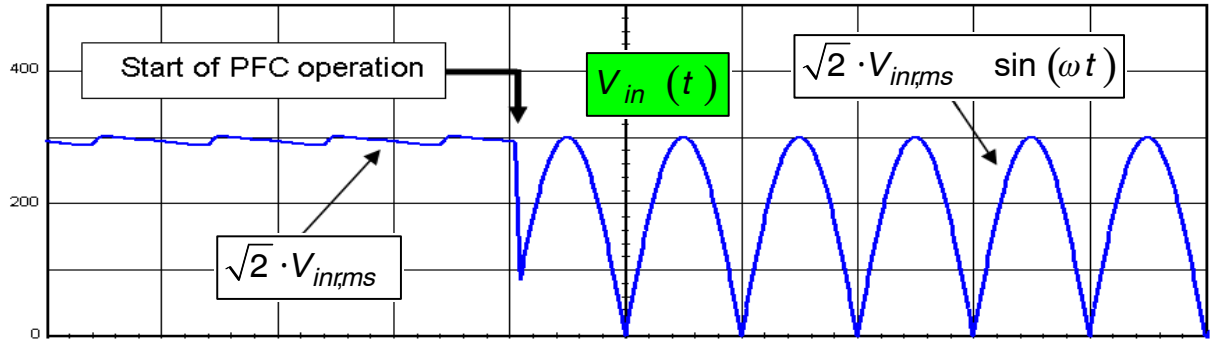


Figure 5. Typical Input Voltage of a PFC Stage

Computing C_{bo}, R_{bo1} and R_{bo2} of Figure 3:

1. Define the line levels at which the circuit should detect a brown−out and recover operation:

Our application being specified to operate from 90 V rms, it can make sense to select the following thresholds:

- The system starts operating when the line voltage is above $(V_{in,rms})_{boH} = 81V$ (90% of 90 V)
- The system detects a fault when the line voltage goes below $(V_{in,rms})_{boL} = 72V$ (80% of 90 V)

2. Define the average input voltage when V_{pin7} (BO pin voltage) crosses the BO thresholds (V_{pin7} rising and falling):

When the line voltage is below the BO threshold, the internal current source $(I_{HYST} = 7\ \mu A, typically)$ is activated to offer some hysteresis and the circuit recovers operation when:

$$\frac{R_{bo2}}{R_{bo1}+R_{bo2}} \cdot (V_{in,avg})_{boH} - \left(\frac{R_{bo1} \cdot R_{bo2}}{R_{bo1}+R_{bo2}} \cdot I_{HYST} \right) = V_{bo(th)} \quad \textit{(eq. 11)}$$

Where $(V_{in,avg})_{boH}$ is the average input voltage above which the circuit turns on and $V_{bo(th)}$ is the BO internal threshold (1 V typically).

Hence:

$$(V_{in,avg})_{boH} = \left(\frac{R_{bo1}+R_{bo2}}{R_{bo2}} \cdot V_{bo(th)} \right) + (R_{bo1} \cdot I_{HYST}) \quad \textit{(eq. 12)}$$

As long as the line is above the BO threshold, the internal current source $(I_{HYST} = 7\ \mu A, typically)$ is off and the BO pin voltage is:

$$V_{pin7} = k_{BO} \cdot V_{in,avg} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}} \right) \quad \textit{(eq. 13)}$$

Where:

- $(V_{in,avg})$ is the average input voltage
- f_{line} is the line frequency
- f_{BO} is the sensing network pole frequency $\left(f_{BO} = \frac{R_{bo1}+R_{bo2}}{2\pi \cdot R_{bo1} \cdot R_{bo2} \cdot C_{bo}} \right)$
- k_{BO} is scale down factor of the BO sensing network $\left(k_{BO} = \frac{R_{bo2}}{R_{bo1}+R_{bo2}} \right)$.

The term $\left(1 - \frac{f_{BO}}{3 \cdot f_{line}} \right)$ of equation 13 enables to take into account the BO pin voltage ripple (first harmonic approximation).

A brown−out fault is detected when the BO pin voltage goes below $V_{bo(th)}$ (BO internal threshold which equates 1 V typically). Hence, the BO protection triggers when the average voltage goes below the $(V_{in,avg})_{boL}$ level expressed by the following equation:

$$(V_{in,avg})_{boL} = \frac{V_{BO(th)}}{k_{BO} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}} \right)} \quad \textit{(eq. 14)}$$

Where $(V_{in,avg})_{boL}$ is the average input voltage below which the circuit turns off, f_{BO} is the sensing network pole frequency $\left(f_{BO} = \frac{R_{bo1}+R_{bo2}}{2\pi \cdot R_{bo1} \cdot R_{bo2} \cdot C_{bo}} \right)$ and f_{line} is the line frequency.

3. Calculation

From eq. 14, we can deduce the following expression of the brown−out scale down factor:

$$K_{BO} = \frac{R_{bo2}}{R_{bo1}+R_{bo2}} = \frac{V_{BO(th)}}{(V_{in,avg})_{boL} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}} \right)} \quad \textit{(eq. 15)}$$

Substitution of equation 15 into equation 12 leads to:

$$(V_{in,avg})_{boH} = \left((V_{in,avg})_{boL} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}} \right) \right) + (R_{bo1} \cdot I_{HYST}) \quad \textit{(eq. 16)}$$

We can then deduce the following expression of R_{bo1}:

$$R_{bo1} = \frac{(V_{in,avg})_{boH} - \left((V_{in,avg})_{boL} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}} \right) \right)}{I_{HYST}} \quad \textit{(eq. 17)}$$

Based on this assumption, we can deduce R_{bo1} from eq. 15 :

$$R_{bo2} = \frac{R_{bo1}}{\left(\frac{(V_{in,avg})_{boL}}{V_{BO(th)}} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}} \right) \right) - 1} \quad \textit{(eq. 18)}$$

If as a rule of the thumb, we will assume that $\left(f_{BO} = \frac{f_{line}}{10} \right)$ that is 6 Hz in the case of a 60−Hz line, we obtain:

$$R_{bo1} = \frac{\left(V_{in,avg}\right)_{boH} - \left(\left(V_{in,avg}\right)_{boL} \cdot \left(1 - \frac{\frac{f_{line}}{10}}{3 \cdot f_{line}}\right)\right)}{I_{HYST}} \cong$$

$$\cong \frac{\left(V_{in,avg}\right)_{boH} - \left(0.967 \cdot \left(V_{in,avg}\right)_{boL}\right)}{I_{HYST}} \quad \textit{(eq. 19)}$$

$$R_{bo2} = \frac{R_{bo1}}{\left(\frac{\left(V_{in,avg}\right)_{boL}}{V_{BO(th)}} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)\right) - 1} \cong$$

$$\cong \frac{R_{bo1}}{\left(0.967 \cdot \frac{\left(V_{in,avg}\right)_{boL}}{V_{BO(th)}}\right) - 1} \quad \textit{(eq. 20)}$$

As an example, we will consider the traditional PFC stage where the average value of the input voltage is 36% lower when the circuit operates (as illustrated by Figure 4).

Let us assume that we need the system to:

- Start operating when the line voltage is above $\left(V_{in,rms}\right)_{boH} = 81V$
- Detect a fault when the line voltage goes below $\left(V_{in,rms}\right)_{boL} = 72V$

The corresponding average input voltage thresholds are:

$$\left(V_{in,avg}\right)_{boH} = \sqrt{2} \cdot \left(V_{in,rms}\right)_{boH} = \sqrt{2} \cdot 81 \quad \textit{(eq. 21)}$$

And:

$$\left(V_{in,avg}\right)_{boL} = \frac{2\sqrt{2}}{\pi} \cdot \left(V_{in,rms}\right)_{boL} = \frac{2\sqrt{2}}{\pi} \cdot 72 \quad \textit{(eq. 22)}$$

We have then to solve:

$$R_{bo1} \cong \frac{\left(\sqrt{2} \cdot 81\right) - \left(0.967 \cdot \frac{2\sqrt{2}}{\pi} \cdot 72\right)}{7 \cdot 10^{-6}} \cong 7410\ k\Omega \quad \textit{(eq. 23)}$$

$$R_{bo2} \cong \frac{7410 \cdot 10^3}{\left(0.967 \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot 72}{1}\right) - 1} \cong 120 k\Omega \quad \textit{(eq. 24)}$$

$$C_{bo} = \frac{R_{bo1} + R_{bo2}}{2\pi \cdot R_{bo1} \cdot R_{bo2} \cdot \frac{f_{line}}{10}} \cong$$

$$\cong \frac{7410k + 120k}{2\pi \cdot 7410k \cdot 120k \cdot \frac{60}{10}} \cong 225\ nF \quad \textit{(eq. 25)}$$

In practice, four 1.8−MΩ resistors are placed in series for $\boldsymbol{R_{bo1}}$ (for a global 7.2−MΩ resistor) and we use a 120−kΩ resistor for $\boldsymbol{R_{bo2}}$ and 220−nF capacitor for $\boldsymbol{C_{bo}}$.

One should note that the NCP1632 brown−out circuitry incorporates a 500−ms blanking delay to help meet hold−up times requirement (see data sheet).

Maximum Power Adjustment

The instantaneous line current is the averaged value (over the switching frequency) of the total current absorbed by the two branches of the PFC stage. It is given by the following formula:

$$i_{in}(t) = \frac{v_{in}(t)}{L} \cdot \frac{\left(R_t\right)^2 \cdot V_{REGUL}}{26.9 \cdot 10^{12} \cdot {k_{BO}}^2 \cdot {V_{in,rms}}^2} \quad \textit{(eq. 26)}$$

Where:

- $\left(\frac{\left(R_t\right)^2 \cdot V_{REGUL}}{26.9 \cdot 10^{12} \cdot {k_{BO}}^2 \cdot {V_{in,rms}}^2}\right)$ is the expression of the on−time in each branch
- (V_{REGUL}) is an internal signal linearly dependent of the output of the regulation block ($V_{CONTROL}$). (V_{REGUL}) varies between 0 and 1.66 V.
- $i_{in}(t)$ and $v_{in}(t)$ are the instantaneous line current and voltage respectively.
- $V_{in,rms}$ is the line rms voltage
- L is the boost inductor value
- k_{BO} is scale down factor of the BO sensing network $\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}}\right)$.

Multiplying $i_{in}(t)$ by $v_{in}(t)$, one can deduce the instantaneous power:

$$P_{in}(t) = \frac{\left(R_t\right)^2 \cdot V_{REGUL} \cdot {V_{in}}^2(t)}{26.9 \cdot 10^{12} \cdot L \cdot {k_{BO}}^2 \cdot {V_{in,rms}}^2} \quad \textit{(eq. 27)}$$

And averaging the instantaneous power over the line period gives the following expression of the mean input power:

$$P_{in,avg} = \frac{\left(R_t\right)^2 \cdot V_{REGUL}}{26.9 \cdot 10^{12} \cdot L \cdot {k_{BO}}^2} \quad \textit{(eq. 28)}$$

As a result of the feed−forward, the delivered power does not depend on the line magnitude. It is the only function of the inductor inductance, of the input voltage sensing network (used and dimensioned for the brown−out detection) and of the R_t capacitor, that is, the timing resistor that is applied to pin3.

Since V_{REGUL} is clamped to 1.66 V, the maximum power $\left((P_{in})_{HL}\right)$ that can be virtually delivered by the PFC stage is:

$$(P_{in})_{HL} = \frac{(R_t)^2 \cdot 1.66}{26.9 \cdot 10^{12} \cdot L \cdot {k_{BO}}^2} \cong \frac{(R_t)^2}{16.2 \cdot 10^{12} \cdot L \cdot {k_{BO}}^2} \quad \textit{(eq. 29)}$$

Hence:

$$R_t \cong 4025 \cdot 10^3 \cdot k_{BO} \cdot \sqrt{L \cdot (P_{in})_{HL}} \quad \textit{(eq. 30)}$$

For the sake of a welcome margin, $\left((P_{in})_{HL}\right)$ should be selected at least 25% higher than the expected maximal input power that is: $(125\% \cdot 325\ \text{W} \cong 400\ \text{W})$ in the application of interest.

In our case,

- L = 165 μH
- Since R_{bo1} = 7200 kΩ and R_{bo2} = 120 kΩ,

$$\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}} = \frac{1}{61}\right)$$

Hence:

$$R_t \cong 4025 \cdot 10^3 \cdot \frac{1}{61} \cdot \sqrt{165 \cdot 10^{-6} \cdot 400} \cong 17\ k\Omega \quad \textit{(eq. 31)}$$

An 18−kΩ resistor is selected that leads to

$$(P_{in})_{HL} = \frac{\left(18 \cdot 10^3\right)^2 \cdot 61^2}{16.2 \cdot 10^{12} \cdot 165 \cdot 10^{-6}} \cong 450\ W$$

Feedback Network

The NCP1632 embeds a transconductance error amplifier which typically features a 200−μS transconductance gain and a ±20 μA maximum capability (see Figure 5). The output voltage of the PFC stage is externally scaled down by a resistors divider and monitored by the feed−back input (pin2). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feedback network. The output of the error amplifier is pinned out for external loop compensation (pin5).

Computation of the feedback / regulation external components

A resistor divider consisting of R_{fb1} and R_{fb2} of Figure 5 must provide pin2 with a voltage proportional to the PFC output voltage so that V_{pin2} equates the internal reference voltage (V_{REF} = 2.5 V) when the PFC output voltage is nominal. In other words:

$$\frac{R_{fb2}}{R_{fb1} + R_{fb2}} \cdot V_{out,nom} = V_{REF} \quad \textit{(eq. 32)}$$

Or:

$$\frac{R_{fb1}}{R_{fb2}} = \frac{V_{out,nom}}{V_{REF}} - 1 \quad \textit{(eq. 33)}$$

Another constraint on the feed−back resistors relates to the power it dissipates. R_{fb1} and R_{fb2} being biased by the PFC output high voltage (in the range of 390 V typically), they can easily consume several hundreds of mW if their resistance is low. Targeting a bias current in the range of 100 μA generally gives a good trade−off between losses and noise immunity.

This criterion leads to:

$$R_{fb2} = \frac{V_{REF}}{100 \mu A} = 25\ k\Omega \quad \textit{(eq. 34)}$$

In practice, $(R_{fb2} = 27\ \text{k}\Omega)$ was selected for our application.

Following eq. 33, R_{fb1} is given by:

$$R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1\right) \quad \textit{(eq. 35)}$$

We target a 390−V regulation level, hence:

$$R_{fb1} = 27\ k\Omega \cdot \left(\frac{390}{2.5} - 1\right) = 4185\ k\Omega \quad \textit{(eq. 36)}$$

Like for the input voltage sensing network, several resistors should be placed in series instead of a single R_{fb1} resistor. In our application, we choose a (1800 kΩ + 1800 kΩ + 560 kΩ) network. This selection together with (R_{fb2} = 27 kΩ) leads to:

$$V_{out,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF} =$$

$$= \frac{1800k + 1800k + 560k + 27k}{27k} \cdot 2.5\,V \cong 388\,V \quad \textit{(eq. 37)}$$

Compensation:

The NCP1632 uses the brown−out input voltage to provide some feed−forward. This allows the small−signal transfer function of PFC stage to be independent from the ac line amplitude. More specifically, the bulk capacitor ESR being neglected, we have:

$$\frac{\hat{v}_{out}(s)}{\hat{v}_{REGUL}(s)} = \frac{(R_t)^2 \cdot R_{out}}{53.8 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2 \cdot V_{out,nom}} \cdot \frac{1}{1+\left(s \cdot \frac{R_{out} \cdot C_{bulk}}{2}\right)} \quad \text{(eq. 38)}$$

Where:

- C_{bulk} is the bulk capacitor.
- R_{out} is the load equivalent resistance.
- R_t is the pin3 external capacitor.
- L is the PFC inductor inductance.
- k_{BO} is the brown−out scale−down factor.
- $V_{out,nom}$ is the regulation level of the PFC output.

However, PFC stages must exhibit a very low regulation bandwidth, in the range of or lower than 20 Hz to yield high power factor ratios. Hence, the regulation loop cannot prevent sharp load/line changes from causing excessive over− or undershoots. The NCP1632 firmly contains the output voltage variations. First, it limits overshoots by the Over−Voltage Protection (see OVP section). In addition, a dynamic Response Enhancer (DRE) circuitry contains the undershoots: an internal comparator monitors the feedback (V_{pin2}) and when V_{pin2} is lower than 95.5% of its nominal value, it connects a 220−μA current source to speed−up the charge of the compensation capacitors. Finally, it is like if the comparator multiplied the error amplifier gain by about 10 [3].

The implementation of the dynamic response enhancer together with the accurate and programmable over−voltage protection, guarantees a small spread of the output voltage in all conditions included sharp line / load transients. These functions operate best when associated with a type−2 compensation scheme which is recommended for such an interleaved PFC stage. The type−2 compensation circuit requires the following external components: the resistor R_Z and the capacitors C_Z and C_P shown by Figure 5.

3. Note that DRE capability is 75% reduced until the PFC stage output voltage has reached its target level (that is when the "pfcOK" signal is high). This is to obtain a fast but smooth start operation (see [3])

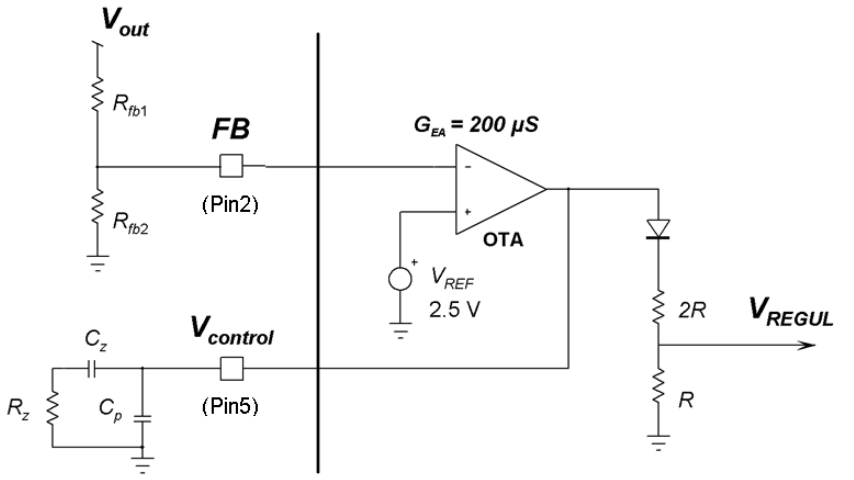


Figure 6. Regulation Trans−conductance Error Amplifier, Feedback and Compensation Network

The output−to−control transfer function of the type−2 compensator is:

$$\frac{\hat{v}_{control}(s)}{\hat{v}_{out}(s)} = \frac{1+sR_zC_z}{sR_o(C_z+C_p)\left(1+sR_z\frac{C_z \cdot C_p}{C_z+C_p}\right)} \quad \text{(eq. 39)}$$

Where $R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}$, G_{EA} being the gain of the trans−conductance error amplifier (OTA), $V_{out,nom}$, the output nominal voltage (V_{out} regulation level) and V_{REF}, the OTA 2.5−V voltage reference.

Actually, The NCP1632 PWM section does not directly use $V_{control}$ but V_{REGUL}. Taking into account the internal resistors divider which produces the ratio (5/9) linking $V_{control}$ and V_{REGUL}, it comes:

$$\frac{\hat{v}_{REGUL}(s)}{\hat{v}_{out}(s)} = \frac{1+sR_zC_z}{s\frac{9 \cdot R_o}{5} \cdot (C_z+C_p)\left(1+sR_z\frac{C_z \cdot C_p}{C_z+C_p}\right)} \quad \text{(eq. 40)}$$

Hence, we have:

$$\frac{\hat{v}_{REGUL}(s)}{\hat{v}_{out}(s)} = \frac{1+\frac{s}{2\pi \cdot f_z}}{\frac{s}{2\pi \cdot f_{p0}}\left(1+\frac{s}{2\pi \cdot f_{p1}}\right)} \quad \text{(eq. 41)}$$

Where:

- f_z is compensator zero frequency: $f_z = \frac{1}{2\pi \cdot R_z \cdot C_z}$
- f_{p1} is high−frequency pole position:

$$f_{p1} = \frac{1}{2\pi \cdot R_z \cdot \left(\frac{C_p \cdot C_z}{C_p + C_z}\right)}$$

- f_{p0} is the frequency of the 0−dB pole position:

$$f_{p0} = \frac{5}{18\pi \cdot R_0 \cdot (C_p + C_z)}$$

- $R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}$

Placing the zero and the high−frequency pole

We can obtain a 60° phase boost and hence, a 60° phase margin by setting the compensation zero at $\left(\frac{f_c}{4}\right)$ and the high frequency pole at $(4 \cdot f_c)$, where f_c is the selected crossover frequency.

From this, it comes that:

$$f_{p1} = 4^2 \cdot f_z \qquad \textit{(eq. 42)}$$

Substitution of the f_{p1} and f_z expressions into eq. 42 leads to:

$$\frac{C_p \cdot C_z}{C_p + C_z} = \frac{C_z}{16} \qquad \textit{(eq. 43)}$$

Hence:

$$C_z = 15 \cdot C_p \qquad \textit{(eq. 44)}$$

Placing the pole at the origin to obtain the proper bandwidth:

Eq. 38 instructs that the static gain of the PFC boost is:

$$G_o = \frac{(R_t)^2 \cdot R_{out}}{53.8 \cdot 10^{12} \cdot L \cdot {k_{BO}}^2 \cdot V_{out,nom}} \qquad \textit{(eq. 45)}$$

If f_c is the desired crossover frequency, the 0−dB pole (f_{p0}) must be placed to cancel the static gain at the load that would set the boost converter pole at the selected compensation zero. Hence:

$$-20 \cdot \log\left(\frac{f_c}{f_{p0}}\right) = -20 \cdot \log\left(G\left|_{\left(R_{out} = \frac{4}{\pi \cdot C_{bulk} \cdot f_c}\right)}\right.\right) \qquad \textit{(eq. 46)}$$

Or:

$$f_{p0} = \frac{f_c}{G_0\left|_{R_{out} = \frac{4}{\pi \cdot C_{bulk} \cdot f_c}}\right.} \qquad \textit{(eq. 47)}$$

This leads to:

$$f_{p0} = \frac{f_c}{\frac{4 \cdot {R_t}^2}{\pi \cdot 53.8 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot {k_{BO}}^2 \cdot f_c \cdot V_{out,nom}}} \qquad \textit{(eq. 48)}$$

This expression simplifies as follows:

$$f_{p0} = \frac{\pi \cdot 53.8 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot {k_{BO}}^2 \cdot {f_c}^2 \cdot V_{out,nom}}{4 \cdot {R_t}^2} \qquad \textit{(eq. 49)}$$

Where:

- k_{BO} is scale down factor of the BO sensing network $\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}}\right)$.

Replacing f_{p0} by its expression of eq. 49, it comes:

$$\frac{5}{18\pi \cdot R_0 \cdot (C_p + C_z)} = \frac{5}{18\pi \cdot \left(\frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}\right) \cdot (16 \cdot C_p)} =$$

$$= \frac{\pi \cdot 53.8 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot {k_{BO}}^2 \cdot {f_c}^2 \cdot V_{out,nom}}{4 \cdot {R_t}^2} \qquad \textit{(eq. 50)}$$

Replacing G_{EA} and V_{REF} by their typical value (200 μS and 2.5 V, respectively, we can write the following equation to calculate C_P:

$$C_p \cong \frac{V_{ref} \cdot G_{EA} \cdot {R_t}^2}{7646.2 \cdot 10^{12} \cdot L \cdot C_{bulk} \cdot {k_{BO}}^2 \cdot {f_c}^2 \cdot (V_{out,nom})^2} \qquad \textit{(eq. 51)}$$

Replacing R_t by this expression of eq. 30, the previous equation simplifies to:

$$C_p \cong \frac{1.06 \cdot 10^{-6} \cdot (P_{in})_{HL}}{C_{bulk} \cdot {f_c}^2 \cdot (V_{out,nom})^2} \qquad \textit{(eq. 52)}$$

ComputingR_z:

The compensation zero being placed at $\left(\frac{f_c}{4}\right)$, it comes:

$$f_z = \frac{1}{2\pi \cdot R_z \cdot C_z} = \frac{f_c}{4} \qquad \textit{(eq. 53)}$$

Finally, from the above computations, we can deduce the following equations to design the compensation network.

$$C_p \cong \frac{1.06 \cdot 10^{-6} \cdot (P_{in})_{HL}}{C_{bulk} \cdot {f_c}^2 \cdot (V_{out,nom})^2} \qquad \textit{(eq. 54)}$$

$$C_z = 15 \cdot C_p \qquad \textit{(eq. 55)}$$

$$R_z = \frac{2}{\pi \cdot C_z \cdot f_c} \qquad \textit{(eq. 56)}$$

In our application,

$$C_p = \frac{1.06 \cdot 10^{-6} \cdot 497}{100 \cdot 10^{-6} \cdot 20^2 \cdot 390^2} \cong 86\,nF \quad \textit{(eq. 57)}$$

Using eq. 44, we can then deduce C_Z :

$$C_z = 15 \cdot C_p = 1020\,nF \quad \textit{(eq. 58)}$$

In practice, a 1−μF standard capacitor is selected.

$$R_z = \frac{2}{\pi \cdot 1 \cdot 10^{-6} \cdot 20} \cong 31.8\,k\Omega \quad \textit{(eq. 59)}$$

A 33−kΩ resistor is implemented.

The compensation is computed to obtain a phase margin in the range of 60°. The high−frequency pole can be set at a lower frequency. Practically, C_p can be increased up to 4 times the proposed value (without changing $\boldsymbol{R_z}$ and $\boldsymbol{C_z}$) to reduce the ripple on the $\boldsymbol{V_{control}}$ pin and further improve the THD. The crossover frequency is unchanged. This is just at the cost of a diminution of the phase margin which can drop as low as 30°. More specifically:

$$\Phi_m = \arctan\left(\frac{f_c}{f_z}\right) - \arctan\left(\frac{f_c}{f_{p1}}\right) \quad \textit{(eq. 60)}$$

Where:

- f_z is the frequency of the compensator zero:

$$f_z = \frac{1}{2\pi \cdot R_z \cdot C_z}$$

- f_{p1} is the frequency of the compensator high−frequency pole:

$$f_{p1} = \frac{1}{2\pi \cdot R_z \cdot \left(\frac{C_p \cdot C_z}{C_p + C_z}\right)}$$

Finally, a 150−nF capacitor is selected for $\boldsymbol{C_p}$, leading to: $(f_z \cong 5\,Hz)$, $(f_{p1} \cong 37\,Hz)$, $\left(\Phi_m \cong 76^\circ - 28^\circ = 48^\circ\right)$

Over−Voltage Protection

The NCP1632 dedicates one specific pin for the under−voltage and over−voltage protections. It is thus possible to implement two separate feedback networks (see Figure 8 and Figure 9):

- One for regulation applied to pin 4 (feedback input).
- Another one for the OVP function.

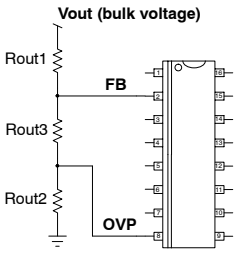


Figure 7. Configuration with One Feedback Network for Both OVP and Regulation

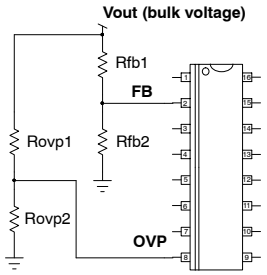


Figure 8. Configuration with Two Separate Feedback Networks

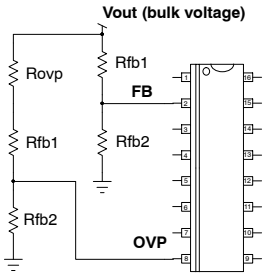


Figure 9. Another Configuration with Two Separate Feedback Networks

The double feedback configuration offers some redundancy and hence, an upgraded safety level as it protects the PFC stage even if one of the two feedback arrangements fails.

However, if desired, one single feedback arrangement can easily be implemented as portrayed by Figure 7. The regulation and OVP blocks having the same reference voltage (V_{REF} = 2.5 V), the resistance ratio R_{out2} over R_{out3} adjusts the OVP threshold. More specifically:

- The bulk regulation voltage is:

$$V_{out,nom} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2} + R_{out3}} \cdot V_{REF} \quad \textit{(eq. 61)}$$

- The (bulk) OVP level is:

$$V_{out,ovp} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2}} \cdot V_{REF} \quad \textit{(eq. 62)}$$

- The ratio OVP level over regulation level is:

$$\frac{V_{out,ovp}}{V_{out,nom}} = 1 + \frac{R_{out3}}{R_{out2}} \quad \textit{(eq. 63)}$$

For instance, $(R_{out3} = 5\% \cdot R_{out2})$ leads to $(V_{out,ovp} = 105\% \cdot V_{out,nom})$.

As soon and as long as the circuit detects that the output voltage exceeds the OVP level, the power switch is turned off to stop the power delivery.

In our application, the option that consists of two separate V_{out} sensing networks is chosen (configuration of Figure 7). Similarly, the impedance of the monitoring resistors must be:

- High enough for a reduced power dissipation. If excessive, the resistors static losses may prevent from complying with the standby requirements to be met by most power supplies
- Low enough for a good noise immunity

Again, a bias current in the range of 100 μA generally gives a good trade−off.

Hence:

$$R_{ovp2} = \frac{V_{ref}}{100\,\mu A} = 25\,k\Omega \qquad \textit{(eq. 64)}$$

In practice, $(R_{ovp2} = 27\ \text{k}\Omega)$ was selected and as a consequence:

$$R_{ovp1} = R_{ovp2} \cdot \left(\frac{V_{out,ovp}}{V_{REF}} - 1\right) \qquad \textit{(eq. 65)}$$

In our application, our 410−V target leads to:

$$R_{ovp1} = 27\,k\Omega \cdot \left(\frac{410}{2.5} - 1\right) = 4401\,k\Omega \qquad \textit{(eq. 66)}$$

For safety reason, several resistors should be placed in series instead of having a single R_{ovp1}. In our application, we choose the following combination: 1800 kΩ + 1800 kΩ + 820 kΩ.

The exact OVP level is then:

$$V_{out,ovp} = \frac{R_{ovp1} + R_{ovp2}}{R_{ovp2}} \cdot V_{REF} =$$

$$= \frac{1800k + 1800k + 820k + 27k}{27k} \cdot 2.5\,V \cong 412\,V \qquad \textit{(eq. 67)}$$

Remark:

As illustrated by Figure 9, another effective means to dimension the OVP sensing network is to select:

- $R_{ovp2} = R_{fb2}$
- $R_{ovp1} = R_{fb1} + R_{ovp}$, where R_{ovp} is a part of the upper resistor of the OVP sensing network.

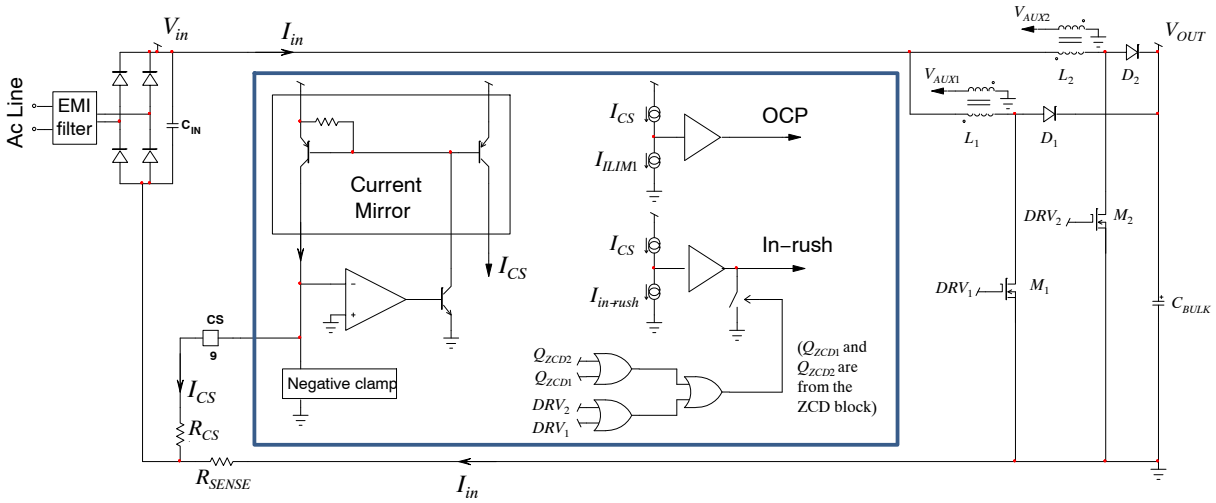
Note that:

- $V_{out,nom} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$
- $V_{out,ovp} = \frac{R_{ovp1} + R_{ovp2}}{R_{ovp2}} \cdot V_{REF} = \frac{R_{fb1} + R_{ovp} + R_{fb2}}{R_{fb2}} \cdot V_{REF}$

Combining the two previous equations, it comes: $V_{out,ovp} = V_{out,nom} + \frac{R_{ovp}}{R_{fb2}} \cdot V_{REF}$.

In other words, the OVP protection trips when the overshoot exceeds: $\left(\frac{R_{ovp}}{R_{fb2}} \cdot V_{REF}\right)$.

Current Sense Network



The CS block performs the over−current protection and detects the in−rush currents.

Figure 10. Current Sense Block

The NCP1632 is designed to monitor a negative voltage proportional to the inductor current. Practically, a current sense resistor (R_{SENSE} of Figure 10) is inserted in the return path to generate a negative voltage proportional to the total

current absorbed by the two branches. The circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage close to zero (refer to Figure 10). By inserting a resistor R_{CS} between the CS pin and R_{SENSE}, we adjust the pin9 current as follows:

$$-\left(R_{SENSE}\cdot i_{in}(t)\right)+\left(R_{CS}\cdot I_{pin9}\right)=V_{pin9}\cong 0 \qquad \text{(eq. 68)}$$

Where $i_{in}(t)$ is the total current drawn by the two phases of the interleaved PFC stage.

Finally, the current I_{CS} absorbed by pin9 is proportional to $i_{in}(t)$ as shown by the following equation:

$$I_{CS}=I_{pin9}=\frac{R_{SENSE}}{R_{CS}}i_{in}(t) \qquad \text{(eq. 69)}$$

The circuit compares I_{CS} to an internal 210−μA current reference (I_{ILIM1}) for a cycle−by−cycle current limitation. Hence, the maximum input current is (eq. 70):

$$I_{in,max}=\frac{R_{CS}}{R_{SENSE}}\cdot I_{ILIM1} \qquad \text{(eq. 70)}$$

Where I_{ILIM1} is the internal over−current threshold (210 μA typically)

Finally, we have two external components to set the current limit (R_{SENSE} and R_{CS}), the current sense resistor can be optimized to have the ***best trade−off between losses and noise immunity***.

Note that as detailed in the data sheet, in the event of an over−current, the circuit reduces the on−time in the two branches, proportionally to the difference between the sensed current and the over−current threshold $\left(I_{CS}-I_{ILIM1}\right)$.

- Maximum current drawn by the two branches:

As shown in [1], the following equations (71 & 72)give the total current that is absorbed by the interleaved PFC

$$I_{in,max}=2\sqrt{2}\cdot\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}}\cdot\left(1-\frac{V_{out,nom}}{4\cdot\left(V_{out,nom}-\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}\right)\right)}\right) \quad \text{if } \left(V_{in,rms}\right)_{LL}\le\frac{V_{out,nom}}{2\sqrt{2}} \qquad \text{(eq. 71)}$$

$$I_{in,max}=2\sqrt{2}\cdot\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}}\cdot\left(1-\frac{V_{out,nom}}{4\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}}\right) \quad \text{if } \left(V_{in,rms}\right)_{LL}\ge\frac{V_{out,nom}}{2\sqrt{2}} \qquad \text{(eq. 72)}$$

Where:

- $(V_{in,rms})_{LL}$ is the lowest level of the line rms voltage.
- $(P_{in,avg})_{max}$ is the maximum level of the input power.
- $V_{out,nom}$ is the nominal level of the output voltage (or the output regulation voltage)

In our case, $\left(\left(V_{in,rms}\right)_{LL}=90\le\frac{V_{out,nom}}{2\sqrt{2}}=\frac{390}{2\sqrt{2}}\cong 138\right)$.

Hence:

$$I_{in,max}=2\sqrt{2}\cdot\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}}\cdot\left(1-\frac{V_{out,nom}}{4\cdot\left(V_{out,nom}-\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}\right)\right)}\right) \qquad \text{(eq. 73)}$$

$$I_{in,max}=2\sqrt{2}\cdot\frac{325}{90}\cdot\left(1-\frac{390}{4\cdot\left(390-\left(\sqrt{2}\cdot 90\right)\right)}\right)\cong 6.4\ A \qquad \text{(eq. 74)}$$

- Selecting R_{SENSE} and R_{CS}:

If we neglect the input current ripple, the R_{SENSE} losses are given by the following simplified equation:

$$p_{R_{SENSE}}=R_{SENSE}\cdot\left(\frac{P_{in,avg}}{V_{in,rms}}\right)^2 \qquad \text{(eq. 75)}$$

One can choose R_{SENSE} as a function of its relative impact on the PFC stage efficiency at low line and full power. If α is the relative percentage of the power that can be consumed by R_{SENSE}, this criterion leads to:

$$\alpha\cdot\left(P_{in,avg}\right)_{max}=R_{SENSE}\cdot\left(\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{min}}\right)^2 \qquad \text{(eq. 76)}$$

Finally:

$$R_{SENSE}=\alpha\cdot\frac{\left(V_{in,rms}\right)_{min}^{2}}{\left(P_{in,avg}\right)_{max}} \qquad \text{(eq. 77)}$$

Generally (α = 0.2%) gives a good trade−off between losses and noise immunity (0.2% of the power is lost in the R_{CS} at low line). This criterion leads to the following R_{SENSE} value:

$$R_{SENSE} = 0.2\% \cdot \frac{90^2}{325} \cong 50\ m\Omega \quad \textit{(eq. 78)}$$

Reusing eq. 70, the above selection results in the following R_{CS} resistor:

$$R_{CS} = 50m \cdot \frac{6.4\ A}{210\ \mu A} \cong 1.5\ k\Omega \quad \textit{(eq. 79)}$$

We hence select R_{SENSE} = 50 mΩ and to offer some margin, R_{CS} = 1.8 kΩ. This selection sets the maximum input current to 7.6 A.

Note that a diode may be necessary across the current sense resistor in case of large inrush currents. See page 22 of [2].

Zero Current Detection (ZCD)

For each phase, a winding taken off of the boost inductor gives the zero current detection (ZCD) information. When the switch is on, the ZCD pin voltage is equal to:

$$V_{zcd} = -\frac{v_{in}(t)}{N} \quad \textit{(eq. 80)}$$

Where $v_{in}(t)$ is the instantaneous ac line voltage and N, the turns ratio (ratio number of turns of the primary winding over the number of turns of the ZCD auxiliary winding)

When the switch is off, the ZCD pin voltage is equal to:

$$V_{zcd} = \frac{V_{out} - v_{in}(t)}{N} \quad \textit{(eq. 81)}$$

The NCP1632 incorporates two ZCD comparators:

- A first one senses pin1 which is to receive the ZCD voltage from branch 2
- A second one monitors pin16 which is to receive the ZCD signal for branch 1.

The ZCD comparators have a 0.5−V threshold (rising, with a 250−mV hysteresis). The maximum value of this threshold is 0.6 V. Therefore, N must be sized such that at least 0.6 V is obtained on the ZCD pin during the demagnetization in all operating conditions. The voltage obtained on the ZCD pin is minimal in high line and at the top of the sinusoid, leading to:

$$N \le \frac{V_{out} - \left(\sqrt{2} \cdot (V_{in,rms})_{HL}\right)}{0.6} \quad \textit{(eq. 82)}$$

With $\left((V_{in,rms})_{HL} = 265\ V\right)$ and $(V_{out} = 390\ V)$, N must be lower than 25. A turns ratio of 10 was selected for this design.

A resistor, R_{ZCD1} is to be added between the phase−1 ZCD winding and pin 16 for branch 1 while another resistance R_{ZCD2} is installed between the phase−2 ZCD winding and pin1 for branch 2. R_{ZCD1} and R_{ZCD2} limit the current flowing into or out of pins 1 and 16. This current is preferably set in the range of 2 mA (sink and source). In general, the pins are the most stressed by the sink current obtained in high−line conditions. Hence, R_{ZCD1} and R_{ZCD2} must be selected high enough so that:

$$R_{ZCD1} = R_{ZCD2} \ge \frac{\sqrt{2} \cdot (V_{in,rms})_{HL}}{I_{ZCD} \cdot N} = \frac{\sqrt{2} \cdot 265}{2m \cdot 10} \cong 19\ k\Omega \quad \textit{(eq. 83)}$$

A 22−kΩ was selected.

However, the value of this resistor and the small parasitic capacitance of the ZCD pin also determine when the ZCD winding information is detected and the next drive pulse begins. Ideally, the ZCD resistor is selected so that the MOSFET closes on at the very moment when its drain−source voltage is minimal (valley turn on). Doing so, the switching losses are minimized. The value of $\boldsymbol{R_{ZCD1}}$ and $\boldsymbol{R_{ZCD2}}$ to accomplish this is best found experimentally. If necessary, a few tens of pF capacitance can be added on the ZCD pin. Too high a value could create a significant delay in detecting the ZCD event. In this case, the controller would operate in discontinuous conduction mode (DCM) and the power factor would suffer. Conversely, if the ZCD pin time constant is too low, then the next driver pulse would start when the MOSFET voltage is still high at a cost of higher switching noise and losses.

Frequency Foldback

The NCP1632 is designed to optimize the efficiency over the whole load range by operating:

- In pure critical conduction mode (CrM) without any frequency−clamp interaction when the line current magnitude is high. This corresponds to the NCP1632 High−frequency−clamp (HFC) mode in which the oscillator swing is minimized (1 V typically).
- In deep discontinuous conduction mode (deep DCM) when the line current magnitude is below a programmed level. Deep DCM means that the oscillator forces a minimum branch frequency which is low enough to ensure a significant dead−time and to prevent possibly noisy transitions between CrM and DCM within the input voltage sinusoid. This mode is obtained when the line current becoming less than the threshold set by the FFOLD pin, the circuit enters the Frequency foldback (FFOLD) mode. In addition, the circuit frequency clamp level is gradually reduced as a function of the line current magnitude in order to lower the switching losses as the power decays. At very low power, the frequency can decrease down to about 30 kHz depending on the OSC pin capacitor.

The transitions between the HFC and FFOLD modes and the frequency foldback characteristics are controlled by the FFOLD pin.

Managing the HFC to FFOLD transition

The NCP1632 FFOLD pin sources a current proportional to the input current (I_{CS}). This current is changed into a dc

voltage by means of an external *R//C* network connected to the FFOLD pin. The obtained V_{FFOLD} voltage is hence proportional to the line average current. As illustrated by Figure 11, the PFC stage enters the frequency foldback mode (FFOLD mode) when V_{FFOLD} goes below 3.0 V, and recovers high−frequency clamp mode (HFC mode) when the FFOLD voltage exceeds 4 V.

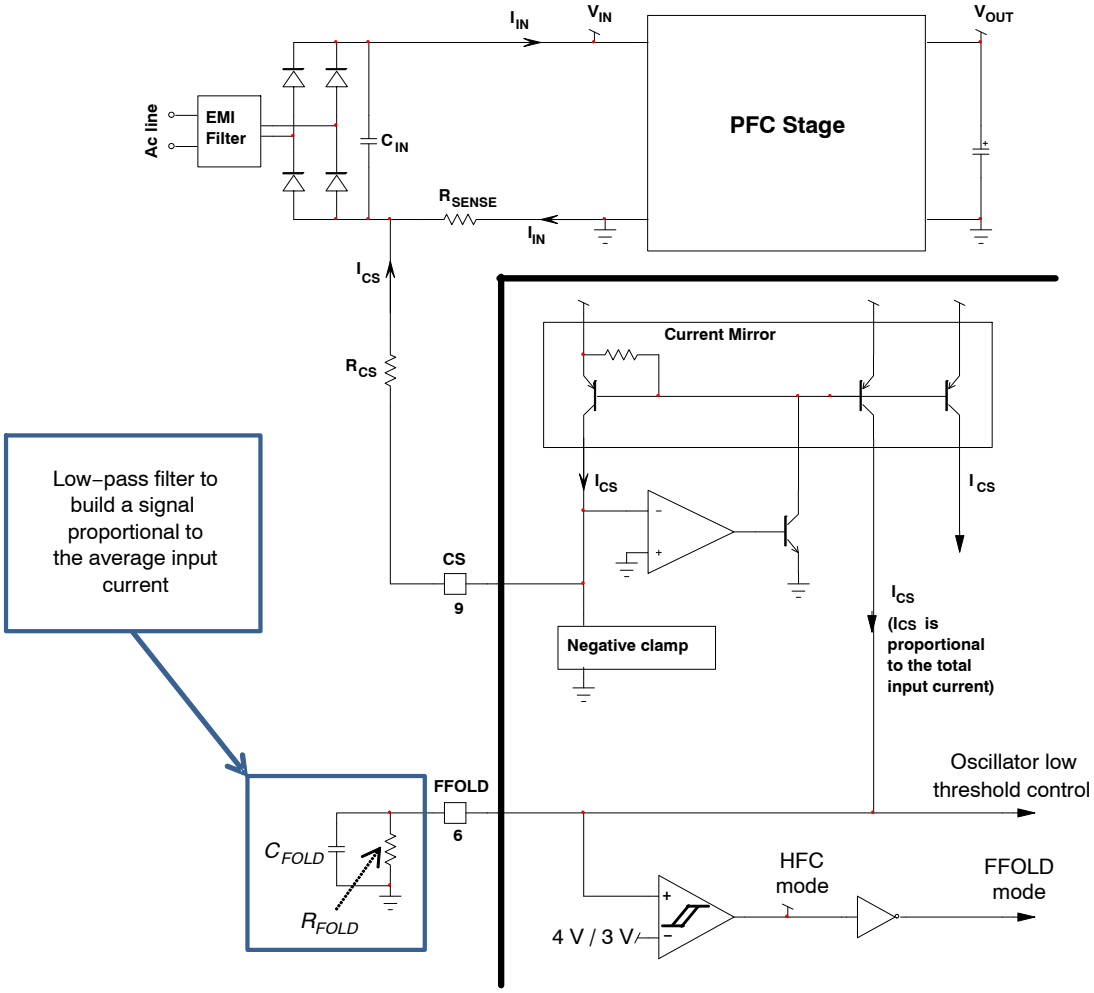


Figure 11. Frequency Foldback Control

In HFC mode, the oscillator lower threshold (V_{OSCL}) is fixed and equal to $V_{OSC(low)}$ (4 V typically).

In FFOLD mode, V_{OSCL} is modulated by the FFOLD pin voltage as follows:

- $V_{OSCL} = V_{FFOLD}$ if V_{FFOLD} is between 1 and 3 V
- V_{OSCL} = 1 V if V_{FFOLD} is below 1 V
- V_{OSCL} = 3 V if V_{FFOLD} exceeds 3 V

Speed−up HFC recovery in case of an abrupt load increase

Note that the FFOLD pin is heavily filtered, which causes long V_{FFOLD} settling phases. If while in very light−load conditions, the load abruptly rises, the FFOLD pin time constant may dramatically delay the HFC−mode recovery. During this delay, the PFC stage may not be able to provide the full power because of the DCM operation caused by the FFOLD mode. To solve this, the NCP1632 forces HFC operation whenever the DRE comparator trips [4] and remains in HFC mode until the output voltage recovers its regulation level. At that moment, the conduction mode is normally selected as a function of the FFOLD pin voltage.

4. The dynamic response enhancer (DRE) comparator trips when the output voltage drops below 95.5% of its regulation level.

FFOLD to HFC line magnitude threshold:

The FFOLD pin sources a current proportional to the input current:

$$I_{FFOLD} = I_{CS} = i_{in}(t) \cdot \frac{R_{SENSE}}{R_{CS}} \qquad \text{(eq. 84)}$$

Where:

- R_{SENSE} is the current sense resistor (see Figure 11)
- R_{CS} is the resistor placed between the CS pin and R_{SENSE} (see Figure 11)

Hence, considering that $i_{in}(t)$ is a rectified sinusoid, the FFOLD average voltage is:

$$V_{FFOLD} = \frac{R_{FFOLD} \cdot R_{SENSE}}{R_{CS}} \cdot \left\langle i_{in}(t) \right\rangle_{T_{line}} = \frac{2\sqrt{2}}{\pi} \cdot \frac{R_{FFOLD} \cdot R_{SENSE}}{R_{CS}} \cdot I_{in,rms} \quad \textit{(eq. 85)}$$

Where R_{FFOLD} is the resistor applied to the FFOLD pin (see Figure 11).

Due to the FFOLD low−frequency ripple (at twice the line frequency), we can consider that the transition between the HFC and FFOLD modes, will nearly occur when V_{FFOLD} is in between the 3−V and 4−V thresholds, that is, $(V_{FFOLD})_{th}$=3.5 V:

$$\left(I_{in,\mathrm{rms}}\right)_{th} = \left(I_{line,\mathrm{rms}}\right)_{th} \cong \frac{\pi}{2\sqrt{2}} \cdot \frac{\left(V_{FFOLD}\right)_{th} \cdot R_{CS}}{R_{FFOLD} \cdot R_{SENSE}} \cong$$

$$\cong 3.9 \cdot \frac{R_{CS}}{R_{FFOLD} \cdot R_{SENSE}} \quad \textit{(eq. 86)}$$

In our application, we have selected R_{FFOLD} =150 kΩ.

Since R_{CS} =1.8 kΩ and R_{SENSE} = 50 mΩ (see current sense section), the line rms current threshold is set to 0.94 A. This will lead the system to transition at about 110 W at 115 V rms and 220 W at 230 V rms.

The hysteresis is modulated by the capacitor which filters the FFOLD pin (C_{FFOLD} of Figure 11). A good trade−off generally consists of selecting C_{FFOLD} so that the FFOLD pin is in the range of 4 times the line frequency:

$$C_{FFOLD} \cong \frac{4}{R_{FFOLD} \cdot f_{line}} \cong \frac{4}{150 \cdot 10^3 \cdot 60} = 444\ nF \quad \textit{(eq. 87)}$$

We have selected 470 nF.

Oscillator

As detailed in [3], the NCP1632 is designed to be used with a 2−slope oscillator, built using either option 1 or option 2 of Figure 12 in which:

- C_{OSC} (which value is much less than the second capacitance C_{FF}) sets the highest possible frequency operation necessary for operating in CrM (high frequency clamp)
- R_{OSC} limits the influence of the C_{FF} capacitor as long as the oscillator swing remains below ($2.R_{OSC}.I_{OSC}$) where I_{OSC} is the charge or discharge current depending on the sequence. The voltage across C_{OSC} being limited by R_{OSC} (to about 1 V with R_{OSC} = 5.1 kΩ), the second much−higher−value capacitor (C_{FF}) is engaged when heavy−load CrM operation imposes a larger oscillator swing.
- C_{FF} is also the major contributor in adjusting the frequency in light load (when the frequency foldback mode forces deep DCM operation). As previously mentioned, C_{FF} also ensures that the oscillator voltage can stay above 1 V in deep CrM conditions.

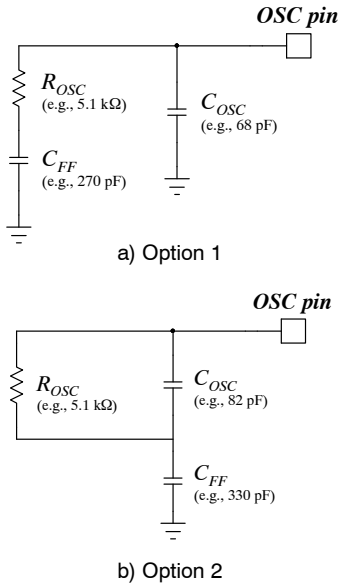
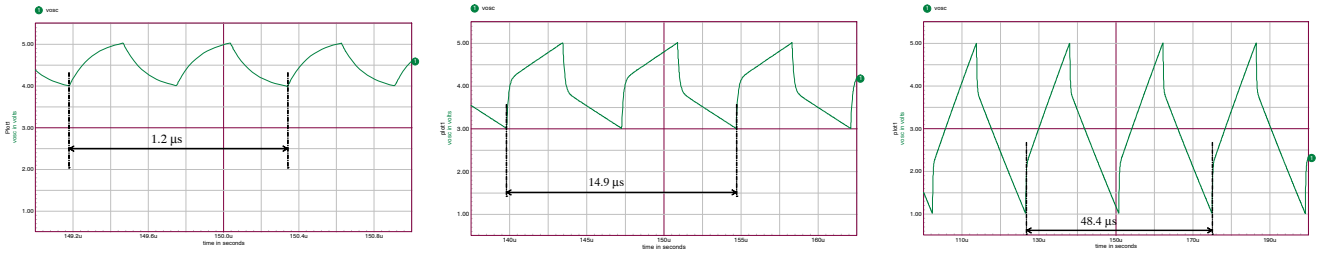


Figure 12. 2−Slope Oscillator

In the rest of the document, only option 1 will be considered with the following default values:

- C_{OSC} = 22 pF and R_{OSC} = 5.1 kΩ to set the clamp frequency at a high level (about 1 MHz) so that CrM operation is obtained in heavy load conditions
- C_{FF} = 470 pF to set the clamping frequency to about 70 kHz when entering the FFOLD mode and adjust the standby frequency to about 22 kHz.

Using this default configuration (C_{OSC} = 22 pF, C_{FF} = 470 pF and R_{OSC} = 5.1 kΩ), we obtain with the Figure 13 characteristics:



833−kHz frequency clamp in HFC mode (V_{FFOLD} > 4 V)

67−kHz frequency clamp when entering FFOLD mode (V_{FFOLD} = 3 V)

21−kHz minimum frequency clamp (deepest DCM @ V_{FFOLD} = 1 V)

Figure 13. Clamp Frequency in Each Individual Branch with the Configuration of Figure 12 a)

Analytically computing the frequency of a 2−slope oscillator frequency as a function of the FFOLD pin voltage is not an easy task. A quick simulation or the iterative process implemented in the Excel spreadsheet (see [4]) should be used instead. In particular, [4] provides the branch frequency when the circuit enters the FFOLD mode and the minimum branch frequency in standby $(V_{FFOLD} \leq 1\,V)$. It also computes the maximum power which can be delivered without exceeding the oscillator range. See the following section.

Oscillator maximum range

Figure 14 shows the oscillator typical waveforms in critical conduction mode. For the sake of simplicity, it is considered that only a capacitor is connected to the OSC pin. In the left side (Figure 14 a), the oscillator is symmetrical. We can see that the discharge phases are prolonged until the demagnetization phase is completed. The same is shown in Figure 14 b) but in the case where the oscillator is asymmetrical. Both waveform types are possible and the system is stable in the two cases.

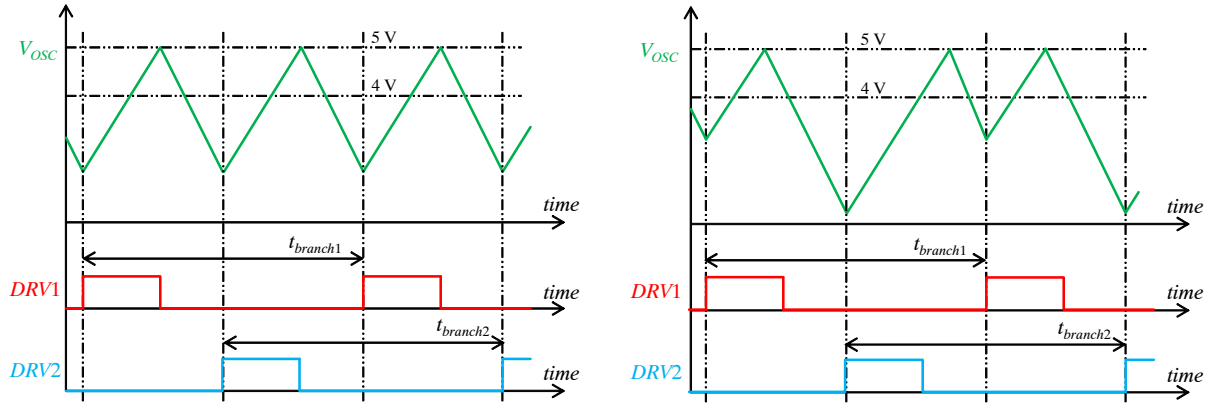


Figure 14. Oscillator Waveform (1−Slope Case)

Now, the circuit needs a minimum OSC pin voltage to properly discharge the oscillator voltage. If not, the discharge slope is no longer linear as shown by Figure 15. In this case, the phase control between the two branches can be affected.

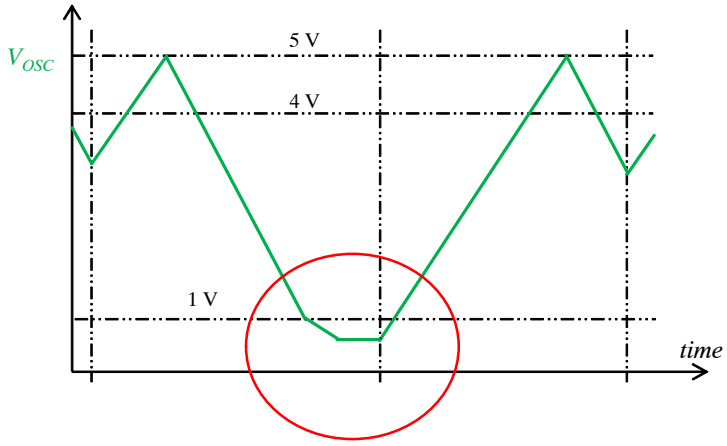


Figure 15. Exceeded Oscillator Range

It is thus important to get sure that the oscillator range is not exceeded in the worst case. The worst case is sketched by Figure 16 where only one discharge phase over two is prolonged to match the current cycle duration.

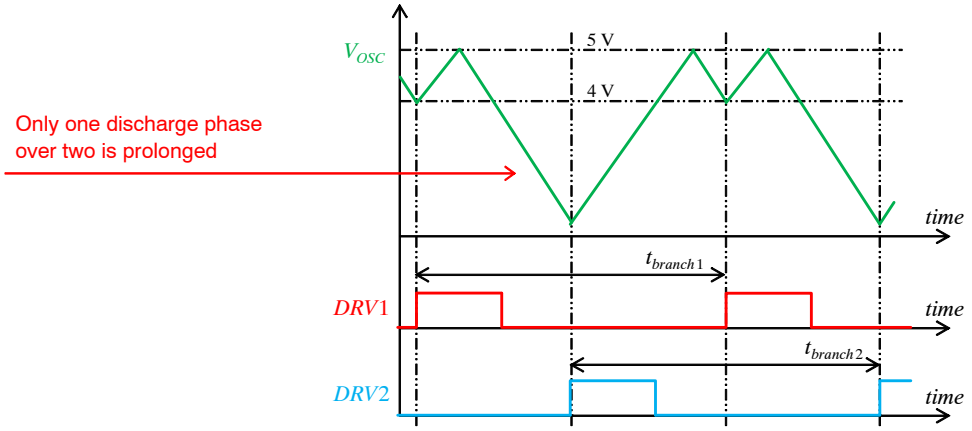


Figure 16. Possible Most Asymmetrical Waveform of the Oscillator

Light−load minimum frequency

The switching frequency is minimal when (V_{FFOLD} = 1 V).

As detailed in [3], we can compute the minimum branch frequency as follows:

$$f_{sw,\min} = \frac{\frac{I_{CH} \cdot I_{DISCH}}{I_{CH} + I_{DISCH}}}{2 \cdot (C_{15} + C_{16})} \cdot \frac{1}{V_{OSC(swing),\max} - R_{OSC} \cdot (I_{CH} + I_{DISCH})} \quad \textit{(eq. 88)}$$

In our case, it comes:

$$f_{sw,\min} = \frac{60 \cdot 10^{-6}}{2 \cdot (22 \cdot 10^{-12} + 470 \cdot 10^{-12})} \cdot \frac{1}{4 - (5.1 \cdot 10^{3} \cdot (140 + 105) \cdot 10^{-6})} \cong 22\ kHz \quad \textit{(eq. 89)}$$

It may happen that the oscillator capacitors (in particular C_{FF}) need to be larger either not have its range exceeded or to force deep DCM (5) when the system enters the FFOLD mode. Unfortunately, this can cause $f_{sw,\min}$ to be low enough to enter the audible range.

5. Deep DCM means that the oscillator forces a minimum branch frequency which is low enough to ensure a significant dead−time and to prevent possibly noisy transitions between CrM and DCM within the input voltage sinusoid

In this case, the following tweaks can be used:

- Clamping the FFOLD pin voltage.

In FFOLD mode, the clamp frequency is reduced as a function of V_{FFOLD} to be minimum when V_{FFOLD} drops to 1 V. This option illustrated by Figure 17 consists of forcing a minimum voltage higher than 1 V on the FFOLD pin. The pfcOK pin provides 5 V in normal operation. A portion of this voltage (resistors divider R_{CLAMP1}, R_{CLAMP2} with R_{CLAMP2} small compared to R_{FFOLD}) can be used through a diode to force this minimum voltage. See [3] for more details.

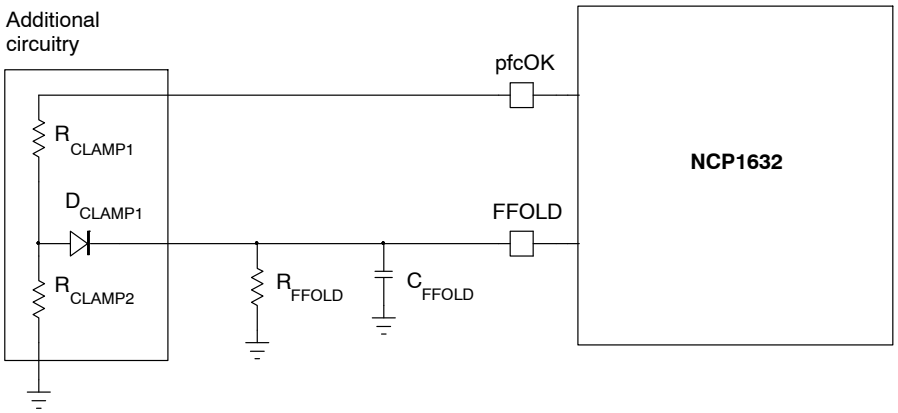


Figure 17. Clamping the Standby Frequency

- Disconnecting part of C_{FF} in light load conditions.

Another option consists of removing part of the biggest capacitor in standby as shown by Figure 18. A "Heavy_load" signal should be used to connect the capacitor C_{FF2} when the load is high and disconnect it in light load conditions.

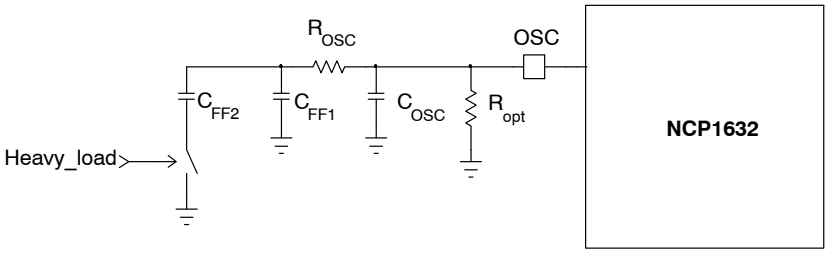


Figure 18. Disconnecting Part of the Oscillator Biggest Capacitor

The need for clamping the standby frequency or for disconnecting part of the biggest capacitor may occur when the C_{FF} capacitor must be larger than the 470−pF value of the default configuration. This can be the case if there is a need for:

- Increasing the oscillator operating range. This can occur in applications where relatively high inductances are used which lead to a low−frequency CrM operation
- Decreasing the switching frequency when entering the FFOLD mode. We generally want to have a deep DCM operation (6) when entering FFOLD. This may happen if relatively large boost inductances being used, the circuit is designed to enter at a high power at which the CrM frequency is still low.

6. Deep DCM means that the oscillator forces a minimum branch frequency which is low enough to ensure a significant dead−time and to prevent possibly noisy transitions between CrM and DCM within the input voltage sinusoid

Conclusion

This application note proposes a systematic process for the eased design of an efficient 2−phase, interleaved PFC. More specifically, this paper provides the key equations and design criteria necessary to dimension the PFC stage. This dimensioning process is illustrated by the practical example of the 300−W, wide−mains evaluation board [5]. Note that a design spreadsheet [4] automates the dimensioning process.

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[1] Joel Turchi, "Characteristics of Interleaved PFC Stages", Application Note AND8355, http://www.onsemi.com/pub/Collateral/AND8355−D.PDF

[2] Joel Turchi, "Key Steps to Design an Interleaved PFC Stage Driven by the NCP1631", Application Note AND8407, http://www.onsemi.com/pub/Collateral/AND8407−D.PDF

[3] Joel Turchi, "Switching from a NCP1631− to a NCP1632−driven Interleaved PFC", Application Note AND9622, http://www.onsemi.com/pub/Collateral/AND9622−D.PDF

[4] NCP1632 Design & Development Tool, http://www.onsemi.com/PowerSolutions/supportDoc.do?type=tools&rpn=NCP1632

[5] Nikhilesh Kamath, NCP1632 Evaluation Board User¿s Manual, http://www.onsemi.com/pub_link/Collateral/EVBUM2049−D.PDF

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