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LLC Resonant Converter Synchronous Rectification Design using FAN6248

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APPLICATION NOTE

INTRODUCTION

Among many resonant converters, LLC resonant converter has been the most popular topology for high power density applications since this topology has many advantages over other resonant topologies; it can regulate the output over entire load variation with a relatively small variation of switching frequency, it can achieve zero voltage switching (ZVS) for the primary side switches and zero current switching (ZCS) for the secondary side rectifiers and the resonant inductor can be integrated into a transformer. In an LLC resonant converter, rectifier diodes are typically used to obtain DC output voltage from the transformer secondary side winding. The conduction loss of diode rectifier contributes significantly to the overall power losses in an LLC resonant converter; especially in low voltage and high current output applications. The conduction loss of a rectifier is proportional to the product of its forward−voltage drop and the forward conduction current. Using synchronous rectification (SR) where the rectifier diode is replaced by MOSFET with a small on resistance R_{DS-ON}, the forward−voltage drop of a synchronous rectifier can be lower than that of a diode rectifier and, consequently, the rectifier conduction loss can be reduced.

The FAN6248 is an advanced synchronous rectifier controller that is optimized for LLC resonant converter topology with minimum external components. It has two driver stages for driving the SR MOSFETs which are rectifying the outputs of the secondary side transformer windings. The two gate driver stages have their own sensing inputs and operate independently each other. The adaptive parasitic inductance compensation function minimizes the body diode conduction and maximizes the efficiency. The advanced control algorithm allows stable SR operation over entire load range. Figure 1 shows the typical application circuit of FAN6248.

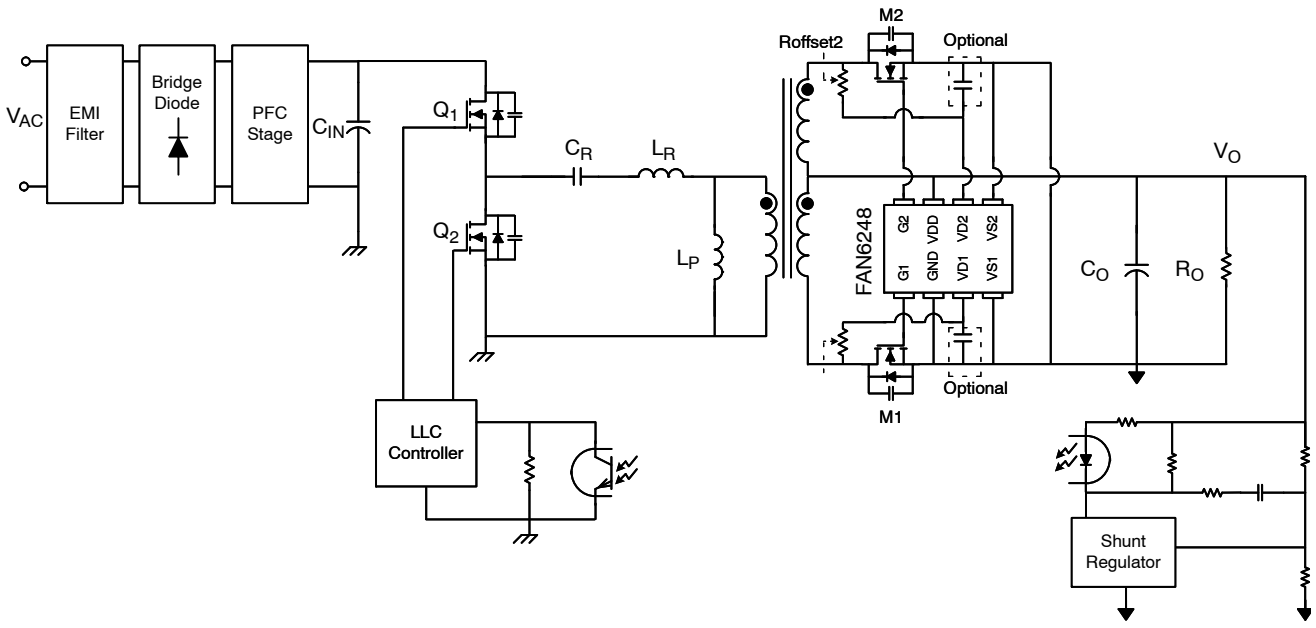


Figure 1. Typical Application Circuit of FAN6248

APPLICATIONS INFORMATION

Basic Operation Principle of FAN6248

Figure 2 shows the key waveforms of SR operation in LLC resonant converter. Basically, FAN6248 controls the SR MOSFET based on the instantaneous drain−to−source voltage sensed across DRAIN and SOURCE pins. Before SR gate is turned on, SR body diode operates as normal diode rectifier. Once the body diode starts conducting, the drain−to−source voltage drops below the turn−on threshold voltage V_{TH_ON} which triggers the turn−on of the SR gate. Then the drain−to−source voltage is determined by the product of R_{DS_ON} and instantaneous SR current. When the drain−to−source voltage reaches the turn−off threshold voltage V_{TH_OFF} as SR MOSFET current decreases to near zero, FAN6248 turns off the gate. If the turn off threshold V_{TH_OFF} is close to zero, the turn off dead time T_{DEAD} can be minimized in ideal case.

Once SR gate is turned on, there exists severe oscillation in drain−to−source voltage which results in several turn−off mis−trigger. To provide stable SR control without the mis−trigger, it is desirable to have large turn−off blanking time (= minimum turn−on time) until the drain voltage oscillation attenuates. However, too large blanking time results in problems at light load condition where the SR conduction time is shorter than the minimum turn−on time. To solve this issue, FAN6248 has adaptive minimum turn−on time where the turn−off blanking time changes in accordance with the SR conduction time T_{SRCOND} measured in previous switching cycle. The SR conduction time is measured by the time from SR gate rising edge to the instant when drain sensing voltage V_{DS_SR} is higher than V_{TH_HGH}. According to the previous cycle T_{SRCOND} measurement result, the minimum turn−on time is determined by 50% of T_{SRCOND} in FAN6248HA(B), and 25% of T_{SRCOND} in FAN6248HC(D) and FAN6248LC(D).

Design Consideration for R_{OFFSET}

The typical stray inductance of the MOSFET packages are summarized in Fig. 3 and the stray inductance effect is described in Figure 4. Due to the stray inductance of the lead frame in Figure 4 (b), positive offset voltage ($V_{LS} = L_{stray} \times$ di/dt) is induced on the stray inductance when SR current decreases. This offset voltage makes SR MOSFET drain−to−source voltage larger than the product of R_{DS_ON} and instantaneous SR current, which results in premature turn−off of SR gate as shown in Figure 4 (b). Since the di/dt of SR current changes as load condition changes, the dead time also changes with load condition. To compensate the induced offset voltage, FAN6248 has a adaptive virtual turn−off threshold voltage which is compared to V_{DS_SR} and determines turn−off of SR MOSFET, as shown in Figure 5.

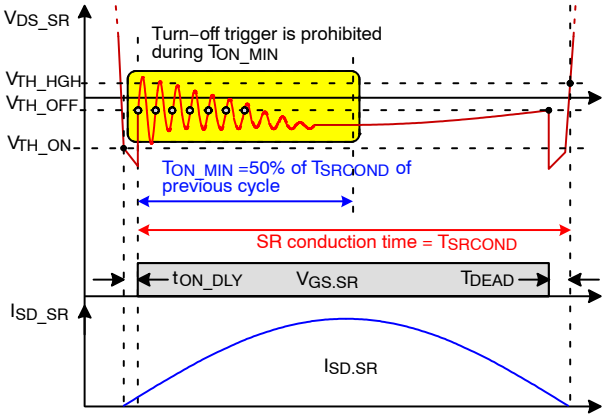
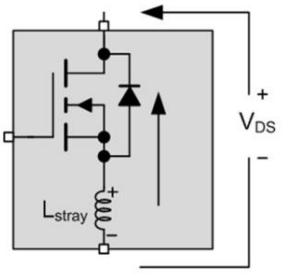


Figure 2. Ideal Waveforms of SR Operation in DCM

The virtual threshold is a combination of variable internal turn−off threshold voltages V_{TH_OFF1} and V_{TH_OFF2} (2 steps) and modulated offset voltage V_{offset} (16 steps) which is determined by 16 steps internal offset currents and an external offset resistor R_{OFFSET}. So, The virtual turn−off threshold voltage can be expressed as:

$$\text{Virtual } V_{TH\_OFF} = V_{TH\_OFF(n)} - R_{OFFSET} \times I_{offset\_step(k)} = V_{TH\_OFF(n)} - V_{offset(k)} \quad \text{(eq. 1)}$$



Package Type	L_{SOURCE} (pH)
TO-220	9000
D2PAK	5000
IPAK	4000
DPAK	3000
SO8	1000

Figure 3. Stray Inductance of MOSFET Package

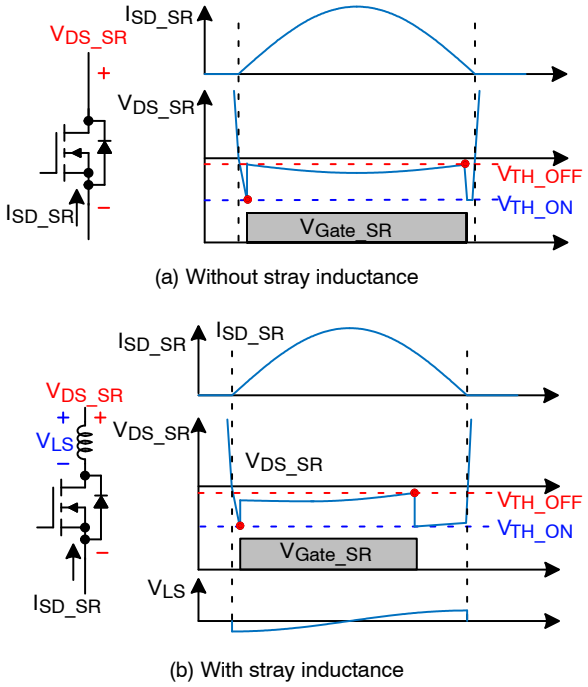


Figure 4. Stray Inductance Effect at SR Turn−off

For R_{OFFSET} selection, since R_{OFFSET} determines V_{offset} step size, R_{OFFSET} should be properly selected for stable operation. If too small R_{OFFSET} is designed, dead time variation becomes narrow. This is good for transient response. But, it can make undefined control range in steady state as shown in Figure 6. When the output load condition is set in the undefined range, FAN6248 repeatedly increases and dicreases the turn−off threshold voltage between V_{TH_OFF1} and V_{TH_OFF2} to maintain dead time target. Therefore it can induce system unstable and audible noise. To avoid this unstable operation, R_{OFFSET} needs to have relatevley large value to make overlap between V_{TH_OFF2} range and V_{TH_OFF1} range as shown in Figure 7. Therefore, recommend R_{OFFSET} is as small as value satisfying :

$$V_{TH\_OFF2} - V_{TH\_OFF1} < R_{OFFSET} \times I_{offset\_step15} \quad \text{(eq. 2)}$$

where, I_{offset_step15} is 135 μA of maximum step of the internal offset current. Table 1 shows recommended R_{OFFSET} for each version.

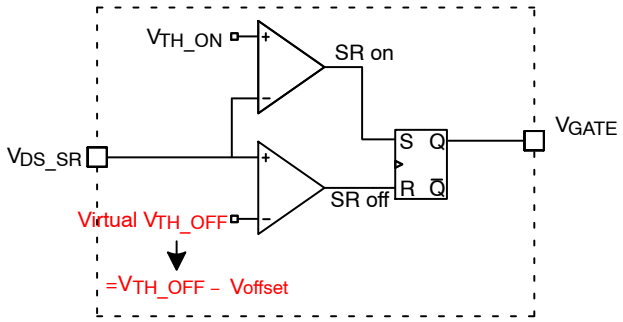


Figure 5. Virtual V_{TH_OFF}

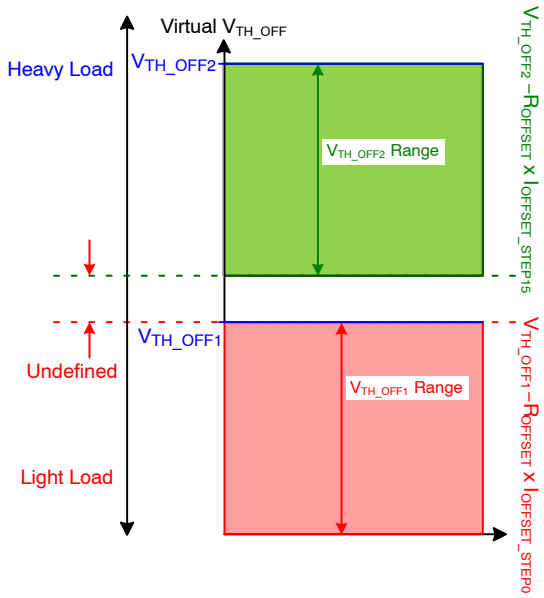


Figure 6. Virtual V_{TH_OFF} with too Small R_{OFFSET}

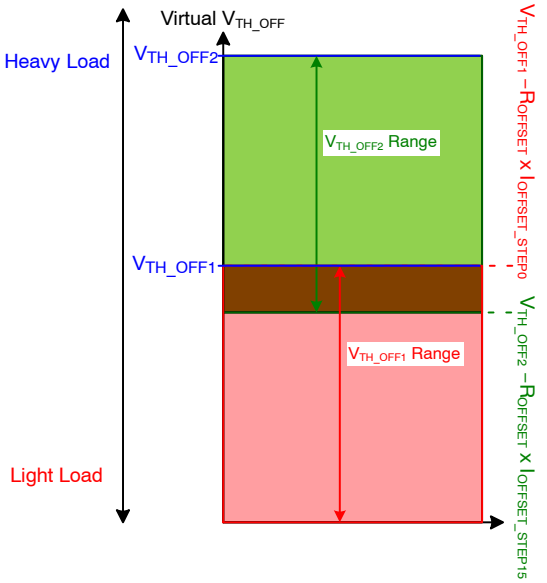


Figure 7. Virtual V_{TH_OFF} with recommended R_{OFFSET}

Table 1. RECOMMENDED R_{OFFSET}

	FAN6248HA	FAN6248HB	FAN6248HC (D), LC(D)
R_{OFFSET}	820 – 910 Ω	680 –750 Ω	240 Ω

Capacitive Current Spike Detection and Design Consideration

A. Heavy Load Condition

Figure 8 shows operational waveforms of the LLC resonant converter in heavy load condition. The switching period is subdivided into 4 modes. The main equivalent circuits for operation modes are shown in Figure 9.

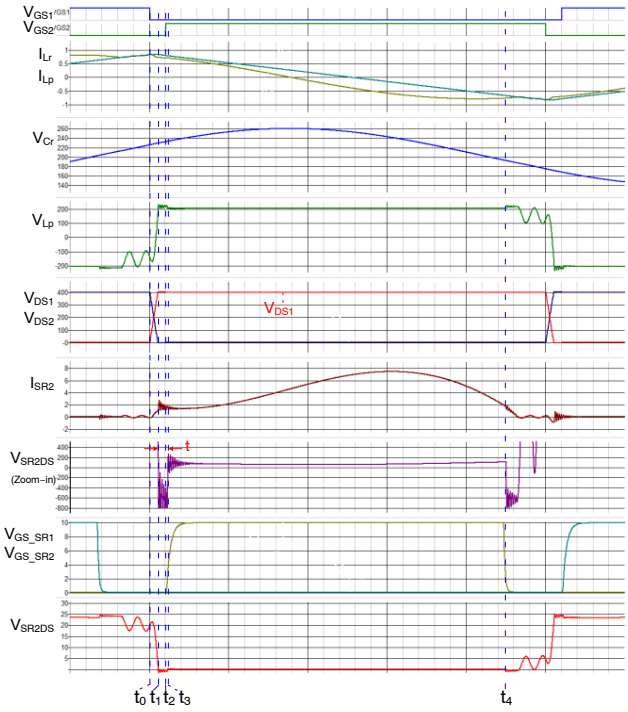


Figure 8. Operational Waveforms in Heavy Load Condition

- Mode 1 ($t_0 \sim t_1$):
  Mode 1 begins at t_0 when the primary switch Q_1 is turned off. An equivalent circuit is shown in Figure 8 (a). In this mode, C_{OSS1} and $C_{OSS}SR1$ are charged, and C_{OSS2} and $C_{OSS}SR2$ are discharged by the resonant current I_{Lr}. In addition, the magnetizing inductor voltage V_{Lp} increases in this mode. When the transition of drain voltages (V_{DS1}, V_{DS2}, V_{SR1DS}, V_{SR2DS}) is completed, this mode ends. In the practical LLC system, the transition of V_{DS1} and V_{DS2} may end earlier than that of V_{SR1DS} and V_{SR2DS}. Zero voltage switching (ZVS) of Q_2 and M_2 can be gurrantted during this mode

- Mode 2 ($t_1 \sim t_2$):
  When mode 1 ends, the body diodes of Q_2 and M_2 are conducted. So, the resonant inductor voltage V_{Lr} is determined by the resonant capacitoer voltage V_{Cr} and V_{Lp} as:

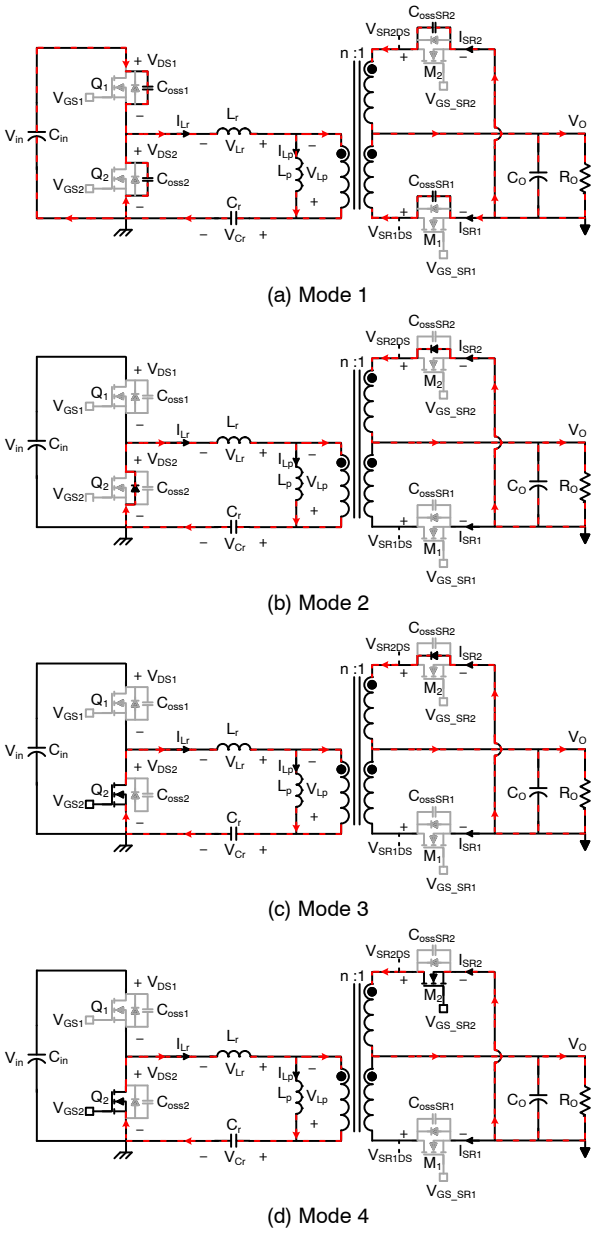


Figure 9. Operation Mode in Heavy Load Condition

$$V_{Lr} = V_{Cr} - V_{Lp} \quad \text{(eq. 3)}$$

where, V_{Lp} is clampled by the output voltage V_o and forward voltage V_F of body diode of M_2. So, V_{Lp} is given by at t_1:

$$V_{Lp} = n(V_o + V_F) \quad \text{(eq. 4)}$$

where n is turns ratio of the transformer. If V_{Cr} is much larger than V_{Lp} by large resonant current I_{Lr} under heavy load condition, V_{Lr} can build up I_{Lr} which starts transfering power to the secondary side in this mode. In the secondary side, V_{SR2DS} becomes $-V_F$ which is lower than SR turn−on threshold voltage V_{TH_ON} at t_1. It makes M_2 turn−on after turn−on delay t_{ON_DLY}.

- Mode 3 ($t_2 \sim t_3$):
  This mode starts when Q_2 is turned on. In the primary side, I_{Lr} flows through channel of Q_2 instead of the body diode. When M_2 is turned on this mode ends
- Mode 4 ($t_3 \sim t_4$):
  After t_{ON_DLY} from t_1, M_2 is turned on so that V_{SR2DS} is determined by product of R_{DS_ON} of M_2 and instantaneous SR current I_{SR2}. When V_{SR2DS} reaches turn−off threshold voltage V_{TH_OFF}, M_2 is turned off and this mode ends

B. Light Load Condition

Figure 10 shows operational waveforms in light load condition. The switching peiod is subdivided into 5 modes. There is an additional mode compared to heavy load condition. The main equivalent circuits for operation modes are shown in Figure 11.

- Mode 1 ($t_0 \sim t_1$):
  Mode 1 begins at t_0 when the primary switch Q_1 is turned off. An equivalent circuit is shown in Figure 11 (a). The operation is almost the same with mode 1 in heavy load condition
- Mode 2 ($t_1 \sim t_2$):
  When mode 1 ends, the body diodes of Q_2 and M_2 are turned−on. The resonant inductor voltage V_{Lr} is still determined by the resonant capacitor voltage V_{Cr} and V_{Lp}. However, since V_{Cr} is not larger enough to build up I_{Lr} and most of the V_{Cr} applies to L_p, the LLC converter cannot transfer power to the secondary side and the secondary SR current I_{SR2} decreases with a slope of $n^2 \times (V_o + V_F) / L_p$. In the secondary side, body diode of M_1 is turned off so that I_{SR1} is added to I_{SR2} at t_1. It results in sudden increase of I_{SR2} which is called capacitive current spike at t_1. In addition, in this mode, V_{SR2DS} becomes $-V_F$ at t_1. It generates turn−on signal of M_2. However, the turn−on signal should be ignored, because there is no power transfer from the primary side. If the turn−on signal is not prevented, abnormal turn−on happen at t_3 as shown in Figure 12. The mis−trigger signal induces inversion current of M_2 from the output capacitor. Mode 2 ends when Q_2 is turned on
- Mode 3 ($t_2 \sim t_3$):
  In this mode, I_{Lp} decreases with the same slope of that of mode 2 until I_{SR2} becomes zero. In the primary side V_{Cr} is charged by I_{Lp}. The equivalent circuit is shown in Figure 11 (c)

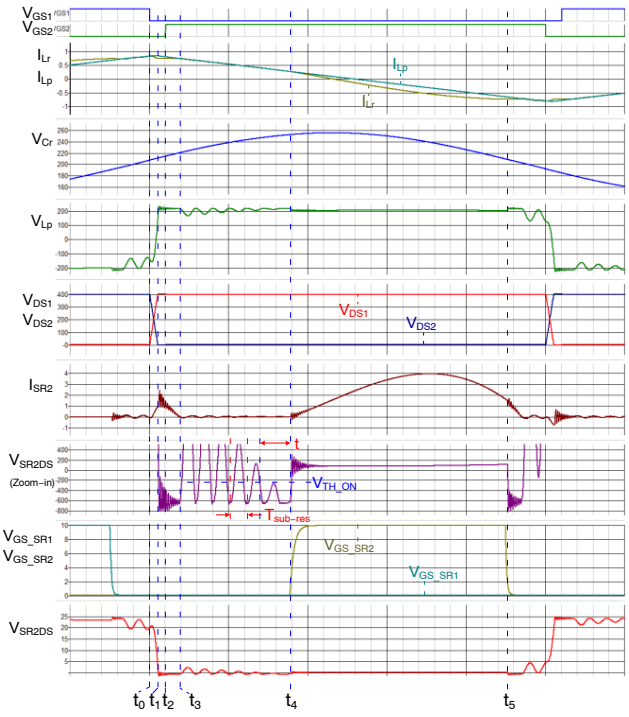


Figure 10. Operational Waveforms in Heavy Load Condition

- Mode 4 ($t_3 \sim t_4$):
  In the primary side, since V_{Lp} is not clampled by the output voltage any more, V_{Cr} is divided into V_{Lp} and V_{Lr} with their inductance ratio:

$$V_{Lp} = V_{Cr} \times L_p/(L_r + L_p) \quad \text{(eq. 5)}$$

$$V_{Lr} = V_{Cr} \times L_r/(L_r + L_p) \quad \text{(eq. 6)}$$

In addition, C_r is gradually charged by I_{Lp}. In the secondary side, since I_{SR2} is zero at t_3, sub−resonance starts between $C_{OSS}SR1$ and $C_{OSS}SR2$, L_r, and L_p. the sub−resonance period $T_{sub-res}$ can be calculated by:

$$T_{sub-res} = 2\pi\sqrt{(L_r \parallel L_p) \times n^2(C_{oss}SR1 + C_{oss}SR2)} \quad \text{(eq. 7)}$$

As a result, V_{SR2DS} oscillates as shown in Figure 10. and I_{Lr} cannot transfer power to the secondary side until V_{Lp} becomes $n \times (V_o + V_F)$. Finally, when V_{Lp} reaches $n \times (V_o + V_F)$, V_{Lp} is clamped by $n \times (V_o + V_F)$ and I_{Lr} builds up and I_{SR2} increases. Therefore, V_{GS_SR2} should be turned on after the sub−resonance ends to prevent the inversion current in Figure 12.

- Mode 5 ($t_4 \sim t_5$):
  After t_{ON_DLY2} finishes, M_2 is turned on as mode 4 in heavy load condition. When V_{SR2DS} is higher than turn−off threshold voltage V_{TH_OFF}, M_2 is turned off and this mode ends

C. Capacitive Current Spike Detection of FAN6248

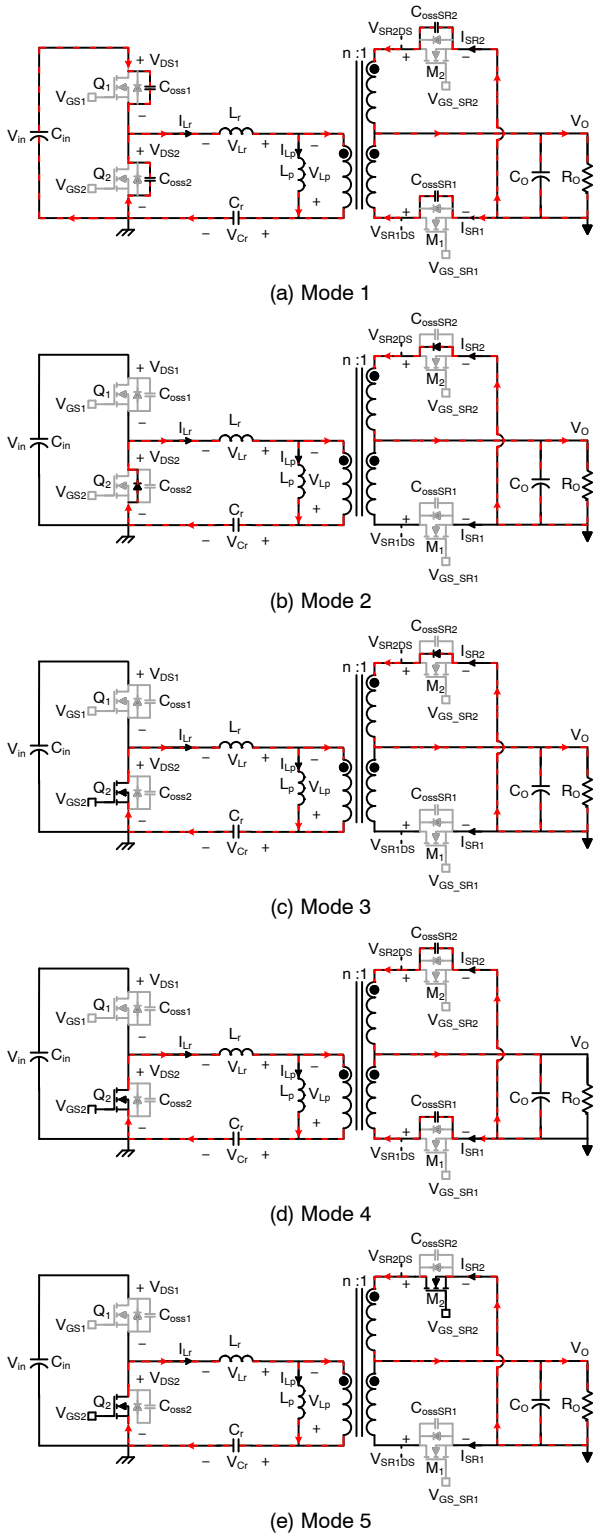


Figure 11. Operation Mode in Light Load Condition

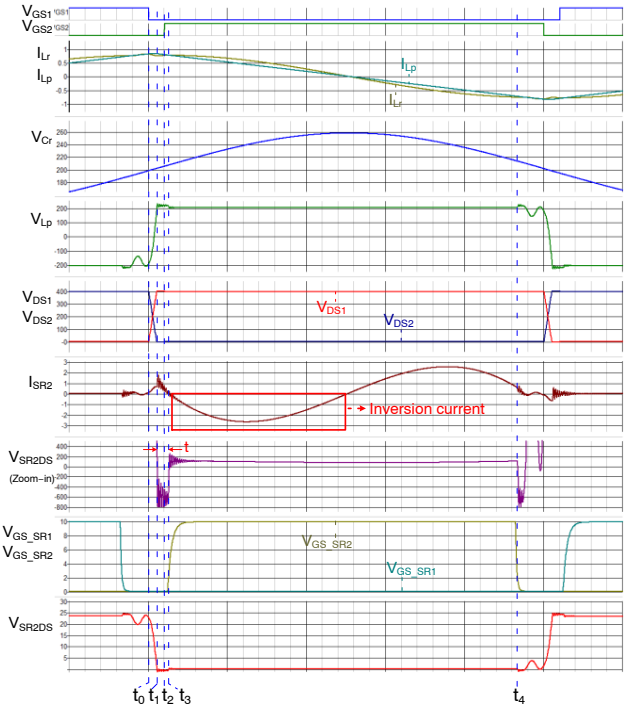


Figure 12. Operational Waveforms in Light Load Condition

When SR current inversion occurs by the mis−tirgger signal as shown in Figure 12, the drain sensing voltage of M_2 becomes positive. In this condition, if V_{SR2DS} is higher than V_{TH_OFF} for t_{INV} (= $T_{SRCOND} \times K_{INV}$), SR current inversion is detected. Then, FAN6248 increases turn−on delay from t_{ON_DLY} to t_{ON_DLY2} in next cycle. When t_{ON_DLY2} is triggered, V_{SR2DS} should be lower than V_{TH_ON} for t_{ON_DLY2} to turn on M_2. If V_{SR2DS} oscillates as shown in mode 4 in light load condition, V_{SR2DS} increases again higher than VTH_ON before t_{ON_DLY2} timer out. This means if the resonance period $T_{sub-res}$ is smaller than t_{ON_DLY2}, the turn−on trigger by the oscillation is ignored. As a result, SR mis−trigger is prevented. To guarantee stable operation under light load condition, the LLC converter needs to meet following equations:

$$t_{ON\_DLY2} > T_{sub-res} \quad \text{(eq. 8)}$$

$$t_{ON\_DLY2} > t_{13} \quad \text{(eq. 9)}$$

where, t_{13} is the time from t_1 to t_3 in Figure 10 and related with L_p, L_r, C_r, C_{OSS1}, C_{OSS2}, $C_{OSS}SR1$, and $C_{OSS}SR2$. To exit the SR current inversion detection mode, 7 consecutive switching cycles in FAN6248HA(B), 31 consecutive switching cycles in FAN6248HC(D) and FAN6248LC(D) without capacitive current spike are required.

Gate Driver and PCB Layout Recommendation

FAN6248 has moderate gate sourcing and sinking current to handle high power up to 800 W system design. If FAN6248 is applied to higher power applications, external gate diriver may be required. It depends on SR MOSFET input capacitance. To guarantee fast turn−off and stable operation pnp−transistor discharging method as shown in Figure 13 is highly recommended. SR gate is turned on through *R1* and *R3*, and discharged by *Q1* and *Q2*.

In PCB layout, drain sensing is important to control SR MOSFET properly. To reduce sensing noise, a quite place sensing is recommened in Figure 14. If SR MOSFET has D−Pak and D2−Pak package, edge side of drain soldermask near SOURCE or GATE pin becomes the optimized drain sensing point.

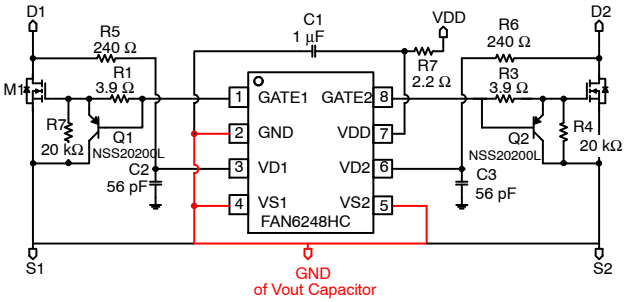


Figure 13. Recommended Circuit for FAN6248HC(D) and LC(D)

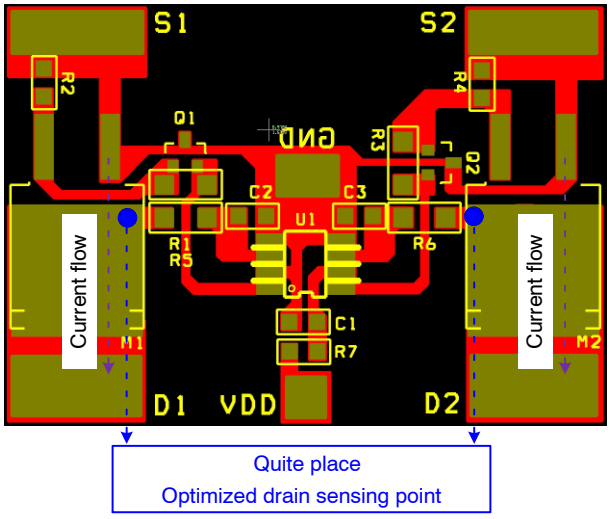


Figure 14. Recommended PCB Layout

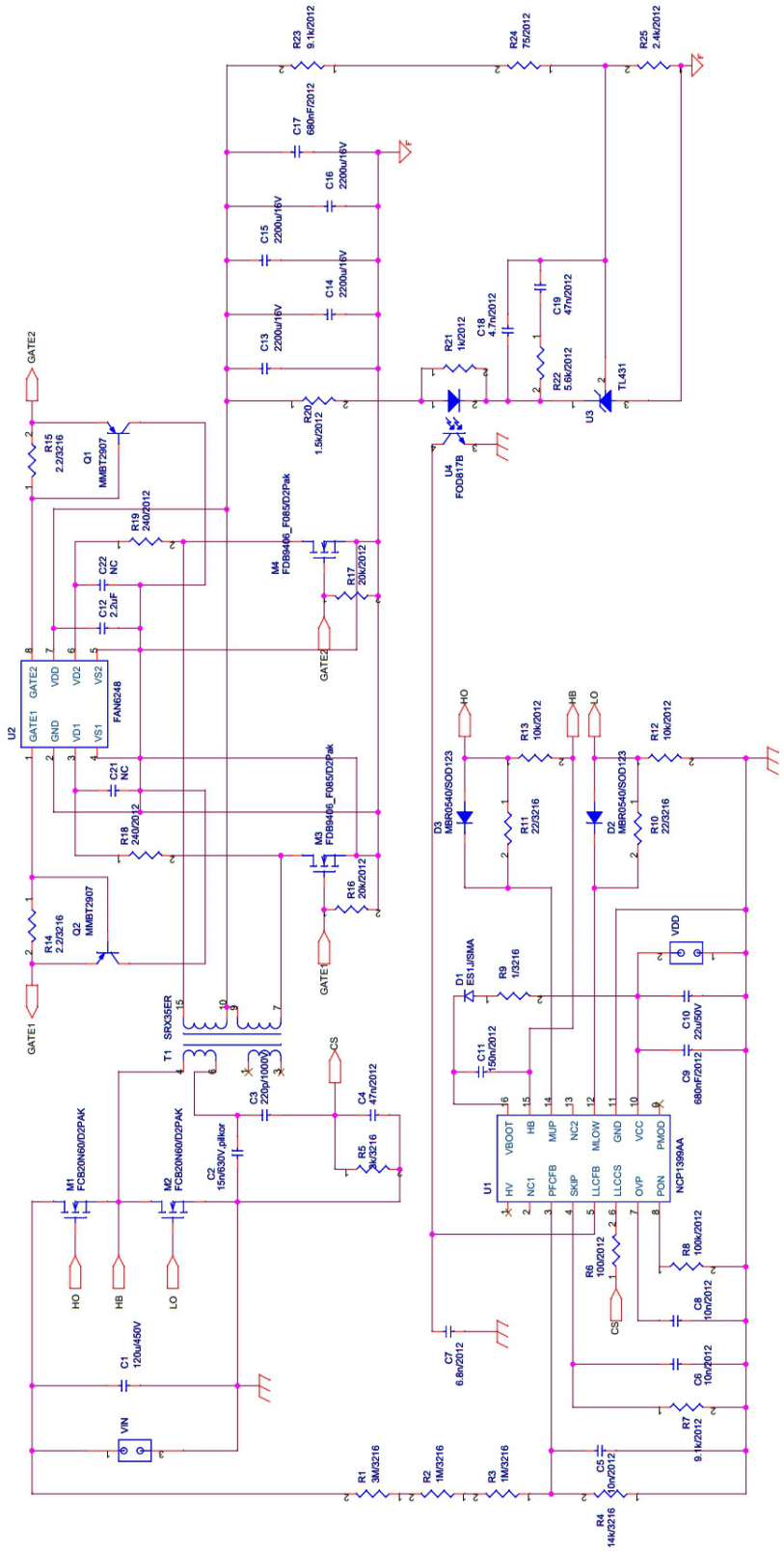
Reference Design

Table 2 shows general information of the reference design. The design utilizes NCP1399AA for the primary side LLC controller, and FAN6248 for the secondary side synchronous rectification controller.

Table 2. GENERAL INFORMATIONS

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	390	VDC
Output Voltage	V_O	12	V
Maximum Output Current	I_{OUTMAX}	20	A
Output Power	P_O	240	W
Operating frequency @ full load condition	f_s	110	kHz
Maximum Efficiency	η	96.9	%
4 points Average Efficiency (100%, 75%, 50%, 25%)	η	95	%
Output voltage ripple I_{OUT} = 20 A	V_{OUT_PK-PK}	384	mV

Evaluation Board Schematic



NOTE: The schematic is reference only. In user design, the circuit should be tested.

Figure 15. Evaluation Board Schematic

Bill of Materials

Table 3. BILL OF MATERIALS

Type	Location	Value	Footprint	Manufacturer	P/N
Capacitor	C1	120 μF / 450 V	Through Hole	Samyoung	NFL series
	C10	22 μF / 50 V	Through Hole	Samyoung	KMG series
	C11	150 nF	0805	Variable	
	C12	2.2 μF	0805	Variable	
	C13, C14, C15, C16	2200 μF / 16 V	Through Hole	Samyoung	NXH series
	C18	4.7 nF	0805	Variable	
	C2	15 nF / 1000 V	Through Hole	Pilkor	MMKP series
	C3	220 pF / 1000 V	Through Hole	Pilkor	MMKP series
	C4,C19	47 nF	0805	Variable	
	C5,C6,C8	10 nF	0805	Variable	
	C7	6.8 nF	0805	Variable	
	C9,C17	680 nF	0805	Variable	
Resistor	R1	3 MΩ	1206	Variable	
	R10,R11	22 Ω	1206	Variable	
	R12,R13	10k Ω	0805	Variable	
	R14,R15	2.2 Ω	1206	Variable	
	R16,R17	20 kΩ	0805	Variable	
	R18,R19	240 Ω	0805	Variable	
	R2,R3	1 MΩ	1206	Variable	
	R20	1.5 kΩ	0805	Variable	
	R21	1 kΩ	0805	Variable	
	R22	5.6 kΩ	0805	Variable	
	R23	9.1 kΩ	0805	Variable	
	R24	75 Ω	0805	Variable	
	R25	2.4 kΩ	0805	Variable	
	R4	14 kΩ	1206	Variable	
	R5	3 kΩ	1206	Variable	
	R6	100 Ω	0805	Variable	
	R7	9.1 kΩ	0805	Variable	
	R8	100 kΩ	0805	Variable	
	R9	1 Ω	1206	Variable	
Transformer	T1	SRX35ER	EER3037	TDK	
IC/ Photo Coupler	U1	NCP1399	SOIC−16NB	On Semiconductor	NCP1399AA
	U2	FAN6248	SOIC−8NB	On Semiconductor	FAN6248HA
	U3	LM431	SOT−23	On Semiconductor	LM431SCCM3X
	U4	FOD817B	DIP−4	On Semiconductor	FOD817B
Connector	CON1	3PIN			Yeonho
	CON2	2PIN			Yeonho
Diode	D1	ES1J	SMA	On Semiconductor	ES1J
	D2,D3,D4,D5	MBR0540	SOD−123	On Semiconductor	MBR0540
MOSFET	M1,M2	FCB20N60	D2PAK	On Semiconductor	FCB20N60
	M3,M4	FDB9406_F085	D2PAK	On Semiconductor	FDB9406_F085
Transistor	Q1	MMBT2907	SOT−23	On Semiconductor	MMBT2907
	Q2	MMBT2907	SOT−23	On Semiconductor	MMBT2907

Transformer specification

SRX35ER which has 97 mm^2 of effective area is utilized for LLC transformer. For the optimal design of the resonant trank, 600 μH of L_p and 100 μH of resonant inductance L_r are designed, respectively. For reference design, TDK SRX35ER is utilized.

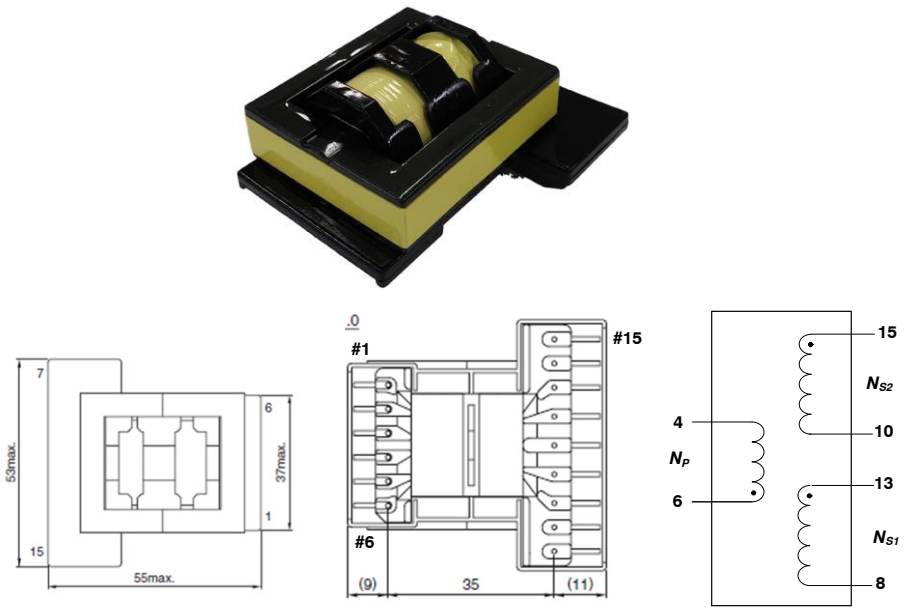


Figure 16. Transformer Dimension and Shapes

Table 4. TRANSFORMER WIDING METHOD

	Pin (Start → Finish)	Wire	Turns	Winding Method
INSULATION: POLYESTER TAPE t = 0.025 mm, 2 LAYERS				
N_p	6 → 4	0.1φ × 50 USTC	37	Solenoid winding
INSULATION: POLYESTER TAPE t = 0.025 mm, 2 LAYERS				
N_s	15 → 10 13 → 8	0.10φ × 75 USTC	2	Bifilar
INSULATION: POLYESTER TAPE t = 0.025 mm, 2 LAYERS				
N_s	14 → 9 12 → 7	0.10φ × 75 USTC	2	Bifilar
INSULATION: POLYESTER TAPE t = 0.025 mm, 2 LAYERS				
N_s	15 → 10 13 → 8	0.10φ × 75 USTC	2	Bifilar
INSULATION: POLYESTER TAPE t = 0.025 mm, 2 LAYERS				
N_s	14 → 9 12 → 7	0.10φ × 75 USTC	2	Bifilar

1. Design parameters : L_p = 600 μH, L_r = 100 μH at f_s = 100 kHz.

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