

## KAE-08151 Charge Binning



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### INTRODUCTION

KAE-08151 sensor has an option to bin charge while maintaining a constant 20 MHz binned pixel output rate. Table 1 lists the frame rates available when binning according to this note. This note describes the method to be used to bin successfully.

### No Horizontal Charge Binning

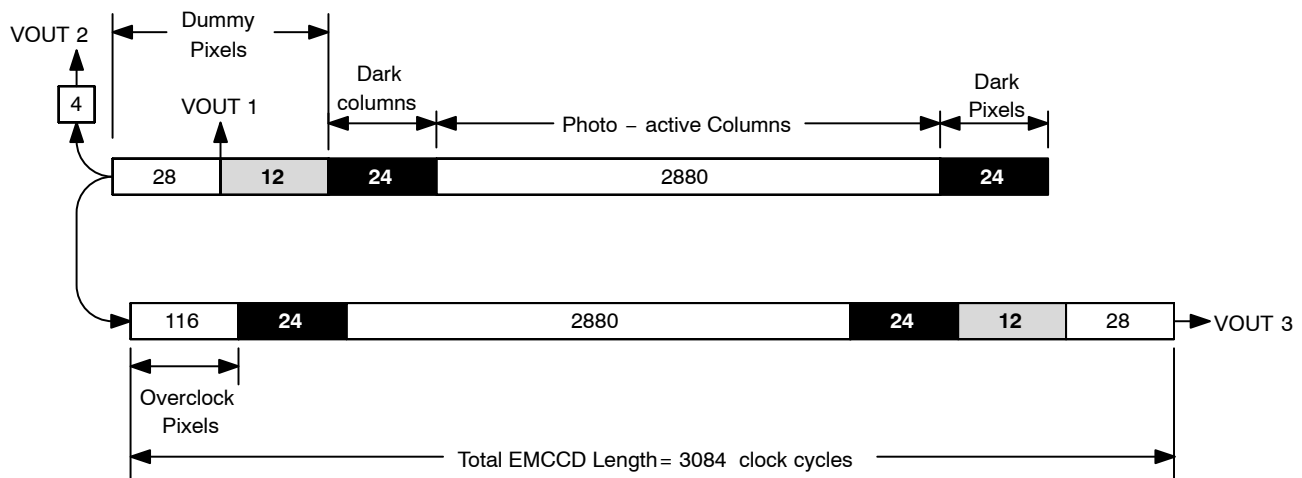
In Figure 1, it is shown that the first photo-active pixel arrives at VOUT1 after 36 (12 + 24) H2L clock cycles. The first photo-active pixel arrives at VOUT2 after 68 (4 + 28 + 12 + 24) H2L clock cycles. The first photo-active pixel arrives at VOUT3 after 64 (28 + 12 + 24) H2L clock cycles. The pixels at VOUT3 are delayed by one line relative to when pixels arrive at VOUT2. Every line must have exactly 3084 clock cycles to preserve the alignment of pixels within the EMCCD register.

In Figure 2, it is shown that the pixels at VOUT3 are delayed by two lines relative to when pixels arrive at VOUT2. Every line must have exactly 1542 clock cycles to preserve the alignment of pixels within the EMCCD register.

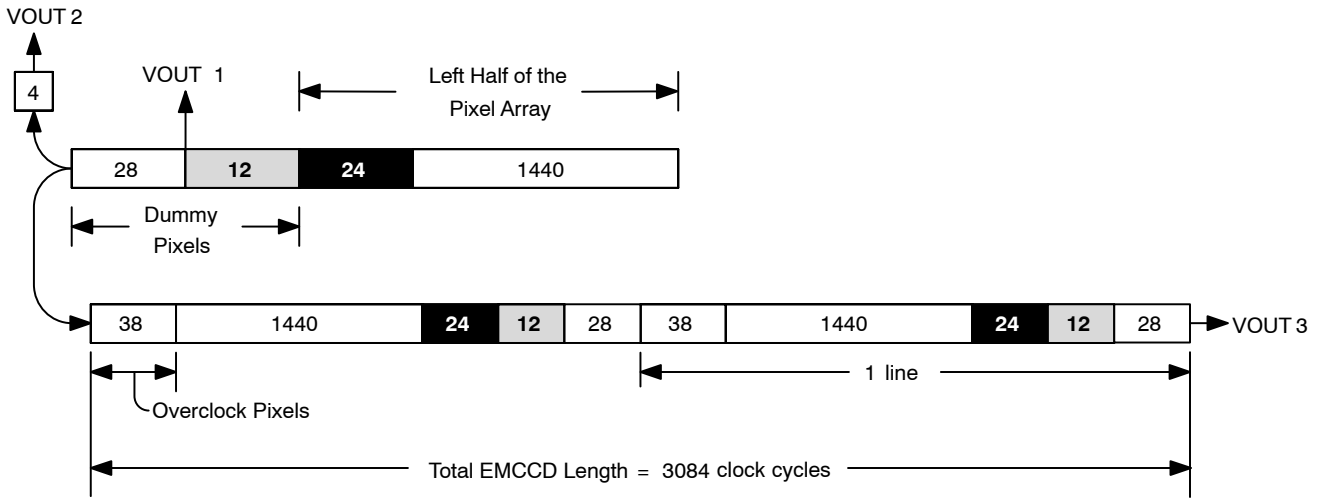
### APPLICATION NOTE

**Table 1. FRAME RATES AVAILABLE WHEN BINNING**

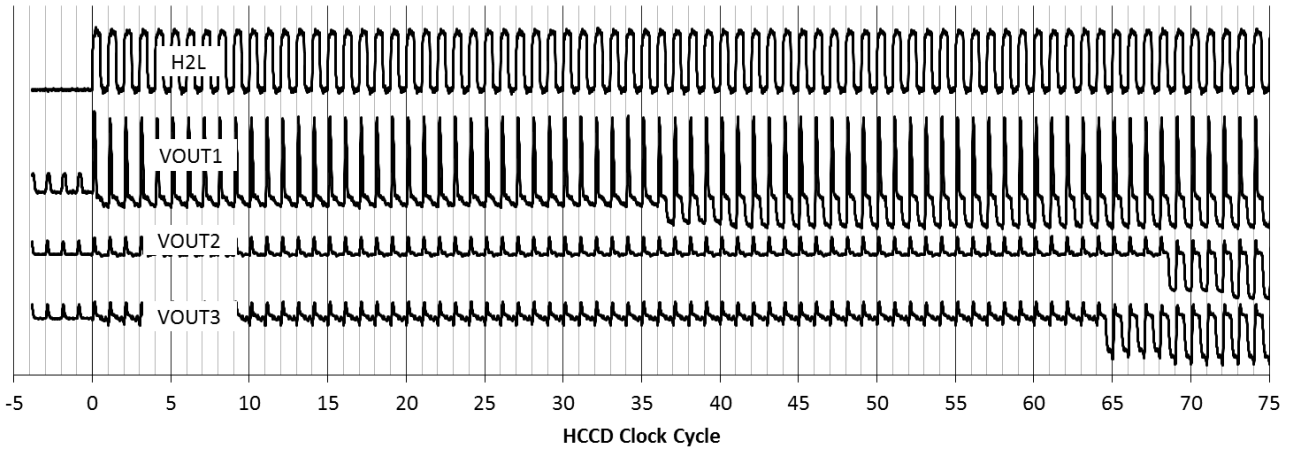
Binning	Single	Dual (Left/Right)	Dual (Top/Bottom)	Quad
1 x 1	2.0	3.5		6.95
2 x 2	5.7	8.4		16.7
3 x 3	8.8	n/a	17.6	n/a
4 x 4	10.9	n/a	21.8	n/a



**Figure 1. The Alignment of Pixels Within the HCCD and EMCCD When Transferring an Entire Line to the Left Side Outputs**



**Figure 2. The Alignment of Pixels Within the HCCD and EMCCD When Transferring the Left Half of the Line to the A and C Outputs and the Right Half of the Line to the B and D Outputs**



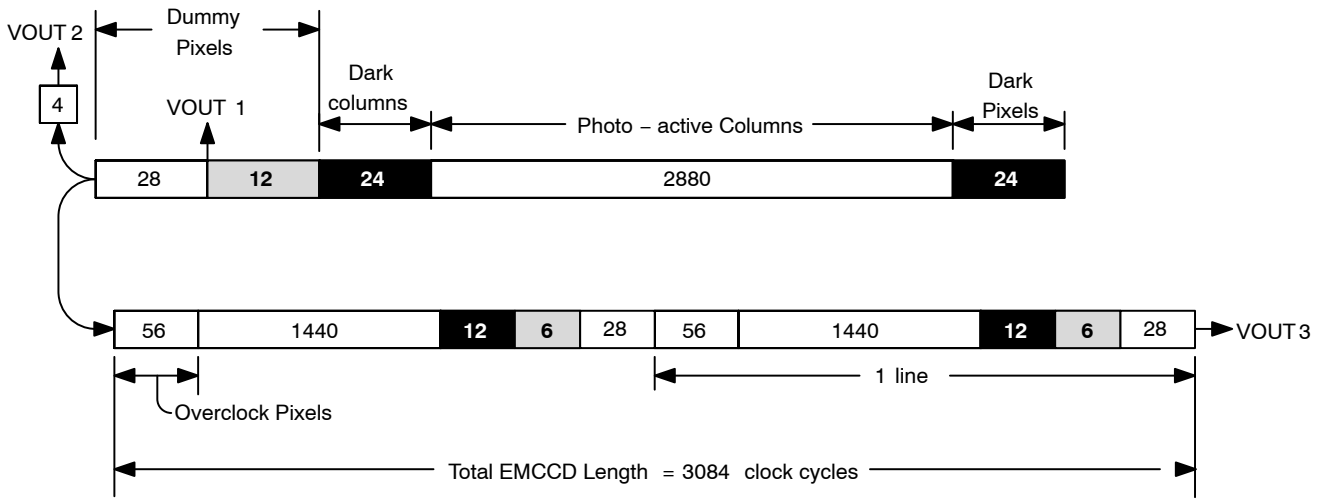
**Figure 3. The Video Output Waveforms at the Start of Each Line with No Horizontal Charge Binning, for 1, 2, or 4 – Output Mode**

**2X Horizontal Charge Binning**

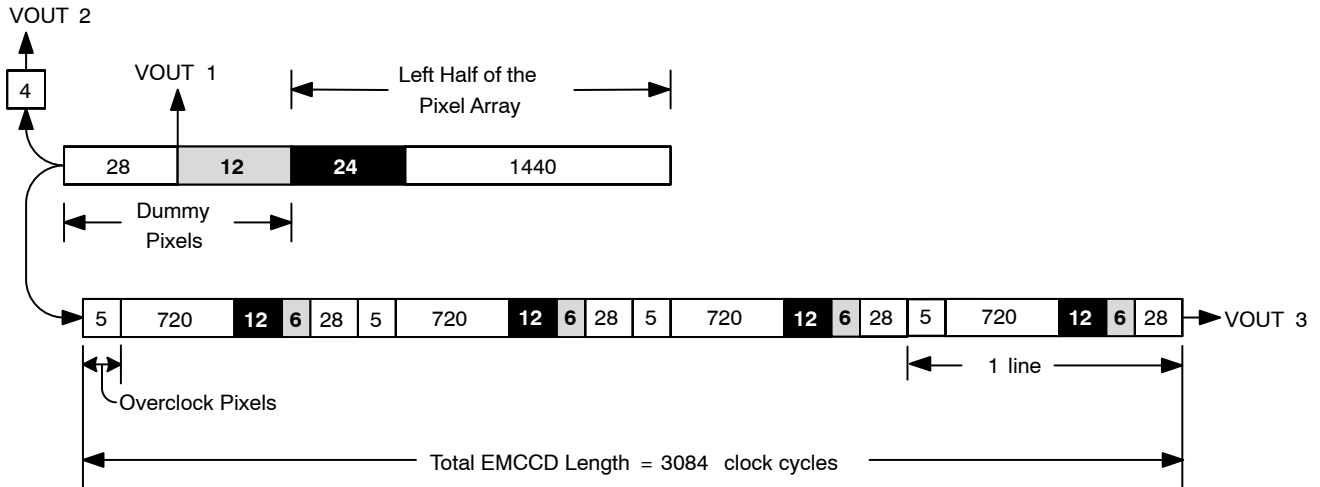
In 2X horizontal binning mode, the H1S, H2S, H1B, and H2B clocks are all run at 40 MHz. The binning occurs in the HCCD just before the VOUT1 floating gate amplifier. The timing of all other HCCD clocks are not changed. The HCCD and EMCCD clocks after VOUT1 continue to operate at 20 MHz. In Figure 4, the first photo-active pixel is shown arriving at VOUT1 after 18 (6 + 12) H2L clock cycles and 36 H2S clock cycles. The 28 dummy pixels after VOUT1 are not binned, only pixels before VOUT1. The first photo-active pixel arrives at VOUT2 after 50 (4 + 28 + 6 +

12) H2L clock cycles and 100 H2S clock cycles. The first photo-active pixel arrives at VOUT3 after 46 (28 + 6 + 12) H2L clock cycles and 92 H2S clock cycles. The pixels at VOUT3 are delayed by two lines relative to when pixels arrive at VOUT2. Every line must have exactly 1542 clock cycles to preserve the alignment of pixels within the EMCCD register. In Figure 5, it is shown that the pixels at VOUT3 are delayed by 4 lines relative to when pixels arrive at VOUT2. Every line must have exactly 771 clock cycles to preserve the alignment of pixels within the EMCCD register.

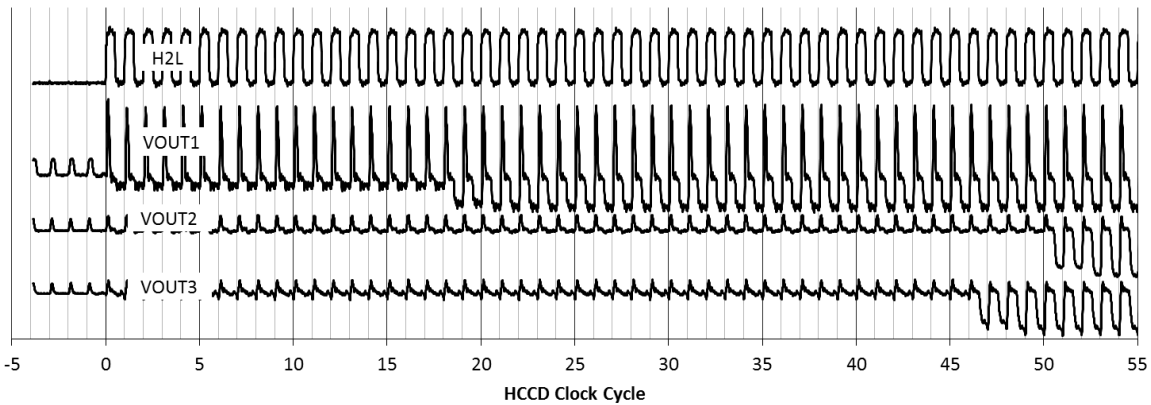
# AND9549/D



**Figure 4. The Alignment of Pixels Within the HCCD and EMCCD for 2X Horizontal Charge Binning When Transferring an Entire Line to the Left Side Outputs**



**Figure 5. The Alignment of Pixels Within the HCCD and EMCCD for 2X Horizontal Charge Binning When Transferring the Left Half of a Line to the A and C outputs and the Right Half of the Line to the B and D outputs**

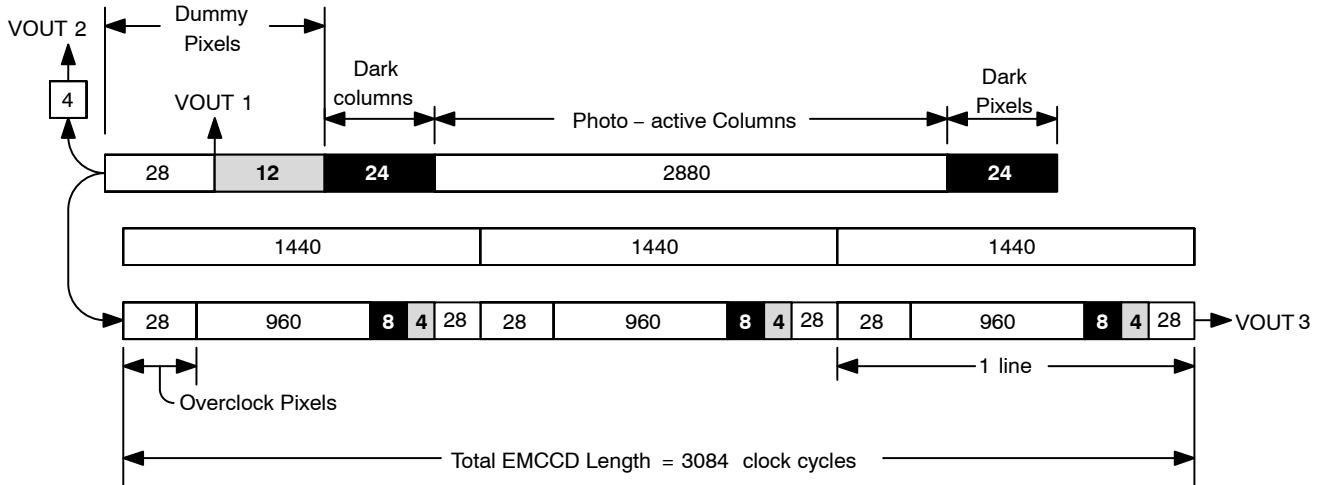


**Figure 6. The Video Output Waveforms at the Start of Each Line with 2X Horizontal Charge Binning, for 1, 2, or 4-Output Mode**

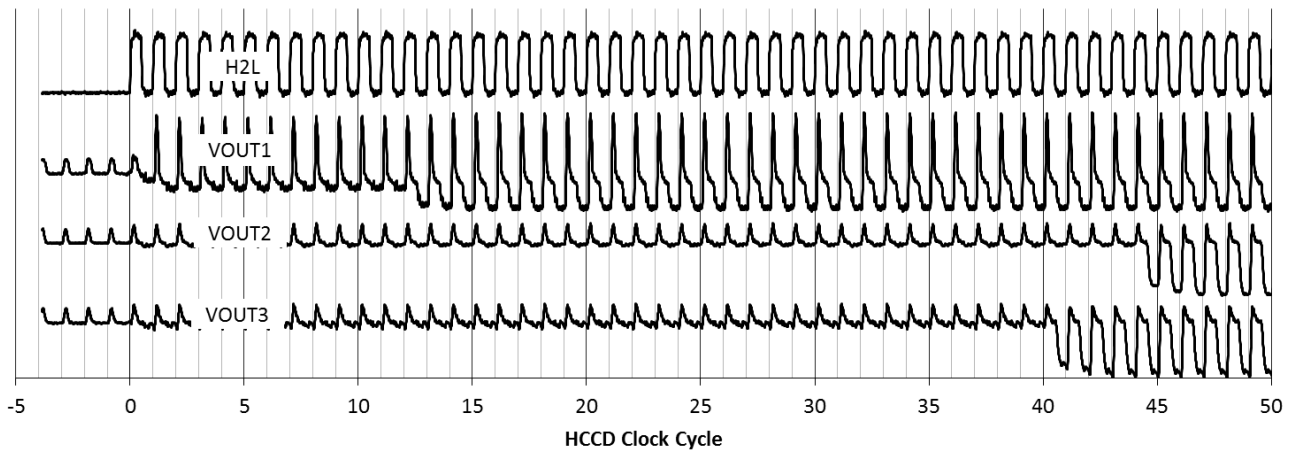
**3X Horizontal Charge Binning**

In 3X horizontal binning mode, the H1S, H2S, H1B, and H2B clocks are all run at 60 MHz. The timing of all other HCCD clocks is not changed. In this mode the HCCD cannot be operated split left/right. 6 half lines of charge cannot fit within the EMCCD register. Only 1 output mode or 2 output mode (split top/bottom) is possible. The first photo-active pixel arrives at VOUT1 after 12 (4 + 8) H2L clock cycles and 36 H2S clock cycles. The 28 dummy pixels after VOUT1 are

not binned, only pixels before VOUT1. The first photo-active pixel arrives at VOUT2 after 44 (4 + 28 + 4 + 8) H2L clock cycles and 88 H2S clock cycles. The first photo-active pixel arrives at VOUT3 after 40 (28 + 4 + 8) H2L clock cycles and 80 H2S clock cycles. The pixels at VOUT3 are delayed by 3 lines relative to when pixels arrive at VOUT2. Every line must have exactly 1028 clock cycles to preserve the alignment of pixels within the EMCCD register.



**Figure 7. The Alignment of Pixels Within the HCCD and EMCCD for 3X Horizontal Charge Binning When Transferring an Entire Line to the Left Side Outputs**

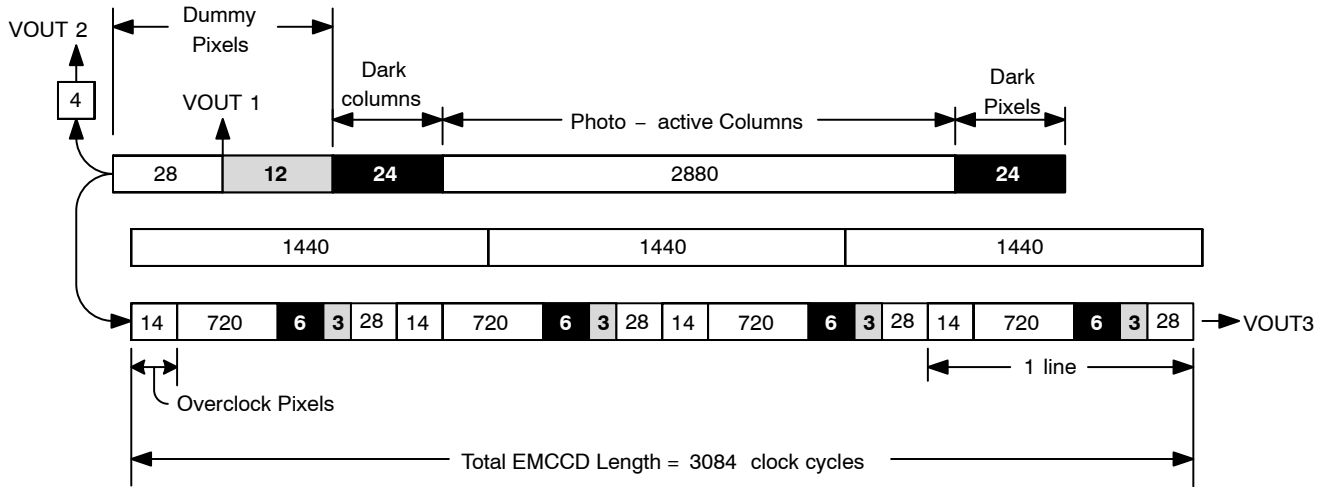


**Figure 8. The Video Output Waveforms at the Start of Each Line with 3X Horizontal Charge Binning, for 1 or 2-Output Mode**

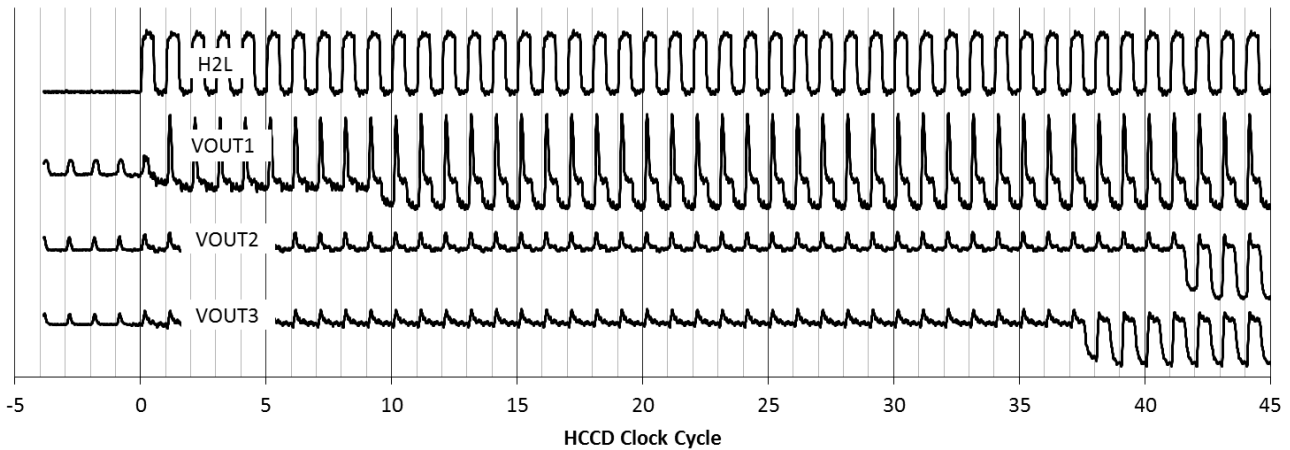
**4X Horizontal Charge Binning**

In 4X horizontal binning mode, the H1S, H2S, H1B, and H2B clocks are all run at 80 MHz. The timing of all other HCCD clocks is not changed. In this mode the HCCD cannot be operated split left/right. 8 half lines of charge cannot fit within the EMCCD register. Only 1 output mode or 2 output mode (split top/bottom) is possible. In Figure 9, it is shown that the first photo-active pixel arrives at VOUT1 after 9 (3 + 6) H2L clock cycles and 36 H2S clock cycles. The 28

dummy pixels after VOUT1 are not binned, only pixels before VOUT1. The first photo-active pixel arrives at VOUT2 after 41 (4 + 28 + 3 + 6) H2L clock cycles and 82 H2S clock cycles. The first photo-active pixel arrives at VOUT3 after 37 (28 + 3 + 6) H2L clock cycles and 74 H2S clock cycles. The pixels at VOUT3 are delayed by 3 lines relative to when pixels arrive at VOUT2. Every line must have exactly 771 clock cycles to preserve the alignment of pixels within the EMCCD register.



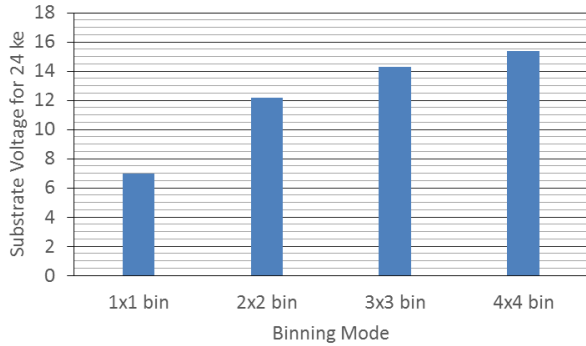
**Figure 9. The Alignment of Pixels Within the HCCD and EMCCD for 4X Horizontal Charge Binning When Transferring an Entire Line to the Left Side Outputs**



**Figure 10. The Video Output Waveforms at the Start of Each Line with 4X Horizontal Charge Binning, for 1 or 2-Output Mode**

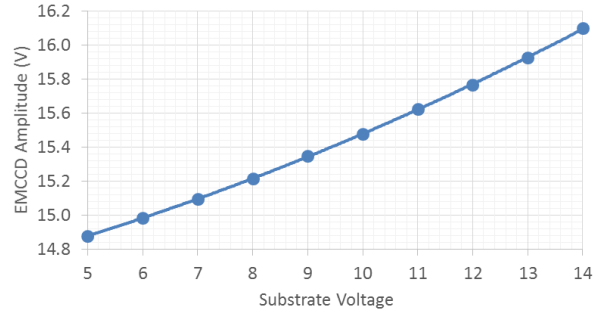
**Substrate Voltage**

To prevent horizontal or vertical blooming of the HCCD or VCCD the substrate voltage will need to be increased to limit the charge capacity of the photodiodes. For example, when binning 2 x 2 the photodiode charge capacity should be set to 5,000 electrons instead of 20,000 electrons. Figure 11 shows the required V<sub>SUB</sub> for the binning modes to produce a saturated signal of 24,000 electrons which has a linear portion up to 20,000 electrons. This represents data from one image sensor and is not necessarily the same for every image sensor. Each sensor has a V<sub>SUBREF</sub> pin that outputs the optimum V<sub>SUB</sub> voltage for no binning. The optimum V<sub>SUB</sub> voltage for the other binning modes must be determined for each sensor.

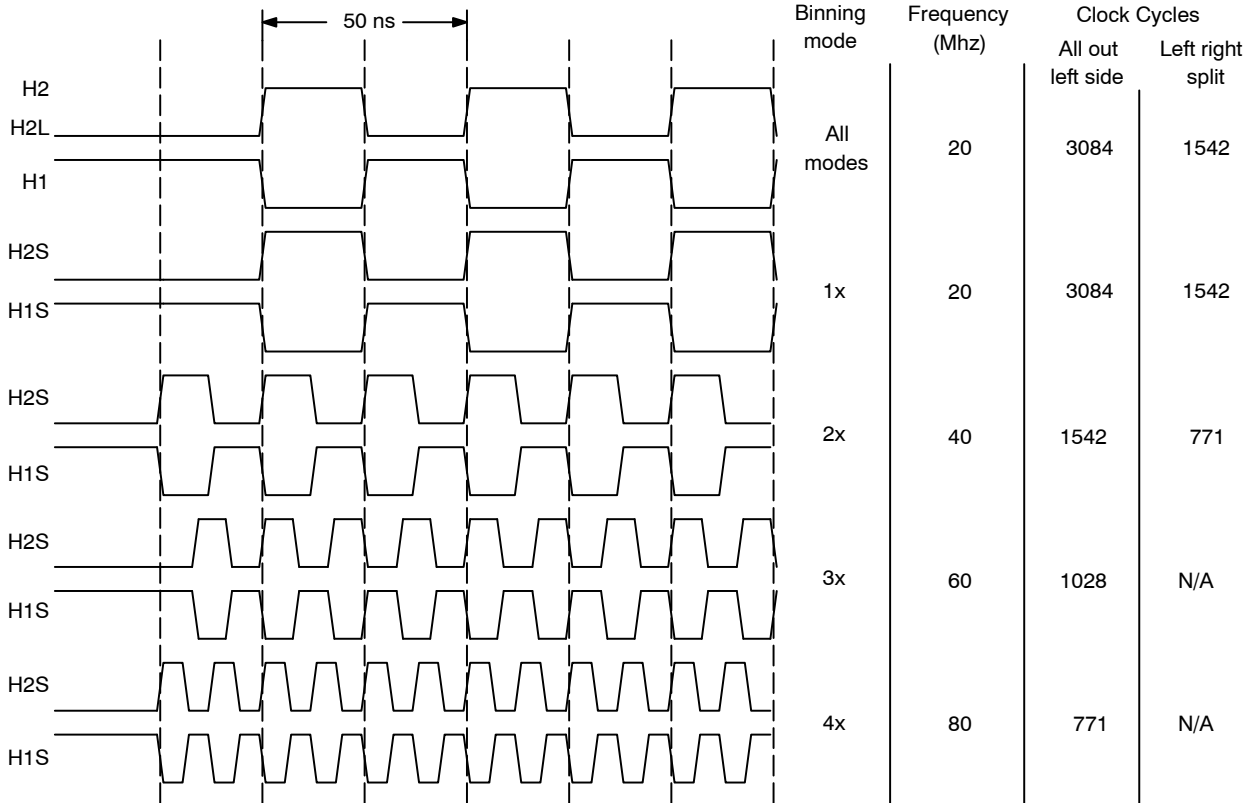


**Figure 11. Optimum V<sub>SUB</sub> voltage for each binning mode.**


Please be aware that the EMCCD gain is dependent upon substrate voltage. If the substrate voltage is changed the EMCCD voltage will have to be adjusted to maintain a particular gain setting from one binning mode to the next. See Figure 12 for an example of how EMCCD voltage must change to maintain a constant gain of 20x when the substrate voltage changes. Figure 12 represents data from one image sensor. There will be minor variations from one image sensor to the next.



**Figure 12. The EMCCD voltage required for 20x gain vs. substrate voltage.**



**Figure 13. The Timing of the HCCD Pins for all of the Charge Binning Modes**

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