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AND9528/D

Power Supply Sequence of LC823450 Series for Audio Applications

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APPLICATION NOTE

Introduction

This application note describes a guideline of power supply sequence for desired application.

Intended audience is customers who are building audio application using LC823450 Series (called LC823450 hereafter).

BACKGROUND

LC823450 has a lot of power supply terminals, which are roughly classified into the following six power supply groups according to their roles.

(1) Internal core power supply
(2) RTC power supply
(3) 1 V series analog power supply
(4) DAMP power supply
(5) External IO power supply
(6) 3 V series analog power supply

This application note describes power supply sequence about these power supply groups.

POWER SUPPLY SEQUENCE

Power supply terminals

Table 1 shows the power supply terminals of LC823450 including the relation to the power supply groups.

Table 1. Power supply terminals

Group	Symbol	Low operation (V)	High operation (V)	Note
(1) Internal core	Vdd1	0.93 - 1.27	1.1 - 1.27	
(2) RTC	VddRTC	0.9 - 1.1		
(3) 1 V series analog	VddXT1	0.93 - 1.3		For X'tal : 12 MHz, 20 MHz
		1.1 - 1.3		For X'tal : 12 MHz, 20 MHz, 24 MHz, 48 MHz
	AVddPLL1	0.93 - 1.3	1.1 - 1.3	
	AVddPLL2	0.9 - 1.3		
	AVddUSBPHY1	1.08 - 1.3		(*1)
	DVddUSBPHY1	1.08 - 1.3		(*1), (*3)
(4) DAMP	AVddDAMPL	0.93 - 1.65		(*2)
	AVddDAMPR	0.93 - 1.65		(*2)
(5) External IO	Vdd2	1.7 - 1.95		For 1.8 V interface
		2.7 - 3.6		For 3.3 V interface
	VddSD0	1.7 - 1.95		For 1.8 V interface
		2.7 - 3.6		For 3.3 V interface
	VddSD1	1.7 - 1.95		For 1.8 V interface
		2.7 - 3.6		For 3.3 V interface
	VddSD2	1.7 - 1.95		For 1.8 V interface
		2.7 - 3.6		For 3.3 V interface
	VddQSPI	1.7 - 1.95		For 1.8 V interface
		2.7 - 3.6		For 3.3 V interface
(6) 3 V series analog	AVddADC	2.7 - 3.6		
	AVddUSBPHY2	3.0 - 3.6		(*1)
	AVddPLL3	2.7 - 3.6		(*3), (*4)
Internal clock frequency (For Cortex-M3, LPDSP32, AHB, APB)		max 100 MHz	max 160 MHz	(*5)

Ta = -20°C to +65°C

(*1) While USB is used (including USB suspend mode).
(*2) While the terminal is used not as GPO (general purpose output) but as headphone amp.
(*3) There are some packages where the terminal is not assigned in LC823450 series.
(*4) PLL3 should not be used as audio PLL if PLL2 is available.
(*5) When the clock is over 100 MHz, internal ROM needs wait control for Cortex-M3 and LPDSP32.

The Low operation item in the table means an operating condition that the internal clock frequency can work up to 100 MHz. In contrast, the High operation item means one that the internal clock frequency can work up to 160 MHz. Vdd1 is the power supply terminal of the internal digital core and AVddPLL1 is that of the system PLL. If you want to give low power consumption to LC823450, in order to work LC823450 with the low operating condition, it is appropriate to supply lower voltage than 1.1 V within the table (for example, 1.0 V) to Vdd1 and AVddPLL1. If you want to give high performance to LC823450, in order to work LC823450 with the high operating condition, it is appropriate to supply higher voltage than 1.1 V within the table (for example, 1.2 V) to Vdd1 and AVddPLL1.

VddXT1 is the power supply terminal of X'tal oscillation. According to the frequency of X'tal oscillation which you use, the available voltage range of VddXT1 is different. If you want to use over 20 MHz X'tal oscillation (24 MHz or 48 MHz), it is necessary to supply higher voltage than 1.1 V within the table (for example, 1.2 V) to VddXT1. In addition, any frequencies other than 12 MHz, 20 MHz, 24 MHz or 48 MHz are not acceptable to LC823450 because they may cause function errors during ROM boot.

There are two audio PLL functions, PLL2 and PLL3. AVddPLL2 is the power supply terminal of PLL2 and AVddPLL3 is that of PLL3. Either PLL2 or PLL3 can be used as an audio PLL function, but it is desired to use PLL2 because of low power consumption by low voltage use. Therefore, if PLL2 is available in the package which you use, you should use only PLL2. In this case, since PLL3 is not used, you should open the AVddPLL3 and VCNT3 terminals for PLL3 electronically.

All the power supply terminals of LC823450 except AVddPLL3 have to be supplied with their regulated voltage listed in the table even if some of the functions related to each power supply terminal are not used in your

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application. For example, even if RTC is not used, VddRTC has to be supplied with its regulated voltage. Even if 10-bit ADC is not used, VddADC has to be supplied with its regulated voltage.

There are five power supply terminals in the External IO group. They can be individually supplied with two kinds of the voltage interface based on the application. One is for 1.8 V IO interface and the other is for 3.3 V IO interface.

Power supply sequence

At first, the basic power supply sequence is the following order (1, 2, 3). In addition, simultaneous power supply on or off is acceptable.

When powering on:

1. Powering on the internal power supply terminals
2. Powering on the external I/O power supply terminals
3. Giving signals to the external I/O terminals

When powering off:

1. Removing signals from the external I/O terminals
2. Powering off the external I/O power supply terminals
3. Powering off the internal power supply terminals

Powering on the external I/O power supply terminals while the internal power supply terminals are not supplied might cause some glitches on the I/O signals and some flow of through current inside. To avoid it, the sequence above is recommended as the basic sequence.

Figure 1 shows the power supply sequence of LC823450. The Rise Timing period is shown as Rn mark and the Fall Timing period is shown as Fn mark in Figure 1.

Vdd1 is the internal core power supply terminal, so Vdd1 has to be powered on at first. VddRTC is the RTC power supply terminal. The RTC block can become independent electrically at General RTC mode or Keyint RTC mode. In these modes, all power domains except the RTC power domain can be powered off by controlling the external regulators while the RTC timer works correctly. VddRTC also has to be powered on at first. The timing relation between Vdd1 and VddRTC doesn't have any constraint (R1), because VddRTC is an independent power supply terminal.

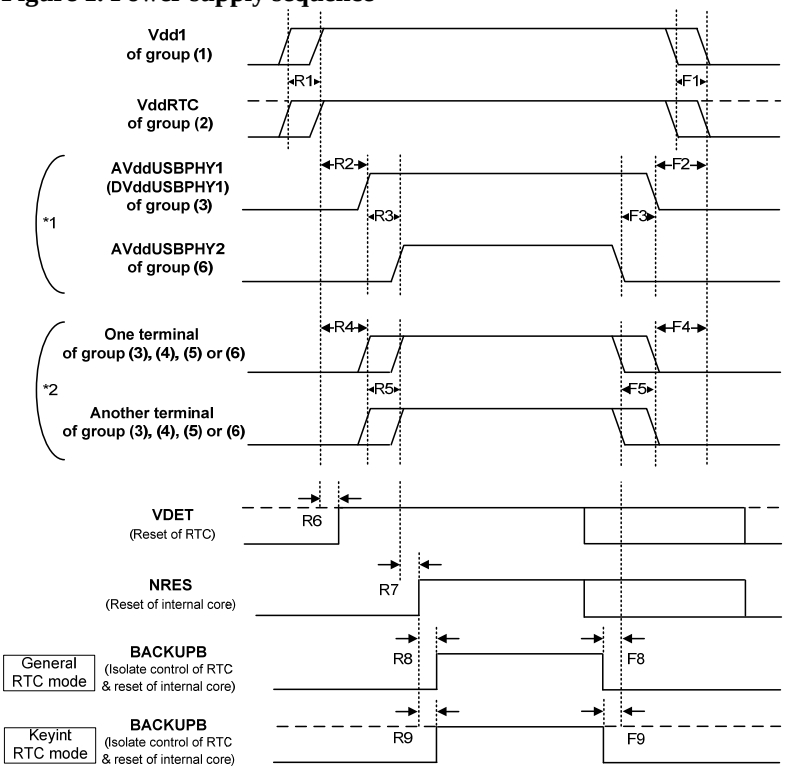
After powering on both Vdd1 and VddRTC, the other power supply terminals (*1, *2) have to be powered on within max 100 ms (R2, R4). Except the timing relation (*1) that AVddUSBPHY2 has to be powered on after AVddUSBPHY1 (and DVddUSBPHY1) within max 100 ms (R3), the timing relation among the other power supply terminals (*2) doesn't have any constraint (R5).

Of course, simultaneous power supply on of R1, R2, R3, R4 and R5 is acceptable.

As for powering off, the power supply terminals need to be powered off to keep the basic power supply sequence as shown in Figure 1 (F1, F2, F3, F4 and F5).

Simultaneous power supply off of F1, F2, F3, F4 and F5 is acceptable as well.

Figure 1. Power supply sequence



Group	Symbol
(1) Internal core	Vdd1
(2) RTC	VddRTC
(3) 1 V series analog	VddXT1
	AVddPLL1
	AVddPLL2
	AVddUSBPHY1
	DVddUSBPHY1
(4) DAMP	AVddDAMPL
	AVddDAMPR
(5) External IO	Vdd2
	VddSD0
	VddSD1
	VddSD2
	VddQSPI
(6) 3 V series analog	AVddADC
	AVddUSBPHY2
	AVddPLL3

Rise Timing	Fall Timing	Min	Max
R1, R5	F1, F5	There is no constraint.	
R2, R3, R4	F2, F3, F4	0 ms	100 ms
R6, R7	-	10 µs	-
R8, R9	F8, F9	0 ns	-

Note: *2 shows any combinations between two power supply terminals in the group (3), (4), (5) or (6) except the combination of *1.

VDET is the reset of RTC and active low. It has to be released to high level after low level is given to it for at least 10 μs after VddRTC is powered on and while it is supplied (R6).

NRES is the main reset of the internal core and active low. It also has to be released to high level after low level is given to it for at least 10 μs after all power supply terminals are powered on and while they are supplied (R7).

BACKUPB is the isolate control terminal which means that all power domains except the RTC power domain can be powered off. When it is low level, the RTC power domain is separated from the other power domains electrically and the internal core is reset. When it is high level, both of the domains are connected electrically.

In General RTC mode, when you want to power off the power domains except RTC, you have to control the timing of BACKUPB correctly as shown in Figure 1. BACKUPB has to be released to high level after NRES is released to high level at powering on (R8), and then, it has to be set to low level before any one of the power domains except RTC is powered off (F8). In other words, the power domains except RTC can be powered off while BACKUPB is low level, and they have to continue being supplied while BACKUPB is high level.

In Keyint RTC mode, LC823450 has an internal isolate control signal inside generated by a sequencer in the RTC block, and the isolation is controlled by the internal isolate control signal as well as BACKUPB. The sequencer can control the isolation of the power domains automatically even when power supply voltage is supplied to LC823450 at first, so it is usually suitable to fix BACKUPB to the high level as shown in the broken line. However, when you need to control the isolation from outside of LC823450 with no relation to the internal sequencer, for example, when you exchange the buttery to new one with a short time while RTC needs to work precisely, BACKUPB have to be controlled as shown in the solid line as well as General RTC mode (R9, F9).

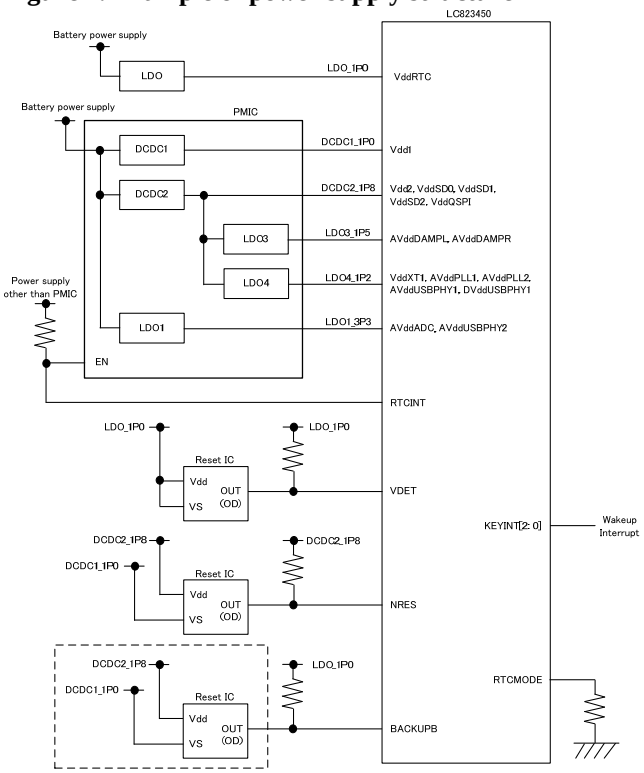
Example of power supply voltage

Table 2 shows an example of power supply voltage for LC823450. The voltage setting is suitable to the low operation condition for low power consumption. Figure 2 shows an example of power supply structure according to Table 2 with Keyint RTC mode.

Table 2. Example of power supply voltage

Group	Symbol	Voltage (V)	Supply source	Note
(1) Internal core	Vdd1	1.0	DCDC1	
(2) RTC	VddRTC	1.0	LDO	
(3) 1 V series analog	VddXT1	1.2	LDO4 (supplied by DCDC2)	For X'tal : 12 MHz, 20 MHz, 24 MHz, 48 MHz
	AVddPLL1	1.2		
	AVddPLL2	1.2		
	AVddUSBPHY1	1.2		
	DVddUSBPHY1	1.2		For available package
(4) DAMP	AVddDAMPL	1.5	LDO3 (supplied by DCDC2)	
	AVddDAMPR	1.5		
(5) External IO	Vdd2	1.8	DCDC2	For 1.8 V interface
	VddSD0	1.8		For 1.8 V interface
	VddSD1	1.8		For 1.8 V interface
	VddSD2	1.8		For 1.8 V interface
	VddQSPI	1.8		For 1.8 V interface
(6) 3 V series analog	AVddADC	3.3	LDO1	
	AVddUSBPHY2	3.3		
	AVddPLL3	-	-	Not supplied (Open)

Figure 2. Example of power supply structure



In this example, two DCDC converters and four LDOs are used for the power supply terminals of LC823450. The battery is connected to DCDC1, DCDC2, LDO and LDO1 as a power supply source, and then DCDC2 is connected to LDO3 and LDO4 as a power supply source to save the battery current consumption as much as possible. The DCDCs and LDOs supply the power supply terminals as shown in Table 2 with each voltage.

PMIC in Figure 2 has DCDCs and LDOs other than LDO for RTC group (2) with an enable pin. The enable pin is controlled to power on/off by RTCINT terminal at Keyint RTC mode with a pull up resistor tied to any power supply other than the power supply that PMIC generates.

LDO for RTC has to continue supplying voltage to VddRTC independently at Keyint RTC mode so as to power off all the power supply terminals except VddRTC.

At Keyint RTC mode, for example, if you need to exchange the buttery to new one with a short time while RTC needs to work precisely, the rectangle part surrounded by the broken line at BACKUPB in Figure 2 needs to be implemented.

In contrast, if you don't have to exchange the buttery to new one, the rectangle part with the broken line doesn't need to be implemented and it is appropriate that BACKUPB is just tied with a pull up resister to the power supply for VddRTC.

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