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AND9466/D

X'tal selection & PLL setting of LC823450 Series for Audio Applications

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APPLICATION NOTE

Introduction

This application note describes the X'tal (XT1) selection and PLL setting for desired application.

Intended audience is customers who are building audio application using LC823450 Series (called LC823450 hereafter).

BACKGROUND

LC823450 has three oscillators and two PLLs inside.

Three oscillators are RC OSC (1MHz, typical), XTRTC OSC (32.768kHz) and XT1 OSC (1-50MHz). RC OSC is internal RC oscillator for initial operation after reset. XTRTC is 32.768KHz X'tal oscillator for RTC (Real Time Clock). XT1 OSC is X'tal oscillator for main operation. And BASIC clock as fundamental clock for CPU, bus system, internal memories and so on can be generated from RC, XTRTC or XT1 depending on the situation.

Two PLLs are PLL1 for system clock and PLL2 for audio clock. By controlling of the register configuration for these, the suitable clocks for system block and audio block are generated respectively. We can provide the software stack including Middleware with Application Interface (API) to control these H/W modules without accessing to their registers directly.

This application note describes the selection of the XT1, PLL1 setting for system clock and PLL2 setting for audio clock.

X'tal (XT1) selection

The oscillation frequency of XT1 depends on the power supply voltage for XT1 (VddXT1). Table1 shows the characteristics of XT1 OSC.

Table1. Characteristics of XT1 OSC

Item	VddXT1 = 0.93 to 1.1V			VddXT1 = 1.1 to 1.3V			Unit
	Min	Typ	Max	Min	Typ	Max	
Frequency	1		20	1		50	MHz
Time for Xtal Stable			3 (*1)			3 (*1)	ms

Vdd1(*2) = 0.93 to 1.27V, Ta = -20°C to +65°C

(*1) Just reference value under Ta=25°C, and need to adjust to customer board situation.

(*2) Power up and power down timing of VddXT1 and Vdd1 should be as close as possible.

When VddXT1 is 0.93 to 1.1V, the maximum oscillation frequency of XT1 is limited to 20MHz or less. In contrast, when VddXT1 is 1.1 to 1.3V, the maximum one is extended to 50MHz. In this case, the power supply voltage for LOGIC (Vdd1) can choose 1.0V typical in addition to 1.2V typical.

The variation of available frequency of XT1 is prescribed by the demand of function as Table 2. For example, only 48MHz is available for USB Host function.

Table2. Variation of available frequency of XT1

Function	12MHz	20MHz	24MHz	48MHz	other
XTALINFO[1:0]	"01"	"10"	"00"	"11"	"XX"
USB Device(*1)	✓	✓	✓	✓	
USB Host(*1)				✓	
ROM boot	✓	✓	✓	✓	(*2)

(*1)The requirements of XT1 are below to use USB function.
- Frequency tolerance:±200ppm or less
- Jitter:±50ps or less

(*2)Frequency other than 12, 20, 24, 48MHz may cause functional error in ROM boot.

LC823450 has two terminals XTALINFO[1:0] to set the frequency of connected XT1 outside. XTALINFO[1:0] terminal should be set in accordance with the frequency of XT1 as above Table2. Some products which don't have XTALINFO[1:0] terminal, they are set internally in accordance with the prescribed frequency of XT1. The frequency of XT1 other than 12, 20, 24, 48MHz may cause functional error during ROM boot, because some internal clock frequencies are determined automatically according to the XTALINFO[1:0] input and connected XT1 frequency .

Instead of using a crystal, you can use the external clock signal through XIN1 terminal with unconnected XOUT terminal which is generated by some oscillation module outside of LC823450. However, the XT1 oscillator is supposed to be used with quartz resonator or ceramic resonator, we have no plan to evaluate the case of external clock signal input.

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PLL1 Setting

The source of system clock can be selected from one of four clocks, RC OSC, XTRTC OSC, XT1 OSC and PLL1.

Table3 shows the characteristics of PLL1. The range of PLL1 oscillation frequency (VCO oscillation frequency) is dependent on AVddPLL1 supply voltage.

Table3. PLL1 Characteristics

Item	condition	AVddPLL1 0.93 to 1.1V			AVddPLL1 1.1 to 1.3V			Unit
		Min	Typ	Max	Min	Typ	Max	
VCO highest oscillation frequency		200			360			MHz
VCO lowest oscillation frequency				90			180	MHz
Phase comparison frequency (Fref)				48			48	MHz
PLL lock time(*1)	Fref >= 32.768KHz		38	52		38	52	ms
	Fref >= 1MHz		3.5	5		3.5	5	ms

Vdd1(*2) = 0.93 to 1.27V, Ta = -20°C to +65°C

(*1) PLL lock time depends on Phase comparison frequency(Fref).

(*2) Power up and power down timing of AVddPLL1 and Vdd1 should be as close as possible.

When PLL1 is selected as the system clock source, there is one division just after PLL1 output, then the system clock is 1/2 or 1/4 of VCO oscillation frequency. Table4 shows the range of internal clock frequency. There is a frequency limit depending on Vdd1 voltage supply, maximum clock at Vdd1 = 0.93 to 1.1V is up to 100MHz while one at Vdd1 = 1.1 to 1.3V is up to 160MHz.

Table4. Internal clock frequency

Clock Frequency	Vdd1= 0.93 to 1.1V			Vdd1= 1.1 to 1.3V			Unit
	Min	Typ	Max	Min	Typ	Max	
Cortex-M3 DSP	0		100	0		160 (*1)	MHz
AHB	0		100	0		160	MHz
APB	0		100	0		160	MHz

(*1) The clock of Cortex-M3 and DSP are over 100MHz, 1 cycle wait is required to access internal ROM.

In addition, there is another consideration about decision of the system clock. For example, the function clock for SD I/F, SDCLK0 is generated from the system clock, but the division ratio are 1/1, 1/2, 1/4 and so on, while the maximum frequency of SDCLK0 is limited to 45MHz. If you use the maximum frequency for SDCLK0, you have to set the system clock to 90MHz as the fastest. On the other hand, if you set the maximum frequency for system clock, you have to use SDCLK0 at 40MHz as the fastest.

You can divide the internal clock frequency depending on each applications by another division even if it is used as the system clock continuously. Therefore, LC823450 can do an intermittent action of change the frequency to reduce the current consumption with appropriate frequency suitable for each applications.

PLL2 Setting

Normally, audio clock uses PLL2 output as the clock source. PLL2 can generates required clock based on various sampling frequencies depending on the audio application. Table5 shows the variation of audio clock and PLL settings. Phase comparison frequency (Fref) and Division and Multiply ratio corresponding to XT1 frequency are determined for each required Sampling frequency (Fs).

Table 5. XT1 selection and Sampling frequency

XT1 frequency	VCO frequency (*1)	Sampling frequency (Fs)	PLL2 Devision ratio	PLL2 Multiply ratio	Phase comparison frequency (Fref)
12MHz	147.456MHz	12/24/48/ 96/192KHz	125	1536	96KHz
	135.4752MHz	11.025/22.05/44.1/ 88.2/176.4KHz	625	7056	19.2KHz
	98.304MHz	8/16/32/ 64/128KHz	125	1024	96KHz
20MHz	147.456MHz	12/24/48/ 96/192KHz	625	4608	32KHz
	135.4752MHz	11.025/22.05/44.1/ 88.2/176.4KHz	3125	21168	6.4KHz
	98.304MHz	8/16/32/ 64/128KHz	625	3072	32KHz
24MHz	147.456MHz	12/24/48/ 96/192KHz	125	768	192KHz
	135.4752MHz	11.025/22.05/44.1/ 88.2/176.4KHz	625	3528	38.4KHz
	98.304MHz	8/16/32/ 64/128KHz	125	512	192KHz
48MHz	147.456MHz	12/24/48/ 96/192KHz	125	384	384KHz
	135.4752MHz	11.025/22.05/44.1/ 88.2/176.4KHz	625	1764	76.8KHz
	98.304MHz	8/16/32/ 64/128KHz	125	256	384KHz

(*1)VCO frequency = 768 x Highest Fs

Phase comparison frequency (Fref) and VCO oscillation frequency have limits as described in Table6.

Table 6. PLL2 Characteristics

Item	condition	AVddPLL2 0.93 to 1.3V			Unit
		Min	Typ	Max	
VCO highest oscillation frequency		150			MHz
VCO lowest oscillation frequency				95	MHz
Phase comparison frequency (Fref)				1	MHz
PLL lock time(*1)	Fref >= 6.4KHz		37	50	ms
	Fref >= 38.4KHz		14	20	ms

Vdd1(*2) = 0.93 to 1.27V, Ta = -20°C to +65°C

(*1) PLL lock time depends on Phase comparison frequency(Fref).
-Fref>=6.4KHz is in the case when XT1 is one of 12,20,24,48 MHz.
-Fref>=38.4KHz is in the case when XT1 is 24 MHz.

(*2) Power up and power down timing of AVddPLL2 and Vdd1 should be as close as possible.

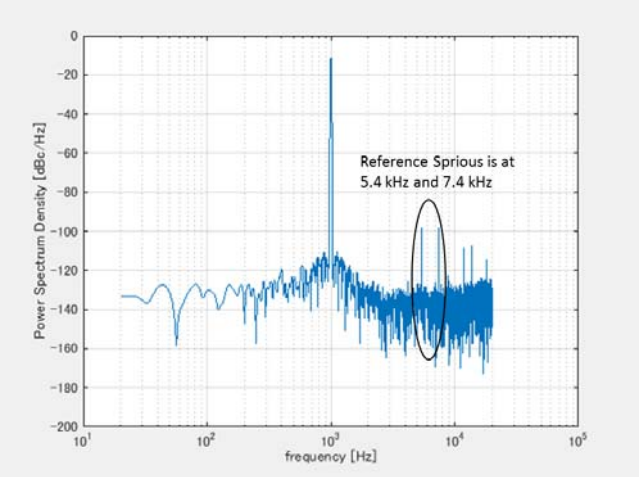
In PLL2, the relation of input XT1 frequency and output VCO frequency is as follows.

$$\text{Phase comparison frequency (Fref)} = \frac{\text{Input XT1 frequency}}{\text{Division ratio}}$$

$$\text{Output VCO frequency} = \text{Phase comparison frequency (Fref)} \times \text{Multiply ratio}$$

Especially, Fref becomes lowest at the combination of XT1 is 20MHz and Sampling frequency is 44.1KHz. Generally, if Fref becomes lower, negative influences on sound quality are caused while PLL lock time also becomes longer. For example, when you use the PLL output for DAC with 20MHz XT1 and 6.4KHz Fref, the simulation result of audio output spectrum is shown like below chart of Figure1.

Figure 1. Reference spurious to 1KHz audio signal



XT1:20MHz, Fref:6.4KHz, Fvco:135.475MHz

The spurious to 1KHz audio signal input occurs at 5.4KHz and 7.4KHz which is in audible range. Thus, when Fref is low and inside of audible range, some spurious of audio output will occur in audible range, and then you may hear it as a noise. Therefore, we recommend you to select another XT1 frequency or another Sampling frequency to raise Fref higher, if you can. Especially, since LC823450 has Synchronous and Asynchronous SRC (Sampling Rate Converter), you can convert to suitable frequency which has higher Fref.

On the other hand, when you select XT1 with higher frequency and/or you use the XT1 with higher voltage supply for VddXT1, current consumption of XT1 oscillator tend to increase.

As described above, it is necessary to consider carefully about X'tal selection and PLL setting depending on your application.