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How to Use Auxiliary Winding Voltage for Biasing the NCP1602 CSZCD Pin

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APPLICATION NOTE

NCP1602 combines the current sense (CS) and the core demagnetization detection (ZCD, zero crossing detection) signals into a single pin named CSZCD. In some noisy environment, a non-optimum choice of sensing resistors combined with a dense PCB layout can lead to a unstable operation of 1602. In this particular situation, the adoption of a more conventional way of sensing via a dedicated winding is an advantageous solution bringing ease of implementation and stronger noise immunity.

This application note describes how the NCP1602, primarily designed to work without the need of an auxiliary voltage for ZCD detection, can use the auxiliary voltage for a better CSZCD pin immunity to noise.

Drain Connection for CSZCD Pin (Sensitivity to PCB Parasitics)

When trying to reduce the no-switching standby consumption current by increasing (above 1 MΩ) the impedance (R_{CS1} + R_{CS2}) of the CSZCD bridge connected between the drain and the source of the power MOSFET (see Figure 1), the sensitivity of the CSZCD pin to PCB parasitic capacitors is increased, leading in some cases to non-functionality caused for example by a constant false triggering of OCP (Over Current Protection) or OVP (Over Voltage Protection). This is due to the fact that the CSZCD voltage is distorted and internal circuitry cannot work as intended. Recommendations for avoiding such CSZCD pin sensitivity are given in [1].

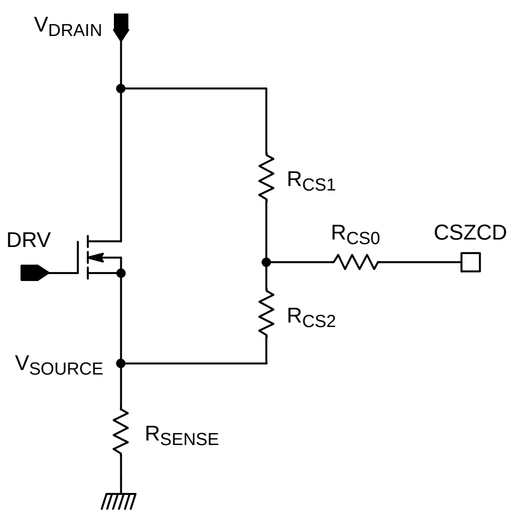

Figure 1. CSZCD Connection without Auxiliary Winding

Auxiliary Winding Circuit for CSZCD Pin (to Avoid Sensitivity to PCB Parasitics)

To avoid pin CSZCD sensitivity, the circuitry shown in Figure 2 can replace the original circuitry of Figure 1. There is no V_{AUX} voltage reflected by the auxiliary winding when the part does not switch and, consequently, no current is flowing through the R_{CS} resistors so the standby current is not affected by R_{CS} resistors. The total resistance value of the R_{CS} bridge can then be set under the 1-MΩ limit originally set to avoid PCB parasitic capacitances and distortion of the CSZCD voltage signal. When an auxiliary winding voltage is available, the circuitry of Figure 2 is then preferred especially in applications where very low standby consumption is important. The only drawback of Figure 2 circuitry is that product options including brown-out detection cannot be used because the controller cannot start switching in this configuration. The reason of this non-functionality is that the brown-out high level can never be reached for allowing the controller to start switching because switching activity is needed for the brown-out level to be sensed through the CSZCD pin.

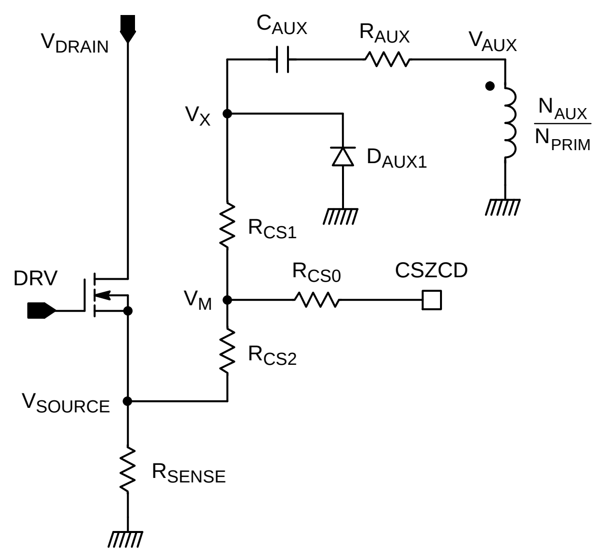

Figure 2. CSZCD Connection with Auxiliary Winding

Calculations of Component Values Used in CSZCD Circuitry

The CSZCD pin has originally been designed to work with the information contained in the instantaneous drain-source voltage (case of R_{CS1} connected to power MOSFET drain as shown in Figure 1). For the CSZCD pin to work when R_{CS1} is not connected to the power MOSFET drain but to V_X node (see Figure 2), the V_X node (which name also represents the voltage between this node and GND) must be proportional to the instantaneous power MOSFET drain voltage V_{DRAIN}. Let's analyze the waveforms corresponding to Figure 2 schematic.

During the on-time, V_{AUX} voltage is given by:

$$V_{AUX} = -V_{IN} \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 1)}$$

Where V_{IN} is the rectified mains voltage, right after the diode rectifier bridge, N_{AUX} & N_{PRIM} are respectively the number of turns of auxiliary and primary windings of the transformer which primary inductor serves as the PFC boost inductor.

During the demagnetization time, V_{AUX} voltage is given by:

$$V_{AUX} = \left(V_{OUT} - V_{IN}\right) \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 2)}$$

During the dead-time, V_{AUX} voltage is given by:

$$V_{AUX} = V_{DRAIN,AC} \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 3)}$$

Where $V_{DRAIN,AC}$ is equal to $V_{DRAIN} - V_{IN}$ (during dead-time V_{DRAIN} is ringing around its mean value which is equal to V_{IN}).

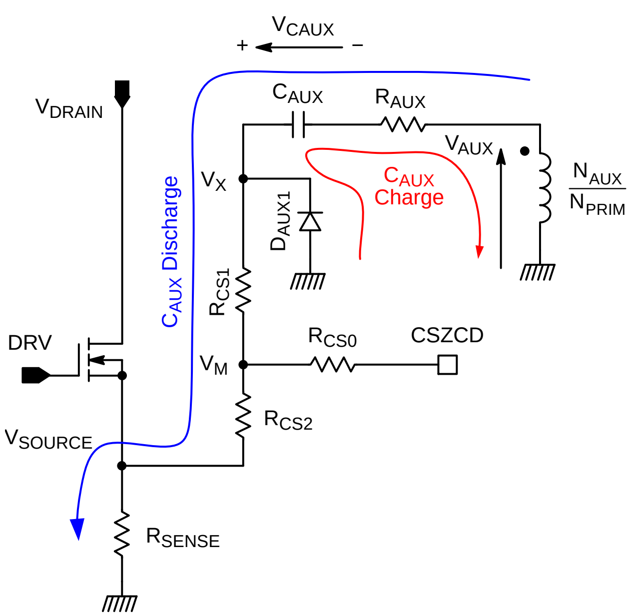

Figure 3. Charge and Discharge of C_{AUX} Capacitor

During the on-time, capacitor C_{AUX} is quickly charged (see Figure 3) through the low value resistor R_{AUX} to a voltage value V_{CAUX} given by:

$$V_{CAUX} = V_{IN} \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 4)}$$

The capacitor can only charge up to a greater value given by Equation 4 so it means that the end of one switching cycle, the voltage across C_{AUX} must be such as V_X voltage is slightly negative so during the following on-time C_{AUX} can be charged at the value given by Equation 4. We can also mention that the voltage drop across D_{AUX1} has been neglected to keep simple equations.

During the on-time, by combining Equation 1 and Equation 4 we get:

$$V_X = V_{AUX} + V_{CAUX} = 0 = V_{DRAIN,INST} \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 5)}$$

Because $v_{DS}(t)$ during the on-time is equal to zero.

During the demagnetization time, by combining Equation 2 and Equation 4 we get:

$$V_X = V_{AUX} + V_{CAUX} = V_{OUT} \cdot \frac{N_{AUX}}{N_{PRIM}} = V_{DRAIN,INST} \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 6)}$$

During the dead-time, by combining Equation 3 and Equation 4 we get:

$$V_X = V_{AUX} + V_{CAUX} = \left(V_{IN} + V_{DRAIN,AC}\right) \cdot \frac{N_{AUX}}{N_{PRIM}} = V_{DRAIN,INST} \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 7)}$$

We just have demonstrated that, during on-time, demagnetization time and dead-time, which means whatever time we have:

$$v_X(t) = v_{DRAIN}(t) \cdot \frac{N_{AUX}}{N_{PRIM}} \qquad \text{(eq. 8)}$$

So $v_X(t)$ is a scaled down (by N_{AUX} / N_{PRIM} which is auxiliary to primary turns ratio) version of $v_{DRAIN}(t)$.

$v_X(t)$ acts as a scaled down instantaneous drain voltage and is then divided by the resistor bridge made with R_{CS1} and R_{CS2}. In order to have the same voltage waveform on CSZCD pin as when R_{CS} divider was directly connected to the power MOSFET drain, the resistor divider ratio must be lowered.

With R_{CS1} connected to drain voltage, the design equation to get R_{CS1} and R_{CS2} is:

$$\frac{R_{CS1} + R_{CS2}}{R_{CS2}} = K_{CS} = 138 \qquad \text{(eq. 9)}$$

Now with R_{CS1} connected to V_X node, the design equation to get R_{CS1} and R_{CS2} is:

$$\left(\frac{N_{AUX}}{N_{PRIM}}\right)^{-1} \cdot \frac{R_{CS1} + R_{CS2}}{R_{CS2}} = K_{CS} = 138 \qquad \text{(eq. 10)}$$

For both cases and dictated by internal circuitry, K_{CS} must be as close as possible to 138 target value, within ±10% and R_{CS2} not being allowed to be under 20 kΩ, it is advised to set it to the normalized value of 22 kΩ. It is also advised to use 1% tolerance resistors for R_{CS1} and R_{CS2} as they are, with internal voltage references, setting the line level detection, the OVP2 (Second Over-Voltage protection), R_{CS0} value is set using the following design equation:

$$\left[\left(R_{CS1} // R_{CS2}\right) + R_{CS0}\right] \cdot 10\ \text{pF} = 500\ \text{ns} \qquad \text{(eq. 11)}$$

Where 10 pF is the parasitic input capacitance of the CSZCD pin and 500 ns the time constant of an internal zero. This zero is there to cancel the un-wanted pole made by associating the R_{CS} resistors with the parasitic input capacitance of the CSZCD pin (10 pF).The internal zero ensures a non-distorted CSZCD voltage signal.

Let's Explain C_{AUX} Capacitor Calculation

The C_{AUX} capacitor charges up during on-time to $((N_{AUX} / N_{PRIM}) \cdot V_{IN})$ minus a D_{AUX} diode V_f and while V_{IN} is rising. It is recommended for D_{AUX} to use a signal diode like the 1N4148. C_{AUX} is charging very fast cycle by cycle because R_{AUX} and C_{AUX} values are chosen so that their time constant equals 100 ns. As can be seen on Figure 4 when V_{IN} is decreasing and the C_{AUX} discharge is not fast enough, the voltage across C_{AUX} cannot track $((N_{AUX} / N_{PRIM}) \cdot V_{IN})$ versus time. The absolute value of C_{AUX} voltage discharge slope when $v_{IN}(t)$ is decreasing must be greater than the slope of $((N_{AUX} / N_{PRIM}) \cdot v_{IN}(t))$ and while the equations are too complex to be shown here, the following design Equation 12 for determining C_{AUX} value can be used.

$$\left(R_{CS1} + R_{CS2}\right) \cdot C_{AUX} = 640\ \mu\text{s} \pm 10\% \qquad \text{(eq. 12)}$$

Once C_{AUX} value is calculated, R_{AUX} is calculated using the following equation which allows the C_{AUX} capacitor to be fully charged during on-time:

$$R_{AUX} \cdot C_{AUX} = 100\ \text{ns} \qquad \text{(eq. 13)}$$

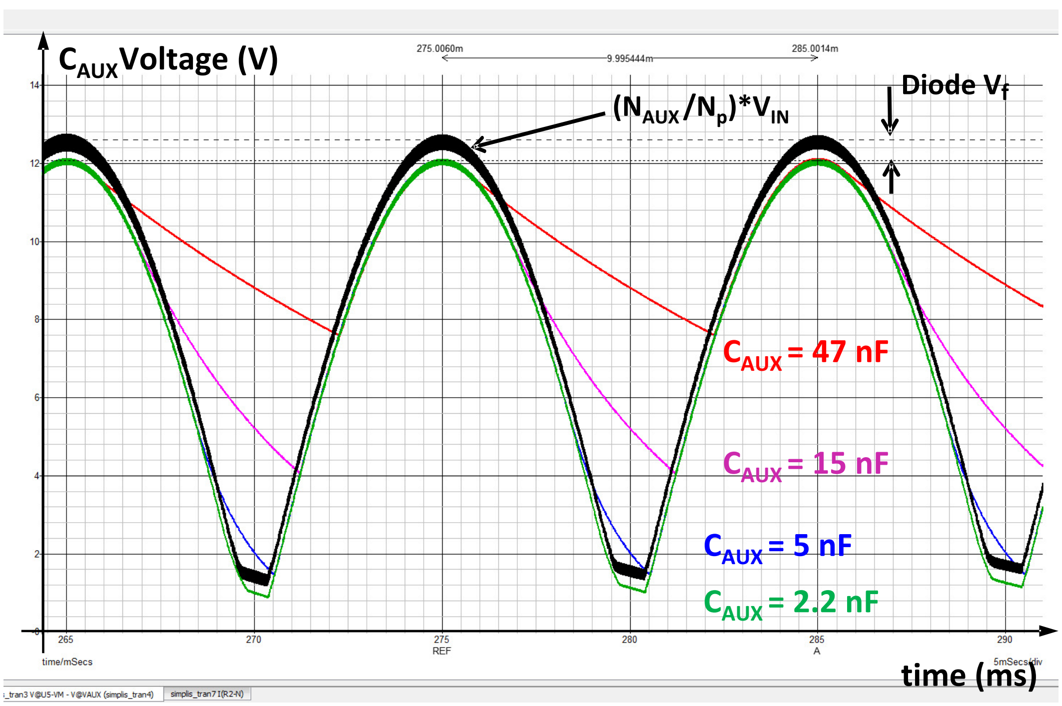

Figure 4. Voltage Across C_{AUX} Capacitor vs. Time and Different C_{AUX} Values

Practical Example of Component Values Calculation

Let's start with:

$$\frac{N_{AUX}}{N_{PRIM}} = 0.1 \qquad \text{(eq. 14)}$$

R_{CS2} must not be less than 20 kΩ so let's adopt the standard value R_{CS} = 22 kΩ.

Solving the following design Equation 10 for R_{CS1} gives:

$$R_{CS1} = R_{CS2} \cdot \left(K_{CS} \cdot \frac{N_{AUX}}{N_{PRIM}} - 1\right) = \qquad \text{(eq. 15)}$$

$$= 22\,k \cdot (138 \cdot 0.1 - 1) = 281.6\,k\Omega$$

Let's select the closest standard value which is: R_{CS1} = 270 kΩ.

Now let's recalculate K_{CS} to see if the new value is within 138 ±10%

The newly calculated K_{CS} value is:

$$K_{CS} = \frac{270\,k + 22\,k}{22\,k} \cdot \frac{1}{0.1} = 132.7 \qquad \text{(eq. 16)}$$

Which is acceptable because 138−10% = 124.2 and K_{CS} = 132.7. This value is above 138−10%.

Now that we have R_{CS1} and R_{CS2} values, let's solve R_{CS0} using the design Equation 11 which gives:

$$R_{CS0} = 50\,k\Omega - \frac{R_{CS1} \cdot R_{CS2}}{R_{CS1} + R_{CS2}} = \qquad \text{(eq. 17)}$$

$$= \frac{270\,k \cdot 22\,k}{270\,k + 22\,k} = 20.34\,k\Omega$$

So we will take the standard value of R_{CS0} = 20 kΩ (we could have taken also 22 kΩ because 10% error is acceptable for matching a time constant)

Now we have to calculate C_{AUX} capacitance value using Equation 12 which gives:

$$\left(R_{CS1} + R_{CS2}\right) \cdot C_{AUX} = 640\,\mu s \pm 10\% \qquad \text{(eq. 18)}$$

$$C_{AUX} = \frac{640\,\mu}{R_{CS1} + R_{CS2}} = \frac{640\,\mu}{270\,k + 22\,k} = 2.19\,nF \qquad \text{(eq. 19)}$$

The closest standard value is: C_{AUX} = 2.2 nF.

To calculate the R_{AUX} value we will use the design Equation 13 which gives:

$$R_{AUX} = \frac{100\,n}{C_{AUX}} = \frac{100\,n}{2.2\,n} = 45.45\,\Omega \qquad \text{(eq. 20)}$$

The closest standard value is: R_{AUX} = 47 Ω.

All the calculated component values which have been calculated are now reported on Figure 5 schematic.

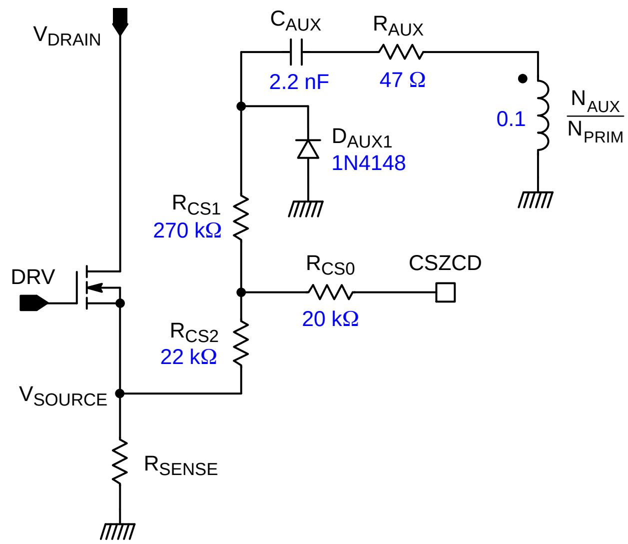

Figure 5. CSZCD Schematic Circuitry with Component Values Previously Calculated

References

[1] Application Note AND9218/D "5 Key Steps to Designing a Compact, High-Efficiency PFC Stage Using the NCP1602" which can be downloaded at: http://www.onsemi.com/pub_link/Collateral/AND9218−D.PDF

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