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Low Power Techniques of LC823450 Series for Audio Applications

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APPLICATION NOTE

ARM

Introduction

This application note describes low power techniques to enable customers to control the power consumption to meet their operation mode.

Intended audience is customers who are building audio application using LC823450 Series (called LC823450 hereafter).

BACKGROUND

Hard-wired MP3 playback

LC823450 has a hard-wired MP3 decoder to realize MP3 playback with low power. Using the MP3 decoder can reduce the current consumption during MP3 playback comparing with using software decoder by DSP because it consists of hard-wired logic designed dedicatedly for MP3 decode and it can work with lower frequency than DSP works.

Sleep mode

LC823450 has Sleep mode to gate the clock of Cortex-M3 (called CPU hereafter) inside with the standby instructions which it implements. To reduce the current consumption, CPU should be set to Sleep mode while it doesn't work anything.

WIC Sleep mode + internal power domain control

LC823450 has WIC (Wake-up Interrupt Controller) Sleep mode to gate the clocks of all blocks except RTC block by stopping oscillation with register setting and the standby instructions which it implements. This mode realizes standby completely except RTC block.

Moreover, LC823450 has some internal power domains which it can isolate. If you set the power domains to power off in addition to WIC Sleep mode, LC823450 will be able to reduce the standby leakage current further.

Keyint RTC mode

: This mode is not available according to the products. Please see the datasheet.

LC823450 has 2 blocks which are separated electrically as power domain. One is RTC block and the other is Main block which has all modules except RTC block. RTC is Real Time Clock and it consists of timers for calculating calendar. Main block has CPU, bus system, internal memories, Audio module and various peripheral modules.

LC823450 has Keyint RTC mode to provide mechanism which powers on/off all power terminals of Main block controlling external regulators. In this mode, it can execute calculating calendar in RTC block with very low power consumption due to power cut of Main block.

About operation for low power control

LC823450 has 3 oscillations of RC, XT1 and XTRTC. RC is internal RC oscillation for initial operation after reset, XT1 is Xtal oscillation for main operation and XTRTC is 32.768kHz oscillation for RTC. And it has a fundamental clock as BASIC clock for CPU, bus system, internal memories and so on, which is made up based on any of RC, XT1 or XTRTC.

Moreover, there are registers to enable or disable the clock of peripherals and the oscillations. You can reduce the current consumption by disabling the clocks of unused peripheral modules and the oscillations individually.

Table 1 shows an operation matrix for low power control. Sleep mode can stop the clock for CPU, WIC Sleep mode can stop all the oscillations except XTRTC, and Keyint RTC mode can power off Main block.

Table 1. Operation matrix for low power control

STATE	Main Block					RTC Block	Wake up sources
	BASIC clock	CPU core clock	Peripherals clock	XT1	RC	XT32K	
Initial after reset	RUN	RUN	STOP	STOP	RUN	RUN	-
Run	RUN	RUN	RUN / STOP	RUN / STOP	RUN / STOP	RUN	-
Sleep	RUN	STOP	RUN / STOP	RUN / STOP	RUN / STOP	RUN	All interrupt / Reset input
WIC Sleep	STOP	STOP	STOP	STOP	STOP	RUN	External interrupt / Reset input
Keyint RTC	POWER OFF					POWER ON	KETINT interrupt or RTC interrupt / VDET input

Figure 1 shows working state transition of oscillation system. When the reset for LC823450 is asserted, LC823450 is located in Reset State. After the reset is

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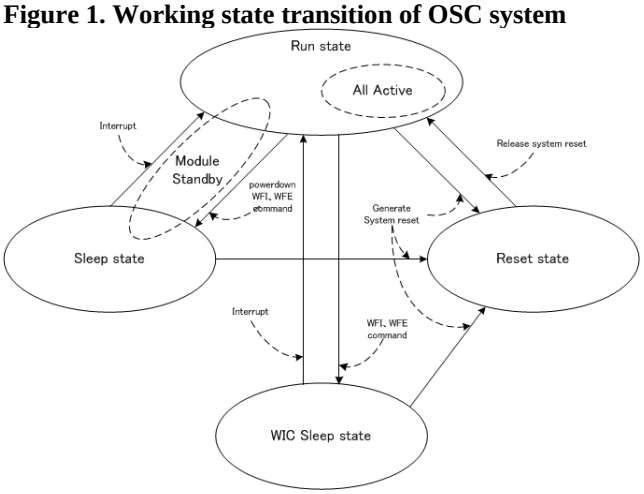
released, it moves to Run state. In Run state, it moves to sleep state when the standby instruction for Sleep mode is executed, and it moves to WIC Sleep state when the standby instruction for WIC Sleep mode is executed. LC823450 can leave Sleep state or WIC Sleep state when the condition to wake up as Table 1 is satisfied, and move to Run state. Furthermore, LC823450 can return back to Reset state even from any states when the reset signal is asserted.

Figure 1. Working state transition of OSC system



LOW POWER TECHNIQUES

Sleep mode

Sleep mode is one of 2 kinds of power management which CPU implements inside. The power management is decided by the value of SLEEPDEEP bit of System Control Register of the core and it shows Sleep mode that SLEEPDEEP bit is 0.

Figure 2 shows clock gate for sleep mode. BASIC clock connected to the clock of CPU is gated while Sleep mode is active. In this mode, the clock for CPU is stopped and the operation of it is stopped as well.

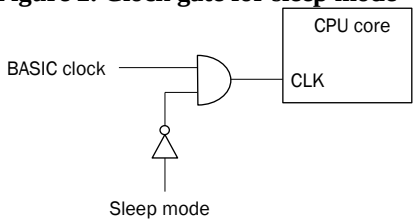
The fundamental procedure to enter Sleep mode is as follows.

1.Clear SLEEPDEEP bit to 0. (Initial value is zero.)
2.Execute WFI instruction or WFE instruction.

The fundamental procedure to release Sleep mode is as follows.

1.Generation of all interrupt requests
2.Generation of the reset to LC823450

Figure 2. Clock gate for sleep mode



WIC Sleep mode

WIC Sleep mode is the other of 2 kinds of power management which CPU implements inside. The power management is decided by the value of SLEEPDEEP bit of System Control Register of the core and it shows WIC Sleep mode that SLEEPDEEP bit is 1.

When the request of WIC Sleep mode happens, the power management system inside communicates with CPU and prepares for stopping all the oscillations except XTRTC. Then, all clocks in LC823450 except RTC block is automatically stopped while WIC Sleep mode is active.

The fundamental procedure to enter WIC Sleep mode is as follows.

1.Set SLEEPDEEP bit to 1.
2.Execute WFI instruction or WFE instruction.

The fundamental procedure to release Sleep mode is as follows.

1.Generation of External interrupt requests
2.Generation of the reset to LC823450

Internal power domain control

LC823450 has 8 internal power domains which it can isolate and power off internally as Table2 and Figure 3. You can isolate and power off these blocks individually by setting 2 registers in system controller to reduce the leakage current while they are not used. The 2 registers to be set are ISOCNT register and LSISTBY register as Table 2. ISOCNT register is used for whether to separate the power domain electrically or not, and LSISTBY register is used for whether to cut the power of the domain or not.

The fundamental procedure to power off is as follows.

1.Set the target bits of ISOCNT to 1.
2.Set the target bits of LSISTBY to 1.

The fundamental procedure to power on is as follows.

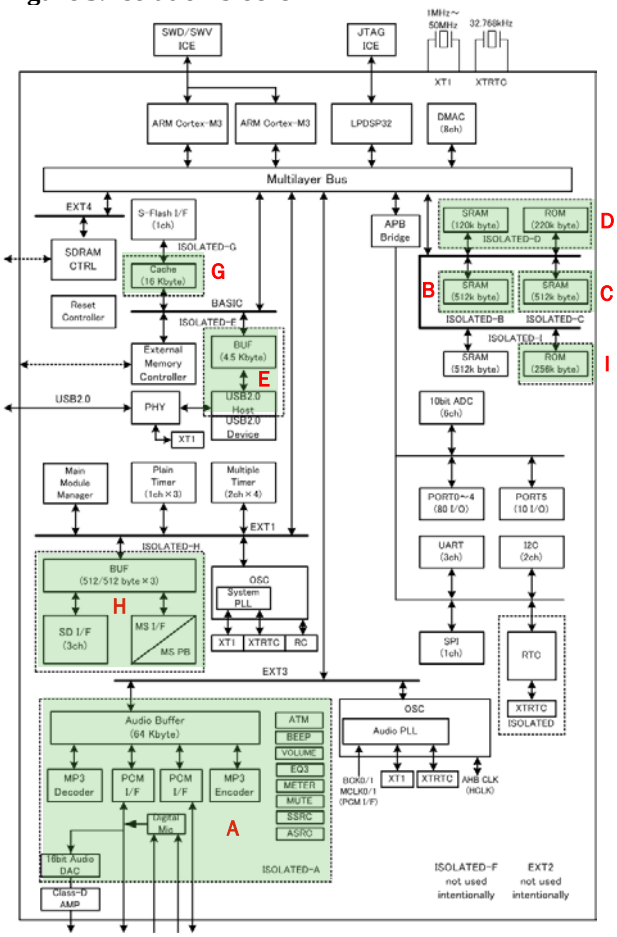
1.Clear the target bits of LSISTBY to 0.
2.Clear the target bits of ISOCNT to 0.

After power on, you should initialize the domains to reuse them by software.

Table 2. Isolation blocks and related registers

name	content	LSISTBY	ISOCNT
ISOLATED-A	Audio Block	Bit0 STBYA	Bit0 ISOCNTA
ISOLATED-B	Internal SRAM(seg 3/4/5)	Bit1 STBYB	Bit1 ISOCNTB
ISOLATED-C	Internal SRAM(seg 6/7/8)	Bit2 STBYC	Bit2 ISOCNTC
ISOLATED-D	Internal SRAM(seg 9) 220KB LPDSP32 ROM	Bit3 STBYD	Bit3 ISOCNTD
ISOLATED-E	USB 2.0 Holt Controller SRAM for USB	Bit4 STBYE	Bit4 ISOCNTE
ISOLATED-G	Cache for S-Flash I/F	Bit6 STBYG	Bit6 ISOCNTG
ISOLATED-H	SD Card I/F Memory Stick I/F	Bit7 STBYH	Bit7 ISOCNTH
ISOLATED-I	Internal ROM 256KB	Bit8 STBYI	Bit8 ISOCNTI

Figure 3. Isolation blocks



Keyint RTC mode

Keyint RTC mode can power on/off all power terminals of Main block controlling external regulators and it can lose the leakage current of Main block as well because the power supply is cut off.

Figure 4 shows electric isolation control between RTC block and Main block. When Internal ISOLATOR control signal is 1, both blocks are connected electrically, and when it is 0, they are cut off electrically and the reset input of Main block is active internally as well.

Figure 5 shows state diagram of Keyint RTC mode. RTC block has a sequencer with 9 states from S0 to S8 and it controls the operation of Keyint RTC mode.

In initial state, power of RTC block is supplied and power of Main block isn't supplied. VDET is a reset input for RTC block, when it is input, the state becomes S0 and the sequencer waits for XTRTC oscillation to be stable.

After this, the state becomes S1 to execute power on sequence. RTCINT signal should be connected to the inputs of external regulators with an external pull up register in your external circuit, in S2, the sequencer generates RTCINT signal to enable the external regulators to supply power for Main block. In S3, the sequencer waits for Vdd1 of Main block to become prescribed voltage level at powering on. In S4, the sequencer generates internal ISOLATOR control signal to electrically connect all signals between RTC block and Main block. In S5, the sequencer releases the reset of Main block by generating internal RESETB signal with high level. Thus, power on sequence completes and LC823450 works normally at S5.

In order to enter Keyint RTC mode from normal operation, RTC master command needs to be issued by setting RTC master register of RTC block. When RTC master command is issued, the sequencer generates internal ISOLATOR control signal to electrically cut off all signals between RTC block and Main block, and resets Main block internally as well by generating internal RESETB signal with low level in S6. In S7, the sequencer generates RTCINT signal for the external regulators to cut all the power supply of Main block, and the state progresses to S8. In S8, power off sequence completes and LC823450 enters Keyint RTC mode. Then, LC823450 becomes very low power state and waits for KEYINT input or internal RTC interrupt to release Keyint RTC mode.

Figure 4. Isolation control

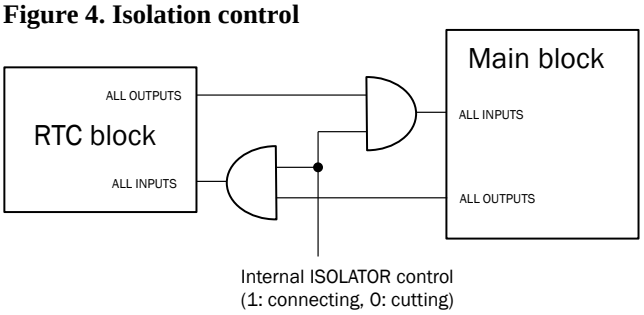
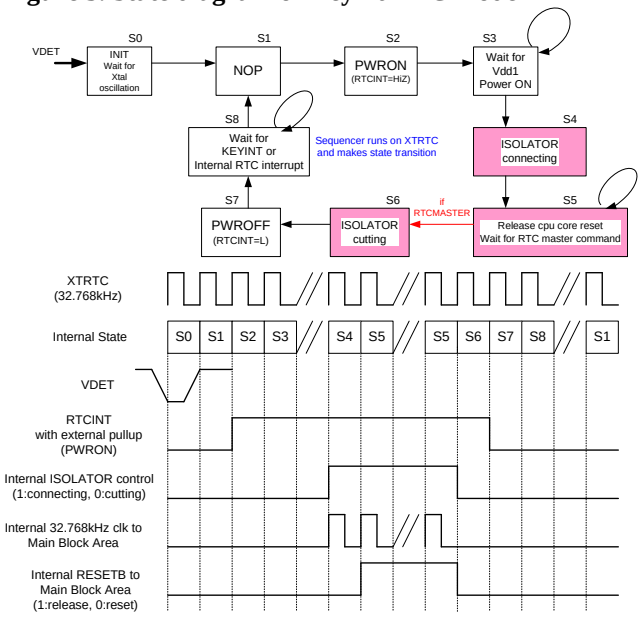


Figure 5. State diagram of Keyint RTC mode



Hard-wired MP3 playback

When LC823450 playbacks the hard-wired MP3, the system of LC823450 can do an intermittent action changing the frequency to reduce the current consumption as shown in Figure 6 if LC823450 has much time that CPU isn't working and it is only waiting.

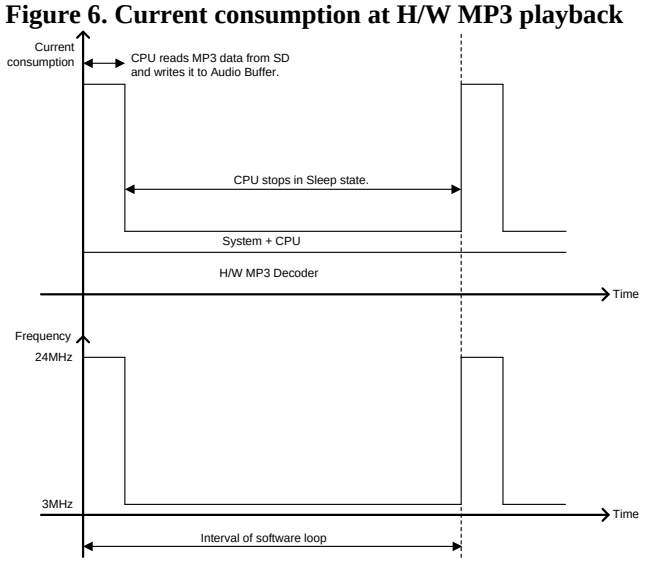
MP3 data is decoded in hard-wired logic. In order to decode the MP3 data, CPU reads it from SD card and writes it to an Audio Buffer inside LC823450 repeatedly with constant interval made by software loop. The hard-wired MP3 logic normally fetches the MP3 data from the Audio Buffer and decode it. In order that the Audio Buffer doesn't become empty, CPU puts the MP3 data from SD card into the Audio Buffer repeatedly. Once putting the data, CPU waits until the repeated timing comes again.

In this case, you can increase the frequency of the system clock while CPU transfers the MP3 data in order to process it quickly. Then, you can decrease the frequency of it while CPU waits in order to reduce the current consumption of the whole system including the system bus, memories, peripherals and so on. In addition, you can set CPU to Sleep mode during the wait in order to reduce it further.

For example, in Figure 6, the hard-wired MP3 logic always works with low speed operation, so it expends only a little current consumption. In order to reduce the current consumption as much as possible, the whole system works at 24MHz while CPU transfers the MP3 data, and it idles at 3MHz while CPU waits in Sleep mode. Generally, the longer the whole system idles at low speed, the more you can reduce the current consumption.

By the way, depending on applications, there may be some cases that CPU and/or DSP inside has to process some software functions during MP3 playback. In these cases, the whole system can't do an intermittent action, and it needs to keep working with appropriate constant frequency during MP3 playback. However, as MP3 playback is provided by hard-wired logic, the applications can implement both hard-wired MP3 playback and the software functions at the same time with lower current consumption with appropriate frequency for the software functions. In addition, if the applications stop clocks of unused peripherals, the current consumption will be decreased further.

Figure 6. Current consumption at H/W MP3 playback

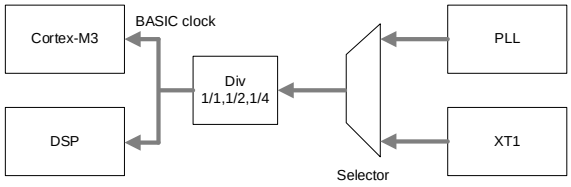


DFS

DFS (Dynamic Frequency Scaling) is implemented in DSP decoded Playback Mode, A2DP Mode and HFP mode. DFS provides a function to dynamically change BASIC clock during operation in order to reduce the current consumption. Normally, the switching of PLL generates a lock period of 10 milliseconds, but the switching of Div (MainDiv) is possible to switch clocks one of 1 time, 1/2 times, 1/4 times of the PLL seamlessly. The DSP operates asynchronously with CPU, but the supplied clock is the same on LC823450. Therefore when the clock of the DSP will be decrease in order to reduce the current consumption, the output speed of the audio data from DSP also will be decreased. In the DFS, AudioMiddle checks the remaining amount in the H/W buffer behind the DSP, if the remaining amount become smaller than threshold, AudioMiddle changes the value of Div to higher to prevent the shortage of sound data.

When both cores of CPU enter WFI (Wait For Interrupt), Selector switchs the source of BASIC clock from PLL to XT1, not only gating the clock of CPU. As a result, it can be expected that the power consumption will be lowered by decreasing the supply clock to the periphery and gating lock to CPU. WFI is managed by OS. When there is no task being executed during each operation, the OS issues a WFI and transitions to the power saving mode. Return from WFI will be triggered by an interrupt.

Figure 7. DFS diagram



TYPICAL DATA OF CURRENT CONSUMPTION

In this chapter, referential and example data of current consumption in each mode is described. The conditions of measurement are as follows.

Hard-wired MP3 playback:

LC823450 does an intermittent action between 24 MHz and 3 MHz decoding MP3 data by hard-wired MP3 with CPU sleeping at 3 MHz.

In addition, LC823450 always keeps working with 24 MHz during hard-wired MP3 playback for the comparison.

DSP decoded MP3 playback:

LC823450 does DFS action between 80 MHz, 40 MHz and 12MHz decoding MP3 data by DSP.

In addition, LC823450 always keeps working with 25MHz during idle in the MP3 playback mode. Idle means the current consumption which is in the stop condition of MP3 playback mode.

Sleep mode:

LC823450 works at 3MHz with CPU sleeping.

WIC Sleep mode + internal power domain control:

LC823450 works with all clocks except XTRTC stopped and with all internal power domains except SDIF isolated and powered off.

Keyint RTC mode:

LC823450 works with power of Main block cut and with power of only RTC block supplied.

Table 3. Example of Current consumption #1

Operation mode		Volume	Vdd1	VddRTC	VddXT1	AVddPLL1	AVddPLL2	VddDAMPL / VddDAMPR
			1.0V	1.0V	1.1V	1.1V	1.1V	1.5V
Hard-wired MP3 playback	24 MHz for constant action *1	0 dBFs	6.7 mA	1.4 uA	0.3 mA	0.2 mA	0.3 mA	2.5 mA
		-20 dBFs						1.4 mA
	24 MHz-3 MHz for intermittent action *2	0 dBFs	4.0 mA	1.4 uA	0.3 mA	0.2 mA	0.3 mA	2.5 mA
		-20 dBFs						1.4 mA
DSP decoded MP3 playback	80MHz/40MHz for DFS *3	0 dBFs	6.6mA	1.6 uA	0.3mA	0.2mA	0.3mA	2.5mA
		-20 dBFs						1.2mA
	25MHz for idle *4	-	5.1mA	1.6 uA	0.3mA	0.2mA	0.3mA	1.2mA *7
Sleep mode 3 MHz *5		-	1.15 mA	1.4 uA	0.3 mA	0.2 mA	0.52 uA	1.4 uA
WIC sleep mode + internal power domain control *6		-	0.54 mA	1.4 uA	0.18 uA	0.3 uA	0.35 uA	1.4 uA
Keyint RTC mode		-	(power off)	1.4 uA	(power off)	(power off)	(power off)	(power off)

Note)
Target Board : LC823450XGEVK
Sample : Typ.
Temperature : Room
XT1 : 24 MHz
XTRTC : 32.768 kHz
Note)
*1 System clock : 24 MHz, Audio clock : 18.432 MHz, DSP : OFF
Volume : R/L 0 dB, 44.1 kHz, 128 kbps MP3
*2 System clock : 24 MHz(active), 3 MHz(sleep), Audio clock : 18.432 MHz, DSP : OFF
Volume : R/L 0 dB, 44.1 kHz, 128 kbps MP3
*3 System clock : 80/40/12MHz (by Dynamic Frequency Scaling), Audio clock : 36.864 MHz
Volume : R/L 0 dB, 44.1 kHz, 128 kbps MP3
*4 System clock : 25 MHz, Audio clock : 36.864 MHz
Volume : R/L 0 dB, 44.1 kHz, 128 kbps MP3
*5 System clock : 3 MHz(sleep), Audio clock : OFF, DSP : OFF
*6 All clocks except RTC are stopped.
All internal power domains except SDIF are isolated and powered off.
*7 It can be achieved approximately zero consumption by software.

A2DP streaming playback:

LC823450 does A2DP streaming playback with DFS action by controlling Bluetooth IC. The system clock is optimized to minimum frequency necessary to decode the streaming data which is SBC encoding sent from Bluetooth IC. The current consumption of VddRTC is the same at another function because it isn't depend on function mode.

"Play" means the current consumption which is in the condition to receive SBC encoding signal from Bluetooth IC by Bluetooth communication.

"Idle" means the current consumption which is in the condition not to receive SBC encoding signal in spite of continuation of Bluetooth communication.

HFP communication:

LC823450 does HFP communication with DFS action by controlling Bluetooth IC. There are two versions LC823450 can handle.

"CVSD" means the HFP communication used CVSD codec as known HFP 1.5 version, it is a standard profile supported up to 8 kHz monaural configuration.

"mSBC" means the HFP communication used modified SBC codec as known HFP 1.6 version, it is added optional support for wide band speech with the mSBC codec up to 16 kHz.

Table 4. Example of Current consumption #2

Operation mode		Vdd1	VddXT1	AVddPLL1	AVddPLL2	VddDAMPL / VddDAMPR
		1.0V	1.1V	1.1V	1.1V	1.5V
A2DP	Play *1	8.37 mA	0.29 mA	0.20 mA	0.29 mA	1.4 mA
	Idle *2	5.09 mA	0.29 mA	0.20 mA	0.29 mA	1.2 mA*5
HFP	CVSD *3	6.19 mA (4.81 mA) *6	0.30 mA	0.21 mA	0.24 mA	1.1 mA
	mSBC *4	9.84 mA (7.81 mA) *6	0.30 mA	0.21 mA	0.24 mA	1.1 mA

Note)
Target Board : LC823450XGEVK
Sample : Typ.
Temperature : Room
XT1 : 24 MHz
XTRTC : 32.768 kHz
Note)
*1 System clock : 30/15/12 MHz (by Dynamic Frequency Scaling), Audio clock : 36.864 MHz
Slave/SBC : 328 kbps, Sampling Freq=48 kHz, Joint Stereo, Block Length=16, Subband=8
Bitpool=51, EQ & Bass boost : off, Volume : 40 mVrms Swing@16ohm load
Class 2: -6 to +4 dBm, No AVRCP signaling
*2 System clock : 25 MHz, Audio clock : 36.864 MHz
Sniff Interval= 500 ms, Link in sniff (1.28 sec interval, 4 attempts, 0 retries)
*3 System clock : 60/30/12 MHz (by Dynamic Frequency Scaling), Audio clock : 24.576 MHz
Slave/eSCO/Setting S3/2EV3/CVSD, Silence on the link, Tx power 8 dBm
Link in sniff(1.28 sec interval, 4 attempts, 0 retries)
*4 System clock : 60/30/12 MHz (by Dynamic Frequency Scaling), Audio clock : 24.576 MHz
Slave/eSCO/Setting S3/2EV3/mSBC, Silence on the link, Tx power 8 dBm
Link in sniff(1.28 sec interval, 4 attempts, 0 retries)
*5 It can be achieved approximately zero consumption by software.
*6 DSP processing (Echo canceller, Noise canceller, 2mic-zoom): off

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