



AX5043 Use with a TCXO Reference Clock

Introduction

This application note describes how to design an optimal connection between different TCXO types and AX5043.

If this connection is not designed in an optimal way, the AX5043 RF Synthesizer may produce higher phase noise than necessary, resulting in reduced selectivity in RX and lower attainable output power for a given regulatory regime in TX.

Connection of Clipped Sine Wave TCXOs

For TCXOs having clipped sine wave outputs an external circuitry consisting of two capacitors C1 and C2 as well as a resistor R are recommended. Component sizes as well as register settings are given in the tables.

The voltage at node V_p should be the TCXO output signal without significant additional distortion. The voltage at V_n should be a DC value equivalent to the mean value of the waveform at V_p .

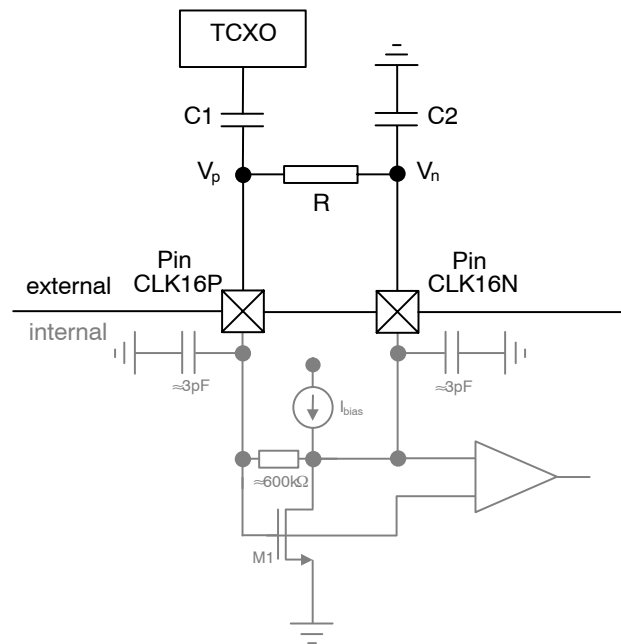


Figure 1. Configuration for a Clipped Sine Wave Output TCXO

Table 1. COMPONENT VALUES

Component	C1	C2	R
Value	1 nF	1 nF	1 kΩ

APPLICATION NOTE

Table 2. REGISTER SETTINGS

Register	Analog Parameter	Value
0xF10	I_{bias}	0x04
0xF11	I_{bias} autoreg.	0x00
0x184	XTALCAP	0x00

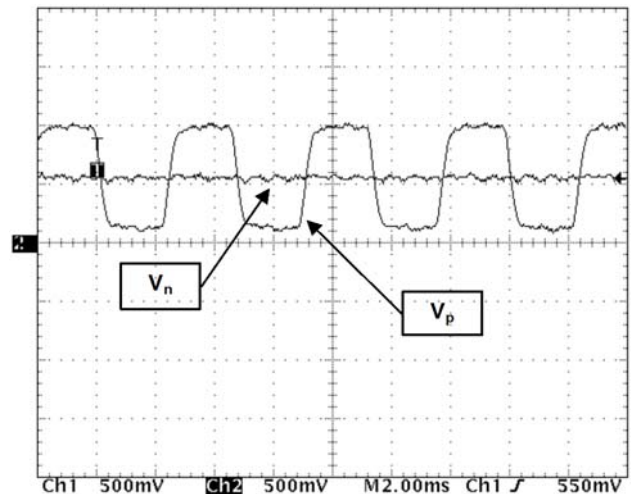


Figure 2. Voltages at Nodes V_p and V_n

Connection of CMOS TCXOs

For TCXOs having CMOS outputs it is recommended to use a capacitive divider (C1 and C2) to reduce the signal swing at the input pin CLK16P to between 1.5–2 V peak-to-peak. Pin CLK16N should be left open, to allow the internal circuitry to work as a fast inverter. Component sizes as well as register settings are given in the tables.

The voltage at V_p should be the TCXO output signal without significant additional distortion and with a peak-to-peak swing no larger than 2 V. The voltage at V_n should be the inverted waveform.

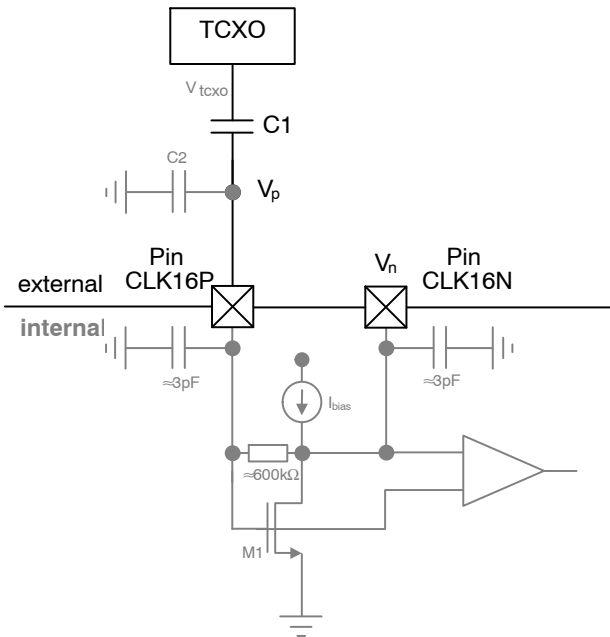


Figure 3. Configuration for a Clipped Sine Wave Output TCXO

Table 3. COMPONENT VALUES

Component	C1	C2
Value	10 pF	6.8 pF

Table 4. REGISTER SETTINGS

Register	Analog Parameter	Value
0xF10	I_{bias}	0x0F
0xF11	I_{bias} autoreg.	0x00
0x184	XTALCAP	0x00

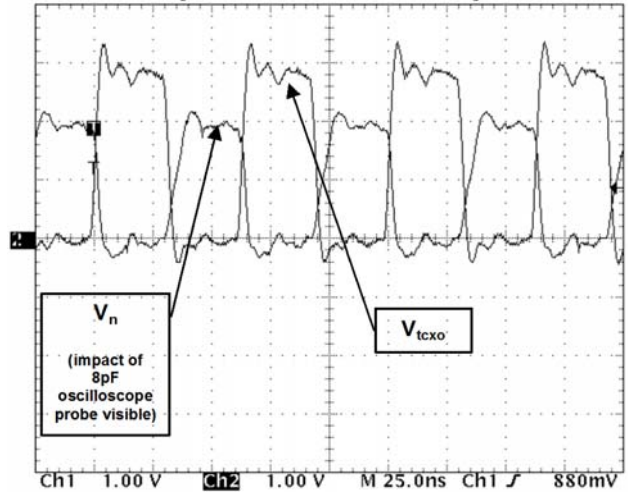


Figure 4. Voltages at Nodes V_p and V_n

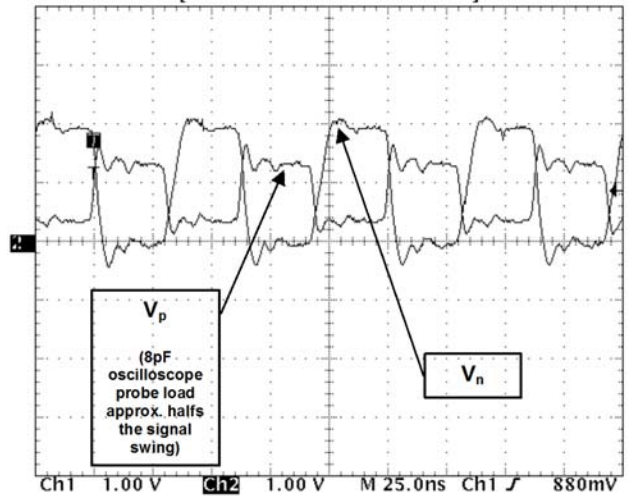


Figure 5. Voltages at Nodes V_p and V_n

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