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# AND9329/D

# AX8052 Power On Reset

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APPLICATION NOTE

### Introduction

This application note discusses designing power−on reset for the AX8052F1xx family of microcontrollers for a wide range of supply voltage conditions. After explaining why a Power−on−Reset (POR) circuit can fail, this application note covers the best ways to make POR work reliably.

### Causes

The AX8052 microcontroller features a built−in Power−On Reset circuit which does not draw current except for negligible leakage. This ultra−low−power consumption is possible because the internal POR circuitry is edge sensitive. Therefore certain rise and fall times of the supply voltage (VDD_IO) are required to trigger the internal POR:

1. Supply voltages starting below 0.1 V with rise and fall times faster than 0.1 V/ms (normal start−up)
2. Supply voltages starting between 0.1 V and 0.7 V with the rise and fall times faster than 3.3 V/ms (fast voltages)

**For other cases an external reset circuit is strongly recommended.**

Operation of the device in the voltage range from 0.4 V to 0.8 V without proper reset can cause flash memory loss.

### Normal Start−up

Figure 1 depicts the VDD_IO waveform for a normal start−up. VDD_IO should start at 0.1 V maximum, and then rise with a slope of at least 0.1 V/ms, to the normal operating voltage.

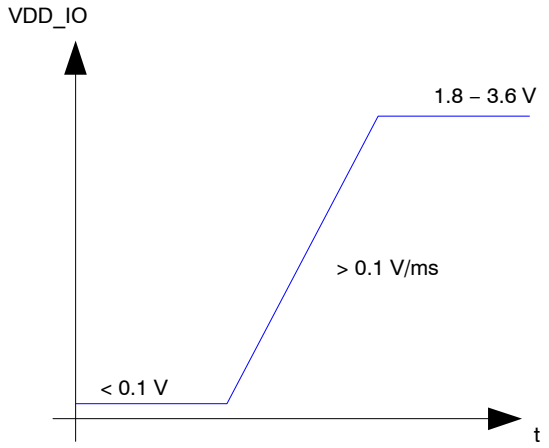


**Figure 1. Normal Start−up**

If either the maximum start voltage or the slope requirement cannot be met, Axsem recommends the use of external reset circuitry or an external reset device.

### Temporary Loss of Power

Figure 2 shows a temporary loss of power waveform. In this scenario, if the VDD_IO voltage does not return to below 0.1 V before reapplying power again, but lingers in the range of approximately 0.45 V to 0.7 V and the rise time is lower than 3.3 V/ms then external reset circuitry or an external reset device should be used.

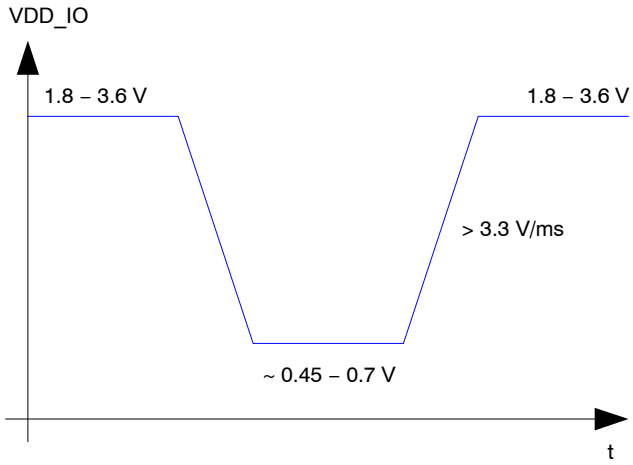


**Figure 2. Temporary Loss of Power**

### Power Management Interrupt

Axsem recommends to use power management interrupt code similar to the example given below. The power management interrupt is triggered by the voltage of VDD_IO falling below brown−out threshold, and then puts the microcontroller into standby mode.

```
void pwrmgmt_irq(void) __interrupt(6)
{
        uint8_t pc = PCON;
        if (!(pc & 0x80))
                return;
        GPIOENABLE = 0;
        IE = EIE = E2IE = 0;
        for (;;)
                PCON |= 0x01;
}
```

The interrupt needs to be enabled (IE_6 = 1; EA = 1;). If the application firmware uses bus master peripherals (like DMA or AES), these peripherals should be shut down in the brownout interrupt as well.

The interrupt protects the circuit from the microcontroller potentially executing arbitrary instructions. The interrupt is effective if the falling slope of VDD_IO is slower than approximately 1 V/ms; otherwise, the remaining time is not sufficient to detect the brown−out condition and to handle the interrupt.

### External Reset Circuit

A reset circuit like the one shown in Figure 3 is suitable to handle difficult power supply situations. The voltage across the zener diode and the turn−on voltage of Q1 are kept constant regardless of VDD_IO. RESET_N is decided as follows:

RESET_N = VDD_IO if VDD_IO > VZD1 + VONQ1

RESET_N = GND if VDD_IO < VZD1 + VONQ1

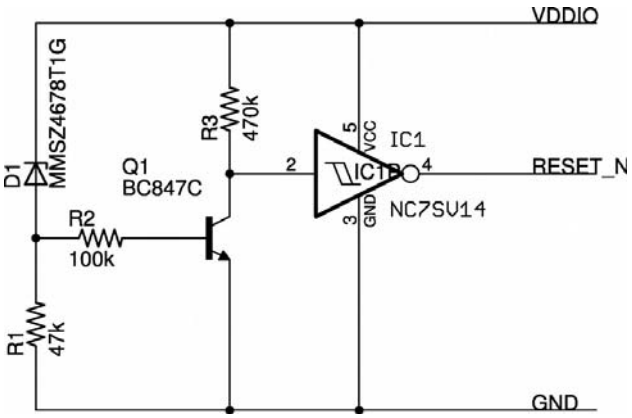


**Figure 3. Standard Reset Circuit**

Alternatively external voltage supervisors and reset generators can be used. Suitable circuits include the Rohm Semiconductors BU4211G or BU4811G.

### Conclusion

POR is a difficult issue to manage. Many unpredictable events can influence the circuitry. A power interruption might not happen often but it can at any time. For many common cases, the AX8052 internal power−on reset circuit ensures reliable start−up and no external components are required. Some corner cases, however, such as temporarily losing power, may require an external reset circuit.



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