AND9290/D

AR1337 Register & Variable Reference ON Semiconductor Imaging

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APPLICATION NOTE

Introduction

This reference document describes the AR1337 registers. Summary and detailed information are presented in separate sections:

- “Register Summary” on page 1
- “Register Descriptions” on page 39

How to Access Registers

All the registers can be accessed by the two-wire serial interface with 16−bit addresses and 16−bit data.

For more detailed information on the interface protocol of the two−wire serial interface, see the AR1337 data sheet.

Reserved Registers

All the reserved bits should not be changed. The user must write the original values back when changing the registers.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

- N−No. Changing the register value will not produce a bad frame. Y−Yes. Changing the register value might produce a bad frame.
- YM−Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to “1.”

Table 1. SMIA CONFIGURATION

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R0 (R0x0000)	chip_version_reg	dddd dddd dddd dddd	595 (0x0253)
R2 (R0x0002)	revision_number	???? ????	0 (0x00)
R3 (R0x0003)	manufacturer_id	???? ????	6 (0x06)
R4 (R0x0004)	smia_version	???? ????	10 (0x0A)
R5 (R0x0005)	frame_count	???? ????	255 (0xFF)
R6 (R0x0006)	pixel_order	0000 00??	0 (0x00)
R8 (R0x0008)	data_pedestal	0000 00dd dddd dddd	42 (0x002A)
R64 (R0x0040)	frame_format_model_type	???? ????	1 (0x01)
R65 (R0x0041)	frame_format_model_subtype	???? ????	18 (0x12)
R66 (R0x0042)	frame_format_descriptor_0	???? ???? ???? ????	20592 (0x5070)

Table 1. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R68 (R0x0044)	frame_format_descriptor_1	???? ???? ???? ????	4098 (0x1002)
R70 (R0x0046)	frame_format_descriptor_2	???? ???? ???? ????	23600 (0x5C30)
R72 (R0x0048)	frame_format_descriptor_3	???? ???? ???? ????	0 (0x0000)
R74 (R0x004A)	frame_format_descriptor_4	???? ???? ???? ????	0 (0x0000)
R76 (R0x004C)	frame_format_descriptor_5	???? ???? ???? ????	0 (0x0000)
R78 (R0x004E)	frame_format_descriptor_6	???? ???? ???? ????	0 (0x0000)
R80 (R0x0050)	frame_format_descriptor_7	???? ???? ???? ????	0 (0x0000)
R82 (R0x0052)	frame_format_descriptor_8	???? ???? ???? ????	0 (0x0000)
R84 (R0x0054)	frame_format_descriptor_9	???? ???? ???? ????	0 (0x0000)
R86 (R0x0056)	frame_format_descriptor_10	???? ???? ???? ????	0 (0x0000)
R88 (R0x0058)	frame_format_descriptor_11	???? ???? ???? ????	0 (0x0000)
R90 (R0x005A)	frame_format_descriptor_12	???? ???? ???? ????	0 (0x0000)
R92 (R0x005C)	frame_format_descriptor_13	???? ???? ???? ????	0 (0x0000)
R94 (R0x005E)	frame_format_descriptor_14	???? ???? ???? ????	0 (0x0000)
R128 (R0x0080)	analogue_gain_capability	???? ???? ???? ????	0 (0x0000)
R132 (R0x0084)	analogue_gain_code_min	???? ???? ???? ????	2 (0x0002)
R134 (R0x0086)	analogue_gain_code_max	???? ???? ???? ????	31 (0x001F)
R136 (R0x0088)	analogue_gain_code_step	???? ???? ???? ????	1 (0x0001)
R138 (R0x008A)	analogue_gain_type	???? ???? ???? ????	0 (0x0000)
R140 (R0x008C)	analogue_gain_m0	???? ???? ???? ????	1 (0x0001)
R142 (R0x008E)	analogue_gain_c0	???? ???? ???? ????	0 (0x0000)
R144 (R0x0090)	analogue_gain_m1	???? ???? ???? ????	0 (0x0000)
R146 (R0x0092)	analogue_gain_c1	???? ???? ???? ????	4 (0x0004)
R192 (R0x00C0)	data_format_model_type	???? ????	1 (0x01)
R193 (R0x00C1)	data_format_model_subtype	???? ????	5 (0x05)
R194 (R0x00C2)	data_format_descriptor_0	???? ???? ???? ????	2570 (0x0A0A)
R196 (R0x00C4)	data_format_descriptor_1	???? ???? ???? ????	2056 (0x0808)

Table 1. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R198 (R0x00C6)	data_format_descriptor_2	???? ???? ???? ????	2568 (0x0A08)
R200 (R0x00C8)	data_format_descriptor_3	???? ???? ???? ????	2566 (0x0A06)
R202 (R0x00CA)	data_format_descriptor_4	???? ???? ???? ????	0 (0x0000)
R204 (R0x00CC)	data_format_descriptor_5	???? ???? ???? ????	0 (0x0000)
R206 (R0x00CE)	data_format_descriptor_6	???? ???? ???? ????	0 (0x0000)
R256 (R0x0100)	mode_select	0000 000d	0 (0x00)
R257 (R0x0101)	image_orientation	0000 00dd	0 (0x00)
R259 (R0x0103)	software_reset	0000 000d	0 (0x00)
R260 (R0x0104)	grouped_parameter_hold	0000 000d	0 (0x00)
R261 (R0x0105)	mask_corrupted_frames	0000 000d	0 (0x00)
R272 (R0x0110)	ccp2_channel_mode	0000 0ddd	0 (0x00)
R273 (R0x0111)	ccp2_signalling_mode	0000 000d	1 (0x01)
R274 (R0x0112)	ccp_data_format	dddd dddd dddd dddd	2570 (0x0A0A)
R288 (R0x0120)	gain_mode	0000 000d	0 (0x00)
R514 (R0x0202)	coarse_integration_time	dddd dddd dddd dddd	1 (0x0001)
R516 (R0x0204)	analogue_gain_code_global	0000 0000 0ddd dddd	4 (0x0004)
R518 (R0x0206)	analogue_gain_code_greenr	0000 0000 0ddd dddd	4 (0x0004)
R520 (R0x0208)	analogue_gain_code_red	0000 0000 0ddd dddd	4 (0x0004)
R522 (R0x020A)	analogue_gain_code_blue	0000 0000 0ddd dddd	4 (0x0004)
R524 (R0x020C)	analogue_gain_code_greenb	0000 0000 0ddd dddd	4 (0x0004)
R526 (R0x020E)	digital_gain_greenr	0000 0ddd dddd dd00	256 (0x0100)
R528 (R0x0210)	digital_gain_red	0000 0ddd dddd dd00	256 (0x0100)
R530 (R0x0212)	digital_gain_blue	0000 0ddd dddd dd00	256 (0x0100)
R532 (R0x0214)	digital_gain_greenb	0000 0ddd dddd dd00	256 (0x0100)
R768 (R0x0300)	vt_pix_clk_div	0000 0000 000d dddd	5 (0x0005)
R770 (R0x0302)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R772 (R0x0304)	pre_pll_clk_div	00dd dddd 00dd dddd	257 (0x0101)

Table 1. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R774 (R0x0306)	pll_multiplier	dddd dddd dddd dddd	11308 (0x2C2C)
R776 (R0x0308)	op_pix_clk_div	0000 0000 000d dddd	10 (0x000A)
R778 (R0x030A)	op_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R832 (R0x0340)	frame_length_lines	dddd dddd dddd dddd	3278 (0x0CCE)
R834 (R0x0342)	line_length_pck	dddd dddd dddd ddd0	4656 (0x1230)
R836 (R0x0344)	x_addr_start	0000 dddd dddd dddd	8 (0x0008)
R838 (R0x0346)	y_addr_start	0000 dddd dddd dddd	8 (0x0008)
R840 (R0x0348)	x_addr_end	000d dddd dddd dddd	4215 (0x1077)
R842 (R0x034A)	y_addr_end	0000 dddd dddd dddd	3127 (0x0C37)
R844 (R0x034C)	x_output_size	000d dddd dddd ddd0	4208 (0x1070)
R846 (R0x034E)	y_output_size	0000 dddd dddd ddd0	3120 (0x0C30)
R900 (R0x0384)	y_even_inc	0000 0000 0000 000?	1 (0x0001)
R902 (R0x0386)	y_odd_inc	0000 0000 00dd dddd	1 (0x0001)
R1024 (R0x0400)	scaling_mode	0000 0000 0000 00dd	0 (0x0000)
R1026 (R0x0402)	spatial_sampling	0000 0000 0000 000d	0 (0x0000)
R1028 (R0x0404)	scale_m	0000 0000 dddd dddd	16 (0x0010)
R1280 (R0x0500)	compression_mode	0000 0000 0000 000?	1 (0x0001)
R1536 (R0x0600)	test_pattern_mode	0000 00dd 0000 0ddd	0 (0x0000)
R1538 (R0x0602)	test_data_red	0000 00dd dddd dddd	0 (0x0000)
R1540 (R0x0604)	test_data_greenr	0000 00dd dddd dddd	0 (0x0000)
R1542 (R0x0606)	test_data_blue	0000 00dd dddd dddd	0 (0x0000)
R1544 (R0x0608)	test_data_greenb	0000 00dd dddd dddd	0 (0x0000)

Table 2. SMIA PARAMETER LIMITS

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R4096 (R0x1000)	integration_time_capability	0000 0000 0000 000?	1 (0x0001)
R4100 (R0x1004)	coarse_integration_time_min	dddd dddd dddd dddd	0 (0x0000)
R4102 (R0x1006)	coarse_integration_time_max_margin	dddd dddd dddd dddd	1 (0x0001)
R4224 (R0x1080)	digital_gain_capability	0000 0000 0000 000?	1 (0x0001)
R4228 (R0x1084)	digital_gain_min	???? ???? ???? ????	256 (0x0100)
R4230 (R0x1086)	digital_gain_max	???? ???? ???? ????	2044 (0x07FC)
R4232 (R0x1088)	digital_gain_step_size	???? ???? ???? ????	4 (0x0004)
R4360 (R0x1108)	min_pre_pll_clk_div	???? ???? ???? ????	1 (0x0001)
R4362 (R0x110A)	max_pre_pll_clk_div	???? ???? ???? ????	64 (0x0040)
R4372 (R0x1114)	min_pll_multiplier	???? ???? ???? ????	32 (0x0020)
R4374 (R0x1116)	max_pll_multiplier	???? ???? ???? ????	384 (0x0180)
R4384 (R0x1120)	min_vt_sys_clk_div	???? ???? ???? ????	1 (0x0001)
R4386 (R0x1122)	max_vt_sys_clk_div	???? ???? ???? ????	16 (0x0010)
R4404 (R0x1134)	min_vt_pix_clk_div	???? ???? ???? ????	4 (0x0004)
R4406 (R0x1136)	max_vt_pix_clk_div	???? ???? ???? ????	16 (0x0010)
R4416 (R0x1140)	min_frame_length_lines	dddd dddd dddd dddd	18 (0x0012)
R4418 (R0x1142)	max_frame_length_lines	dddd dddd dddd dddd	65535 (0xFFFF)
R4420 (R0x1144)	min_line_length_pck	dddd dddd dddd dddd	4656 (0x1230)
R4422 (R0x1146)	max_line_length_pck	dddd dddd dddd dddd	65532 (0xFFFC)
R4424 (R0x1148)	min_line_blanking_pck	dddd dddd dddd dddd	240 (0x00F0)
R4426 (R0x114A)	min_frame_blanking_lines	dddd dddd dddd dddd	16 (0x0010)
R4448 (R0x1160)	min_op_sys_clk_div	???? ???? ???? ????	1 (0x0001)
R4450 (R0x1162)	max_op_sys_clk_div	???? ???? ???? ????	16 (0x0010)
R4460 (R0x116C)	min_op_pix_clk_div	???? ???? ???? ????	6 (0x0006)
R4462 (R0x116E)	max_op_pix_clk_div	???? ???? ???? ????	10 (0x000A)
R4480 (R0x1180)	x_addr_min	???? ???? ???? ????	0 (0x0000)
R4482 (R0x1182)	y_addr_min	???? ???? ???? ????	0 (0x0000)

Table 2. SMIA PARAMETER LIMITS (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R4484 (R0x1184)	x_addr_max	???? ???? ???? ????	4223 (0x107F)
R4486 (R0x1186)	y_addr_max	???? ???? ???? ????	3135 (0x0C3F)
R4544 (R0x11C0)	min_even_inc	???? ???? ???? ????	1 (0x0001)
R4546 (R0x11C2)	max_even_inc	???? ???? ???? ????	1 (0x0001)
R4548 (R0x11C4)	min_odd_inc	???? ???? ???? ????	1 (0x0001)
R4550 (R0x11C6)	max_odd_inc	???? ???? ???? ????	7 (0x0007)
R4608 (R0x1200)	scaling_capability	0000 0000 0000 00??	2 (0x0002)
R4612 (R0x1204)	scaler_m_min	???? ???? ???? ????	16 (0x0010)
R4614 (R0x1206)	scaler_m_max	???? ???? ???? ????	128 (0x0080)
R4616 (R0x1208)	scaler_n_min	???? ???? ???? ????	16 (0x0010)
R4618 (R0x120A)	scaler_n_max	???? ???? ???? ????	16 (0x0010)
R4864 (R0x1300)	compression_capability	0000 0000 0000 000?	1 (0x0001)

Table 3. MANUFACTURER SPECIFIC

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12288 (R0x3000)	model_id_	dddd dddd dddd dddd	595 (0x0253)
R12290 (R0x3002)	y_addr_start_	0000 dddd dddd dddd	8 (0x0008)
R12292 (R0x3004)	x_addr_start_	000d dddd dddd dddd	8 (0x0008)
R12294 (R0x3006)	y_addr_end_	0000 dddd dddd dddd	3127 (0x0C37)
R12296 (R0x3008)	x_addr_end_	000d dddd dddd dddd	4215 (0x1077)
R12298 (R0x300A)	frame_length_line_	dddd dddd dddd dddd	3278 (0x0CCE)
R12300 (R0x300C)	line_length_pck_	dddd dddd dddd dddd	4656 (0x1230)
R12304 (R0x3010)	fine_correction	0ddd dddd dddd dddd	0 (0x0000)
R12306 (R0x3012)	coarse_integration_time_	dddd dddd dddd dddd	1 (0x0001)
R12308 (R0x3014)	shutter_fine	0ddd dddd dddd dddd	0 (0x0000)
R12310 (R0x3016)	row_speed	0000 0ddd 0ddd 0ddd	273 (0x0111)
R12312 (R0x3018)	extra_delay	dddd dddd dddd dddd	0 (0x0000)
R12314 (R0x301A)	reset_register	dddd dddd 00dd dddd	24 (0x0018)
R12316 (R0x301C)	mode_select_	0000 000d	0 (0x00)
R12317 (R0x301D)	image_orientation_	0000 00dd	0 (0x00)
R12318 (R0x301E)	data_pedestal_	0000 00dd dddd dddd	42 (0x002A)
R12321 (R0x3021)	software_reset_	0000 000d	0 (0x00)
R12322 (R0x3022)	grouped_parameter_hold_	0000 000d	0 (0x00)
R12323 (R0x3023)	mask_corrupted_frames_	0000 000d	0 (0x00)
R12324 (R0x3024)	pixel_order_	0000 00??	0 (0x00)
R12326 (R0x3026)	gpi_status	ddd? ??dd dddd ????	65535 (0xFFFF)
R12328 (R0x3028)	global_analog_gain_	0000 0000 00dd dddd	2 (0x0002)
R12330 (R0x302A)	analog_gain_greenr_	0000 0000 00dd dddd	2 (0x0002)
R12332 (R0x302C)	analog_gain_red_	0000 0000 00dd dddd	2 (0x0002)
R12334 (R0x302E)	analog_gain_blue_	0000 0000 00dd dddd	2 (0x0002)
R12336 (R0x3030)	analog_gain_greenb_	0000 0000 00dd dddd	2 (0x0002)
R12338 (R0x3032)	digital_gain_greenr_	0000 0ddd dddd dd00	256 (0x0100)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12340 (R0x3034)	digital_gain_red_	0000 0ddd dddd dd00	256 (0x0100)
R12342 (R0x3036)	digital_gain_blue_	0000 0ddd dddd dd00	256 (0x0100)
R12344 (R0x3038)	digital_gain_greenb_	0000 0ddd dddd dd00	256 (0x0100)
R12346 (R0x303A)	smia_version_	???? ????	10 (0x0A)
R12347 (R0x303B)	frame_count_	???? ????	255 (0xFF)
R12348 (R0x303C)	frame_status	0000 0000 0000 0???	0 (0x0000)
R12350 (R0x303E)	read_style	ddd0 0ddd ?ddd dddd	0 (0x0000)
R12352 (R0x3040)	read_mode	dddd dddd dddd dddd	65 (0x0041)
R12354 (R0x3042)	dark_control2	0ddd dddd dddd dddd	0 (0x0000)
R12356 (R0x3044)	dark_control	d0dd dddd dddd dddd	1408 (0x0580)
R12358 (R0x3046)	flash	00dd dddd dddd dddd	1544 (0x0608)
R12360 (R0x3048)	flash_count	dddd dddd dddd dddd	8 (0x0008)
R12362 (R0x304A)	otpm_control	0000 0ddd d??d d??d	0 (0x0000)
R12364 (R0x304C)	otpm_record	dddd dddd dddd dddd	512 (0x0200)
R12374 (R0x3056)	greenr_gain	dddd dddd dddd dddd	8208 (0x2010)
R12376 (R0x3058)	blue_gain	dddd dddd dddd dddd	8208 (0x2010)
R12378 (R0x305A)	red_gain	dddd dddd dddd dddd	8208 (0x2010)
R12380 (R0x305C)	greenb_gain	dddd dddd dddd dddd	8208 (0x2010)
R12382 (R0x305E)	global_gain	dddd dddd dddd dddd	8208 (0x2010)
R12384 (R0x3060)	vsync_override_code	dddd dddd dddd dddd	0 (0x0000)
R12386 (R0x3062)	hsync_override_code	dddd dddd dddd dddd	0 (0x0000)
R12388 (R0x3064)	smia_test	dddd dddd 0ddd dddd	22592 (0x5840)
R12390 (R0x3066)	framer_test_mode	0000 00dd dddd dddd	0 (0x0000)
R12392 (R0x3068)	i2c_control	0000 0000 0000 000d	0 (0x0000)
R12394 (R0x306A)	odp_status	0000 0000 00?? ?000	0 (0x0000)
R12398 (R0x306E)	datapath_select	dddd dddd ?ddd dddd	36992 (0x9080)
R12400 (R0x3070)	test_pattern_mode_	0000 00dd 0000 0ddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12402 (R0x3072)	test_data_red_	0000 00dd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr_	0000 00dd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue_	0000 00dd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb_	0000 00dd dddd dddd	0 (0x0000)
R12410 (R0x307A)	test_raw_mode	0000 0000 0000 00dd	0 (0x0000)
R12412 (R0x307C)	test_user_data	dddd dddd dddd dddd	0 (0x0000)
R12414 (R0x307E)	reset_lpf_register	0000 0000 00dd dddd	32 (0x0020)
R12424 (R0x3088)	coarse_integration2_time	dddd dddd dddd dddd	1 (0x0001)
R12448 (R0x30A0)	x_even_inc_	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc_	0000 0000 0000 dddd	1 (0x0001)
R12452 (R0x30A4)	y_even_inc_	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc_	0000 0000 00dd dddd	1 (0x0001)
R12464 (R0x30B0)	digital_test	dddd dddd 0ddd 00dd	1024 (0x0400)
R12466 (R0x30B2)	hispi_override_bba_control	dddd dddd dddd dddd	0 (0x0000)
R12476 (R0x30BC)	y_output_offset	0000 dddd dddd dddd	0 (0x0000)
R12478 (R0x30BE)	x_output_offset	0000 dddd dddd dddd	0 (0x0000)
R12520 (R0x30E8)	ctx_control_reg	dd00 00dd dddd dddd	0 (0x0000)
R12522 (R0x30EA)	ctx_wr_data	dddd dddd dddd dddd	63488 (0xF800)
R12524 (R0x30EC)	ctx_rd_data	dddd dddd dddd dddd	0 (0x0000)
R12534 (R0x30F6)	dark_control4	ddd0 0000 0000 dddd	0 (0x0000)
R12536 (R0x30F8)	gpio_ctrl	00dd 00dd 00dd 00dd	51 (0x0033)
R12538 (R0x30FA)	gpio_select	dddd dddd dddd ????	64652 (0xFC8C)
R12544 (R0x3100)	adacd_control	0000 0000 0000 00d0	0 (0x0000)
R12562 (R0x3112)	hispi_timing_2	dddd d000 dddd dddd	32768 (0x8000)
R12564 (R0x3114)	hispi_timing_3	dddd d000 dddd dddd	32768 (0x8000)
R12566 (R0x3116)	hispi_timing_4	dddd d000 dddd dddd	32768 (0x8000)
R12576 (R0x3120)	gain_dither_control	0000 0000 0000 000d	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12578 (R0x3122)	temp_threshold_value	dddd dddd dddd dddd	7 (0x0007)
R12580 (R0x3124)	tempsens_data_reg	0000 00?? ???? ????	0 (0x0000)
R12582 (R0x3126)	tempsens_ctrl_reg	0000 0000 0ddd dddd	0 (0x0000)
R12584 (R0x3128)	tempsens_calib1	dddd dddd dddd dddd	291 (0x0123)
R12586 (R0x312A)	tempsens_calib2	dddd dddd dddd dddd	17767 (0x4567)
R12588 (R0x312C)	tempsens_calib3	dddd dddd dddd dddd	35243 (0x89AB)
R12590 (R0x312E)	tempsens_calib4	dddd dddd dddd dddd	52719 (0xCDEF)
R12626 (R0x3152)	global_boost_rst	0000 0000 dddd dddd	16 (0x0010)
R12628 (R0x3154)	global_boost	dddd dddd dddd dddd	12807 (0x3207)
R12630 (R0x3156)	global_done	dddd dddd dddd dddd	51447 (0xC8F7)
R12632 (R0x3158)	slave_mode_control	dddd d000 0000 0000	0 (0x0000)
R12634 (R0x315A)	global_flash_start	dddd dddd dddd dddd	0 (0x0000)
R12636 (R0x315C)	global_bulb_trigger_count	dddd dddd dddd dddd	0 (0x0000)
R12638 (R0x315E)	global_seq_trigger	dddd dd00 dddd dddd	0 (0x0000)
R12640 (R0x3160)	global_rst_end	dddd dddd dddd dddd	236 (0x00EC)
R12642 (R0x3162)	global_shutter_start	dddd dddd dddd dddd	791 (0x0317)
R12644 (R0x3164)	global_shutter_start2	0000 0000 dddd dddd	0 (0x0000)
R12646 (R0x3166)	global_read_start	dddd dddd dddd dddd	807 (0x0327)
R12648 (R0x3168)	global_read_start2	0000 0000 dddd dddd	0 (0x0000)
R12656 (R0x3170)	analog_control	dddd dddd dddd dddd	9070 (0x236E)
R12658 (R0x3172)	analog_control2	0ddd 00dd 0ddd dddd	513 (0x0201)
R12660 (R0x3174)	analog_control3	dddd dddd dddd dddd	0 (0x0000)
R12662 (R0x3176)	analog_control4	dddd dddd dddd dddd	4096 (0x1000)
R12718 (R0x31AE)	serial_format	d000 00dd 000d dddd	516 (0x0204)
R12720 (R0x31B0)	frame_preamble	0000 0000 dddd dddd	92 (0x005C)
R12722 (R0x31B2)	line_preamble	0000 0000 dddd dddd	45 (0x002D)
R12724 (R0x31B4)	mipi_timing_0	dddd dddd dddd ddd0	9170 (0x23D2)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12726 (R0x31B6)	mipi_timing_1	dddd dddd dddd dddd	5130 (0x140A)
R12728 (R0x31B8)	mipi_timing_2	dddd dddd dddd dddd	9235 (0x2413)
R12730 (R0x31BA)	mipi_timing_3	dddd dddd dddd d0dd	7280 (0x1C70)
R12732 (R0x31BC)	mipi_timing_4	dddd dddd dddd dddd	34315 (0x860B)
R12734 (R0x31BE)	mipi_config	???d ddd0 dddd dddd	53379 (0xD083)
R12736 (R0x31C0)	hispi_timing_1	dddd d000 dddd dddd	32768 (0x8000)
R12738 (R0x31C2)	hispi_blanking	dddd dddd dddd dddd	65535 (0xFFFF)
R12740 (R0x31C4)	hispi_sync_patt	dddd dddd dddd dddd	62805 (0xF555)
R12742 (R0x31C6)	hispi_control_status	??dd dddd dddd dddd	32768 (0x8000)
R12744 (R0x31C8)	hispi_ckecksum0	???? ???? ???? ????	0 (0x0000)
R12746 (R0x31CA)	hispi_ckecksum1	???? ???? ???? ????	0 (0x0000)
R12748 (R0x31CC)	hispi_ckecksum2	???? ???? ???? ????	0 (0x0000)
R12750 (R0x31CE)	hispi_ckecksum3	???? ???? ???? ????	0 (0x0000)
R12752 (R0x31D0)	mipi_compress_8_data_type	00dd dddd 00dd dddd	12849 (0x3231)
R12754 (R0x31D2)	mipi_compress_7_data_type	00dd dddd 00dd dddd	13620 (0x3534)
R12756 (R0x31D4)	mipi_compress_6_data_type	00dd dddd 00dd dddd	14134 (0x3736)
R12758 (R0x31D6)	mipi_jpeg_pn9_data_type	d0dd dddd dddd dddd	13163 (0x336B)
R12762 (R0x31DA)	pll_dither_1	dddd dddd dddd dddd	0 (0x0000)
R12764 (R0x31DC)	pll_dither_2	dddd dddd dddd dddd	0 (0x0000)
R12766 (R0x31DE)	pll_dither_3	0000 0000 dddd dddd	0 (0x0000)
R12768 (R0x31E0)	pix_def_id	000d 0000 0000 000d	1 (0x0001)
R12770 (R0x31E2)	pix_def_id_ram_write	dddd dddd dddd dddd	0 (0x0000)
R12772 (R0x31E4)	pix_def_id_ram_read	???? ???? ???? ????	0 (0x0000)
R12784 (R0x31F0)	chain_control	00dd dddd 0000 0000	0 (0x0000)
R12786 (R0x31F2)	i2c_ids_mipi_default	dddd dddd dddd dddd	28268 (0x6E6C)
R12796 (R0x31FC)	i2c_ids	dddd dddd dddd dddd	28268 (0x6E6C)
R12798 (R0x31FE)	customer_rev	???? ???? ???? ????	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12810 (R0x320A)	pll_dither_4	dddd dddd dddd dddd	0 (0x0000)
R12812 (R0x320C)	pll_dither_5	dddd dddd dddd dddd	0 (0x0000)
R12814 (R0x320E)	pll_dither_6	0000 0000 dddd dddd	0 (0x0000)
R12832 (R0x3220)	pdaf_control	d000 dddd 0ddd dddd	3 (0x0003)
R12834 (R0x3222)	pdaf_row_control	ddd0 dddd dddd dddd	57536 (0xE0C0)
R12836 (R0x3224)	pdaf_pat_control	0000 0000 0000 00dd	1 (0x0001)
R12838 (R0x3226)	pdaf_row_start	0000 dddd dddd dddd	224 (0x00E0)
R12840 (R0x3228)	pdaf_row_end	0000 dddd dddd dddd	2912 (0x0B60)
R12842 (R0x322A)	pdaf_col_start	000d dddd dddd dddd	200 (0x00C8)
R12844 (R0x322C)	pdaf_col_end	000d dddd dddd dddd	4021 (0x0FB5)
R12846 (R0x322E)	pdaf_pedestal	000d dddd dddd dddd	168 (0x00A8)
R12848 (R0x3230)	pdaf_sat_th	000d dddd dddd dddd	4094 (0x0FFE)
R12850 (R0x3232)	pdaf_sc_origin_y	0000 dddd dddd dddd	0 (0x0000)
R12852 (R0x3234)	pdaf_sc_origin_x	000d dddd dddd dddd	0 (0x0000)
R12854 (R0x3236)	pdaf_sc_f_sh_0	dddd dddd dddd dddd	0 (0x0000)
R12856 (R0x3238)	pdaf_sc_f_sh_1	dddd dddd dddd dddd	0 (0x0000)
R12858 (R0x323A)	pdaf_sc_f_sh_2	dddd dddd dddd dddd	0 (0x0000)
R12860 (R0x323C)	pdaf_sc_f_sh_3	dddd dddd dddd dddd	0 (0x0000)
R12862 (R0x323E)	pdaf_sc_f_sh_4	dddd dddd dddd dddd	0 (0x0000)
R12864 (R0x3240)	pdaf_sc_f_sh_5	dddd dddd dddd dddd	0 (0x0000)
R12866 (R0x3242)	pdaf_sc_f_sh_6	dddd dddd dddd dddd	0 (0x0000)
R12868 (R0x3244)	pdaf_sc_f_sh_7	dddd dddd dddd dddd	0 (0x0000)
R12870 (R0x3246)	pdaf_sc_f_sh_8	dddd dddd dddd dddd	0 (0x0000)
R12872 (R0x3248)	pdaf_sc_f_sh_9	dddd dddd dddd dddd	0 (0x0000)
R12874 (R0x324A)	pdaf_sc_f_sh_10	dddd dddd dddd dddd	0 (0x0000)
R12876 (R0x324C)	pdaf_sc_f_sh_11	dddd dddd dddd dddd	0 (0x0000)
R12878 (R0x324E)	pdaf_sc_f_sh_12	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12880 (R0x3250)	pdaf_sc_f_sh_13	dddd dddd dddd dddd	0 (0x0000)
R12882 (R0x3252)	pdaf_sc_f_sh_14	dddd dddd dddd dddd	0 (0x0000)
R12884 (R0x3254)	pdaf_sc_f_sh_15	dddd dddd dddd dddd	0 (0x0000)
R12886 (R0x3256)	pdaf_sc_f_sh_16	dddd dddd dddd dddd	0 (0x0000)
R12888 (R0x3258)	pdaf_sc_f_sh_17	dddd dddd dddd dddd	0 (0x0000)
R12890 (R0x325A)	pdaf_sc_f_sh_18	dddd dddd dddd dddd	0 (0x0000)
R12892 (R0x325C)	pdaf_sc_f_sh_19	dddd dddd dddd dddd	0 (0x0000)
R12894 (R0x325E)	pdaf_sc_f_sh_20	dddd dddd dddd dddd	0 (0x0000)
R12896 (R0x3260)	pdaf_sc_f_sh_21	dddd dddd dddd dddd	0 (0x0000)
R12898 (R0x3262)	pdaf_sc_slope_x_0	dddd dddd dddd dddd	0 (0x0000)
R12900 (R0x3264)	pdaf_sc_slope_x_1	dddd dddd dddd dddd	0 (0x0000)
R12902 (R0x3266)	pdaf_sc_slope_x_2	dddd dddd dddd dddd	0 (0x0000)
R12904 (R0x3268)	pdaf_sc_slope_x_3	dddd dddd dddd dddd	0 (0x0000)
R12906 (R0x326A)	pdaf_sc_slope_x_4	dddd dddd dddd dddd	0 (0x0000)
R12908 (R0x326C)	pdaf_sc_slope_x_5	dddd dddd dddd dddd	0 (0x0000)
R12910 (R0x326E)	pdaf_sc_slope_x_6	dddd dddd dddd dddd	0 (0x0000)
R12912 (R0x3270)	pdaf_sc_slope_x_7	dddd dddd dddd dddd	0 (0x0000)
R12914 (R0x3272)	pdaf_sc_slope_x_8	dddd dddd dddd dddd	0 (0x0000)
R12916 (R0x3274)	pdaf_sc_slope_x_9	dddd dddd dddd dddd	0 (0x0000)
R12918 (R0x3276)	pdaf_sc_slope_x_10	dddd dddd dddd dddd	0 (0x0000)
R12920 (R0x3278)	pdaf_sc_slope_x_11	dddd dddd dddd dddd	0 (0x0000)
R12922 (R0x327A)	pdaf_sc_slope_x_12	dddd dddd dddd dddd	0 (0x0000)
R12924 (R0x327C)	pdaf_sc_slope_x_13	dddd dddd dddd dddd	0 (0x0000)
R12926 (R0x327E)	pdaf_sc_slope_x_14	dddd dddd dddd dddd	0 (0x0000)
R12928 (R0x3280)	pdaf_sc_slope_x_15	dddd dddd dddd dddd	0 (0x0000)
R12930 (R0x3282)	pdaf_sc_slope_x_16	dddd dddd dddd dddd	0 (0x0000)
R12932 (R0x3284)	pdaf_sc_slope_x_17	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12934 (R0x3286)	pdaf_sc_slope_x_18	dddd dddd dddd dddd	0 (0x0000)
R12936 (R0x3288)	pdaf_sc_slope_x_19	dddd dddd dddd dddd	0 (0x0000)
R12938 (R0x328A)	pdaf_sc_slope_x_20	dddd dddd dddd dddd	0 (0x0000)
R12940 (R0x328C)	pdaf_sc_slope_x_21	dddd dddd dddd dddd	0 (0x0000)
R12942 (R0x328E)	pdaf_sc_slope_y_0	dddd dddd dddd dddd	0 (0x0000)
R12944 (R0x3290)	pdaf_sc_slope_y_1	dddd dddd dddd dddd	0 (0x0000)
R12946 (R0x3292)	pdaf_sc_slope_y_2	dddd dddd dddd dddd	0 (0x0000)
R12948 (R0x3294)	pdaf_sc_slope_y_3	dddd dddd dddd dddd	0 (0x0000)
R12950 (R0x3296)	pdaf_sc_slope_y_4	dddd dddd dddd dddd	0 (0x0000)
R12952 (R0x3298)	pdaf_sc_slope_y_5	dddd dddd dddd dddd	0 (0x0000)
R12954 (R0x329A)	pdaf_sc_slope_y_6	dddd dddd dddd dddd	0 (0x0000)
R12956 (R0x329C)	pdaf_sc_slope_y_7	dddd dddd dddd dddd	0 (0x0000)
R12958 (R0x329E)	pdaf_sc_slope_y_8	dddd dddd dddd dddd	0 (0x0000)
R12960 (R0x32A0)	pdaf_sc_slope_y_9	dddd dddd dddd dddd	0 (0x0000)
R12962 (R0x32A2)	pdaf_sc_slope_y_10	dddd dddd dddd dddd	0 (0x0000)
R12964 (R0x32A4)	pdaf_sc_slope_y_11	dddd dddd dddd dddd	0 (0x0000)
R12966 (R0x32A6)	pdaf_sc_slope_y_12	dddd dddd dddd dddd	0 (0x0000)
R12968 (R0x32A8)	pdaf_sc_slope_y_13	dddd dddd dddd dddd	0 (0x0000)
R12970 (R0x32AA)	pdaf_sc_slope_y_14	dddd dddd dddd dddd	0 (0x0000)
R12972 (R0x32AC)	pdaf_sc_slope_y_15	dddd dddd dddd dddd	0 (0x0000)
R12974 (R0x32AE)	pdaf_sc_slope_y_16	dddd dddd dddd dddd	0 (0x0000)
R12976 (R0x32B0)	pdaf_sc_slope_y_17	dddd dddd dddd dddd	0 (0x0000)
R12978 (R0x32B2)	pdaf_sc_slope_y_18	dddd dddd dddd dddd	0 (0x0000)
R12980 (R0x32B4)	pdaf_sc_slope_y_19	dddd dddd dddd dddd	0 (0x0000)
R12982 (R0x32B6)	pdaf_sc_slope_y_20	dddd dddd dddd dddd	0 (0x0000)
R12984 (R0x32B8)	pdaf_sc_slope_y_21	dddd dddd dddd dddd	0 (0x0000)
R12986 (R0x32BA)	pdaf_sc_visual_tag	0000 0000 dddd dddd	4 (0x0004)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R12988 (R0x32BC)	pdaf_dc_th_abs	0000 00dd dddd dddd	0 (0x0000)
R12990 (R0x32BE)	pdaf_dc_th_rel	0000 0000 dddd dddd	0 (0x0000)
R12992 (R0x32C0)	pdaf_dc_diff_factor	0000 0000 000d dddd	0 (0x0000)
R12994 (R0x32C2)	pdaf_dma_start	000d dddd dddd dddd	0 (0x0000)
R12996 (R0x32C4)	pdaf_dma_size	000d dddd dddd dddd	0 (0x0000)
R12998 (R0x32C6)	pdaf_dma_y	0ddd dddd 0ddd dddd	0 (0x0000)
R13000 (R0x32C8)	pdaf_seq_start	dddd dddd dddd dddd	2140 (0x085C)
R13002 (R0x32CA)	pdaf_odp_llength	dddd dddd dddd dddd	1158 (0x0486)
R13008 (R0x32D0)	pe_param_addr	dddd dddd dddd dddd	0 (0x0000)
R13012 (R0x32D4)	pe_param_value	dddd dddd dddd dddd	0 (0x0000)
R13106 (R0x3332)	read_mode2	dddd 0000 0000 0000	0 (0x0000)
R13120 (R0x3340)	lp_ctx_ctrl	0000 0000 0000 000d	0 (0x0000)
R13122 (R0x3342)	lp_ctx_cnth	dddd dddd dddd dddd	0 (0x0000)
R13124 (R0x3344)	lp_ctx_cntl	dddd dddd dddd dddd	0 (0x0000)
R13824 (R0x3600)	p_gr_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13826 (R0x3602)	p_gr_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13828 (R0x3604)	p_gr_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13830 (R0x3606)	p_gr_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13832 (R0x3608)	p_gr_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13834 (R0x360A)	p_rd_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13836 (R0x360C)	p_rd_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13838 (R0x360E)	p_rd_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13840 (R0x3610)	p_rd_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13842 (R0x3612)	p_rd_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13844 (R0x3614)	p_bl_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13846 (R0x3616)	p_bl_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13848 (R0x3618)	p_bl_p0q2	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R13850 (R0x361A)	p_bl_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13852 (R0x361C)	p_bl_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13854 (R0x361E)	p_gb_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13856 (R0x3620)	p_gb_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13858 (R0x3622)	p_gb_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13860 (R0x3624)	p_gb_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13862 (R0x3626)	p_gb_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13888 (R0x3640)	p_gr_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13890 (R0x3642)	p_gr_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13892 (R0x3644)	p_gr_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13894 (R0x3646)	p_gr_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13896 (R0x3648)	p_gr_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13898 (R0x364A)	p_rd_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13900 (R0x364C)	p_rd_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13902 (R0x364E)	p_rd_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13904 (R0x3650)	p_rd_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13906 (R0x3652)	p_rd_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13908 (R0x3654)	p_bl_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13910 (R0x3656)	p_bl_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13912 (R0x3658)	p_bl_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13914 (R0x365A)	p_bl_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13916 (R0x365C)	p_bl_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13918 (R0x365E)	p_gb_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13920 (R0x3660)	p_gb_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13922 (R0x3662)	p_gb_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13924 (R0x3664)	p_gb_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13926 (R0x3666)	p_gb_p1q4	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R13952 (R0x3680)	p_gr_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13954 (R0x3682)	p_gr_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13956 (R0x3684)	p_gr_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13958 (R0x3686)	p_gr_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13960 (R0x3688)	p_gr_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13962 (R0x368A)	p_rd_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13964 (R0x368C)	p_rd_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13966 (R0x368E)	p_rd_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13968 (R0x3690)	p_rd_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13970 (R0x3692)	p_rd_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13972 (R0x3694)	p_bl_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13974 (R0x3696)	p_bl_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13976 (R0x3698)	p_bl_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13978 (R0x369A)	p_bl_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13980 (R0x369C)	p_bl_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13982 (R0x369E)	p_gb_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13984 (R0x36A0)	p_gb_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13986 (R0x36A2)	p_gb_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13988 (R0x36A4)	p_gb_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13990 (R0x36A6)	p_gb_p2q4	dddd dddd dddd dddd	0 (0x0000)
R14016 (R0x36C0)	p_gr_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14018 (R0x36C2)	p_gr_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14020 (R0x36C4)	p_gr_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14022 (R0x36C6)	p_gr_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14024 (R0x36C8)	p_gr_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14026 (R0x36CA)	p_rd_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14028 (R0x36CC)	p_rd_p3q1	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14030 (R0x36CE)	p_rd_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14032 (R0x36D0)	p_rd_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14034 (R0x36D2)	p_rd_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14036 (R0x36D4)	p_bl_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14038 (R0x36D6)	p_bl_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14040 (R0x36D8)	p_bl_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14042 (R0x36DA)	p_bl_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14044 (R0x36DC)	p_bl_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14046 (R0x36DE)	p_gb_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14048 (R0x36E0)	p_gb_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14050 (R0x36E2)	p_gb_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14052 (R0x36E4)	p_gb_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14054 (R0x36E6)	p_gb_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14080 (R0x3700)	p_gr_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14082 (R0x3702)	p_gr_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14084 (R0x3704)	p_gr_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14086 (R0x3706)	p_gr_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14088 (R0x3708)	p_gr_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14090 (R0x370A)	p_rd_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14092 (R0x370C)	p_rd_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14094 (R0x370E)	p_rd_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14096 (R0x3710)	p_rd_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14098 (R0x3712)	p_rd_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14100 (R0x3714)	p_bl_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14102 (R0x3716)	p_bl_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14104 (R0x3718)	p_bl_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14106 (R0x371A)	p_bl_p4q3	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14108 (R0x371C)	p_bl_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14110 (R0x371E)	p_gb_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14112 (R0x3720)	p_gb_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14114 (R0x3722)	p_gb_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14116 (R0x3724)	p_gb_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14118 (R0x3726)	p_gb_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14208 (R0x3780)	poly_sc_enable	d000 0000 0000 0000	0 (0x0000)
R14210 (R0x3782)	poly_origin_c	000d dddd dddd dddd	2895 (0x0B4F)
R14212 (R0x3784)	poly_origin_r	000d dddd dddd dddd	2167 (0x0877)
R14272 (R0x37C0)	p_gr_q5	dddd dddd dddd dddd	0 (0x0000)
R14274 (R0x37C2)	p_rd_q5	dddd dddd dddd dddd	0 (0x0000)
R14276 (R0x37C4)	p_bl_q5	dddd dddd dddd dddd	0 (0x0000)
R14278 (R0x37C6)	p_gb_q5	dddd dddd dddd dddd	0 (0x0000)
R14336 (R0x3800)	otpm_data_000	dddd dddd dddd dddd	0 (0x0000)
R14338 (R0x3802)	otpm_data_001	dddd dddd dddd dddd	0 (0x0000)
R14340 (R0x3804)	otpm_data_002	dddd dddd dddd dddd	0 (0x0000)
R14342 (R0x3806)	otpm_data_003	dddd dddd dddd dddd	0 (0x0000)
R14344 (R0x3808)	otpm_data_004	dddd dddd dddd dddd	0 (0x0000)
R14346 (R0x380A)	otpm_data_005	dddd dddd dddd dddd	0 (0x0000)
R14348 (R0x380C)	otpm_data_006	dddd dddd dddd dddd	0 (0x0000)
R14350 (R0x380E)	otpm_data_007	dddd dddd dddd dddd	0 (0x0000)
R14352 (R0x3810)	otpm_data_008	dddd dddd dddd dddd	0 (0x0000)
R14354 (R0x3812)	otpm_data_009	dddd dddd dddd dddd	0 (0x0000)
R14356 (R0x3814)	otpm_data_010	dddd dddd dddd dddd	0 (0x0000)
R14358 (R0x3816)	otpm_data_011	dddd dddd dddd dddd	0 (0x0000)
R14360 (R0x3818)	otpm_data_012	dddd dddd dddd dddd	0 (0x0000)
R14362 (R0x381A)	otpm_data_013	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14364 (R0x381C)	otpm_data_014	dddd dddd dddd dddd	0 (0x0000)
R14366 (R0x381E)	otpm_data_015	dddd dddd dddd dddd	0 (0x0000)
R14368 (R0x3820)	otpm_data_016	dddd dddd dddd dddd	0 (0x0000)
R14370 (R0x3822)	otpm_data_017	dddd dddd dddd dddd	0 (0x0000)
R14372 (R0x3824)	otpm_data_018	dddd dddd dddd dddd	0 (0x0000)
R14374 (R0x3826)	otpm_data_019	dddd dddd dddd dddd	0 (0x0000)
R14376 (R0x3828)	otpm_data_020	dddd dddd dddd dddd	0 (0x0000)
R14378 (R0x382A)	otpm_data_021	dddd dddd dddd dddd	0 (0x0000)
R14380 (R0x382C)	otpm_data_022	dddd dddd dddd dddd	0 (0x0000)
R14382 (R0x382E)	otpm_data_023	dddd dddd dddd dddd	0 (0x0000)
R14384 (R0x3830)	otpm_data_024	dddd dddd dddd dddd	0 (0x0000)
R14386 (R0x3832)	otpm_data_025	dddd dddd dddd dddd	0 (0x0000)
R14388 (R0x3834)	otpm_data_026	dddd dddd dddd dddd	0 (0x0000)
R14390 (R0x3836)	otpm_data_027	dddd dddd dddd dddd	0 (0x0000)
R14392 (R0x3838)	otpm_data_028	dddd dddd dddd dddd	0 (0x0000)
R14394 (R0x383A)	otpm_data_029	dddd dddd dddd dddd	0 (0x0000)
R14396 (R0x383C)	otpm_data_030	dddd dddd dddd dddd	0 (0x0000)
R14398 (R0x383E)	otpm_data_031	dddd dddd dddd dddd	0 (0x0000)
R14400 (R0x3840)	otpm_data_032	dddd dddd dddd dddd	0 (0x0000)
R14402 (R0x3842)	otpm_data_033	dddd dddd dddd dddd	0 (0x0000)
R14404 (R0x3844)	otpm_data_034	dddd dddd dddd dddd	0 (0x0000)
R14406 (R0x3846)	otpm_data_035	dddd dddd dddd dddd	0 (0x0000)
R14408 (R0x3848)	otpm_data_036	dddd dddd dddd dddd	0 (0x0000)
R14410 (R0x384A)	otpm_data_037	dddd dddd dddd dddd	0 (0x0000)
R14412 (R0x384C)	otpm_data_038	dddd dddd dddd dddd	0 (0x0000)
R14414 (R0x384E)	otpm_data_039	dddd dddd dddd dddd	0 (0x0000)
R14416 (R0x3850)	otpm_data_040	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14418 (R0x3852)	otpm_data_041	dddd dddd dddd dddd	0 (0x0000)
R14420 (R0x3854)	otpm_data_042	dddd dddd dddd dddd	0 (0x0000)
R14422 (R0x3856)	otpm_data_043	dddd dddd dddd dddd	0 (0x0000)
R14424 (R0x3858)	otpm_data_044	dddd dddd dddd dddd	0 (0x0000)
R14426 (R0x385A)	otpm_data_045	dddd dddd dddd dddd	0 (0x0000)
R14428 (R0x385C)	otpm_data_046	dddd dddd dddd dddd	0 (0x0000)
R14430 (R0x385E)	otpm_data_047	dddd dddd dddd dddd	0 (0x0000)
R14432 (R0x3860)	otpm_data_048	dddd dddd dddd dddd	0 (0x0000)
R14434 (R0x3862)	otpm_data_049	dddd dddd dddd dddd	0 (0x0000)
R14436 (R0x3864)	otpm_data_050	dddd dddd dddd dddd	0 (0x0000)
R14438 (R0x3866)	otpm_data_051	dddd dddd dddd dddd	0 (0x0000)
R14440 (R0x3868)	otpm_data_052	dddd dddd dddd dddd	0 (0x0000)
R14442 (R0x386A)	otpm_data_053	dddd dddd dddd dddd	0 (0x0000)
R14444 (R0x386C)	otpm_data_054	dddd dddd dddd dddd	0 (0x0000)
R14446 (R0x386E)	otpm_data_055	dddd dddd dddd dddd	0 (0x0000)
R14448 (R0x3870)	otpm_data_056	dddd dddd dddd dddd	0 (0x0000)
R14450 (R0x3872)	otpm_data_057	dddd dddd dddd dddd	0 (0x0000)
R14452 (R0x3874)	otpm_data_058	dddd dddd dddd dddd	0 (0x0000)
R14454 (R0x3876)	otpm_data_059	dddd dddd dddd dddd	0 (0x0000)
R14456 (R0x3878)	otpm_data_060	dddd dddd dddd dddd	0 (0x0000)
R14458 (R0x387A)	otpm_data_061	dddd dddd dddd dddd	0 (0x0000)
R14460 (R0x387C)	otpm_data_062	dddd dddd dddd dddd	0 (0x0000)
R14462 (R0x387E)	otpm_data_063	dddd dddd dddd dddd	0 (0x0000)
R14464 (R0x3880)	otpm_data_064	dddd dddd dddd dddd	0 (0x0000)
R14466 (R0x3882)	otpm_data_065	dddd dddd dddd dddd	0 (0x0000)
R14468 (R0x3884)	otpm_data_066	dddd dddd dddd dddd	0 (0x0000)
R14470 (R0x3886)	otpm_data_067	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14472 (R0x3888)	otpm_data_068	dddd dddd dddd dddd	0 (0x0000)
R14474 (R0x388A)	otpm_data_069	dddd dddd dddd dddd	0 (0x0000)
R14476 (R0x388C)	otpm_data_070	dddd dddd dddd dddd	0 (0x0000)
R14478 (R0x388E)	otpm_data_071	dddd dddd dddd dddd	0 (0x0000)
R14480 (R0x3890)	otpm_data_072	dddd dddd dddd dddd	0 (0x0000)
R14482 (R0x3892)	otpm_data_073	dddd dddd dddd dddd	0 (0x0000)
R14484 (R0x3894)	otpm_data_074	dddd dddd dddd dddd	0 (0x0000)
R14486 (R0x3896)	otpm_data_075	dddd dddd dddd dddd	0 (0x0000)
R14488 (R0x3898)	otpm_data_076	dddd dddd dddd dddd	0 (0x0000)
R14490 (R0x389A)	otpm_data_077	dddd dddd dddd dddd	0 (0x0000)
R14492 (R0x389C)	otpm_data_078	dddd dddd dddd dddd	0 (0x0000)
R14494 (R0x389E)	otpm_data_079	dddd dddd dddd dddd	0 (0x0000)
R14496 (R0x38A0)	otpm_data_080	dddd dddd dddd dddd	0 (0x0000)
R14498 (R0x38A2)	otpm_data_081	dddd dddd dddd dddd	0 (0x0000)
R14500 (R0x38A4)	otpm_data_082	dddd dddd dddd dddd	0 (0x0000)
R14502 (R0x38A6)	otpm_data_083	dddd dddd dddd dddd	0 (0x0000)
R14504 (R0x38A8)	otpm_data_084	dddd dddd dddd dddd	0 (0x0000)
R14506 (R0x38AA)	otpm_data_085	dddd dddd dddd dddd	0 (0x0000)
R14508 (R0x38AC)	otpm_data_086	dddd dddd dddd dddd	0 (0x0000)
R14510 (R0x38AE)	otpm_data_087	dddd dddd dddd dddd	0 (0x0000)
R14512 (R0x38B0)	otpm_data_088	dddd dddd dddd dddd	0 (0x0000)
R14514 (R0x38B2)	otpm_data_089	dddd dddd dddd dddd	0 (0x0000)
R14516 (R0x38B4)	otpm_data_090	dddd dddd dddd dddd	0 (0x0000)
R14518 (R0x38B6)	otpm_data_091	dddd dddd dddd dddd	0 (0x0000)
R14520 (R0x38B8)	otpm_data_092	dddd dddd dddd dddd	0 (0x0000)
R14522 (R0x38BA)	otpm_data_093	dddd dddd dddd dddd	0 (0x0000)
R14524 (R0x38BC)	otpm_data_094	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14526 (R0x38BE)	otpm_data_095	dddd dddd dddd dddd	0 (0x0000)
R14528 (R0x38C0)	otpm_data_096	dddd dddd dddd dddd	0 (0x0000)
R14530 (R0x38C2)	otpm_data_097	dddd dddd dddd dddd	0 (0x0000)
R14532 (R0x38C4)	otpm_data_098	dddd dddd dddd dddd	0 (0x0000)
R14534 (R0x38C6)	otpm_data_099	dddd dddd dddd dddd	0 (0x0000)
R14536 (R0x38C8)	otpm_data_100	dddd dddd dddd dddd	0 (0x0000)
R14538 (R0x38CA)	otpm_data_101	dddd dddd dddd dddd	0 (0x0000)
R14540 (R0x38CC)	otpm_data_102	dddd dddd dddd dddd	0 (0x0000)
R14542 (R0x38CE)	otpm_data_103	dddd dddd dddd dddd	0 (0x0000)
R14544 (R0x38D0)	otpm_data_104	dddd dddd dddd dddd	0 (0x0000)
R14546 (R0x38D2)	otpm_data_105	dddd dddd dddd dddd	0 (0x0000)
R14548 (R0x38D4)	otpm_data_106	dddd dddd dddd dddd	0 (0x0000)
R14550 (R0x38D6)	otpm_data_107	dddd dddd dddd dddd	0 (0x0000)
R14552 (R0x38D8)	otpm_data_108	dddd dddd dddd dddd	0 (0x0000)
R14554 (R0x38DA)	otpm_data_109	dddd dddd dddd dddd	0 (0x0000)
R14556 (R0x38DC)	otpm_data_110	dddd dddd dddd dddd	0 (0x0000)
R14558 (R0x38DE)	otpm_data_111	dddd dddd dddd dddd	0 (0x0000)
R14560 (R0x38E0)	otpm_data_112	dddd dddd dddd dddd	0 (0x0000)
R14562 (R0x38E2)	otpm_data_113	dddd dddd dddd dddd	0 (0x0000)
R14564 (R0x38E4)	otpm_data_114	dddd dddd dddd dddd	0 (0x0000)
R14566 (R0x38E6)	otpm_data_115	dddd dddd dddd dddd	0 (0x0000)
R14568 (R0x38E8)	otpm_data_116	dddd dddd dddd dddd	0 (0x0000)
R14570 (R0x38EA)	otpm_data_117	dddd dddd dddd dddd	0 (0x0000)
R14572 (R0x38EC)	otpm_data_118	dddd dddd dddd dddd	0 (0x0000)
R14574 (R0x38EE)	otpm_data_119	dddd dddd dddd dddd	0 (0x0000)
R14576 (R0x38F0)	otpm_data_120	dddd dddd dddd dddd	0 (0x0000)
R14578 (R0x38F2)	otpm_data_121	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14580 (R0x38F4)	otpm_data_122	dddd dddd dddd dddd	0 (0x0000)
R14582 (R0x38F6)	otpm_data_123	dddd dddd dddd dddd	0 (0x0000)
R14584 (R0x38F8)	otpm_data_124	dddd dddd dddd dddd	0 (0x0000)
R14586 (R0x38FA)	otpm_data_125	dddd dddd dddd dddd	0 (0x0000)
R14588 (R0x38FC)	otpm_data_126	dddd dddd dddd dddd	0 (0x0000)
R14590 (R0x38FE)	otpm_data_127	dddd dddd dddd dddd	0 (0x0000)
R14592 (R0x3900)	otpm_data_128	dddd dddd dddd dddd	0 (0x0000)
R14594 (R0x3902)	otpm_data_129	dddd dddd dddd dddd	0 (0x0000)
R14596 (R0x3904)	otpm_data_130	dddd dddd dddd dddd	0 (0x0000)
R14598 (R0x3906)	otpm_data_131	dddd dddd dddd dddd	0 (0x0000)
R14600 (R0x3908)	otpm_data_132	dddd dddd dddd dddd	0 (0x0000)
R14602 (R0x390A)	otpm_data_133	dddd dddd dddd dddd	0 (0x0000)
R14604 (R0x390C)	otpm_data_134	dddd dddd dddd dddd	0 (0x0000)
R14606 (R0x390E)	otpm_data_135	dddd dddd dddd dddd	0 (0x0000)
R14608 (R0x3910)	otpm_data_136	dddd dddd dddd dddd	0 (0x0000)
R14610 (R0x3912)	otpm_data_137	dddd dddd dddd dddd	0 (0x0000)
R14612 (R0x3914)	otpm_data_138	dddd dddd dddd dddd	0 (0x0000)
R14614 (R0x3916)	otpm_data_139	dddd dddd dddd dddd	0 (0x0000)
R14616 (R0x3918)	otpm_data_140	dddd dddd dddd dddd	0 (0x0000)
R14618 (R0x391A)	otpm_data_141	dddd dddd dddd dddd	0 (0x0000)
R14620 (R0x391C)	otpm_data_142	dddd dddd dddd dddd	0 (0x0000)
R14622 (R0x391E)	otpm_data_143	dddd dddd dddd dddd	0 (0x0000)
R14624 (R0x3920)	otpm_data_144	dddd dddd dddd dddd	0 (0x0000)
R14626 (R0x3922)	otpm_data_145	dddd dddd dddd dddd	0 (0x0000)
R14628 (R0x3924)	otpm_data_146	dddd dddd dddd dddd	0 (0x0000)
R14630 (R0x3926)	otpm_data_147	dddd dddd dddd dddd	0 (0x0000)
R14632 (R0x3928)	otpm_data_148	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14634 (R0x392A)	otpm_data_149	dddd dddd dddd dddd	0 (0x0000)
R14636 (R0x392C)	otpm_data_150	dddd dddd dddd dddd	0 (0x0000)
R14638 (R0x392E)	otpm_data_151	dddd dddd dddd dddd	0 (0x0000)
R14640 (R0x3930)	otpm_data_152	dddd dddd dddd dddd	0 (0x0000)
R14642 (R0x3932)	otpm_data_153	dddd dddd dddd dddd	0 (0x0000)
R14644 (R0x3934)	otpm_data_154	dddd dddd dddd dddd	0 (0x0000)
R14646 (R0x3936)	otpm_data_155	dddd dddd dddd dddd	0 (0x0000)
R14648 (R0x3938)	otpm_data_156	dddd dddd dddd dddd	0 (0x0000)
R14650 (R0x393A)	otpm_data_157	dddd dddd dddd dddd	0 (0x0000)
R14652 (R0x393C)	otpm_data_158	dddd dddd dddd dddd	0 (0x0000)
R14654 (R0x393E)	otpm_data_159	dddd dddd dddd dddd	0 (0x0000)
R14656 (R0x3940)	otpm_data_160	dddd dddd dddd dddd	0 (0x0000)
R14658 (R0x3942)	otpm_data_161	dddd dddd dddd dddd	0 (0x0000)
R14660 (R0x3944)	otpm_data_162	dddd dddd dddd dddd	0 (0x0000)
R14662 (R0x3946)	otpm_data_163	dddd dddd dddd dddd	0 (0x0000)
R14664 (R0x3948)	otpm_data_164	dddd dddd dddd dddd	0 (0x0000)
R14666 (R0x394A)	otpm_data_165	dddd dddd dddd dddd	0 (0x0000)
R14668 (R0x394C)	otpm_data_166	dddd dddd dddd dddd	0 (0x0000)
R14670 (R0x394E)	otpm_data_167	dddd dddd dddd dddd	0 (0x0000)
R14672 (R0x3950)	otpm_data_168	dddd dddd dddd dddd	0 (0x0000)
R14674 (R0x3952)	otpm_data_169	dddd dddd dddd dddd	0 (0x0000)
R14676 (R0x3954)	otpm_data_170	dddd dddd dddd dddd	0 (0x0000)
R14678 (R0x3956)	otpm_data_171	dddd dddd dddd dddd	0 (0x0000)
R14680 (R0x3958)	otpm_data_172	dddd dddd dddd dddd	0 (0x0000)
R14682 (R0x395A)	otpm_data_173	dddd dddd dddd dddd	0 (0x0000)
R14684 (R0x395C)	otpm_data_174	dddd dddd dddd dddd	0 (0x0000)
R14686 (R0x395E)	otpm_data_175	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14688 (R0x3960)	otpm_data_176	dddd dddd dddd dddd	0 (0x0000)
R14690 (R0x3962)	otpm_data_177	dddd dddd dddd dddd	0 (0x0000)
R14692 (R0x3964)	otpm_data_178	dddd dddd dddd dddd	0 (0x0000)
R14694 (R0x3966)	otpm_data_179	dddd dddd dddd dddd	0 (0x0000)
R14696 (R0x3968)	otpm_data_180	dddd dddd dddd dddd	0 (0x0000)
R14698 (R0x396A)	otpm_data_181	dddd dddd dddd dddd	0 (0x0000)
R14700 (R0x396C)	otpm_data_182	dddd dddd dddd dddd	0 (0x0000)
R14702 (R0x396E)	otpm_data_183	dddd dddd dddd dddd	0 (0x0000)
R14704 (R0x3970)	otpm_data_184	dddd dddd dddd dddd	0 (0x0000)
R14706 (R0x3972)	otpm_data_185	dddd dddd dddd dddd	0 (0x0000)
R14708 (R0x3974)	otpm_data_186	dddd dddd dddd dddd	0 (0x0000)
R14710 (R0x3976)	otpm_data_187	dddd dddd dddd dddd	0 (0x0000)
R14712 (R0x3978)	otpm_data_188	dddd dddd dddd dddd	0 (0x0000)
R14714 (R0x397A)	otpm_data_189	dddd dddd dddd dddd	0 (0x0000)
R14716 (R0x397C)	otpm_data_190	dddd dddd dddd dddd	0 (0x0000)
R14718 (R0x397E)	otpm_data_191	dddd dddd dddd dddd	0 (0x0000)
R14720 (R0x3980)	otpm_data_192	dddd dddd dddd dddd	0 (0x0000)
R14722 (R0x3982)	otpm_data_193	dddd dddd dddd dddd	0 (0x0000)
R14724 (R0x3984)	otpm_data_194	dddd dddd dddd dddd	0 (0x0000)
R14726 (R0x3986)	otpm_data_195	dddd dddd dddd dddd	0 (0x0000)
R14728 (R0x3988)	otpm_data_196	dddd dddd dddd dddd	0 (0x0000)
R14730 (R0x398A)	otpm_data_197	dddd dddd dddd dddd	0 (0x0000)
R14732 (R0x398C)	otpm_data_198	dddd dddd dddd dddd	0 (0x0000)
R14734 (R0x398E)	otpm_data_199	dddd dddd dddd dddd	0 (0x0000)
R14736 (R0x3990)	otpm_data_200	dddd dddd dddd dddd	0 (0x0000)
R14738 (R0x3992)	otpm_data_201	dddd dddd dddd dddd	0 (0x0000)
R14740 (R0x3994)	otpm_data_202	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14742 (R0x3996)	otpm_data_203	dddd dddd dddd dddd	0 (0x0000)
R14744 (R0x3998)	otpm_data_204	dddd dddd dddd dddd	0 (0x0000)
R14746 (R0x399A)	otpm_data_205	dddd dddd dddd dddd	0 (0x0000)
R14748 (R0x399C)	otpm_data_206	dddd dddd dddd dddd	0 (0x0000)
R14750 (R0x399E)	otpm_data_207	dddd dddd dddd dddd	0 (0x0000)
R14752 (R0x39A0)	otpm_data_208	dddd dddd dddd dddd	0 (0x0000)
R14754 (R0x39A2)	otpm_data_209	dddd dddd dddd dddd	0 (0x0000)
R14756 (R0x39A4)	otpm_data_210	dddd dddd dddd dddd	0 (0x0000)
R14758 (R0x39A6)	otpm_data_211	dddd dddd dddd dddd	0 (0x0000)
R14760 (R0x39A8)	otpm_data_212	dddd dddd dddd dddd	0 (0x0000)
R14762 (R0x39AA)	otpm_data_213	dddd dddd dddd dddd	0 (0x0000)
R14764 (R0x39AC)	otpm_data_214	dddd dddd dddd dddd	0 (0x0000)
R14766 (R0x39AE)	otpm_data_215	dddd dddd dddd dddd	0 (0x0000)
R14768 (R0x39B0)	otpm_data_216	dddd dddd dddd dddd	0 (0x0000)
R14770 (R0x39B2)	otpm_data_217	dddd dddd dddd dddd	0 (0x0000)
R14772 (R0x39B4)	otpm_data_218	dddd dddd dddd dddd	0 (0x0000)
R14774 (R0x39B6)	otpm_data_219	dddd dddd dddd dddd	0 (0x0000)
R14776 (R0x39B8)	otpm_data_220	dddd dddd dddd dddd	0 (0x0000)
R14778 (R0x39BA)	otpm_data_221	dddd dddd dddd dddd	0 (0x0000)
R14780 (R0x39BC)	otpm_data_222	dddd dddd dddd dddd	0 (0x0000)
R14782 (R0x39BE)	otpm_data_223	dddd dddd dddd dddd	0 (0x0000)
R14784 (R0x39C0)	otpm_data_224	dddd dddd dddd dddd	0 (0x0000)
R14786 (R0x39C2)	otpm_data_225	dddd dddd dddd dddd	0 (0x0000)
R14788 (R0x39C4)	otpm_data_226	dddd dddd dddd dddd	0 (0x0000)
R14790 (R0x39C6)	otpm_data_227	dddd dddd dddd dddd	0 (0x0000)
R14792 (R0x39C8)	otpm_data_228	dddd dddd dddd dddd	0 (0x0000)
R14794 (R0x39CA)	otpm_data_229	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14796 (R0x39CC)	otpm_data_230	dddd dddd dddd dddd	0 (0x0000)
R14798 (R0x39CE)	otpm_data_231	dddd dddd dddd dddd	0 (0x0000)
R14800 (R0x39D0)	otpm_data_232	dddd dddd dddd dddd	0 (0x0000)
R14802 (R0x39D2)	otpm_data_233	dddd dddd dddd dddd	0 (0x0000)
R14804 (R0x39D4)	otpm_data_234	dddd dddd dddd dddd	0 (0x0000)
R14806 (R0x39D6)	otpm_data_235	dddd dddd dddd dddd	0 (0x0000)
R14808 (R0x39D8)	otpm_data_236	dddd dddd dddd dddd	0 (0x0000)
R14810 (R0x39DA)	otpm_data_237	dddd dddd dddd dddd	0 (0x0000)
R14812 (R0x39DC)	otpm_data_238	dddd dddd dddd dddd	0 (0x0000)
R14814 (R0x39DE)	otpm_data_239	dddd dddd dddd dddd	0 (0x0000)
R14816 (R0x39E0)	otpm_data_240	dddd dddd dddd dddd	0 (0x0000)
R14818 (R0x39E2)	otpm_data_241	dddd dddd dddd dddd	0 (0x0000)
R14820 (R0x39E4)	otpm_data_242	dddd dddd dddd dddd	0 (0x0000)
R14822 (R0x39E6)	otpm_data_243	dddd dddd dddd dddd	0 (0x0000)
R14824 (R0x39E8)	otpm_data_244	dddd dddd dddd dddd	0 (0x0000)
R14826 (R0x39EA)	otpm_data_245	dddd dddd dddd dddd	0 (0x0000)
R14828 (R0x39EC)	otpm_data_246	dddd dddd dddd dddd	0 (0x0000)
R14830 (R0x39EE)	otpm_data_247	dddd dddd dddd dddd	0 (0x0000)
R14832 (R0x39F0)	otpm_data_248	dddd dddd dddd dddd	0 (0x0000)
R14834 (R0x39F2)	otpm_data_249	dddd dddd dddd dddd	0 (0x0000)
R14836 (R0x39F4)	otpm_data_250	dddd dddd dddd dddd	0 (0x0000)
R14838 (R0x39F6)	otpm_data_251	dddd dddd dddd dddd	0 (0x0000)
R14840 (R0x39F8)	otpm_data_252	dddd dddd dddd dddd	0 (0x0000)
R14842 (R0x39FA)	otpm_data_253	dddd dddd dddd dddd	0 (0x0000)
R14844 (R0x39FC)	otpm_data_254	dddd dddd dddd dddd	0 (0x0000)
R14846 (R0x39FE)	otpm_data_255	dddd dddd dddd dddd	0 (0x0000)
R14848 (R0x3A00)	otpm_data_256	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14850 (R0x3A02)	otpm_data_257	dddd dddd dddd dddd	0 (0x0000)
R14852 (R0x3A04)	otpm_data_258	dddd dddd dddd dddd	0 (0x0000)
R14854 (R0x3A06)	otpm_data_259	dddd dddd dddd dddd	0 (0x0000)
R14856 (R0x3A08)	otpm_data_260	dddd dddd dddd dddd	0 (0x0000)
R14858 (R0x3A0A)	otpm_data_261	dddd dddd dddd dddd	0 (0x0000)
R14860 (R0x3A0C)	otpm_data_262	dddd dddd dddd dddd	0 (0x0000)
R14862 (R0x3A0E)	otpm_data_263	dddd dddd dddd dddd	0 (0x0000)
R14864 (R0x3A10)	otpm_data_264	dddd dddd dddd dddd	0 (0x0000)
R14866 (R0x3A12)	otpm_data_265	dddd dddd dddd dddd	0 (0x0000)
R14868 (R0x3A14)	otpm_data_266	dddd dddd dddd dddd	0 (0x0000)
R14870 (R0x3A16)	otpm_data_267	dddd dddd dddd dddd	0 (0x0000)
R14872 (R0x3A18)	otpm_data_268	dddd dddd dddd dddd	0 (0x0000)
R14874 (R0x3A1A)	otpm_data_269	dddd dddd dddd dddd	0 (0x0000)
R14876 (R0x3A1C)	otpm_data_270	dddd dddd dddd dddd	0 (0x0000)
R14878 (R0x3A1E)	otpm_data_271	dddd dddd dddd dddd	0 (0x0000)
R14880 (R0x3A20)	otpm_data_272	dddd dddd dddd dddd	0 (0x0000)
R14882 (R0x3A22)	otpm_data_273	dddd dddd dddd dddd	0 (0x0000)
R14884 (R0x3A24)	otpm_data_274	dddd dddd dddd dddd	0 (0x0000)
R14886 (R0x3A26)	otpm_data_275	dddd dddd dddd dddd	0 (0x0000)
R14888 (R0x3A28)	otpm_data_276	dddd dddd dddd dddd	0 (0x0000)
R14890 (R0x3A2A)	otpm_data_277	dddd dddd dddd dddd	0 (0x0000)
R14892 (R0x3A2C)	otpm_data_278	dddd dddd dddd dddd	0 (0x0000)
R14894 (R0x3A2E)	otpm_data_279	dddd dddd dddd dddd	0 (0x0000)
R14896 (R0x3A30)	otpm_data_280	dddd dddd dddd dddd	0 (0x0000)
R14898 (R0x3A32)	otpm_data_281	dddd dddd dddd dddd	0 (0x0000)
R14900 (R0x3A34)	otpm_data_282	dddd dddd dddd dddd	0 (0x0000)
R14902 (R0x3A36)	otpm_data_283	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14904 (R0x3A38)	otpm_data_284	dddd dddd dddd dddd	0 (0x0000)
R14906 (R0x3A3A)	otpm_data_285	dddd dddd dddd dddd	0 (0x0000)
R14908 (R0x3A3C)	otpm_data_286	dddd dddd dddd dddd	0 (0x0000)
R14910 (R0x3A3E)	otpm_data_287	dddd dddd dddd dddd	0 (0x0000)
R14912 (R0x3A40)	otpm_data_288	dddd dddd dddd dddd	0 (0x0000)
R14914 (R0x3A42)	otpm_data_289	dddd dddd dddd dddd	0 (0x0000)
R14916 (R0x3A44)	otpm_data_290	dddd dddd dddd dddd	0 (0x0000)
R14918 (R0x3A46)	otpm_data_291	dddd dddd dddd dddd	0 (0x0000)
R14920 (R0x3A48)	otpm_data_292	dddd dddd dddd dddd	0 (0x0000)
R14922 (R0x3A4A)	otpm_data_293	dddd dddd dddd dddd	0 (0x0000)
R14924 (R0x3A4C)	otpm_data_294	dddd dddd dddd dddd	0 (0x0000)
R14926 (R0x3A4E)	otpm_data_295	dddd dddd dddd dddd	0 (0x0000)
R14928 (R0x3A50)	otpm_data_296	dddd dddd dddd dddd	0 (0x0000)
R14930 (R0x3A52)	otpm_data_297	dddd dddd dddd dddd	0 (0x0000)
R14932 (R0x3A54)	otpm_data_298	dddd dddd dddd dddd	0 (0x0000)
R14934 (R0x3A56)	otpm_data_299	dddd dddd dddd dddd	0 (0x0000)
R14936 (R0x3A58)	otpm_data_300	dddd dddd dddd dddd	0 (0x0000)
R14938 (R0x3A5A)	otpm_data_301	dddd dddd dddd dddd	0 (0x0000)
R14940 (R0x3A5C)	otpm_data_302	dddd dddd dddd dddd	0 (0x0000)
R14942 (R0x3A5E)	otpm_data_303	dddd dddd dddd dddd	0 (0x0000)
R14944 (R0x3A60)	otpm_data_304	dddd dddd dddd dddd	0 (0x0000)
R14946 (R0x3A62)	otpm_data_305	dddd dddd dddd dddd	0 (0x0000)
R14948 (R0x3A64)	otpm_data_306	dddd dddd dddd dddd	0 (0x0000)
R14950 (R0x3A66)	otpm_data_307	dddd dddd dddd dddd	0 (0x0000)
R14952 (R0x3A68)	otpm_data_308	dddd dddd dddd dddd	0 (0x0000)
R14954 (R0x3A6A)	otpm_data_309	dddd dddd dddd dddd	0 (0x0000)
R14956 (R0x3A6C)	otpm_data_310	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R14958 (R0x3A6E)	otpm_data_311	dddd dddd dddd dddd	0 (0x0000)
R14960 (R0x3A70)	otpm_data_312	dddd dddd dddd dddd	0 (0x0000)
R14962 (R0x3A72)	otpm_data_313	dddd dddd dddd dddd	0 (0x0000)
R14964 (R0x3A74)	otpm_data_314	dddd dddd dddd dddd	0 (0x0000)
R14966 (R0x3A76)	otpm_data_315	dddd dddd dddd dddd	0 (0x0000)
R14968 (R0x3A78)	otpm_data_316	dddd dddd dddd dddd	0 (0x0000)
R14970 (R0x3A7A)	otpm_data_317	dddd dddd dddd dddd	0 (0x0000)
R14972 (R0x3A7C)	otpm_data_318	dddd dddd dddd dddd	0 (0x0000)
R14974 (R0x3A7E)	otpm_data_319	dddd dddd dddd dddd	0 (0x0000)
R14976 (R0x3A80)	otpm_data_320	dddd dddd dddd dddd	0 (0x0000)
R14978 (R0x3A82)	otpm_data_321	dddd dddd dddd dddd	0 (0x0000)
R14980 (R0x3A84)	otpm_data_322	dddd dddd dddd dddd	0 (0x0000)
R14982 (R0x3A86)	otpm_data_323	dddd dddd dddd dddd	0 (0x0000)
R14984 (R0x3A88)	otpm_data_324	dddd dddd dddd dddd	0 (0x0000)
R14986 (R0x3A8A)	otpm_data_325	dddd dddd dddd dddd	0 (0x0000)
R14988 (R0x3A8C)	otpm_data_326	dddd dddd dddd dddd	0 (0x0000)
R14990 (R0x3A8E)	otpm_data_327	dddd dddd dddd dddd	0 (0x0000)
R14992 (R0x3A90)	otpm_data_328	dddd dddd dddd dddd	0 (0x0000)
R14994 (R0x3A92)	otpm_data_329	dddd dddd dddd dddd	0 (0x0000)
R14996 (R0x3A94)	otpm_data_330	dddd dddd dddd dddd	0 (0x0000)
R14998 (R0x3A96)	otpm_data_331	dddd dddd dddd dddd	0 (0x0000)
R15000 (R0x3A98)	otpm_data_332	dddd dddd dddd dddd	0 (0x0000)
R15002 (R0x3A9A)	otpm_data_333	dddd dddd dddd dddd	0 (0x0000)
R15004 (R0x3A9C)	otpm_data_334	dddd dddd dddd dddd	0 (0x0000)
R15006 (R0x3A9E)	otpm_data_335	dddd dddd dddd dddd	0 (0x0000)
R15008 (R0x3AA0)	otpm_data_336	dddd dddd dddd dddd	0 (0x0000)
R15010 (R0x3AA2)	otpm_data_337	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R15012 (R0x3AA4)	otpm_data_338	dddd dddd dddd dddd	0 (0x0000)
R15014 (R0x3AA6)	otpm_data_339	dddd dddd dddd dddd	0 (0x0000)
R15016 (R0x3AA8)	otpm_data_340	dddd dddd dddd dddd	0 (0x0000)
R15018 (R0x3AAA)	otpm_data_341	dddd dddd dddd dddd	0 (0x0000)
R15020 (R0x3AAC)	otpm_data_342	dddd dddd dddd dddd	0 (0x0000)
R15022 (R0x3AAE)	otpm_data_343	dddd dddd dddd dddd	0 (0x0000)
R15024 (R0x3AB0)	otpm_data_344	dddd dddd dddd dddd	0 (0x0000)
R15026 (R0x3AB2)	otpm_data_345	dddd dddd dddd dddd	0 (0x0000)
R15028 (R0x3AB4)	otpm_data_346	dddd dddd dddd dddd	0 (0x0000)
R15030 (R0x3AB6)	otpm_data_347	dddd dddd dddd dddd	0 (0x0000)
R15032 (R0x3AB8)	otpm_data_348	dddd dddd dddd dddd	0 (0x0000)
R15034 (R0x3ABA)	otpm_data_349	dddd dddd dddd dddd	0 (0x0000)
R15036 (R0x3ABC)	otpm_data_350	dddd dddd dddd dddd	0 (0x0000)
R15038 (R0x3ABE)	otpm_data_351	dddd dddd dddd dddd	0 (0x0000)
R15040 (R0x3AC0)	otpm_data_352	dddd dddd dddd dddd	0 (0x0000)
R15042 (R0x3AC2)	otpm_data_353	dddd dddd dddd dddd	0 (0x0000)
R15044 (R0x3AC4)	otpm_data_354	dddd dddd dddd dddd	0 (0x0000)
R15046 (R0x3AC6)	otpm_data_355	dddd dddd dddd dddd	0 (0x0000)
R15048 (R0x3AC8)	otpm_data_356	dddd dddd dddd dddd	0 (0x0000)
R15050 (R0x3ACA)	otpm_data_357	dddd dddd dddd dddd	0 (0x0000)
R15052 (R0x3ACC)	otpm_data_358	dddd dddd dddd dddd	0 (0x0000)
R15054 (R0x3ACE)	otpm_data_359	dddd dddd dddd dddd	0 (0x0000)
R15056 (R0x3AD0)	otpm_data_360	dddd dddd dddd dddd	0 (0x0000)
R15058 (R0x3AD2)	otpm_data_361	dddd dddd dddd dddd	0 (0x0000)
R15060 (R0x3AD4)	otpm_data_362	dddd dddd dddd dddd	0 (0x0000)
R15062 (R0x3AD6)	otpm_data_363	dddd dddd dddd dddd	0 (0x0000)
R15064 (R0x3AD8)	otpm_data_364	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R15066 (R0x3ADA)	otpm_data_365	dddd dddd dddd dddd	0 (0x0000)
R15068 (R0x3ADC)	otpm_data_366	dddd dddd dddd dddd	0 (0x0000)
R15070 (R0x3ADE)	otpm_data_367	dddd dddd dddd dddd	0 (0x0000)
R15072 (R0x3AE0)	otpm_data_368	dddd dddd dddd dddd	0 (0x0000)
R15074 (R0x3AE2)	otpm_data_369	dddd dddd dddd dddd	0 (0x0000)
R15076 (R0x3AE4)	otpm_data_370	dddd dddd dddd dddd	0 (0x0000)
R15078 (R0x3AE6)	otpm_data_371	dddd dddd dddd dddd	0 (0x0000)
R15080 (R0x3AE8)	otpm_data_372	dddd dddd dddd dddd	0 (0x0000)
R15082 (R0x3AEA)	otpm_data_373	dddd dddd dddd dddd	0 (0x0000)
R15084 (R0x3AEC)	otpm_data_374	dddd dddd dddd dddd	0 (0x0000)
R15086 (R0x3AEE)	otpm_data_375	dddd dddd dddd dddd	0 (0x0000)
R15088 (R0x3AF0)	otpm_data_376	dddd dddd dddd dddd	0 (0x0000)
R15090 (R0x3AF2)	otpm_data_377	dddd dddd dddd dddd	0 (0x0000)
R15092 (R0x3AF4)	otpm_data_378	dddd dddd dddd dddd	0 (0x0000)
R15094 (R0x3AF6)	otpm_data_379	dddd dddd dddd dddd	0 (0x0000)
R15096 (R0x3AF8)	otpm_data_380	dddd dddd dddd dddd	0 (0x0000)
R15098 (R0x3AFA)	otpm_data_381	dddd dddd dddd dddd	0 (0x0000)
R15100 (R0x3AFC)	otpm_data_382	dddd dddd dddd dddd	0 (0x0000)
R15102 (R0x3AFE)	otpm_data_383	dddd dddd dddd dddd	0 (0x0000)
R15104 (R0x3B00)	otpm_data_384	dddd dddd dddd dddd	0 (0x0000)
R15106 (R0x3B02)	otpm_data_385	dddd dddd dddd dddd	0 (0x0000)
R15108 (R0x3B04)	otpm_data_386	dddd dddd dddd dddd	0 (0x0000)
R15110 (R0x3B06)	otpm_data_387	dddd dddd dddd dddd	0 (0x0000)
R15112 (R0x3B08)	otpm_data_388	dddd dddd dddd dddd	0 (0x0000)
R15114 (R0x3B0A)	otpm_data_389	dddd dddd dddd dddd	0 (0x0000)
R15116 (R0x3B0C)	otpm_data_390	dddd dddd dddd dddd	0 (0x0000)
R15118 (R0x3B0E)	otpm_data_391	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R15120 (R0x3B10)	otpm_data_392	dddd dddd dddd dddd	0 (0x0000)
R15122 (R0x3B12)	otpm_data_393	dddd dddd dddd dddd	0 (0x0000)
R15124 (R0x3B14)	otpm_data_394	dddd dddd dddd dddd	0 (0x0000)
R15126 (R0x3B16)	otpm_data_395	dddd dddd dddd dddd	0 (0x0000)
R15128 (R0x3B18)	otpm_data_396	dddd dddd dddd dddd	0 (0x0000)
R15130 (R0x3B1A)	otpm_data_397	dddd dddd dddd dddd	0 (0x0000)
R15132 (R0x3B1C)	otpm_data_398	dddd dddd dddd dddd	0 (0x0000)
R15134 (R0x3B1E)	otpm_data_399	dddd dddd dddd dddd	0 (0x0000)
R15136 (R0x3B20)	otpm_data_400	dddd dddd dddd dddd	0 (0x0000)
R15138 (R0x3B22)	otpm_data_401	dddd dddd dddd dddd	0 (0x0000)
R15140 (R0x3B24)	otpm_data_402	dddd dddd dddd dddd	0 (0x0000)
R15142 (R0x3B26)	otpm_data_403	dddd dddd dddd dddd	0 (0x0000)
R15144 (R0x3B28)	otpm_data_404	dddd dddd dddd dddd	0 (0x0000)
R15146 (R0x3B2A)	otpm_data_405	dddd dddd dddd dddd	0 (0x0000)
R15148 (R0x3B2C)	otpm_data_406	dddd dddd dddd dddd	0 (0x0000)
R15150 (R0x3B2E)	otpm_data_407	dddd dddd dddd dddd	0 (0x0000)
R15152 (R0x3B30)	otpm_data_408	dddd dddd dddd dddd	0 (0x0000)
R15154 (R0x3B32)	otpm_data_409	dddd dddd dddd dddd	0 (0x0000)
R15156 (R0x3B34)	otpm_data_410	dddd dddd dddd dddd	0 (0x0000)
R15158 (R0x3B36)	otpm_data_411	dddd dddd dddd dddd	0 (0x0000)
R15160 (R0x3B38)	otpm_data_412	dddd dddd dddd dddd	0 (0x0000)
R15162 (R0x3B3A)	otpm_data_413	dddd dddd dddd dddd	0 (0x0000)
R15164 (R0x3B3C)	otpm_data_414	dddd dddd dddd dddd	0 (0x0000)
R15166 (R0x3B3E)	otpm_data_415	dddd dddd dddd dddd	0 (0x0000)
R15168 (R0x3B40)	otpm_data_416	dddd dddd dddd dddd	0 (0x0000)
R15170 (R0x3B42)	otpm_data_417	dddd dddd dddd dddd	0 (0x0000)
R15172 (R0x3B44)	otpm_data_418	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R15174 (R0x3B46)	otpm_data_419	dddd dddd dddd dddd	0 (0x0000)
R15176 (R0x3B48)	otpm_data_420	dddd dddd dddd dddd	0 (0x0000)
R15178 (R0x3B4A)	otpm_data_421	dddd dddd dddd dddd	0 (0x0000)
R15180 (R0x3B4C)	otpm_data_422	dddd dddd dddd dddd	0 (0x0000)
R15182 (R0x3B4E)	otpm_data_423	dddd dddd dddd dddd	0 (0x0000)
R15184 (R0x3B50)	otpm_data_424	dddd dddd dddd dddd	0 (0x0000)
R15186 (R0x3B52)	otpm_data_425	dddd dddd dddd dddd	0 (0x0000)
R15188 (R0x3B54)	otpm_data_426	dddd dddd dddd dddd	0 (0x0000)
R15190 (R0x3B56)	otpm_data_427	dddd dddd dddd dddd	0 (0x0000)
R15192 (R0x3B58)	otpm_data_428	dddd dddd dddd dddd	0 (0x0000)
R15194 (R0x3B5A)	otpm_data_429	dddd dddd dddd dddd	0 (0x0000)
R15196 (R0x3B5C)	otpm_data_430	dddd dddd dddd dddd	0 (0x0000)
R15198 (R0x3B5E)	otpm_data_431	dddd dddd dddd dddd	0 (0x0000)
R15200 (R0x3B60)	otpm_data_432	dddd dddd dddd dddd	0 (0x0000)
R15202 (R0x3B62)	otpm_data_433	dddd dddd dddd dddd	0 (0x0000)
R15204 (R0x3B64)	otpm_data_434	dddd dddd dddd dddd	0 (0x0000)
R15206 (R0x3B66)	otpm_data_435	dddd dddd dddd dddd	0 (0x0000)
R15208 (R0x3B68)	otpm_data_436	dddd dddd dddd dddd	0 (0x0000)
R15210 (R0x3B6A)	otpm_data_437	dddd dddd dddd dddd	0 (0x0000)
R15212 (R0x3B6C)	otpm_data_438	dddd dddd dddd dddd	0 (0x0000)
R15214 (R0x3B6E)	otpm_data_439	dddd dddd dddd dddd	0 (0x0000)
R15216 (R0x3B70)	otpm_data_440	dddd dddd dddd dddd	0 (0x0000)
R15218 (R0x3B72)	otpm_data_441	dddd dddd dddd dddd	0 (0x0000)
R15220 (R0x3B74)	otpm_data_442	dddd dddd dddd dddd	0 (0x0000)
R15222 (R0x3B76)	otpm_data_443	dddd dddd dddd dddd	0 (0x0000)
R15224 (R0x3B78)	otpm_data_444	dddd dddd dddd dddd	0 (0x0000)
R15226 (R0x3B7A)	otpm_data_445	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R15228 (R0x3B7C)	otpm_data_446	dddd dddd dddd dddd	0 (0x0000)
R15230 (R0x3B7E)	otpm_data_447	dddd dddd dddd dddd	0 (0x0000)
R15232 (R0x3B80)	otpm_data_448	dddd dddd dddd dddd	0 (0x0000)
R15234 (R0x3B82)	otpm_data_449	dddd dddd dddd dddd	0 (0x0000)
R15236 (R0x3B84)	otpm_data_450	dddd dddd dddd dddd	0 (0x0000)
R15238 (R0x3B86)	otpm_data_451	dddd dddd dddd dddd	0 (0x0000)
R15240 (R0x3B88)	otpm_data_452	dddd dddd dddd dddd	0 (0x0000)
R15242 (R0x3B8A)	otpm_data_453	dddd dddd dddd dddd	0 (0x0000)
R15244 (R0x3B8C)	otpm_data_454	dddd dddd dddd dddd	0 (0x0000)
R15246 (R0x3B8E)	otpm_data_455	dddd dddd dddd dddd	0 (0x0000)
R15248 (R0x3B90)	otpm_data_456	dddd dddd dddd dddd	0 (0x0000)
R15250 (R0x3B92)	otpm_data_457	dddd dddd dddd dddd	0 (0x0000)
R15252 (R0x3B94)	otpm_data_458	dddd dddd dddd dddd	0 (0x0000)
R15254 (R0x3B96)	otpm_data_459	dddd dddd dddd dddd	0 (0x0000)
R15256 (R0x3B98)	otpm_data_460	dddd dddd dddd dddd	0 (0x0000)
R15258 (R0x3B9A)	otpm_data_461	dddd dddd dddd dddd	0 (0x0000)
R15260 (R0x3B9C)	otpm_data_462	dddd dddd dddd dddd	0 (0x0000)
R15262 (R0x3B9E)	otpm_data_463	dddd dddd dddd dddd	0 (0x0000)
R15264 (R0x3BA0)	otpm_data_464	dddd dddd dddd dddd	0 (0x0000)
R15266 (R0x3BA2)	otpm_data_465	dddd dddd dddd dddd	0 (0x0000)
R15268 (R0x3BA4)	otpm_data_466	dddd dddd dddd dddd	0 (0x0000)
R15270 (R0x3BA6)	otpm_data_467	dddd dddd dddd dddd	0 (0x0000)
R15272 (R0x3BA8)	otpm_data_468	dddd dddd dddd dddd	0 (0x0000)
R15274 (R0x3BAA)	otpm_data_469	dddd dddd dddd dddd	0 (0x0000)
R15276 (R0x3BAC)	otpm_data_470	dddd dddd dddd dddd	0 (0x0000)
R15278 (R0x3BAE)	otpm_data_471	dddd dddd dddd dddd	0 (0x0000)
R15280 (R0x3BB0)	otpm_data_472	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R15282 (R0x3BB2)	otpm_data_473	dddd dddd dddd dddd	0 (0x0000)
R15284 (R0x3BB4)	otpm_data_474	dddd dddd dddd dddd	0 (0x0000)
R15286 (R0x3BB6)	otpm_data_475	dddd dddd dddd dddd	0 (0x0000)
R15288 (R0x3BB8)	otpm_data_476	dddd dddd dddd dddd	0 (0x0000)
R15290 (R0x3BBA)	otpm_data_477	dddd dddd dddd dddd	0 (0x0000)
R15292 (R0x3BBC)	otpm_data_478	dddd dddd dddd dddd	0 (0x0000)
R15294 (R0x3BBE)	otpm_data_479	dddd dddd dddd dddd	0 (0x0000)
R15296 (R0x3BC0)	otpm_data_480	dddd dddd dddd dddd	0 (0x0000)
R15298 (R0x3BC2)	otpm_data_481	dddd dddd dddd dddd	0 (0x0000)
R15300 (R0x3BC4)	otpm_data_482	dddd dddd dddd dddd	0 (0x0000)
R15302 (R0x3BC6)	otpm_data_483	dddd dddd dddd dddd	0 (0x0000)
R15304 (R0x3BC8)	otpm_data_484	dddd dddd dddd dddd	0 (0x0000)
R15306 (R0x3BCA)	otpm_data_485	dddd dddd dddd dddd	0 (0x0000)
R15308 (R0x3BCC)	otpm_data_486	dddd dddd dddd dddd	0 (0x0000)
R15310 (R0x3BCE)	otpm_data_487	dddd dddd dddd dddd	0 (0x0000)
R15312 (R0x3BD0)	otpm_data_488	dddd dddd dddd dddd	0 (0x0000)
R15314 (R0x3BD2)	otpm_data_489	dddd dddd dddd dddd	0 (0x0000)
R15316 (R0x3BD4)	otpm_data_490	dddd dddd dddd dddd	0 (0x0000)
R15318 (R0x3BD6)	otpm_data_491	dddd dddd dddd dddd	0 (0x0000)
R15320 (R0x3BD8)	otpm_data_492	dddd dddd dddd dddd	0 (0x0000)
R15322 (R0x3BDA)	otpm_data_493	dddd dddd dddd dddd	0 (0x0000)
R15324 (R0x3BDC)	otpm_data_494	dddd dddd dddd dddd	0 (0x0000)
R15326 (R0x3BDE)	otpm_data_495	dddd dddd dddd dddd	0 (0x0000)
R15328 (R0x3BE0)	otpm_data_496	dddd dddd dddd dddd	0 (0x0000)
R15330 (R0x3BE2)	otpm_data_497	dddd dddd dddd dddd	0 (0x0000)
R15332 (R0x3BE4)	otpm_data_498	dddd dddd dddd dddd	0 (0x0000)
R15334 (R0x3BE6)	otpm_data_499	dddd dddd dddd dddd	0 (0x0000)

Table 3. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Name	Data Format (Binary)	Default Value Dec (Hex)
R15336 (R0x3BE8)	otpm_data_500	dddd dddd dddd dddd	0 (0x0000)
R15338 (R0x3BEA)	otpm_data_501	dddd dddd dddd dddd	0 (0x0000)
R15340 (R0x3BEC)	otpm_data_502	dddd dddd dddd dddd	0 (0x0000)
R15342 (R0x3BEE)	otpm_data_503	dddd dddd dddd dddd	0 (0x0000)
R15344 (R0x3BF0)	otpm_data_504	dddd dddd dddd dddd	0 (0x0000)
R15346 (R0x3BF2)	otpm_data_505	dddd dddd dddd dddd	0 (0x0000)
R15348 (R0x3BF4)	otpm_data_506	dddd dddd dddd dddd	0 (0x0000)
R15350 (R0x3BF6)	otpm_data_507	dddd dddd dddd dddd	0 (0x0000)
R15352 (R0x3BF8)	otpm_data_508	dddd dddd dddd dddd	0 (0x0000)
R15354 (R0x3BFA)	otpm_data_509	dddd dddd dddd dddd	0 (0x0000)
R15356 (R0x3BFC)	otpm_data_510	dddd dddd dddd dddd	0 (0x0000)
R15358 (R0x3BFE)	otpm_data_511	dddd dddd dddd dddd	0 (0x0000)
R16160 (R0x3F20)	gth_control	0000 ddd0 00dd d00d	8 (0x0008)
R16168 (R0x3F28)	gth_clip_rtn	dddd dddd dddd dddd	0 (0x0000)
R16186 (R0x3F3A)	analog_control8	0000 0000 dddd dddd	128 (0x0080)
R16188 (R0x3F3C)	analog_control9	0000 0000 0000 d0dd	3 (0x0003)

Table 4. SMIA CONFIGURATION

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R0 (R0x0000)	**15:0**	**0x0253**	**chip_version_reg (R/W)**	**N**	**N**
	This register is an alias of R0x3000−1. Read-only. Can be made read/write by clearing R0x301A−B[3]. Legal values: [0, 65535].				
R2 (R0x0002)	**7:0**	**0x00**	**revision_number (RO)**	**N**	**N**
	ON Semiconductor assigned revision number. Read-only. Can be made read/write by clearing R0x301A−B[3]. Read-only. Legal values: [0, 255].				
R3 (R0x0003)	**7:0**	**0x06**	**manufacturer_id (RO)**	**N**	**N**
	Manufacturer ID assigned to ON Semiconductor. Read-only. Can be made read/write by clearing R0x301A−B[3]. Read-only. Legal values: [0, 255].				
R4 (R0x0004)	**7:0**	**0x0A**	**smia_version (RO)**	**N**	**N**
	This register is an alias of R0x303A. Read-only. Read-only. Legal values: [0, 255].				
R5 (R0x0005)	**7:0**	**0xFF**	**frame_count (RO)**	**N**	**N**
	This register is an alias of R0x303B. Read-only. Read-only. Legal values: [0, 255].				
R6 (R0x0006)	**7:0**	**0x00**	**pixel_order (RO)**	**N**	**N**
	The value in this register changes as a function of R0x3040[1:0]. 00 = First row is GreenR/Red, first pixel is GreenR 01 = First row is GreenR/Red, first pixel is Red 02 = First row is Blue/GreenB, first pixel is Blue 03 = First row is Blue/GreenB, first pixel is GreenB Read-only. Legal values: [0, 3].				
R8 (R0x0008)	**15:0**	**0x002A**	**data_pedestal (R/W)**	**N**	**N**
	This register is an alias of R0x301E−F. Read-only. Can be made read/write by clearing R0x301A−B[3]. Legal values: [0, 1023].				
R64 (R0x0040)	**7:0**	**0x01**	**frame_format_model_type (RO)**	**N**	**N**
	This register is an alias of R0x303B. Read-only. Read-only. Legal values: [0, 255].				
R65 (R0x0041)	**7:0**	**0x12**	**frame_format_model_subtype (RO)**	**N**	**N**
	Number of descriptors: 1 X (column) descriptor and two Y (row) descriptors. Read-only. Read-only. Legal values: [0, 255].				
R66 (R0x0042)	**15:0**	**0x5070**	**frame_format_descriptor_0 (RO)**	**N**	**N**
	X descriptor Bits[11:0] of this register reflect the current value of x_output_size[11:0]. Upper 4 bits is the pixel code; 5 = Visible Pixel Data. Read-only, dynamic. Read-only. Legal values: [0, 65535].				
R68 (R0x0044)	**15:0**	**0x1002**	**frame_format_descriptor_1 (RO)**	**N**	**N**
	Y descriptor In normal operation, returns 0x1000 to indicates that there is no embedded data.				
R70 (R0x0046)	**15:0**	**0x5C30**	**frame_format_descriptor_2 (RO)**	**N**	**N**
	Y descriptor Bits[11:0] of this register reflect the current value of y_output_size[11:0]. Upper 4 bits is the pixel code; 5 = Visible Pixel Data. Read-only, dynamic. Read-only. Legal values: [0, 65535].				
R72 (R0x0048)	**15:0**	**0x0000**	**frame_format_descriptor_3 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R74 (R0x004A)	**15:0**	**0x0000**	**frame_format_descriptor_4 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R76 (R0x004C)	**15:0**	**0x0000**	**frame_format_descriptor_5 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				

Table 4. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R78 (R0x004E)	**15:0**	**0x0000**	**frame_format_descriptor_6 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R80 (R0x0050)	**15:0**	**0x0000**	**frame_format_descriptor_7 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R82 (R0x0052)	**15:0**	**0x0000**	**frame_format_descriptor_8 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R84 (R0x0054)	**15:0**	**0x0000**	**frame_format_descriptor_9 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R86 (R0x0056)	**15:0**	**0x0000**	**frame_format_descriptor_10 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R88 (R0x0058)	**15:0**	**0x0000**	**frame_format_descriptor_11 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R90 (R0x005A)	**15:0**	**0x0000**	**frame_format_descriptor_12 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R92 (R0x005C)	**15:0**	**0x0000**	**frame_format_descriptor_13 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R94 (R0x005E)	**15:0**	**0x0000**	**frame_format_descriptor_14 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R128 (R0x0080)	**15:0**	**0x0000**	**analogue_gain_capability (RO)**	**N**	**N**
	Indicates support for analog gain coding typo 0 (baseline SMIA). Read-only. Read-only. Legal values: [0, 65535]				
R132 (R0x0084)	**15:0**	**0x0002**	**analogue_gain_code_min (RO)**	**N**	**N**
	Minimum gain code. Read-only. Read-only. Legal values: [0, 65535].				
R134 (R0x0086)	**15:0**	**0x001F**	**analogue_gain_code_max (RO)**	**N**	**N**
	Maximum gain code. Read-only. Read-only. Legal values: [0, 65535].				
R136 (R0x0088)	**15:0**	**0x0001**	**analogue_gain_code_step (RO)**	**N**	**N**
	Gain code step size. Read-only. Read-only. Legal values: [0, 65535].				
R138 (R0x008A)	**15:0**	**0x0000**	**analogue_gain_type (RO)**	**N**	**N**
	Indicates support for analog gain coding type 0 (baseline SMIA). Read-only. Read-only. Legal values: [0, 65535].				
R140 (R0x008C)	**15:0**	**0x0001**	**analogue_gain_m0 (RO)**	**N**	**N**
	Constants for the gain equation. Read-only. Read-only. Legal values: [0, 65535].				
R142 (R0x008E)	**15:0**	**0x0000**	**analogue_gain_c0 (RO)**	**N**	**N**
	Constants for the gain equation. Read-only. Read-only. Legal values: [0, 65535].				
R144 (R0x0090)	**15:0**	**0x0000**	**analogue_gain_m1 (RO)**	**N**	**N**
	Constants for the gain equation. Read-only. See "SMIA Gain Model" in "Frame Rate and Integration Time.doc". Read-only. Legal values: [0, 65535].				

Table 4. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R146 (R0x0092)	**15:0**	**0x0004**	**analogue_gain_c1 (RO)**	**N**	**N**
	Constants for the gain equation. Read-only. See "SMIA Gain Model" in "Frame Rate and Integration Time.doc". Read-only. Legal values: [0, 255].				
R192 (R0x00C0)	**7:0**	**0x01**	**data_format_model_type (RO)**	**N**	**N**
	Indicates the use of 2-byte data format. Read-only. Read-only. Legal values: [0, 255]				
R193 (R0x00C1)	**7:0**	**0x05**	**data_format_model_subtype (RO)**	**N**	**N**
	Indicates the provision of 3 data format descriptors. Read-only. Read-only. Legal values: [0, 255]				
R194 (R0x00C2)	**15:0**	**0x0A0A**	**data_format_descriptor_0 (RO)**	**N**	**N**
	Indicates support fo RAW10, uncompressed data format. Read-only. Read-only. Legal values: [0, 65535]				
R196 (R0x00C4)	**15:0**	**0x0808**	**data_format_descriptor_1 (RO)**	**N**	**N**
	Indicates support for RAW8 data format in which the two LSB of each 10-bit pixel data value are discarded. Read-only. Read-only. Legal values: [0, 65535]				
R198 (R0x00C6)	**15:0**	**0x0A08**	**data_format_descriptor_2 (RO)**	**N**	**N**
	Indicates support for RAW8 data format in which each 10-bit pixel data value is compressed to an 8-bit value. Read-only. Read-only. Legal values: [0, 65535]				
R200 (R0x00C8)	**15:0**	**0x0A06**	**data_format_descriptor_3 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R202 (R0x00CA)	**15:0**	**0x0000**	**data_format_descriptor_4 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R204 (R0x00CC)	**15:0**	**0x0000**	**data_format_descriptor_5 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R206 (R0x00CE)	**15:0**	**0x0000**	**data_format_descriptor_6 (RO)**	**N**	**N**
	Read-only. Read-only. Legal values: [0, 65535].				
R256 (R0x0100)	**7:0**	**0x00**	**mode_select (R/W)**	**N**	**N**
	This bit is an alias of R0x301A–B[2].				
R257 (R0x0101)	**7:0**	**0x00**	**image_orientation (R/W)**		
	7:2	X	Reserved		
	1	0x00	vert_flip This register field is an alias of R0x3040[15]	N	N
	0	0x00	horiz_mirror This register field is an alias of R0x3040[14]	N	N
R259 (R0x0103)	**7:0**	**0x00**	**software_reset (R/W)**	**N**	**N**
	This register field is an alias of R0x301A–B[0].				
R260 (R0x0104)	**7:0**	**0x00**	**grouped_parameter_hold (R/W)**	**N**	**N**
	This register field is an alias of R0x301A–B[15].				
R261 (R0x0105)	**7:0**	**0x00**	**mask_corrupted_frames (R/W)**	**N**	**N**
	This register field is an alias of R0x301A–B[9].				
R272 (R0x0110)	**7:0**	**0x00**	**ccp2_channel_mode (R/W)**		
	7:3	X	Reserved		
	2:0	0x00	ccp2_channel_identifier ccp2_channel_identifier Legal values: [0, 7].	N	N

Table 4. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R273 (R0x0111)	**7:0**	**0x01**	**ccp2_signalling_mode (R/W)**	**N**	**N**
	0: Use Data/Clock signaling on the CCP2 serial interface. 1: Use Data/Strobe signaling on the CCP2 serial interface.				
R274 (R0x0112)	**15:0**	**0x0A0A**	**ccp_data_format (R/W)**		
	15:12	X	Reserved		
	11:8	0x000A	raw_data_format The bit-width of the uncompressed pixel data Legal values: [0, 15].	N	N
	7:4	X	Reserved		
	3:0	0x000A	compressed_data_format The bit-width of the compressed pixel data Legal values: [0, 15].	N	N
R288 (R0x0120)	**7:0**	**0x00**	**gain_mode (R/W)**	**N**	**N**
	gain_mode				
R514 (R0x0202)	**15:0**	**0x0001**	**coarse_integration_time (R/W)**	**N**	**N**
	Integration time programmed in units of line_length_pck. This register is an alias of R0x3012−3. Legal values: [0, 65535].				
R516 (R0x0204)	**15:0**	**0x0004**	**analogue_gain_code_global (R/W)**	**N**	**N**
	Global analog gain. Available analog gains : 1x, 2x, 3x, 4x,6x and 8x Legal values: [0,8].				
R518 (R0x0206)	**15:0**	**0x0004**	**analogue_gain_code_green (R/W)**		
	15:7	X	Reserved		
	6:0	0x0004	gain_code_greenr Analog gain for green R. Legal values: [0,32].	N	N
R520 (R0x0208)	**15:0**	**0x0004**	**analogue_gain_code_red (R/W)**		
	15:7	X	Reserved		
	6:0	0x0004	gain_code_red Analog gain for red. Legal values: [0,32].	N	N
R522 (R0x020A)	**15:0**	**0x0004**	**analogue_gain_code_blue (R/W)**		
	15:7	X	Reserved		
	6:0	0x0004	gain_code_blue Analog gain for blue. Legal values: [0,32].	N	N
R524 (R0x020C)	**15:0**	**0x0004**	**analogue_gain_code_greenb (R/W)**		
	15:7	X	Reserved		
	6:0	0x0004	gain_code_greenb Analog gain for green B. Legal values: [0,32].	N	N
R526 (R0x020E)	**15:0**	**0x0100**	**digital_gain_greenr (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_greenr Global digital gain, gain = register value/128. Legal values: [0,2047].	N	N
	1:0	X	Reserved		
R528 (R0x0210)	**15:0**	**0x0100**	**digital_gain_red (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_red Global digital gain, gain = register value/128. Legal values: [0,2047].	N	N
	1:0	X	Reserved		

Table 4. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R530 (R0x0212)	**15:0**	**0x0100**	**digital_gain_blue (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_blue Global digital gain, gain = register value/128. Legal values: [0,2047].	N	N
	1:0	X	Reserved		
R532 (R0x0214)	**15:0**	**0x0100**	**digital_gain_greenb (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_greenb Global digital gain, gain = register value/128. Legal values: [0,2047].	N	N
	1:0	X	Reserved		
R768 (R0x0300)	**15:0**	**0x0005**	**vt_pix_clk_div (R/W)**	**N**	**N**
	Clock divisor applied to video timing system clock to generate video timing pixel clock. Legal values: [0, 31].				
R770 (R0x0302)	**15:0**	**0x0001**	**vt_sys_clk_div (R/W)**	**N**	**N**
	Clock divisor applied to PLL output clock to generate video timing system clock. Legal values: [0, 31].				
R772 (R0x0304)	**15:0**	**0x0101**	**pre_pll_clk_div (R/W)**		
	15:14	X	Reserved		
	13:8	0x0001	pre_pll_clk_div_2 Clock divisor applied to EXTCLK to generate second PLL input clock. Legal values: [1, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0001	pre_pll_clk_div_1 Clock divisor applied to EXTCLK to generate first PLL input clock. Legal values: [1, 63].	N	N
	Clock divisor applied to EXTCLK to generate PLL input clock. Legal values: [1, 63].				
R774 (R0x0306)	**15:0**	**0x2C2C**	**pll_multiplier (R/W)**		
	15:8	0x002C	pll_multiplier_2 Clock multiplier applied to second PLL input clock. Legal values: [32, 254].	N	N
	7:0	0x002C	pll_multiplier_1 Clock multiplier applied to first PLL input clock. Legal values: [32, 254].	N	N
	Clock multiplier applied to PLL input clock. Legal values: [32, 254].				
R776 (R0x0308)	**15:0**	**0x000A**	**op_pix_clk_div (R/W)**	**N**	**N**
	Clock divisor applied to the output system clock to generate the output pixel clock. Legal values: [0, 31].				
R778 (R0x030A)	**15:0**	**0x0001**	**op_sys_clk_div (R/W)**	**N**	**N**
	Clock divisor applied to PLL output clock to generate output system clock. Legal values: [0, 31].				
R832 (R0x0340)	**15:0**	**0x0CCE**	**frame_length_lines (R/W)**	**N**	**N**
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. Legal values: [0, 65535].				
R834 (R0x0342)	**15:0**	**0x1230**	**line_length_pck (R/W)**	**N**	**N**
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Need to set twice value of the number of pixel clock in one line row time. Legal values: [0, 65535].				

Table 4. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R836 (R0x0344)	**15:0**	**0x0008**	**x_addr_start (R/W)**	**N**	**N**
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. Legal values: [0, 3279].				
R838 (R0x0346)	**15:0**	**0x0008**	**y_addr_start (R/W)**	**N**	**N**
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. Legal values: [0, 2463].				
R840 (R0x0348)	**15:0**	**0x1077**	**x_addr_end (R/W)**	**N**	**N**
	The last column of visible pixels to read out. Legal values: [0, 3279].				
R842 (R0x034A)	**15:0**	**0x0C37**	**y_addr_end (R/W)**	**N**	**N**
	The last row of visible pixels to be read out. Legal values: [0, 2463].				
R844 (R0x034C)	**15:0**	**0x1070**	**x_output_size (R/W)**	**N**	**N**
	Set X output size of displayed image. Bit[0] is read-only 0. The default value of this register is set to be consistent with the default values of x_addr_end and x_addr_start. Legal values: [0, 4095].				
R846 (R0x034E)	**15:0**	**0x0C30**	**y_output_size (R/W)**	**N**	**N**
	Set Y output size of the displayed image. Bit[0] is read-only 0. The default value of this register is set to be consistent with the default values of y_addr_end and y_addr_start. Legal values: [0, 4095].				
R900 (R0x0384)	**15:0**	**0x0001**	**y_even_inc (RO)**	**N**	**N**
	Read-only.				
R902 (R0x0386)	**15:0**	**0x0001**	**y_odd_inc (R/W)**	**N**	**N**
	This register field is an alias of R0x3040[5:0] Legal values: [0, 63].				
R1024 (R0x0400)	**15:0**	**0x0000**	**scaling_mode (R/W)**	**N**	**N**
	0: Disable scaler 1: Enable horizontal scaling 2: Enable horizontal and vertical scaling 3: Reserved Legal values: [0, 2].				
R1026 (R0x0402)	**15:0**	**0x0000**	**spatial_sampling (R/W)**	**N**	**N**
	0: Bayer sampling 1: Co-sited sampling				
R1028 (R0x0404)	**15:0**	**0x0010**	**scale_m (R/W)**	**N**	**N**
	scale factor M (horizontal scale factor) Legal values: [16, 127].				
R1280 (R0x0500)	**15:0**	**0x0001**	**compression_mode (RO)**	**N**	**N**
	Read-only. 0x0001 = 10-bit to 8-bit compression uses the DPCM/PCM Simple Predictor algorithm. This register controls the algorithm that is to be used for compression. The sensor only supports a single algorithm and therefore this register is read-only. This register does not control whether data compression is enabled; that is controlled by the ccp_data_format register (R0x0012–3). Read-only.				

Table 4. SMIA CONFIGURATION (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R1536 (R0x0600)	**15:0**	**0x0000**	**test_pattern_mode (R/W)**		
	15:10	X	Reserved		
	9:8	0x0000	marching_one_pattern_enable marching one pattern 256: Walking 1 s test pattern (10-bit) 257: Walking 1 s test pattern (8-bit) other = Reserved. Legal values: [0, 3].	N	N
	7:3	X	Reserved		
	2:0	0x0000	test_pattern_select select test pattern 0: Normal operation, Generate output data from pixel array 1: Solid color test pattern. 2: 100% color bar test pattern 3: Fade to grey color bar test pattern 4: PN9 Link integrity test pattern Legal values: [0, 7].	N	N
R1538 (R0x0602)	**15:0**	**0x0000**	**test_data_red (R/W)**	**N**	**N**
	Red test data for solid test pattern. Legal values: [0, 1023].				
R1540 (R0x0604)	**15:0**	**0x0000**	**test_data_greenr (R/W)**	**N**	**N**
	GreenR test data for solid test pattern. Legal values: [0, 1023].				
R1542 (R0x0606)	**15:0**	**0x0000**	**test_data_blue (R/W)**	**N**	**N**
	Blue test data for solid test pattern. Legal values: [0, 1023].				
R1544 (R0x0608)	**15:0**	**0x0000**	**test_data_greenb (R/W)**	**N**	**N**
	GreenB test data for solid test pattern. Legal values: [0, 1023].				

Table 5. SMIA PARAMETER LIMITS

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R4096 (R0x1000)	15:0	0x0001	integration_time_capability (RO)	N	N
	Indicates the provision of coarse and fine integration time control. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4100 (R0x1004)	15:0	0x0000	coarse_integration_time_min (R/W)	N	N
	The minimum coarse integration time. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4102 (R0x1006)	15:0	0x0001	coarse_integration_time_max_margin (R/W)	N	N
	The maximum coarse integration time is (frame_length_lines − coarse_integration_time_max_margin). Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4224 (R0x1080)	15:0	0x0001	digital_gain_capability (RO)	N	N
	Indicates the provision of separate (per color) digital gain control. Read-only.				
R4228 (R0x1084)	15:0	0x0100	digital_gain_min (RO)	N	N
	UFIX16. Minimum value of digital gain is 1.0. Read-only.				
R4230 (R0x1086)	15:0	0x07FC	digital_gain_max (RO)	N	N
	UFIX16. Maximum value of digital gain is 7.0. Read-only.				
R4232 (R0x1088)	15:0	0x0004	digital_gain_step_size (RO)	N	N
	UFIX16. Step size for digital gain is 1.0. Read-only.				
R4360 (R0x1108)	15:0	0x0001	min_pre_pll_clk_div (RO)	N	N
	Minimum clock divisor applied to PLL input clock. Read-only.				
R4362 (R0x110A)	15:0	0x0040	max_pre_pll_clk_div (RO)	N	N
	Maximum clock divisor applied to PLL input clock. Read-only.				
R4372 (R0x1114)	15:0	0x0020	min_pll_multiplier (RO)	N	N
	Minimum multiplier applied by PLL. Read-only.				
R4374 (R0x1116)	15:0	0x0180	max_pll_multiplier (RO)	N	N
	Maximum multiplier applied by PLL. Read-only.				
R4384 (R0x1120)	15:0	0x0001	min_vt_sys_clk_div (RO)	N	N
	Minimum divisor for the video timing sys_clk. Read-only.				
R4386 (R0x1122)	15:0	0x0010	max_vt_sys_clk_div (RO)	N	N
	Maximum divisor for the video timing sys_clk. Read-only.				
R4404 (R0x1134)	15:0	0x0004	min_vt_pix_clk_div (RO)	N	N
	Minimum divisor for the video timing pix_clk. Read-only.				
R4406 (R0x1136)	15:0	0x0010	max_vt_pix_clk_div (RO)	N	N
	Maximum divisor for the video timing pix_clk. Read-only.				
R4416 (R0x1140)	15:0	0x0012	min_frame_length_lines (R/W)	N	N
	Minimum frame length. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4418 (R0x1142)	15:0	0xFFFF	max_frame_length_lines (R/W)	N	N
	Maximum frame length. The maximum frame length is only constrained by the size of the read/write field in the frame_length_lines register (16-bits). Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4420 (R0x1144)	15:0	0x1230	min_line_length_pck (R/W)	N	N
	Minimum line length. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4422 (R0x1146)	15:0	0xFFFC	max_line_length_pck (R/W)	N	N
	Maximum line length. The maximum line length is only constrained by the size of the read/write field in the line_length_pck register (16 bits). Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4424 (R0x1148)	15:0	0x00F0	min_line_blanking_pck (R/W)	N	N
	Minimum line blanking time. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4426 (R0x114A)	15:0	0x0010	min_frame_blanking_lines (R/W)	N	N
	Minimum frame blanking time. Read-only. Can be made read/write by clearing R0x301A−B[3].				
R4448 (R0x1160)	15:0	0x0001	min_op_sys_clk_div (RO)	N	N
	Minimum divisor for the output sys_clk. Read-only.				

Table 5. SMIA PARAMETER LIMITS (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R4450 (R0x1162)	**15:0**	**0x0010**	**max_op_sys_clk_div (RO)**	**N**	**N**
	Maximum divisor for the output sys_clk. Read-only.				
R4460 (R0x116C)	**15:0**	**0x0006**	**min_op_pix_clk_div (RO)**	**N**	**N**
	Minimum divisor for output pix_clk. Read-only.				
R4462 (R0x116E)	**15:0**	**0x000A**	**max_op_pix_clk_div (RO)**	**N**	**N**
	Maximum divisor for output pix_clk. Read-only.				
R4480 (R0x1180)	**15:0**	**0x0000**	**x_addr_min (RO)**	**N**	**N**
	Minimum value for x_addr_start, x_addr_end. Read-only.				
R4482 (R0x1182)	**15:0**	**0x0000**	**y_addr_min (RO)**	**N**	**N**
	Minimum value for y_addr_start, y_addr_end. Read-only.				
R4484 (R0x1184)	**15:0**	**0x107F**	**x_addr_max (RO)**	**N**	**N**
	Maximum value for x_addr_start, x_addr_end. Read-only.				
R4486 (R0x1186)	**15:0**	**0x0C3F**	**y_addr_max (RO)**	**N**	**N**
	Maximum value for y_addr_start, y_addr_end. Read-only.				
R4544 (R0x11C0)	**15:0**	**0x0001**	**min_even_inc (RO)**	**N**	**N**
	Minimum value for increment of even X/Y addresses when sub-sampling is enabled. Read-only.				
R4546 (R0x11C2)	**15:0**	**0x0001**	**max_even_inc (RO)**	**N**	**N**
	Maximum value for increment of even X/Y addresses when sub-sampling is enabled. Read-only.				
R4548 (R0x11C4)	**15:0**	**0x0001**	**min_odd_inc (RO)**	**N**	**N**
	Minimum value for increment of odd X/Y addresses when sub-sampling is enabled. Read-only.				
R4550 (R0x11C6	**15:0**	**0x0007**	**max_odd_inc (RO)**	**N**	**N**
	Maximum value for increment of odd X/Y addresses when sub-sampling is enabled. Read-only. Higher increment values are supported by the sensor, but only the values 1, 3 and 7 for x_odd_inc and 1, 3, 7, 15 and 31 for y_odd_inc. A value of 3 gives 2x sub-sampling and a value of 7 gives 4x sub-sampling.				
R4608 (R0x1200)	**15:0**	**0x0002**	**scaling_capability (RO)**	**N**	**N**
	Indicates the provision of a full (horizontal and vertical) scaler. Read-only.				
R4612 (R0x1204)	**15:0**	**0x0010**	**scaler_m_min (RO)**	**N**	**N**
	Indicates the minimum M value for the scaler. Read-only.				
R4614 (R0x1206)	**15:0**	**0x0080**	**scaler_m_max (RO)**	**N**	**N**
	Indicates the maximum M value for the scaler. Read-only.				
R4616 (R0x1208)	**15:0**	**0x0010**	**scaler_n_min (RO)**	**N**	**N**
	Indicates the minimum N value for the scaler. Read-only.				
R4618 (R0x120A)	**15:0**	**0x0010**	**scaler_n_max (RO)**	**N**	**N**
	Indicates the maximum N value for the scaler. Read-only.				
R4864 (R0x1300)	**15:0**	**0x0001**	**compression_capability (RO)**	**N**	**N**
	Indicates the capability for performing 10-bit to 8-bit pixel data compression. Read-only.				

Table 6. MANUFACTURER SPECIFIC

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12288 (R0x3000)	**15:0**	**0x0253**	**model_id_ (R/W)**	**N**	**N**
	This register is an alias of R0x3000−1. Read-only. Can be made read/write by clearing R0x301A−B[3]. Legal values: [0, 65535].				
R12290 (R0x3002)	**15:0**	**0x0008**	**y_addr_start_ (R/W)**	**Y**	**Y**
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value. Legal values: [0, 3133].				
R12292 (R0x3004)	**15:0**	**0x0008**	**x_addr_start_ (R/W)**	**Y**	**Y**
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value. Legal values: [0, 4221].				
R12294 (R0x3006)	**15:0**	**0x0C37**	**y_addr_end_ (R/W)**	**Y**	**Y**
	The last row of visible pixels to be read out. Legal values: [2, 3135].				
R12296 (R0x3008)	**15:0**	**0x1077**	**x_addr_end_ (R/W)**	**Y**	**Y**
	The last column of visible pixels to read out. Legal values: [2, 4223].				
R12298 (R0x300A)	**15:0**	**0x0CCE**	**frame_length_line_ (R/W)**	**Y**	**Y**
	The number of complete lines (rows) in the output frame. This includes visible lines and vertical blanking lines. Legal values: [0, 65535].				
R12300 (R0x300C)	**15:0**	**0x1230**	**line_length_pck_ (R/W)**	**Y**	**Y**
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Legal values: [0, 65535].				
R12304 (R0x3010)	**15:0**	**0x0000**	**fine_correction (R/W)**	**Y**	**N**
	Reversed. Legal values: [0, 32767].				
R12306 (R0x3012)	**15:0**	**0x0001**	**coarse_integration_time_ (R/W)**	**Y**	**N**
	Integration time 1 specified in multiples of line_length_pck_. Legal values: [0, 65535].				
R12308 (R0x3014)	**15:0**	**0x0000**	**shutter_fine (R/W)**	**Y**	**N**
	Reversed. Legal values: [0, 32767].				
R12310 (R0x3016)	**15:0**	**0x0111**	**row_speed (R/W)**		
	15:11	X	Reserved		
	10:8	0x0001	op_speed Slows down the output pixel clock frequency relative to the system clock frequency. A programmed value of N gives a output pixel clock period of N system clocks. Only values 1, 2 and 4 are supported. A value of 0 is illegal: it causes the clock to stop. Legal values: [0, 7].	N	N
	7	X	Reserved		
	6:4	0x0001	Reserved		
	3	X	Reserved		
	2:0	0x0001	pc_speed Slows down the internal pixel clock frequency relative to the system clock frequency. A programmed value of N gives a pixel clock period of N system clocks. Only values 1, 2 and 4 are supported. A value of 0 is illegal: it causes the clock to stop. Legal values: [0, 7].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12312 (R0x3018)	**15:0**	**0x0000**	**extra_delay (R/W)**	**Y**	**N**
	extra delay Extra blanking inserted between frames. A programmed value of N increases the vertical blanking time by N pixel clock periods. Can be used to get a more exact frame rate. May affect the integration times of parts of the image when the integration time is less than 1 frame Legal values: [0, 65535].				
R12314 (R0x301A)	**15:0**	**0x0018**	**reset_register (R/W)**		
	15	0x0000	grouped_parameter_hold_ctl Group parameter hold 0: insert of many of the registers is synchronized to frame start. 1: Inhibit register inserts; register changes will remain pending until this bit is returned to 0. When this bit is returned to 0, all pending register inserts will be made on the next frame start.	N	N
	14	0x0000	gain_update_all_frame with this bit set, gain is updated at next frame regardless integration time update. With this bit reset, gain is synced with integration time update.	N	N
	13	0x0000	fast_integration_time_update 0= integration time update is done conventionally 1= integration time could be updated right next frame	N	N
	12	0x0000	smia_dis This bit disables the SMIA high-speed serializer and differential output buffers.	N	N
	11	0x0000	pll_always_on Set to 1, to make PLL always on to shorten the state transaction from standby to streaming it is used in 3D support mode	N	N
	10	0x0000	restart_bad Restart at bad frame 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N
	8	0x0000	gpi_en 0: The primary input buffers associated with the GPI0, GPI1, GPI2, GPI3 inputs are powered down and the GPI cannot be used. 1: The input buffers are enabled and can be read through R0x3026−7.	N	N
	7:6	X	Reserved		
	5	0x0000	reset_lpf_enable T prevent reset from POR glitch, enable digital low pass filter	N	N
	4	0x0001	Reserved		
	3	0x0001	lock_reg Many SMIA registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N
	2	0x0000	stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	1	0x0000	restart This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time.	N	N
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	N
R12316 (R0x301C)	**7:0**	**0x00**	**mode_select_ (R/W)**	**N**	**N**
	This bit is an alias of R0x301A−B[2].				
R12317 (R0x301D)	**7:0**	**0x00**	**image_orientation_ (R/W)**		
	7:2	X	Reserved		
	1	0x00	image_orientation_vert_flip_ This register field is an alias of R0x3040[15] Writes are synchronized to frame boundaries. Causes a Bad Frame if written.	Y	Y
	0	0x00	image_orientation_horiz_mirror_ This register field is an alias of R0x3040[14] Writes are synchronized to frame boundaries. Causes a Bad Frame if written.	Y	Y
R12318 (R0x301E)	**15:0**	**0x002A**	**data_pedestal_ (R/W)**	**N**	**N**
	Constant offset that is added to the ADC output for all visible pixels in order to set the black level to a value greater than 0. Read-only. Can be made read/write by clearing R0x301A−B[3]. Legal values: [0, 1023].				
R12321 (R0x3021)	**7:0**	**0x00**	**software_reset_ (R/W)**	**N**	**N**
	This bit is an alias of R0x301A−B[0].				
R12322 (R0x3022)	**7:0**	**0x00**	**grouped_parameter_hold_ (R/W)**	**N**	**N**
	This bit is an alias of R0x301A−B[15].				
R12323 (R0x3023)	**7:0**	**0x00**	**mask_corrupted_frames_ (R/W)**		
	7:1	X	Reserved		
	0	0x00	mask_bad_frames This bit is an alias of R0x301A−B[9].	N	N
R12324 (R0x3024)	**7:0**	**0x00**	**pixel_order_ (RO)**	**N**	**N**
	Pixel Order 00 = First row is GreenR/Red, first pixel is GreenR, 01 = First row is GreenR/Red, first pixel is Red, 02 = First row is Blue/GreenB, first pixel is Blue, 03 = First row is Blue/GreenB,first pixel is GreenB The value in this register changes as a function of R0x3040[1:0]. Read-only. Legal values: [0, 3].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12326 (R0x3026)	**15:0**	**0xFFFF**	**gpi_status (R/W)**		
	15:13	0x0007	standby_pin_select Associate the standby function with an active-high input pin 0: Associate with GPI0 1: associate with GPI1 2: Associate with GPI2 3: Associate with GPI3 4−6: RESERVED 7: Standby function cannot be controlled by any pin Must be set to 7 if reset[8]=0. Legal values: [0, 7].	N	N
	12:10	RO	Reserved		
	9:7	0x0007	trigger_pin_select Associate the trigger function with an active-high input pin 0: Associate with GPI0 1: associate with GPI1 2: Associate with GPI2 3: Associate with GPI3 4−6: RESERVED 7: Trigger function is not controlled by any pin Must be set to 7 if R0x301A−B[8]=0. Legal values: [0, 7].	N	N
	6:4	0x0007	saddr_pin_select Associate the SADDR function with an active-high input pin 0: Associate with GPI0 1: associate with GPI1 2: Associate with GPI2 3: Associate with GPI3 4−6: RESERVED 7: SADDR function is not controlled by any pin Must be set to 7 if R0x301A−B[8]=0. Legal values: [0, 7].	N	N
	3	RO	gpi3 Read-only. Return the current state of the GPI3 input pin. Invalid if R0x301A−B[8]=0. Read-only.	N	N
	2	RO	gpi2 Read-only. Return the current state of the GPI2 input pin. Invalid if R0x301A−B[8]=0. Read-only.	N	N
	1	RO	gpi1 Read-only. Return the current state of the GPI1 input pin. Invalid if R0x301A−B[8]=0. Read-only.	N	N
	0	RO	gpi0 Read-only. Return the current state of the GPI0 input pin. Invalid if R0x301A−B[8]=0. Read-only.	N	N
R12328 (R0x3028)	**15:0**	**0x0002**	**global_analog_gain_ (R/W)**	**Y**	**N**
	Global analog gain. Available analog gains: 0.5x through 16x, with step of 0.5 Writes are synchronized to frame boundaries. Legal values: [0, 32].				
R12330 (R0x302A)	**15:0**	**0x0002**	**analog_gain_greenr_ (R/W)**		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_greenr_ Analog gain for green R. Writes are synchronized to frame boundaries. Legal values: [0, 32].	Y	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12332 (R0x302C)	**15:0**	**0x0002**	**analog_gain_red_ (R/W)**		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_red_ Analog gain for red. Writes are synchronized to frame boundaries. Legal values: [0, 32].	Y	N
R12334 (R0x302E)	**15:0**	**0x0002**	**analog_gain_blue_ (R/W)**		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_blue_ Analog gain for blue. Writes are synchronized to frame boundaries. Legal values: [0, 32].	Y	N
R12336 (R0x3030)	**15:0**	**0x0002**	**analog_gain_greenb_ (R/W)**		
	15:6	X	Reserved		
	5:0	0x0002	analog_gain_for_greenb_ Analog gain for green B. Writes are synchronized to frame boundaries. Legal values: [0, 32].	Y	N
R12338 (R0x3032)	**15:0**	**0x0100**	**digital_gain_greenr_ (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_greenr_ Same as digital_gain_for_greenr_data, gain = register value/64 Writes are synchronized to frame boundaries. Legal values: [0, 511].	Y	N
	1:0	X	Reserved		
R12340 (R0x3034)	**15:0**	**0x0100**	**digital_gain_red_ (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_red_ Same as digital_gain_for_red_data, gain = register value/64 Writes are synchronized to frame boundaries. Legal values: [0, 511].	Y	N
	1:0	X	Reserved		
R12342 (R0x3036)	**15:0**	**0x0100**	**digital_gain_blue_ (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_blue_ Same as digital_gain_for_blue_data, gain = register value/64 Writes are synchronized to frame boundaries. Legal values: [0, 511].	Y	N
	1:0	X	Reserved		

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12344 (R0x3038)	**15:0**	**0x0100**	**digital_gain_greenb_ (R/W)**		
	15:11	X	Reserved		
	10:2	0x0040	digital_gain_for_greenb_ Same as digital_gain_for_greenb_data, gain = register value/64 Writes are synchronized to frame boundaries. Legal values: [0, 511].	Y	N
	1:0	X	Reserved		
R12346 (R0x303A)	**7:0**	**0x0A**	**smia_version_ (RO)**	**N**	**N**
	SMIA version. Return the value 10 to indicate an implementation of revision 1.0 of the SMIA specification. Read-only. Legal values: [0, 255].				
R12347 (R0x303B)	**7:0**	**0xFF**	**frame_count_ (RO)**	**N**	**N**
	frame count In the soft standby state this counter is set to 0xFF. In streaming state this counter increments by 1 (modulo 255) at the start of each frame. The counter is incremented for both good frames and bad (corrupted) frames – its behavior is not affected by the state of R0x301A–B[9] (mask_corrupted_frames). Read-only. Legal values: [0, 255].				
R12348 (R0x303C)	**15:0**	**0x0000**	**frame_status (RO)**		
	15:3	X	Reserved		
	2	RO	frame_status_bad_frame indicates current frame is bad Read-only.	N	N
	1	RO	frame_status_standby frame status standby This bit tells you whether the sensor is in standby state. Can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit 0x301A[4]. Read-only. Read-only.	N	N
	0	RO	frame_status_framesync frame status frame synced Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization. Read-only. Read-only.	N	N
R12350 (R0x303E)	**15:0**	**0x0000**	**read_style (R/W)**		
	15	0x0000	dual_hdr_enable enable dual HDR. 0: disable 1: enable Writes are synchronized to frame boundaries.	Y	N
	14:13	0x0000	fdoc_option 00: normal 8 rows, binning 16 rows 01: normal 16 rows, binning 32 rows 10: normal 24 rows, binning 48 rows 11: normal 48 rows, binning 48 rows Writes are synchronized to frame boundaries. Legal values: [0, 3].	Y	N
	12:11	X	Reserved		
	10	0x0000	dark_column_option 0: use 160 dark columns. 1: use 224 dark columns. Writes are synchronized to frame boundaries.	Y	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12350 (R0x303E)	9	0x0000	ihdr_rskip_fdc_select In IHDR rskip mode, T2 pairs may use fdoc coefficients of group 0 or group1. 0: use fdoc coefficient group0 (by location) 1: Use fdoc coefficient group1 (by integration) Writes are synchronized to frame boundaries.	Y	N
	8	0x0000	ihdr_t1_t2_alternate_row_enable When set, IHDR readout T1, T2 alternate rows. Writes are synchronized to frame boundaries.	Y	N
	7	RO	ihdr_field_auto_swap_status read back IHDR field status, Read Only. Read-only. Writes are synchronized to frame boundaries.	Y	N
	6	0x0000	ihdr_field_auto_swap When set, Swap T1, T2 rows each valid frame. Writes are synchronized to frame boundaries.	Y	N
	5	0x0000	Reserved		
	4	0x0000	Reserved		
	3	0x0000	ihdr_gain_mode When set, T1/T2 rows can have different gain.	N	N
	2	0x0000	ihdr_field_sel When set, the first two rows are with exposure T2. Writes are synchronized to frame boundaries.	Y	N
	1	0x0000	ihdr_first_field When this bit is set to 0, the first two rows readout and every subsequent alternate two rows are with exposure T1 Writes are synchronized to frame boundaries.	Y	N
	0	0x0000	ihdr_enable Enable iHDR 0: disable 1: enable Writes are synchronized to frame boundaries.	Y	N
R12352 (R0x3040)	**15:0**	**0x0041**	**read_mode (R/W)**		
	15	0x0000	vert_flip 0 = Normal readout 1 = Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ is read out of the sensor first. Setting this bit will change the bayer pixel order (see R0x3024). Writes are synchronized to frame boundaries. Causes a Bad Frame if written.	Y	Y
	14	0x0000	horiz_mirror 0 = Normal readout 1 = Readout is mirrored horizontally so that the column specified by x_addr_end_ is read out of the sensor first. Setting this bit will change the bayer pixel order (see R0x3024). Writes are synchronized to frame boundaries. Causes a Bad Frame if written.	Y	Y
	13	0x0000	row_sum Enable analogue summing in Y (row) direction. When set, y_odd_inc must be set to 3 for row summing along with other register changes Writes are synchronized to frame boundaries. Causes a Bad Frame if written.	Y	Y
	12	0x0000	eis_mode when eis_mode is 1, to disable the bad frame generation when y_start/_end is changed within the window	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12352 (R0x3040)	11	0x0000	x_bin_en Enable analogue binning in X (column) direction. When set, x_odd_inc must be set to 3 for column binning along with other register changes. Writes are synchronized to frame boundaries. Causes a Bad Frame if written.	Y	Y
	10	0x0000	Reserved		
	9:6	0x0001	x_odd_inc Increment applied in X (column) direction. Read out 1= Normal 3= 1 out of 2 pixels 7= 1 out of 4 pixels 15= 1 out of 8 pixels Writes are synchronized to frame boundaries. Causes a Bad Frame if written. Legal values: [0, 15].	Y	Y
	5:0	0x0001	y_odd_inc Increment applied in Y (row) direction. Read out 1= Normal 3= 1 out of 2 pixels 7= 1 out of 4 pixels 15= 1 out of 8 pixels 31= 1 out of 16 pixels, 63= 1 out of 32 pixels, Writes are synchronized to frame boundaries. Causes a Bad Frame if written. Legal values: [0, 63].	Y	Y
R12354 (R0x3042)	**15:0**	**0x0000**	**dark_control2 (R/W)**		
	15	X	Reserved		
	14	0x0000	Reserved		
	13	0x0000	Reserved		
	12	0x0000	vtx_lo_control When set to 1, vtx lo to gnd signal is toggling only during vblank time. when set to 0, vtx lo to gnd signal is toggling all time.	N	N
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7	0x0000	Reserved		
	6	0x0000	Reserved		
	5	0x0000	Reserved		
	4	0x0000	Reserved		
	3	0x0000	Reserved		
	2	0x0000	Reserved		
	1	0x0000	Reserved		
	0	0x0000	rownoise_corr_mode 1 = Not allow read dark cols even if read_dark_cols bit is set. 0 = Allow read dark cols if read_dark_cols bit is set.	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12356 (R0x3044)	**15:0**	**0x0580**	**dark_control (R/W)**		
	15	0x0000	s_addr_park Select parking address during column correction time, 0: Not specified parking address 1: Use 0 as the parking address	N	N
	14	X	Reserved		
	13	0x0000	no_bad_frame_by_frame_length_change 0 = Generate bad frame when frame length line changes, 1 = Do not generate bad frame when frame length line changes	N	N
	12	0x0000	dark_control_show_colcorr_rows Read out column correction rows even if column correction is disabled. This allows these rows to be shown through dark_control[11]. Writes are synchronized to frame boundaries.	Y	N
	11	0x0000	dark_control_show_dark_rows When sequencing the pixel array, 0= Normal readout 1= Readout (16−BLC related rows+ 16/32/64/128−CC rows+ 16-FDOC related rows+ 8-top-border rows + 8-bottom-border rows) Writes are synchronized to frame boundaries.	Y	N
	10	0x0001	row_noise_enable row noise correction enable	N	N
	9	0x0000	dark_control_show_dark_cols When set, the dark columns from global reference(160 or 224 columns)and GGR(48 columns) will be output before the active pixels in a line. There is an idle period of 8 pixels between dark column readout and active image readout Writes are synchronized to frame boundaries.	Y	N
	8	0x0001	dark_control_read_dark_cols 0 = Dark column readout is disabled. the row-wise noise cancellation algorithm cannot be used (set bit[10]=0). 1= 160 Dark columns are read at the start of each row and used in the row-wise noise cancellation algorithm (set bit[10]=1). Writes are synchronized to frame boundaries.	Y	N
	7	0x0001	dark_control_read_balance_rows 0 = Do not read out dark rows used for the column balance algorithm. 1 = Read out 2 dark rows used by the column balance algorithm.	N	N
	6	0x0000	finedigcorr_threshold_enable Enable local FineDigCorr_threshold Writes are synchronized to frame boundaries.	Y	N
	5	0x0000	finedigcorr_split_enable Enable even/odd columns with separate calculation Writes are synchronized to frame boundaries.	Y	N
	4	0x0000	Reserved		
	3	0x0000	dark_control_use_physical_address In default mode(x_addr_start, y_addr_start)= (0, 0) corresponds to the first active pixel. Set this bit, x/y_addr_start correspond to the physical addresses used in sensor pixel array. Writes are synchronized to frame boundaries.	Y	N
	2	0x0000	dark_control_dark_row_nolatch Correction rows access with tx latch on or off 0: tx latch on 1: tx latch off	N	N
	1:0	0x0000	dark_control_calib_start First tied row used for offset calibration algorithm. 00 = 4 01 = 6 10 = 16 11 = 20 Legal values: [0, 3].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12358 (R0x3046)	**15:0**	**0x0608**	**flash (R/W)**		
	15:14	X	Reserved		
	13	0x0000	flash_xenon_flash Indicates that the FLASH output signal was asserted for the current frame. Read−only.	N	N
	12:10	0x0001	flash_frame_delay Delay time of Xenon flash When set, the FLASH output signal will assert for the programmed period (bits [7:0]) during vertical blanking. This is achieved by keeping the integration time equal to one frame, and the pulse width less than the vertical blanking time. Legal values: [0, 7].	N	N
	9	0x0001	flash_end_of_reset Flash pulse delay measured in frames.	N	N
	8	0x0000	flash_every_frame 1 = In Xenon mode, the flash is triggered after resetting a frame. 0 = In Xenon mode, the flash is triggered after a frame readout.	N	N
	7	0x0000	flash_led_flash 1 = Flash should be enabled every frame. 0 = Flash should be enabled for 1 frame only.	N	N
	6	0x0000	flash_invert_flash Enable LED flash. When set, the FLASH output signal will assert prior to the start of the resetting of a frame and will remain asserted until the end of the frame readout.	N	N
	5	0x0000	flash_xenon_no_delay Invert flash output signal. When set, the FLASH output signal will be active low.	N	N
	4	0x0000	flash_trigger_timed At the start of streaming, no frame delay will occur before the xenon flash pulse is triggered.	N	N
	3:0	0x0008	flash_scale Scale the flash count down counter with 2^(flash_scale+1) Legal values: [0, 15].	N	N
R12360 (R0x3048)	**15:0**	**0x0008**	**flash_count (R/W)**	**N**	**N**
	Length of flash pulse when Xenon flash is enabled. The value specifies the length in units of 256 x system_clock. When the Xenon count is set to its maximum value (0x3FF), the flash pulse will automatically be truncated prior to the readout of the first row, giving the longest pulse possible. Legal values: [0, 65535].				
R12362 (R0x304A)	**15:0**	**0x0000**	**otpm_control (R/W)**		
	15:11	X	Reserved		
	10	0x0000	otpm_enable_standby OTPM standby enable. When this bit is 0, the "standby" signal will never be asserted to the HV switch. When this bit is 1, the "standby" signal will be controlled automatically to the HV switch: negated when an OTPM read or write operation is being performed, and asserted otherwise. Asserting the "standby" signal to the HV switch connects the internal vcmn signal to gndio preventing leakage though any programmed anti-fuses. Legal values: [0,1].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12362 (R0x304A)	9	0x0000	otpm_single_record_only OTPM single record only. 1: Automatic read sequence will end after one record has been read from OTPM. 0: Automatic read sequence will end after all records (of specicied record type) have been read from OTPM. The total size of the records read must not exceed the space available; the total size of the otpm_data_* registers. Legal values: [0,1].	N	N
	8	0x0000	otpm_auto_rd_start_next Automatic read start next. When bypass_record (in otpm_expr) = 0, and single_record_only = 1, determine the start address for an automatic read sequence triggered by auto_rd_start: 0: Read first record that matches (search from start of OTPM). 1: Read next record that matches (search from current location in OTPM). Legal values: [0,1].	N	N
	7	0x0000	otpm_auto_invalidate When register bit is set to 1, invalidates record written to OTPM address. Legal values: [0,1].	N	N
	6	RO	otpm_auto_rd_success Indicates whether the automatic read sequence was successful. Read-only. Legal values: [0,1].	N	N
	5	RO	otpm_auto_rd_end Indicates whether the automatic read sequence has finished. Read-only. Legal values: [0,1].	N	N
	4	0x0000	otpm_auto_rd_start Trigger OTPM automatic read sequence. Legal values: [0,1].	N	N
	3	0x0000	otpm_disable_auto_rd When register bit is set to 1, disable automatic OTPM read sequence. Legal values: [0,1].	N	N
	2	RO	otpm_auto_wr_success Indicates whether the automatic write sequence was successful. Read-only. Legal values: [0,1].	N	N
	1	RO	otpm_auto_wr_end Indicates whether the automatic write sequence has finished. Read-only. Legal values: [0,1].	N	N
	0	0x0000	otpm_auto_wr_start Trigger OTPM automatic write sequence. The high voltage must be available on the high voltage pad before the write sequence is triggered. bypass_record (in otpm_expr) = 0: The OTPM address at which to start the write is determined automatically by searching the existing OTPM contents for the next free location. The record type and length is taken from the otpm_record register. The record payload (data to write) is taken from the otpm_data* registers. bypass_record=1: The OTPM address at which to start the write is taken from the otpm_manual_addr register. The length of the data to program is taken from the otpm_record register. The data to write is taken from the otpm_data* registers. Legal values: [0,1].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12364 (R0x304C)	**15:0**	**0x0200**	**otpm_record (R/W)**		
	15:8	0x0002	otpm_record_type OTPM record type. Currently supported types are x02 – Default registers; x2n – Register sets. Legal values: [0,255].	N	N
	7:0	0x0000	otpm_record_length OTPM record length. Length of record payload in 16-bit words (between 1 and 128). Legal values: [0,128].	N	N
R12374 (R0x3056)	**15:0**	**0x2010**	**greenr_gain (R/W)**		
	15:7	0x0040	digital_gain_for_greenr greenr digital gain/64. 0x40 for 1x.	Y	N
	6:4	0x0001	analog_coarse_gain coarse_gain = 2^(coarse_gain−1) that is, 0 for 0.5x, 1 for 1x, 2 for 2x, 3 for 4x	Y	N
	3:0	0x0000	analog_fine_gain fine_gain = (16+fine_gain)/16, 0 for 1x, 15 for 1.9375x	Y	N
R12376 (R0x3058)	**15:0**	**0x2010**	**blue_gain (R/W)**		
	15:7	0x0040	blue_gain_digital_gain blue digital gain/64. 0x40 for 1x.	Y	N
	6:4	0x0001	analog_coarse_gain coarse_gain aliased with 0x3056	Y	N
	3:0	0x0000	analog_fine_gain fine_gain aliased with 0x3056	Y	N
R12378 (R0x305A)	**15:0**	**0x2010**	**red_gain (R/W)**	**N**	**N**
	15:7	0x0040	red_gain_digital_gain red digital gain/64. 0x40 for 1x.	Y	N
	6:4	0x0001	analog_coarse_gain coarse_gain aliased with 0x3056	Y	N
	3:0	0x0000	analog_fine_gain fine_gain aliased with 0x3056	Y	N
R12380 (R0x305C)	**15:0**	**0x2010**	**greenb_gain (R/W)**		
	15:7	0x0040	greenb_gain_digital_gain greenb digital gain/64. 0x40 for 1x.	Y	N
	6:4	0x0001	analog_coarse_gain coarse_gain aliased with 0x3056	Y	N
	3:0	0x0000	analog_fine_gain fine_gain aliased with 0x3056	Y	N
R12382 (R0x305E)	**15:0**	**0x2010**	**global_gain (R/W)**		
	15:7	0x0040	digital_gain_for_global global digital gain/64. 0x40 for 1x. Accessing these bits will update digital gain of 0x3056 0x3058 0x305a and 0x305c.	Y	N
	6:4	0x0001	analog_coarse_gain coarse_gain aliased with 0x3056	Y	N
	3:0	0x0000	analog_fine_gain fine_gain aliased with 0x3056	Y	N
R12384 (R0x3060)	**15:0**	**0x0000**	**vsync_override_code (R/W)**		
	15:0	0x0000	vsync_overrride_code When vsync_overrride_code=1 the word−size number of lsbs of vsync_override_code are output(lbs first) in place of the eighth (last) word of the vsync code Legal values: [0, 65535].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12386 (R0x3062)	**15:0**	**0x0000**	**hsync_override_code (R/W)**		
	When hsync_overrride_code=1 the word-size number of lsbs of hsync_override_code are output(lbs first) in place of the eighth (last) word of the hsync code Legal values: [0, 65535].				
R12388 (R0x3064)	**15:0**	**0x5840**	**smia_test (R/W)**		
	15:14	0x0001	pll_vco_range pll_vco_range(for 40is PLL) Legal values: [0, 3].	N	N
	13	0x0000	pll_div2 Connected to the enable_div2 input of the PLL. When set the vt_pix_clk will be divided by 2 internally in the PLL. The purpose is to allow the vt_pix_clk dividers to be set without needing to take into account that the sensor has 2 digital data paths. The divide by 2 compensates for the 2 data paths and ensures the equations using vt_pix_clk stays independent of 2 data paths.	N	N
	12	0x0001	pll_pfd_h MSB of PFD[4:0]. Allows adjustment of the PLL phase frequency detector (PFD).	N	N
	11:10	0x0002	pll_lock_mode Control signals for PLL lock mode input of PLL Legal values: [0, 3].	N	N
	9	0x0000	pll_test_bypass 0 = Normal operation 1 = Bypass the PLL VCO so that EXTCLK drives the PLL output clock divisors. In order to perform any repeatable phase-accurate testing, the PLL must be bypassed: either implicitly (by remaining in standby mode) or explicitly by setting this bit.	N	N
	8	0x0000	embedded_data_en Enable embedded data function	N	N
	7	X	Reserved		
	6	0x0001	shift_vt_pix_clk_div Divides internal pixel clock by 2	N	N
	5	0x0000	Reserved		
	4	0x0000	Reserved		
	3:0	0x0000	pll_pfd_l PFD[3:0]. Allows adjustment of the PLL phase frequency detector (PFD). Legal values: [0, 15].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12390 (R0x3066)	**15:0**	**0x0000**	**framer_test_mode (R/W)**		
	15:10	X	Reserved		
	9:6	0x0000	test_lane_en Enables for each data lane (b0 = data lane 0...b3 = data lane 3) Legal values: [0, 15].	N	N
	5:2	0x0000	test_mode Define test mode to be applied MIPI/CCP interface if test_en is asserted MIPI: 0 = Transmit LP−00 on all enabled data and clock lanes 1 = Transmit LP−11 on all enabled data and clock lanes 2 = Transmit HS−0 on all enabled data and clock lanes 3 = Transmit HS−1 on all enabled data and clock lanes 4 = Transmit a square wave at half the potential serial data rate on all enabled data and clock lanes 5 = Transmit a square wave at the pixel data rate on all enabled data and clock lanes 6 = Transmit a LP square wave at half the pixel data rate on all enabled data and clock lanes 7 = Transmit a continuous, repeated, prbs31 (non−packetised), copied on all enabled data lanes 8 = Transmit a continuous, repeated, prbs9 (non−packetised), copied on all enabled data lanes HiSPi: 0 = Transmit 0 on each physical line of all enabled data and clock lanes (reserved if using separate HiSPi phy) 1 = Reserved 2 = Transmit differential 0 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi phy) 3 = Transmit differential 1 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi phy) 4 = Transmit a square wave at half the potential serial data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi phy) 5 = Transmit a square wave at the pixel data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi phy) 6 = Serialize and transmit the data pattern specified by test_user_data[15:0] 7 = Transmit a continuous, repeated, prbs31, with no SAV code, copied on all enabled data lanes 8 = Transmit a continuous, repeated, prbs9, with no SAV code, copied on all enabled data lanes Legal values: [0, 15].	N	N
	1	0x0000	test_sublvds_data_en When test_sublvds_en =1 the output from the subLVDS pads is determined by the state of this signal 0: Vdiff = 0(both lines ~0.9 V); Zout = 40−100 Ω 1: HS data output determined by the state of test_mode; Zout = ~450 Ω	N	N
	0	0x0000	test_sublvds_en Whem asserted the PHY enter the subLVDS debug mode	N	N
R12392 (R0x3068)	**15:0**	**0x0000**	**i2c_control (R/W)**		
	15:1	X	Reserved		
	0	0x0000	i2c_auto_inc_disable Disable auto increment of addresses during I^2C access	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12394 (R0x306A)	**15:0**	**0x0000**	**odp_status (RO)**	**N**	**N**
	15:6	X	Reserved		
	5	RO	mipi_preamble_err MIPI preamble error A fatal error occurred because frame pixel data arrived at the MIPI data framer before the MIPI wakeup sequence and start-of-frame short packet had completed. Probable cause is that the value programmed for FRAME_PREAMBLE is too small. Read-only.	N	N
	4	RO	mipi_line_byte_err MIPI line byte error A fatal error occurred because the line length of the pixel data that the MIPI serialiser expected to transmit did not match the line length set by X_OUTPUT_SIZE. Read-only.	N	N
	3	RO	hispi_mode_change_rdy When asserted all active HiSpi lanes are driving a differential-0 and it is safe for the sensor to reconfigure the link eg. Change pixel_depth_in/out Read-only.	N	N
	2:0	X	Reserved		
R12398 (R0x306E)	**15:0**	**0x9080**	**datapath_select (R/W)**		
	15:13	0x0004	slew_a slew rate control a Legal values: [0, 7].	N	N
	12:10	0x0004	slew_b slew rate control b Legal values: [0, 7].	N	N
	9	0x0000	hi_vcm_sel hi_vcm select	N	N
	8	0x0000	xor_lv XOR LV	N	N
	7	RO	profile12 SMIA profile mode Read-only. Legal values: [1, 1].	N	N
	6	0x0000	sum2x2 [6] =1 : enable sum 2X2 mode Writes are synchronized to frame boundaries.	Y	N
	5	0x0000	true_bin [5] =1 : enable True_bin Writes are synchronized to frame boundaries.	Y	N
	4	0x0000	true_bayer [4] =1 : enable True_bayer Writes are synchronized to frame boundaries.	Y	N
	3:1	0x0000	embedded_data_sel emebedded data selection Legal values: [0, 7].	N	N
	0	0x0000	cont_lv cont LV	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12400 (R0x3070)	**15:0**	**0x0000**	**test_pattern_mode_ (R/W)**		
	15:10	X	Reserved		
	9:8	0x0000	walking_one_pattern_enable_ 1: enable walking one pattern other = Reserved. Legal values: [0, 3].	N	N
	7:3	X	Reserved		
	2:0	0x0000	test_pattern_select_ If [8]=0, select following test pattern 0: Normal operation, Generate output data from pixel array 1: Solid color test pattern. 2: 100% color bar test pattern 3: Fade to grey color bar test pattern 4: PN9 Link integrity test pattern if [8]=1, select following walking one pattern For 10 bit data, 0: 10 bit walking one 1: 8 bit walking one For 12 bit data, 0: 12 bit walking one 1: 10 bit walking one 2: 8 bit walking one Legal values: [0, 7].	N	N
R12402 (R0x3072)	**15:0**	**0x0000**	**test_data_red_ (R/W)**		
	Red test data for solid test pattern. Legal values: [0, 1023].				
R12404 (R0x3074)	**15:0**	**0x0000**	**test_data_greenr_ (R/W)**		
	GreenR test data for solid test pattern. Legal values: [0, 1023].				
R12406 (R0x3076)	**15:0**	**0x0000**	**test_data_blue_ (R/W)**		
	Blue test data for solid test pattern. Legal values: [0, 1023].				
R12408 (R0x3078)	**15:0**	**0x0000**	**test_data_greenb_ (R/W)**		
	greenB test data for solid test pattern. Legal values: [0, 1023].				
R12410 (R0x307A)	**15:0**	**0x0000**	**test_raw_mode (R/W)**	**N**	**N**
	15:2	X	Reserved		
	1	0x0000	test_pat_override 1: Prevents test_pattern from turning off corrections Writes are synchronized to frame boundaries.	Y	N
	0	0x0000	raw_data Enable this bit to turn off all corrections Writes are synchronized to frame boundaries.	Y	N
R12412 (R0x307C)	**15:0**	**0x0000**	**test_user_data (R/W)**	**N**	**N**
	When HiSPi is selected and test_mode = 6, the data pattern input in this bus will be serialized (from b0) and transmitted across the HiSPi link Legal values: [0, 65535].				
R12414 (R0x307E)	**15:0**	**0x0020**	**reset_lpf_register (R/W)**	**N**	**N**
	15:6	X	Reserved		
	5:0	0x0020	reset_lpf_tap_size control POR digital filter tap size. Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12424 (R0x3088)	**15:0**	**0x0001**	**coarse_integration2_time (R/W)**	**Y**	**N**
	iHDR Integration time 2 specified in multiples of line_length_pck_. Legal values: [0, 65535].				
R12448 (R0x30A0)	**15:0**	**0x0001**	**x_even_inc_ (RO)**		
	Read-only. Read-only.				
R12450 (R0x30A2)	**15:0**	**0x0001**	**x_odd_inc_ (R/W)**	**Y**	**Y**
	This register field is an alias of R0x3040[9:6] Legal values: [0, 15].				
R12452 (R0x30A4)	**15:0**	**0x0001**	**y_even_inc_ (RO)**		
	Read-only. Read-only.				
R12454 (R0x30A6)	**15:0**	**0x0001**	**y_odd_inc_ (R/W)**	**Y**	**Y**
	This register field is an alias of R0x3040[5:0] Legal values: [0, 63].				
R12464 (R0x30B0)	**15:0**	**0x0400**	**digital_test (R/W)**	**N**	**N**
	15	0x0000	framer_altc_tst_stick 0 = sticky mode off 1 = sticky mode on	N	N
	14	0x0000	Reserved		
	13	0x0000	Reserved		
	12	0x0000	Reserved		
	11	0x0000	halt_col Halt Column Sequencer 0 = Normal operation. 1 = Halt the column sequencer. This is a manufacturing test mode. Stopping the column sequencer may reduce switching noise within the analog block.	N	N
	10	0x0001	Reserved		
	9	0x0000	framer_altc_tst_select 0 = Outputs even frame first 1 = Outputs odd frame first	N	N
	8	0x0000	framer_altc_tst_en 0 = Disable 1 = Enable	N	N
	7	X	Reserved		
	6	0x0000	adc_raw_op Enable this bit to turn off all corrections	N	N
	5	0x0000	Reserved		
	4	0x0000	Reserved		
	3:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	reset_skipped_rows Reset Skipped Rows When set (= 1), enables anti-blooming feature for skip modes. Shutter pointer 2 will be used to reset unused rows in skip modes. Since shutter pointer 2 is used to change integration time smoothly, unused rows will not be reset when the shutter pointer 2 is used for this purpose. Also, in higher skip modes only the immediate neighboring row to the active used rows will be reset using shutter pointer 2	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12466 (R0x30B2)	**15:0**	**0x0000**	**hispi_override_bba_control (R/W)**	**N**	**N**
	15:11	0x0000	t_vreg Time allowed for internal voltage regulator to settle before driving the LP drivers in 512*clk cycles Legal values: [0, 31].	N	N
	10:7	0x0000	t_dll_lock Time allowed for DLL (if present) to lock (in units of 16*clk cycles) Legal values: [0, 15].	N	N
	6	0x0000	hispi_standby_state Defines the state of each lane of the HiSPilink when the framer is in standby or the lane is not enabled 0: Hi-Z 1: 00	N	N
	5	0x0000	hsync_overrride_en When asserted , the eighth (last) word of the hsync code is replaced by hsync_override_code	N	N
	4	0x0000	vsync_override_en When asserted , the eighth (last) word of the vsync code is replaced by vsync_override_code	N	N
	3	0x0000	sov_override_sol When asserted, SOL(or SOF) sync code that would normally be pre-pended to HiSPi output line will be replaced with SOV sync code	N	N
	2:1	0x0000	hispi_bba_linecnt Number of blanking line before active for HiSpi BBA mode Legal values: [0, 3].	N	N
	0	0x0000	hispi_bba_en Enable HiSpi BBA mode	N	N
R12476 (R0x30BC)	**15:0**	**0x0000**	**y_output_offset (R/W)**	**N**	**N**
	Number of rows offset to start of the displayed image (Y output size) Legal values: [0, 4095].				
R12478 (R0x30BE)	**15:0**	**0x0000**	**x_output_offset (R/W)**	**N**	**N**
	Number of columns offset to start of the displayed image (X output size) Legal values: [0,4095].				
R12520 (R0x30E8)	**15:0**	**0x0000**	**ctx_control_reg (R/W)**		
	15	0x0000	context_load Load context immediately	N	N
	14	0x0000	context_load_frame_end Load context at frame end	N	N
	13:10	X	Reserved		
	9	0x0000	context_multi_cycle_mode context_multi_cycle_mode	N	N
	8	0x0000	context_multi_sync_mode When set, multiple contexts are synced to the start of readout frames, else they are synced to the start of exposure frames	N	N
	7	0x0000	context_multi Enable Multiple context to be read out	N	N
	6:4	0x0000	context_multi_num Set number of consecutive contexts to read out when ctx_multi is set Legal values: [0, 7].	N	N
	3:0	0x0000	context_select select context Legal values: [0, 15].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12522 (R0x30EA)	**15:0**	**0xF800**	**ctx_wr_data (R/W)**		
	15:8	0x00F8	ctx_wr_control_word First Control Word. Legal values: [0, 255].	N	N
	7:4	0x0000	ctx_wr_context_num Number of Contexts This set the number of values (contexts) to store for each register address. A value of 0 indicates 1 context. You have two contexts, so this should be 0x1. Legal values: [0, 15].	N	N
	3:0	0x0000	ctx_wr_addr_value_high Upper address value. This set the value of A15:A12 of the register address that will be stored in the ram. For 0x30E8, this will be 0x3. So the value of the first control word should be 0xF813 (not0xF823). Legal values: [0, 15].	N	N
R12524 (R0x30EC)	**15:0**	**0x0000**	**ctx_rd_data (R/W)**	**N**	**N**
	context read data Legal values: [0, 65535].				
R12534 (R0x30F6)	**15:0**	**0x0000**	**dark_control4 (R/W)**	**N**	**N**
	15	0x0000	Reserved		
	14:13	0x0000	Reserved		
	12:4	X	Reserved		
	3:1	0x0000	tx_pulse_ratio tx pulse length control: 0: 4 rows 1: 8 rows 2: 16 rows 3: 32 rows 4: 64 rows 5: 128 rows 6: 256 rows 7: 512 rows Writes are synchronized to frame boundaries. Legal values: [0, 7].	Y	N
	0	0x0000	tx_pulse_enable enable tx pulse Writes are synchronized to frame boundaries.	Y	N
R12536 (R0x30F8)	**15:0**	**0x0033**	**gpio_ctrl (R/W)**		
	15:14	X	Reserved		
	13	0x0000	gpio1_hold GPIO1 hold	N	N
	12	0x0000	gpio0_hold GPIO0 hold	N	N
	11:10	X	Reserved		
	9	0x0000	gpio1_fsafe GPIO1 disable output and disconnect from supplt	N	N
	8	0x0000	gpio0_fsafe GPIO0 disable output and disconnect from supply	N	N
	7:6	X	Reserved		
	5	0x0001	gpio1_ip_pd GPIO1 input power down	N	N
	4	0x0001	gpio0_ip_pd GPIO0 input power down	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12536 (R0x30F8)	**3:2**	**X**	**Reserved**		
	1	0x0001	gpio1_oe GPIO1 output enable	N	N
	0	0x0001	gpio0_oe GPIO0 output enable	N	N
R12538 (R0x30FA)	**15:0**	**0xFC8C**	**gpio_select (R/W)**		
	15:13	0x0007	gpio3_pin_select Not used Legal values: [0, 7].	N	N
	12:10	0x0007	gpio2_pin_select Not used Legal values: [0, 7].	N	N
	9:7	0x0001	gpio1_pin_select default is output for Shutter signal Legal values: [0, 7].	N	N
	6:4	0x0000	gpio0_pin_select default is output for Flash signal Legal values: [0, 7].	N	N
	3	RO	gpio3 Not used Read-only.	N	N
	2	RO	gpio2 Not used Read-only.	N	N
	1	RO	gpio1 Read-only. Return the current state of the GPIO1 output pin. Invalid if R0x30F8[1]=0. Read-only.	N	N
	0	RO	gpio0 Read-only. Return the current state of the GPIO0 output pin. Invalid if R0x30F8[0]=0. Read-only.	N	N
R12544 (R0x3100)	**15:0**	**0x0000**	**adacd_control (R/W)**		
	15:2	X	Reserved		
	1	0x0000	adacdnr_filter_en When set, adacdnr filter is enabled	N	N
	0	X	Reserved		
R12562 (R0x3112)	**15:0**	**0x8000**	**hispi_timing_2 (R/W)**		
	15	0x0001	hispi_reva_comp_2 Should always be tied to "1"	N	N
	14:12	0x0000	cp_del_in_2 DLL setting for clock lane(1 step shifted by 1/8th UI) Legal values: [0, 7].	N	N
	11	0x0000	hres_in_2 Output bridge resistor trim value	N	N
	10:8	X	Reserved		
	7:0	0x0000	dll_trim_in_2 Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps. Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12564 (R0x3114)	**15:0**	**0x8000**	**hispi_timing_3 (R/W)**		
	15	0x0001	hispi_reva_comp_3 should always be tied to "1"	N	N
	14:12	0x0000	cp_del_in_3 DLL setting for clock lane(1 step shifted by 1/8th UI) Legal values: [0, 7].	N	N
	11	0x0000	hres_in_3 Output bridge resistor trim value	N	N
	10:8	X	Reserved		
	7:0	0x0000	dll_trim_in_3 Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps. Legal values: [0, 255].	N	N
R12566 (R0x3116)	**15:0**	**0x8000**	**hispi_timing_4 (R/W)**		
	15	0x0001	hispi_reva_comp_4 Should always be tied to "1"	N	N
	14:12	0x0000	cp_del_in_4 DLL setting for clock lane(1 step shifted by 1/8th UI) Legal values: [0, 7].	N	N
	11	0x0000	hres_in_4 Output bridge resistor trim value	N	N
	10:8	X	Reserved		
	7:0	0x0000	dll_trim_in_4 Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps. Legal values: [0, 255].	N	N
R12576 (R0x3120)	**15:0**	**0x0000**	**gain_dither_control (R/W)**	**N**	**N**
	15:1	X	Reserved		
	0	0x0000	gain_dither_enable gain dither enable. Writes are synchronized to frame boundaries.	Y	N
R12578 (R0x3122)	**15:0**	**0x0007**	**temp_threshold_value (R/W)**		
	tempsens_threshold Legal values: [0,65535].				
R12580 R0x3124	**15:0**	**0x0000**	**tempsens_data_reg (RO)**		
	Data from temperature sensor Read-only. Legal values: [0,1023].				
R12582 (R0x3126)	**15:0**	**0x0000**	**tempsens_ctrl_reg (R/W)**		
	15:7	X	Reserved		
	6	0x0000	tempsens_blc_trig_en Enable blc retrigger if temperature difference is more than threshold	N	N
	5	0x0000	temp_clear_value tempsens clear value when set.	N	N
	4	0x0000	temp_start_conversion tempsens start conversion when set	N	N
	3:1	0x0000	tempsens_test_ctrl tempsens test ctrl	N	N
	0	0x0000	tempsens_power_on tempsens power on when set.	N	N
R12584 (R0x3128)	**15:0**	**0x0123**	**tempsens_calib1 (R/W)**		
	User calibration register 1 Legal values: [0,65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12586 (R0x312A)	**15:0**	**0x4567**	**tempsens_calib2 (R/W)**		
	User calibration register 2 Legal values: [0,65535].				
R12588 (R0x312C)	**15:0**	**0x89AB**	**tempsens_calib3 (R/W)**		
	User calibration register 3 Legal values: [0,65535].				
R12590 (R0x312E)	**15:0**	**0xCDEF**	**tempsens_calib4 (R/W)**		
	user calibration register 4 Legal values: [0,65535].				
R12626 (R0x3152)	**15:0**	**0x0010**	**global_boost_rst (R/W)**		
	15:8	X	Reserved		
	7:0	0x0010	row_rstg_ctrl_done Defines the length of the row_rstg_ctrl off after row_rstd_ctrl is 64*global_boost_rst[7:0]+1 Legal values: [0, 255].	N	N
R12628 (R0x3154)	**15:0**	**0x3207**	**global_boost (R/W)**		
	15:8	0x0032	enable_cnt_g_boost_u Defines the time vtx hi back to VAA so that the total time is 64**global_boost[15:8]+1 Legal values: [0, 255].	N	N
	7:0	0x0007	util_pause Defines the length of the utility debug pause is 64*global_boost[7:0]+1 Legal values: [0, 255].	N	N
R12630 (R0x3156)	**15:0**	**0xC8F7**	**global_done (R/W)**		
	15:8	0x00C8	enable_cnt_g_end Defines time of precharge period is 64*global_done[15:8]+1 Legal values: [0, 255].	N	N
	7:0	0x00F7	enable_cnt_g_go Defines the time of tx back to ground is 64*global_done[7:0]+1 Legal values: [0, 255].	N	N
	Legal values: [0: 255].				
R12632 (R0x3158)	**15:0**	**0x0000**	**slave_mode_control (R/W)**		
	15	0x0000	vd_trig_new_frame vd trigger new frame Set to enable slave mode	N	N
	14	0x0000	vd_timer vd timer Set to limit the detection of slave mode trigger pulse around internal start of frame	N	N
	13	0x0000	vd_trig_grst vd triggered grst Set to enable slave mode in global reset mode	N	N
	12	0x0000	grr_burst_mode enable consecutive GRR frames Writes are synchronized to frame boundaries.	Y	N
	11	0x0000	vd_new_frame_only gate off external trigger pn	N	N
	10:0	X	Reserved		
R12634 (R0x315A)	**15:0**	**0x0000**	**global_flash_start (R/W)**		
	Global Flash Start If global_seq_trigger[2] = 1 (Global Flash enabled) and global_seq_trigger[6] = 1 (Use Flash Start), when a Global Reset sequence is triggered, the FLASH output signal will be pulsed during the integration phase of the Global Reset sequence. The start of the FLASH pulse is determined by global_flash_start. If global_flash_start < global_rst_end, the FLASH pulse will only be asserted at a fixed delay after global_rst_end. The FLASH output will not be asserted if global_flash_start > global_read_start. Writes are synchronized to frame boundaries. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12636 (R0x315C)	**15:0**	**0x0000**	**global_bulb_trigger_count (R/W)**		
	Bulb Trigger Count If global_seq_trigger[1] = 1 (Global Bulb enabled) when a Global Reset sequence is triggered and global_seq_trigger[10] = 1 (Bulb Trigger Timer), the end of the integration phase is determined by Bulb Trigger Count and global_seq_trigger[15:12] (Bulb Trigger Scale). Writes are synchronized to frame boundaries. Legal values: [0, 65535].				
R12638 (R0x315E)	**15:0**	**0x0000**	**global_seq_trigger (R/W)**		
	15:12	0x0000	global_seq_trigger_bulb_trig_scale Bulb Trigger Scale If global_seq_trigger[1] = 1 (Global Bulb enabled) when a Global Reset sequence is triggered and global_seq_trigger[10] = 1 (Bulb Trigger Timer), the end of the integration phase is determined by Bulb Trigger Count and global_seq_trigger[15:12] (Bulb Trigger Scale). Bulb Trigger Scale determines the number of cycles per count: 00 = 256 cycles per count 01 = 1024 cycles per count 10 = 64 cycles per count 11 = 1 cycle per count Legal values: [0, 15].	N	N
	11	0x0000	ggr_enable GGR_enable Writes are synchronized to frame boundaries.	Y	N
	10	0x0000	global_seq_trigger_bulb_trig_tmr Bulb Trigger If global_seq_trigger[1]=1 (Global Bulb enabled) when a Global Reset sequence is triggered this bits determines how the integration time is controlled: 0 = The end of the integration phase is controlled by the level of trigger (global_seq_trigger[0], or the associated GPI input). 1 = The end of the integration phase is determined by Bulb Trigger Count and global_seq_trigger[15:12] (Bulb Trigger Scale).	N	N
	9:8	X	Reserved		
	7	0x0000	global_seq_trigger_flash_sync When set, the flash output in global reset bulb mode will start after the falling edge of the global reset trigger signal.	N	N
	6	0x0000	global_seq_trigger_use_flash_start When set, the start of the FLASH pulse is determined by global_flash_start.	N	N
	5:4	0x0000	global_seq_trigger_global_scale Global Scale Decoded value (lets call it global_scale_factor) of this field is used as the step size for duration of integration time/shutter starting from end of row reset phase of Global reset. The field is decoded as 0 = 512 1 = 2048 2 = 128 3 = 32 I.E. for integration time, of A value of N of the 24 bit field {global_read_start2[7:0], global_read_start[15:0]} gives an assertion time of (N − global_reset_end[15:0])* global_scale_factor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Writes are synchronized to frame boundaries. Legal values: [0, 3].	Y	N
	3	0x0000	grst_ggr_enable Grst_GGR_enable Writes are synchronized to frame boundaries.	Y	N
	2	0x0000	global_seq_trigger_global_flash Global Flash 0 = When a Global Reset sequence is triggered, the FLASH output will remain negated. 1 = When a Global Reset sequence is triggered, the FLASH output will pulse during the integration phase.	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12638 (R0x315E)	1	0x0000	global_seq_trigger_global_bulb Global Bulb 0 = Shutter open is triggered from bit[0] and shutter close is timed from the trigger point. 1 = Shutter open and close are triggered from bit[0]. This corresponds to the shutter "B" setting on a traditional camera, where "B" originally stood for "Bulb" (the shutter setting used for synchronization with a magnesium foil flash bulb) and was later considered to stand for "Brief" (an exposure that was longer than the shutter could automatically accommodate).	N	N
	0	0x0000	global_seq_trigger_global_trigger Global Trigger When bit[1] = 0, a 0−to−1 transition of this bit initiates (triggers) a global reset sequence. When bit[1] = 1,a 0-to-1 transition of this bit initiates a global reset sequence, and leaves the shutter open; a 1-to-0 transition of this bit closes the shutter. These operations can also be controlled from the signal interface by enabling one of the GPI[3:0] signals as a trigger input.	N	N
R12640 (R0x3160)	**15:0**	**0x00EC**	**global_rst_end (R/W)**	**N**	**N**
	Controls the duration of the global reset row reset phase. A value of N gives a duration of N * 512 / vt_pix_clk_freq_mhz. Legal values: [0, 65535].				
R12642 (R0x3162)	**15:0**	**0x0317**	**global_shutter_start (R/W)**	**Y**	**N**
	Blobal Shutter Start Bits 15−0 of a 24-bit value which controls the delay before the assertion of the SHUTTER output during a global reset sequence. A value of N of the 24 bit field {global_stutter_start2[7:0], global_shutter_start} gives an assertion time of (N − global_reset_end[15:0])* global_scale_factor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 65535].				
R12644 (R0x3164)	**15:0**	**0x0000**	**global_shutter_start2 (R/W)**		
	Global Shutter Start 2 Bits 23−16 of a 24-bit value which controls the delay before the assertion of the SHUTTER output during a global reset sequence. A value of N of the 24 bit field {global_stutter_start2[7:0], global_shutter_start} gives an assertion time of (N − global_reset_end[15:0])* global_scale_factor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 255].				
R12646 (R0x3166)	**15:0**	**0x0327**	**global_read_start (R/W)**	**Y**	**N**
	Global Read Start Bits 15−0 of a 24-bit value which controls the delay before the start of the global reset readout phase (equivalent to the end of global reset integration phase). A value of N of the 24 bit field {global_read_start2[7:0], global_read_start[15:0]} gives an assertion time of (N − global_reset_end[15:0])* global_scale_factor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 65535].				
R12648 (R0x3168)	**15:0**	**0x0000**	**global_read_start2 (R/W)**	**N**	**N**
	Global Read Start2 Bits 23−16 of a 24-bit value which controls the delay before the start of the global reset readout phase (equivalent to the end of global reset integration phase). A value of N of the 24 bit field {global_read_start2[7:0], global_read_start[15:0]} gives an assertion time of (N − global_reset_end[15:0])* global_scale_factor / vt_pix_clk_freq_mhz timed from the end of row reset phase of Global reset. Legal values: [0, 255].				
R12656 (R0x3170)	**15:0**	**0x236E**	**analog_control (R/W)**	**N**	**N**
	15:14	0x0000	Reserved		
	13	0x0001	Reserved		
	12	0x0000	asc_test Enable ASC test	N	N
	11:0	0x036E	Reserved		

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12658 (R0x3172)	**15:0**	**0x0201**	**analog_control2 (R/W)**	**N**	**N**
	15	X	Reserved		
	14	0x0000	adc_diff_data_width adc_diff_data_width Writes are synchronized to frame boundaries.	Y	N
	13	0x0000	Reserved		
	12	0x0000	Reserved		
	11:10	X	Reserved		
	9:8	0x0002	Reserved		
	7	X	Reserved		
	6	0x0000	ana_bin Enable analog binning.	N	N
	5	0x0000	opt_dig_bin Enable digital binning.	N	N
	4	0x0000	Reserved		
	3	0x0000	Reserved		
	2:0	0x0001	Reserved		
R12660 (R0x3174)	**15:0**	**0x0000**	**analog_control3 (R/W)**	**N**	**N**
	15	0x0000	dynamic_power_control_ers_enable Enable bit for DYNAMIC_POWER_CONTROL_ERS 0: disable 1: enable	N	N
	14:12	0x0000	scale Sets pixel timing scale value Legal values: [0, 7].	N	N
	11:0	0x0000	dynamic_power_control_ers Used when bit 15 is set to 1 and sensor is in ERS mode if coarse integration is equal or greater than the value of (bit[11:0] * 16), pwr_dynamic<1> will be off (logic 0) during vertical blanking when dark rows are not being read. Legal values: [0, 4095].	N	N
R12662 (R0x3176)	**15:0**	**0x1000**	**analog_control4 (R/W)**	**N**	**N**
	15	0x0000	dynamic_power_control_grr_enable Enable bit for DYNAMIC_POWER_CONTROL_GRR 0: disable 1: enable	N	N
	14	0x0000	t_context_0 Dual pixel timing context switching Writes are synchronized to frame boundaries.	Y	N
	13	0x0000	t_context_1 Dual pixel timing context switching	N	N
	12	0x0001	glatch_dis Set to disable global latch Writes are synchronized to frame boundaries.	Y	N
	11:0	0x0000	dynamic_power_control_grr Used when bit 15 is set to 1 and sensor is in GRR mode if register-controlled integration is equal or greater than the value of (bit[11:0]*16), pwr_dynamic<1> is off (logic 0), If in bulb mode, pwr_dynamic<1> is off during integration phase. Legal values: [0, 4095].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12718 (R0x31AE)	**15:0**	**0x0204**	**serial_format (R/W)**	**N**	**N**
	15	0x0000	serial__format_lock Prevent serial format from power definition	N	N
	14:10	X	Reserved		
	9:8	0x0002	serial__format_type Serial interface type 2: MIPI 3:Hispi Legal values: [0, 3].	N	N
	7:5	X	Reserved		
	4:0	0x0004	serial__format_lanes Serial data lanes Legal values: [0, 31].	N	N
R12720 (R0x31B0)	**15:0**	**0x005C**	**frame_preamble (R/W)**		
	frame preamble This timing value, expressed in op_pix_clk periods, must be large enough to allow the MIPI wake-up and start-of-frame short packet to be transmitted prior to the start of a frame of pixel data. The default value should be correct for most applications. Too small a value will result in an INSUFFICIENT_FRAME_PREAMBLE error being flagged in the DATAPATH_STATUS register. Legal values: [0, 255].				
R12722 (R0x31B2)	**15:0**	**0x002D**	**line_preamble (R/W)**		
	line preamble This timing value, expressed in op_pix_clk periods, must be large enough to allow the MIPI long packet header to be transmitted prior to the start of a line of pixel data. The default value should be correct for most applications. Too small a value will result in an INSUFFICIENT_LINE_PREAMBLE error being flagged in the DATAPATH_STATUS register. Legal values: [0, 255].				
R12724 (R0x31B4)	**15:0**	**0x23D2**	**mipi_timing_0 (R/W)**		
	15:12	0x0002	t_hs_prepare Time (in clk cycles) to drive LP−00 prior to entering HS data transmission mode Legal values: [0, 15].	N	N
	11:6	0x000F	t_hs_zero Time, in op_pix_clk periods, to drive HS−0 before the sync sequence Legal values: [0, 63].	N	N
	5:1	0x0009	t_hs_trail Time, in op_pix_clk periods, to drive flipped differential state after last payload data bit of an HS transmission burst Legal values: [0, 31].	N	N
	0	X	Reserved		
R12726 (R0x31B6)	**15:0**	**0x140A**	**mipi_timing_1 (R/W)**		
	15:12	0x0001	t_clk_prepare Time, in op_pix_clk periods, to drive LP−00 prior to entering HS data transmission mode Legal values: [0, 15].	N	N
	11:5	0x0020	t_clk_zero Minimum time, in op_pix_clk periods, to drive HS−0 on clock lane prior to starting clock Legal values: [0, 127].	N	N
	4:0	0x000A	t_clk_trail Time, in op_pix_clk periods, to drive HS differentialstate after last payload clock bit of an HS transmission burst Legal values: [0, 31].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12728 (R0x31B8)	**15:0**	**0x2413**	**mipi_timing_2 (R/W)**	**N**	**N**
	15:10	0x0009	t_bgap bandgap settling time Legal values: [0, 63].	N	N
	9:4	0x0001	t_clk_pre Time, in op_pix_clk periods, to drive the HS clock before any data lane might start up Legal values: [0, 63].	N	N
	3:0	0x0003	t_clk_post_h Time, in op_pix_clk periods, to drive the HS clock after the data lane has gone into low-power mode (high part) Legal values: [0, 15].	N	N
R12730 (R0x31BA)	**15:0**	**0x1C70**	**mipi_timing_3 (R/W)**	**N**	**N**
	15:10	0x0007	t_lpx Time, in op_pix_clk periods, of any low-power state period Legal values: [0, 63].	N	N
	9:3	0x000E	t_wake_up Time to recover from ultra low-power mode (ULPM). ULPM is exited by applying a mark state for (8192) * T_WAKE_UP * op_pix_clk Legal values: [0, 127].	N	N
	2	X	Reserved		
	1:0	0x0000	t_clk_post_l Time, in op_pix_clk periods, to drive the HS clock after the data lane has gone into low-power mode(low part) Legal values: [0, 3].	N	N
R12732 (R0x31BC)	**15:0**	**0x860B**	**mipi_timing_4 (R/W)**		
	15	0x0001	cont_tx_clk Keep MIPI clock active between packets/ HiSPi transmitted clock continues to run when HiSPi is in the "inactive" operating mode	N	N
	14	0x0000	heavy_lp_load_in contol of phy heavy_lp_load pin	N	N
	13	0x0000	vreg_mode_in 0= internal voltage regulator turned OFF 1= internal voltage regulator turned ON	N	N
	12:7	0x000C	t_hs_exit Time, in op_pix_clk periods, to drive LP−11 after HS burst Legal values: [0, 63].	N	N
	6:0	0x000B	t_init Initialisation time when first entering stop state (LP−11) after powerup or reset. LP−11 is transmitted for a minimum of (1024) * T_INIT * op_pix_clk. Legal values: [0, 127].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12734 (R0x31BE)	**15:0**	**0xD083**	**mipi_config (R/W)**	**N**	**N**
	15	RO	reg_frame_sync Safe to update the frame synced registers Read-only.	N	N
	14	RO	mipi_standby MIPI standby Read-only.	N	N
	13	RO	mipi_rdy_for_data MIPI ready for data Read-only.	N	N
	12	0x0001	phy_init_state Define Phy initial state	N	N
	11	0x0000	hispi_mode_change_req When asserted all active HiSPi lanes will drive a differential-0 and hispi_mode_change_rdy will be asserted in response	N	N
	10	0x0000	mipi_mirror_2lanes mirror mipi lanes 0,1 to lanes 2,3	N	N
	9	0x0000	test_mipi_start_checksum start mipi checksum	N	N
	8	X	Reserved		
	7	0x0001	hispi_mirror_mode mirror 1st HiSPi (4lanes) to other HiSPi (4lanes) existed in the system	N	N
	6:4	0x0000	lp_slew_in MIPI low power driver slew rate trim Legal values: [0, 7].	N	N
	3:2	0x0000	hispi_phy_mode select PHY signaling standard 00: SLVS PHY signaling internal regulator (0.2V common mode) 01: SLVS PHY signaling external regulator (0.2V common mode) 10: subLVDS PHY signaling (0.9V common mode) 11: Reserved Legal values: [0, 3].	N	N
	1	0x0001	frame_cnt_reset mipi frame count reset	N	N
	0	0x0001	frame_cnt_en mipi frame count enable	N	N
R12736 (R0x31C0)	**15:0**	**0x8000**	**hispi_timing_1 (R/W)**	**N**	**N**
	15	0x0001	hispi_reva_comp_1 Should always be tied to "1"	N	N
	14:12	0x0000	cp_del_in_1 DLL setting for clock lane(1 step shifted by 1/8th UI) Legal values: [0, 7].	N	N
	11	0x0000	hres_in_1 Output bridge resistor trim value	N	N
	10:8	X	Reserved		
	7:0	0x0000	dll_trim_in_1 Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps. Legal values: [0, 255].	N	N
R12738 (R0x31C2)	**15:0**	**0xFFFF**	**hispi_blanking (R/W)**	**N**	**N**
	HiSpi Blanking Data output during during blanking period if blanking_data_enable =1 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12740 (R0x31C4)	**15:0**	**0xF555**	**hispi_sync_patt (R/W)**	**N**	**N**
	15:8	0x00F5	vsync_patt Defines pattern for the 8 word sync code transmitted prior to the first line of a frame (hispi Actistart−SP8)− a 1 means the corresponding word = all 1s; b0 corresponds to the first transmitted word of the code, b7 to the last. Optionally the last transmitted word can be overwriten with a code specified by vsync_override_code Legal values: [0, 255].	N	N
	7:0	0x0055	hsync_patt Defines pattern for the 8 word sync code transmitted prior to any line other than the first line of a frame (hispi Actistart−SP8)− a 1 means the corresponding word = all 1 s; b0 corresponds to the first transmitted word of the code, b7 to the last Legal values: [0, 255].	N	N
R12742 (R0x31C6)	**15:0**	**0x8000**	**hispi_control_status (R/W)**	**N**	**N**
	15	RO	mipi_hispi_idle MIPI/ HiSPi idle Read-only.	N	N
	14	RO	checksum_valid checksum valid Read-only.	N	N
	13	0x0000	mask_framer_standby mask framer standby	N	N
	12	0x0000	transmit_checksum transmit checksum	N	N
	11:10	0x0000	hispi_mode_select hispi mode select 00: HiSPi S protocol 01: HiSPi SP protocol 10: HiSPi Actistart− SP8 protocol Legal values: [0, 3].	N	N
	9	0x0000	test_hispi_start_checksum Start HiSPi checksum	N	N
	8	0x0000	io_tri_state_test IO tri_state test	N	N
	7	0x0000	test_en Enables test data (as defined by the test_mode[3:0])	N	N
	6:4	0x0000	mipi_hispi_framer_status_select MIPI/ HiSPi framer status select − for framer status 000: 1st framer status select 001: 2nd framer status select 010: 3rd framer status select 100: 4th framer status select Legal values: [0, 7].	N	N
	3	0x0000	blanking_data_enable blanking_data_enable	N	N
	2	0x0000	hispi_sp_protocol HiSPisp protocol 0: packetised 1: streaming	N	N
	1	0x0000	output_msb_first output msb first	N	N
	0	0x0000	vert_left_bar_en vert left bar en	N	N
R12744 (R0x31C8)	**15:0**	**0x0000**	**hispi_ckecksum0 (RO)**		
	hispi_ckecksum0 Read-only. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12746 (R0x31CA)	**15:0**	**0x0000**	**hispi_ckecksum1 (RO)**		
	hispi_ckecksum1 Read-only. Legal values: [0, 65535].				
R12748 (R0x31CC)	**15:0**	**0x0000**	**hispi_ckecksum2 (RO)**		
	hispi_ckecksum2 Read−only. Legal values: [0, 65535].				
R12750 (R0x31CE)	**15:0**	**0x0000**	**hispi_ckecksum3 (RO)**		
	hispi_ckecksum3 Read-only. Legal values: [0, 65535].				
R12752 (R0x31D0)	**15:0**	**0x3231**	**mipi_compress_8_data_type (R/W)**		
	15:14	X	Reserved		
	13:8	0x0032	data_type_10_8_10 data type for 10_8_10 Legal values: [0, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0031	data_type_12_8_12 data type for 12_8_12 Legal values: [0, 63].	N	N
R12754 (R0x31D2)	**15:0**	**0x3534**	**mipi_compress_7_data_type (R/W)**		
	15:14	X	Reserved		
	13:8	0x0035	data_type_10_7_10 data type for 10_7_10 Legal values: [0, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0034	data_type_12_7_12 data type for 12_7_12 Legal values: [0, 63].	N	N
R12756 (R0x31D4)	**15:0**	**0x3736**	**mipi_compress_6_data_type (R/W)**		
	15:14	X	Reserved		
	13:8	0x0037	data_type_10_6_10 data type for 10_6_10 Legal values: [0, 63].	N	N
	7:6	X	Reserved		
	5:0	0x0036	data_type_12_6_12 data type for 12_6_12 Legal values: [0, 63].	N	N
R12758 (R0x31D6)	**15:0**	**0x336B**	**mipi_jpeg_pn9_data_type (R/W)**		
	15	0x0000	big_endian 0 = Little Endian; 1 = Big Endian	N	N
	14	X	Reserved		
	13:8	0x0033	data_type_pn9 data type for pn9 Legal values: [0, 63].	N	N
	7:6	0x0001	virtual_chan 00 = Virtual Channel 1; 01 = Virtual Channel 2; 10 = Virtual Channel 3; 11 = Virtual Channel 4	N	N
	5:0	0x002B	data_type_jpeg data type for jpeg Legal values: [0, 63].	N	N
R12762 (R0x31DA)	**15:0**	**0x0000**	**pll_dither_1 (R/W)**		
	pll_dither[15:0] Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12764 (R0x31DC)	**15:0**	**0x0000**	**pll_dither_2 (R/W)**		
	pll_dither[31:16] Legal values: [0, 65535].				
R12766 (R0x31DE)	**15:0**	**0x0000**	**pll_dither_3 (R/W)**	**N**	**N**
	pll_dither[41:32] Legal values: [0, 1023].				
R12768 (R0x31E0)	**15:0**	**0x0001**	**pix_def_id (R/W)**	**N**	**N**
	15:13	X	Reserved		
	12	0x0000	pix_def_id_crm_tag_enable Enables CRM tagging 0: disable 1: enable	N	N
	11:1	X	Reserved		
	0	0x0001	pix_def_id_en Enable pixel defect identification 0: disable 1: enable Writes are synchronized to frame boundaries.	Y	N
R12770 (R0x31E2)	**15:0**	**0x0000**	**pix_def_id_ram_write (R/W)**	**N**	**N**
	Data written to pixel identification memory Legal values: [0, 65535].				
R12772 (R0x31E4)	**15:0**	**0x0000**	**pix_def_id_ram_read (RO)**	**N**	**N**
	Data read from pixel identification memory Read-only. Legal values: [0, 65535].				
R12784 (R0x31F0)	**15:0**	**0x0000**	**chain_control (R/W)**	**N**	**N**
	15:14	X	Reserved		
	13	0x0000	i2c_alias When set (1) I^2C I/F responds to both primary and secondary I^2C IDs. When used in multi-chip mode these are device and global IDs.	N	N
	12	0x0000	i2c_passive When set (1) responds Read/Write to I^2C device ID and accepts Writes (without ACK) to global ID. This allows for one device to be master(give ACK) and others passive.	N	N
	11:8	0x0000	vd_del Tap on 16-bit shift register used for delay of internal trigger. Shift register is clocked using EXTCLK. Allows daisy chained devices to align internal trigger. Legal values: [0, 15].	N	N
	7:0	X	Reserved		
R12786 (R0x31F2)	**15:0**	**0x6E6C**	**i2c_ids_mipi_default (R/W)**	**N**	**N**
	i2c_ids_mipi_default Legal values: [0, 65535].				
R12796 (R0x31FC)	**15:0**	**0x6E6C**	**i2c_ids (R/W)**	**N**	**N**
	Two-wire serial interface (I^2C) addresses. Legal values: [0, 65535].				
R12798 (R0x31FE)	**15:0**	**0x0000**	**customer_rev (RO)**	**N**	**N**
	Customer revision Read-only. Legal values: [0, 65535].				
R12810 (R0x320A)	**15:0**	**0x0000**	**pll_dither_4 (R/W)**		
	pll_dither[57:42] Legal values: [0, 65535].				
R12812 (R0x320C)	**15:0**	**0x0000**	**pll_dither_5 (R/W)**		
	pll_dither[73:58] Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12814 (R0x320E)	**15:0**	**0x0000**	**pll_dither_6 (R/W)**	**N**	**N**
	pll_dither[83:74] Legal values: [0, 1023].				
R12832 (R0x3220)	**15:0**	**0x0003**	**pdaf_control (R/W)**	**N**	**N**
	15	0x0000	pdaf_test_en Enable pdaf test. 0: disable 1: enable. When set, extend pdaf row output columns to the same length as visual path by padding 0 s to the end of valid pdaf data.	Y	N
	14:12	X	Reserved		
	11	0x0000	pdaf_pe_en Enable pdaf programmable engine on focus data. 0: disable 1: enable	Y	N
	10:8	0x0000	pdaf_den_w 3-tap denoise weight on focus data. 0: turn off denoise Legal values: [0, 7].	Y	N
	7	X	Reserved		
	6:5	0x0000	pdaf_bin_size Enable x-bin on focus data. Bin_factor = 1 ^ bin_size Legal values: [0, 3].	Y	N
	4	0x0000	pdaf_dc_en Enable 1ddc on focus data. 0: disable 1: enable	Y	N
	3	0x0000	pdaf_sc_pdaf_sh Right-shift spatial correction amount1-bit on focus path. 0: No-shift 1: Right-shift 1-bit	Y	N
	2	0x0000	pdaf_sc_pdaf_en enable spatial correction on focus path. 0: disabale 1: enable	Y	N
	1	0x0001	pdaf_sc_en enable spatial correction on visual path. 0: disable 1: enable	Y	N
	0	0x0001	pdaf_en enable pdaf module 0: disable 1: enable. When this bit disabled, all pdaf module functions are disabled.	Y	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12834 (R0x3222)	**15:0**	**0xE0C0**	**pdaf_row_control (R/W)**		
	15	0x0001	pdaf_pat_en enable pdaf row pattern. 0: disable 1: enable	Y	N
	14:13	0x0003	pdaf_bin_op pdaf analog row binning option. 00: no pdaf rows in pixel array. 01: output un-binned pdaf row data. 10: output un-binned normal row data. 11: output binned pdaf/normal row data. Legal values: [0, 3].	Y	N
	12	X	Reserved		
	11:0	0x00C0	pdaf_pat_yd number of rows between two adjacent pdaf rows Legal values: [0, 4095].	Y	N
R12836 (R0x3224)	**15:0**	**0x0001**	**pdaf_pat_control (R/W)**		
	15:2	X	Reserved		
	1:0	0x0001	pdaf_pat_dash dash-line pattern. 0: full pdaf line. 1: dashed 2−1 pdaf line. 2: dashed 2−2 pdaf line Legal values: [0,2].	N	N
R12838 (R0x3226)	**15:0**	**0x00E0**	**pdaf_row_start (R/W)**		
	The first pdaf row address within y_addr_start/y_addr_end window Writes are synchronized to frame boundaries. Legal values: [0, 4095].				
R12840 (R0x3228)	**15:0**	**0x0B60**	**pdaf_row_end (R/W)**		
	The last pdaf row address within y_addr_start/y_addr_end window Writes are synchronized to frame boundaries. Legal values: [0, 4095].				
R12842 (R0x322A)	**15:0**	**0x00C8**	**pdaf_col_start (R/W)**		
	The first pdaf column address Legal values: [0, 8191].				
R12844 (R0x322C)	**15:0**	**0x0FB5**	**pdaf_col_end (R/W)**		
	The last pdaf column address Legal values: [0, 8191].				
R12846 (R0x322E)	**15:0**	**0x00A8**	**pdaf_pedestal (R/W)**		
	Focus path data pedestal after spatial correction Legal values: [0, 8191].				
R12848 (R0x3230)	**15:0**	**0x0FFE**	**pdaf_sat_th (R/W)**	**Y**	**N**
	focus path saturation threshold Legal values: [0, 8191].				
R12850 (R0x3232)	**15:0**	**0x0000**	**pdaf_sc_origin_y (R/W)**		
	spatial correction image center x coordinate Legal values: [0, 4095].				
R12852 (R0x3234)	**15:0**	**0x0000**	**pdaf_sc_origin_x (R/W)**		
	spatial correction image center y coordinate Legal values: [0, 8191].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12854 (R0x3236)	**15:0**	**0x0000**	**pdaf_sc_f_sh_0 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_0 Spatial correction shift for channel 0 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_0 Spatial correction mantissa for channel 0 Legal values: [0, 4095].	N	N
R12856 (R0x3238)	**15:0**	**0x0000**	**pdaf_sc_f_sh_1 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_1 Spatial correction shift for channel 1 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_1 Spatial correction mantissa for channel 1 Legal values: [0, 4095].	N	N
R12858 (R0x323A)	**15:0**	**0x0000**	**pdaf_sc_f_sh_2 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_2 Spatial correction shift for channel 2 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_2 Spatial correction mantissa for channel 2 Legal values: [0, 4095].	N	N
R12860 (R0x323C)	**15:0**	**0x0000**	**pdaf_sc_f_sh_3 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_3 Spatial correction shift for channel 3 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_3 Spatial correction mantissa for channel 3 Legal values: [0, 4095].	N	N
R12862 (R0x323E)	**15:0**	**0x0000**	**pdaf_sc_f_sh_4 (R/W)**		
	15:12	0x0000	pdaf_sc_sh_4 Spatial correction shift for channel 4 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_4 Spatial correction mantissa for channel 4 Legal values: [0, 4095].	N	N
R12864 (R0x3240)	**15:0**	**0x0000**	**pdaf_sc_f_sh_5 (R/W)**		
	15:12	0x0000	pdaf_sc_sh_5 Spatial correction shift for channel 5 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_5 Spatial correction mantissa for channel 5 Legal values: [0, 4095].	N	N
R12866 (R0x3242)	**15:0**	**0x0000**	**pdaf_sc_f_sh_6 (R/W)**		
	15:12	0x0000	pdaf_sc_sh_6 Spatial correction shift for channel 6 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_6 Spatial correction mantissa for channel 6 Legal values: [0, 4095].	N	N
R12868 (R0x3244)	**15:0**	**0x0000**	**pdaf_sc_f_sh_7 (R/W)**		
	15:12	0x0000	pdaf_sc_sh_7 spatial correction shift for channel 7 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_7 Spatial correction mantissa for channel 7 Legal values: [0, 4095].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12870 (R0x3246)	**15:0**	**0x0000**	**pdaf_sc_f_sh_8 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_8 Spatial correction shift for channel 8 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_8 Spatial correction mantissa for channel 8 Legal values: [0, 4095].	N	N
R12872 (R0x3248)	**15:0**	**0x0000**	**pdaf_sc_f_sh_9 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_9 Spatial correction shift for channel 9 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_9 Spatial correction mantissa for channel 9 Legal values: [0, 4095].	N	N
R12874 (R0x324A)	**15:0**	**0x0000**	**pdaf_sc_f_sh_10 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_10 Spatial correction shift for channel 10 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_10 Spatial correction mantissa for channel 10 Legal values: [0, 4095].	N	N
R12876 (R0x324C)	**15:0**	**0x0000**	**pdaf_sc_f_sh_11 (R/W)**		
	15:12	0x0000	pdaf_sc_sh_11 Spatial correction shift for channel 11 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_11 Spatial correction mantissa for channel 11 Legal values: [0, 4095].	N	N
R12878 (R0x324E)	**15:0**	**0x0000**	**pdaf_sc_f_sh_12 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_12 spatial correction shift for channel 12 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_12 Spatial correction mantissa for channel 12 Legal values: [0, 4095].	N	N
R12880 (R0x3250)	**15:0**	**0x0000**	**pdaf_sc_f_sh_13 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_13 Spatial correction shift for channel 13 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_13 Spatial correction mantissa for channel 13 Legal values: [0, 4095].	N	N
R12882 (R0x3252)	**15:0**	**0x0000**	**pdaf_sc_f_sh_14 (R/W)**		
	15:12	0x0000	pdaf_sc_sh_14 Spatial correction shift for channel 14 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_14 Spatial correction mantissa for channel 14 Legal values: [0, 4095].	N	N
R12884 (R0x3254)	**15:0**	**0x0000**	**pdaf_sc_f_sh_15 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_15 Spatial correction shift for channel 15 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_15 Spatial correction mantissa for channel 15 Legal values: [0, 4095].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12886 (R0x3256)	**15:0**	**0x0000**	**pdaf_sc_f_sh_16 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_16 Spatial correction shift for channel 16 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_16 Spatial correction mantissa for channel 16 Legal values: [0, 4095].	N	N
R12888 (R0x3258)	**15:0**	**0x0000**	**pdaf_sc_f_sh_17 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_17 Spatial correction shift for channel 17 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_17 Spatial correction mantissa for channel 17 Legal values: [0, 4095].	N	N
R12890 (R0x325A)	**15:0**	**0x0000**	**pdaf_sc_f_sh_18 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_18 Spatial correction shift for channel 18 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_18 Spatial correction mantissa for channel 18 Legal values: [0, 4095].	N	N
R12892 (R0x325C)	**15:0**	**0x0000**	**pdaf_sc_f_sh_19 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_19 spatial correction shift for channel 19 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_19 spatial correction mantissa for channel 19 Legal values: [0, 4095].	N	N
R12894 (R0x325E)	**15:0**	**0x0000**	**pdaf_sc_f_sh_20 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_20 spatial correction shift for channel 20 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_20 spatial correction mantissa for channel 20 Legal values: [0, 4095].	N	N
R12896 (R0x3260)	**15:0**	**0x0000**	**pdaf_sc_f_sh_21 (R/W)**	**N**	**N**
	15:12	0x0000	pdaf_sc_sh_21 spatial correction shift for channel 21 Legal values: [0, 15].	N	N
	11:0	0x0000	pdaf_sc_f_21 Spatial correction mantissa for channel 21 Legal values: [0, 4095].	N	N
R12898 (R0x3262)	**15:0**	**0x0000**	**pdaf_sc_slope_x_0 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_0 Spatial correction slope from center to left for channel 0 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_0 Spatial correction slope from center to right for channel 0 Legal values: [0, 255].	N	N
R12900 (R0x3264)	**15:0**	**0x0000**	**pdaf_sc_slope_x_1 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_1 Spatial correction slope from center to left for channel 1 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_1 Spatial correction slope from center to right for channel 1 Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12902 (R0x3266)	**15:0**	**0x0000**	**pdaf_sc_slope_x_2 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_2 Spatial correction slope from center to left for channel 2 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_2 Spatial correction slope from center to right for channel 2 Legal values: [0, 255].	N	N
R12904 (R0x3268)	**15:0**	**0x0000**	**pdaf_sc_slope_x_3 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_3 Spatial correction slope from center to left for channel 3 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_3 Spatial correction slope from center to right for channel 3 Legal values: [0, 255].	N	N
R12906 (R0x326A)	**15:0**	**0x0000**	**pdaf_sc_slope_x_4 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_4 Spatial correction slope from center to left for channel 4 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_4 Spatial correction slope from center to right for channel 4 Legal values: [0, 255].	N	N
R12908 (R0x326C)	**15:0**	**0x0000**	**pdaf_sc_slope_x_5 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_5 Spatial correction slope from center to left for channel 5 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_5 Spatial correction slope from center to right for channel 5 Legal values: [0, 255].	N	N
R12910 (R0x326E)	**15:0**	**0x0000**	**pdaf_sc_slope_x_6 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_6 Spatial correction slope from center to left for channel 6 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_6 spatial correction slope from center to right for channel 6 Legal values: [0, 255].	N	N
R12912 (R0x3270)	**15:0**	**0x0000**	**pdaf_sc_slope_x_7 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_left_7 Spatial correction slope from center to left for channel 7 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_7 spatial correction slope from center to right for channel 7 Legal values: [0, 255].	N	N
R12914 (R0x3272)	**15:0**	**0x0000**	**pdaf_sc_slope_x_8 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_left_8 Spatial correction slope from center to left for channel 8 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_8 spatial correction slope from center to right for channel 8 Legal values: [0, 255].	N	N
R12916 (R0x3274)	**15:0**	**0x0000**	**pdaf_sc_slope_x_9 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_left_9 Spatial correction slope from center to left for channel 9 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_9 Spatial correction slope from center to right for channel 9 Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12918 (R0x3276)	**15:0**	**0x0000**	**pdaf_sc_slope_x_10 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_10 Spatial correction slope from center to left for channel 10 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_10 Spatial correction slope from center to right for channel 10 Legal values: [0, 255].	N	N
R12920 (R0x3278)	**15:0**	**0x0000**	**pdaf_sc_slope_x_11 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_11 Spatial correction slope from center to left for channel 11 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_11 Spatial correction slope from center to right for channel 11 Legal values: [0, 255].	N	N
R12922 (R0x327A)	**15:0**	**0x0000**	**pdaf_sc_slope_x_12 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_12 Spatial correction slope from center to left for channel 12 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_12 Spatial correction slope from center to right for channel 12 Legal values: [0, 255].	N	N
R12924 (R0x327C)	**15:0**	**0x0000**	**pdaf_sc_slope_x_13 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_13 Spatial correction slope from center to left for channel 13 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_13 Spatial correction slope from center to right for channel 13 Legal values: [0, 255].	N	N
R12926 (R0x327E)	**15:0**	**0x0000**	**pdaf_sc_slope_x_14 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_14 Spatial correction slope from center to left for channel 14 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_14 Spatial correction slope from center to right for channel 14 Legal values: [0, 255].	N	N
R12928 (R0x3280)	**15:0**	**0x0000**	**pdaf_sc_slope_x_15 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_15 Spatial correction slope from center to left for channel 15 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_15 Spatial correction slope from center to right for channel 15 Legal values: [0, 255].	N	N
R12930 (R0x3282)	**15:0**	**0x0000**	**pdaf_sc_slope_x_16 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_16 Spatial correction slope from center to left for channel 16 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_16 Spatial correction slope from center to right for channel 16 Legal values: [0, 255].	N	N
R12932 (R0x3284)	**15:0**	**0x0000**	**pdaf_sc_slope_x_17 (R/W)**	**N**	**N**
	15:8	0x0000	pdaf_sc_slope_x_left_17 Spatial correction slope from center to left for channel 17 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_17 Spatial correction slope from center to right for channel 17 Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12934 (R0x3286)	**15:0**	**0x0000**	**pdaf_sc_slope_x_18 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_left_18 Spatial correction slope from center to left for channel 18 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_18 Spatial correction slope from center to right for channel 18 Legal values: [0, 255].	N	N
R12936 (R0x3288)	**15:0**	**0x0000**	**pdaf_sc_slope_x_19 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_left_19 Spatial correction slope from center to left for channel 19 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_19 Spatial correction slope from center to right for channel 19 Legal values: [0, 255].	N	N
R12938 (R0x328A)	**15:0**	**0x0000**	**pdaf_sc_slope_x_20 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_left_20 Spatial correction slope from center to left for channel 20 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_20 Spatial correction slope from center to right for channel 20 Legal values: [0, 255].	N	N
R12940 (R0x328C)	**15:0**	**0x0000**	**pdaf_sc_slope_x_21 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_left_21 Spatial correction slope from center to left for channel 21 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_right_21 Spatial correction slope from center to right for channel 21 Legal values: [0, 255].	N	N
R12942 (R0x328E)	**15:0**	**0x0000**	**pdaf_sc_slope_y_0 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_0 Spatial correction slope from center downwards 0 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_0 Spatial correction slope from center upwards 0 Legal values: [0, 255].	N	N
R12944 (R0x3290)	**15:0**	**0x0000**	**pdaf_sc_slope_y_1 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_1 Spatial correction slope from center downwards 1 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_1 Spatial correction slope from center upwards 1 Legal values: [0, 255].	N	N
R12946 (R0x3292)	**15:0**	**0x0000**	**pdaf_sc_slope_y_2 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_2 Spatial correction slope from center downwards 2 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_2 Spatial correction slope from center upwards 2 Legal values: [0, 255].	N	N
R12948 (R0x3294)	**15:0**	**0x0000**	**pdaf_sc_slope_y_3 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_3 Spatial correction slope from center downwards 3 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_3 spatial correction slope from center upwards 3 Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12950 (R0x3296)	**15:0**	**0x0000**	**pdaf_sc_slope_y_4 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_4 Spatial correction slope from center downwards 4 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_4 Spatial correction slope from center upwards 4 Legal values: [0, 255].	N	N
R12952 (R0x3298)	**15:0**	**0x0000**	**pdaf_sc_slope_y_5 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_5 Spatial correction slope from center downwards 5 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_5 Spatial correction slope from center upwards 5 Legal values: [0, 255].	N	N
R12954 (R0x329A)	**15:0**	**0x0000**	**pdaf_sc_slope_y_6 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_6 Spatial correction slope from center downwards 6 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_6 Spatial correction slope from center upwards 6 Legal values: [0, 255].	N	N
R12956 (R0x329C)	**15:0**	**0x0000**	**pdaf_sc_slope_y_7 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_7 Spatial correction slope from center downwards 7 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_7 Spatial correction slope from center upwards 7 Legal values: [0, 255].	N	N
R12958 (R0x329E)	**15:0**	**0x0000**	**pdaf_sc_slope_y_8 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_8 spatial correction slope from center downwards 8 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_8 Spatial correction slope from center upwards 8 Legal values: [0, 255].	N	N
R12960 (R0x32A0)	**15:0**	**0x0000**	**pdaf_sc_slope_y_9 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_9 Spatial correction slope from center downwards 9 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_9 Spatial correction slope from center upwards 9 Legal values: [0, 255].	N	N
R12962 (R0x32A2)	**15:0**	**0x0000**	**pdaf_sc_slope_y_10 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_10 Spatial correction slope from center downwards 10 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_10 Spatial correction slope from center upwards 10 Legal values: [0, 255].	N	N
R12964 (R0x32A4)	**15:0**	**0x0000**	**pdaf_sc_slope_y_11 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_11 Spatial correction slope from center downwards 11 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_11 Spatial correction slope from center upwards 11 Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12966 (R0x32A6)	**15:0**	**0x0000**	**pdaf_sc_slope_y_12 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_12 Spatial correction slope from center downwards 12 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_12 Spatial correction slope from center upwards 12 Legal values: [0, 255].	N	N
R12968 (R0x32A8)	**15:0**	**0x0000**	**pdaf_sc_slope_y_13 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_13 Spatial correction slope from center downwards 13 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_13 Spatial correction slope from center upwards 13 Legal values: [0, 255].	N	N
R12970 (R0x32AA)	**15:0**	**0x0000**	**pdaf_sc_slope_y_14 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_14 Spatial correction slope from center downwards 14 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_14 Spatial correction slope from center upwards 14 Legal values: [0, 255].	N	N
R12972 (R0x32AC)	**15:0**	**0x0000**	**pdaf_sc_slope_y_15 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_15 Spatial correction slope from center downwards 15 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_15 Spatial correction slope from center upwards 15 Legal values: [0, 255].	N	N
R12974 (R0x32AE)	**15:0**	**0x0000**	**pdaf_sc_slope_y_16 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_x_down_16 Spatial correction slope from center downwards 16 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_x_up_16 Spatial correction slope from center upwards 16 Legal values: [0, 255].	N	N
R12976 (R0x32B0)	**15:0**	**0x0000**	**pdaf_sc_slope_y_17 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_y_down_17 Spatial correction slope from center downwards 17 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_y_up_17 Spatial correction slope from center upwards 17 Legal values: [0, 255].	N	N
R12978 (R0x32B2)	**15:0**	**0x0000**	**pdaf_sc_slope_y_18 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_y_down_18 Spatial correction slope from center downwards 18 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_y_up_18 Spatial correction slope from center upwards 18 Legal values: [0, 255].	N	N
R12980 (R0x32B4)	**15:0**	**0x0000**	**pdaf_sc_slope_y_19 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_y_down_19 Spatial correction slope from center downwards 19 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_y_up_19 Spatial correction slope from center upwards 19 Legal values: [0, 255].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12982 (R0x32B6)	**15:0**	**0x0000**	**pdaf_sc_slope_y_20 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_y_down_20 spatial correction slope from center downwards 20 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_y_up_20 Spatial correction slope from center upwards 20 Legal values: [0, 255].	N	N
R12984 (R0x32B8)	**15:0**	**0x0000**	**pdaf_sc_slope_y_21 (R/W)**		
	15:8	0x0000	pdaf_sc_slope_y_down_21 Spatial correction slope from center downwards 21 Legal values: [0, 255].	N	N
	7:0	0x0000	pdaf_sc_slope_y_up_21 Spatial correction slope from center upwards 21 Legal values: [0, 255].	N	N
R12986 (R0x32BA)	**15:0**	**0x0004**	**pdaf_sc_visual_tag (R/W)**		
	15:8	X	Reserved		
	7:6	0x0000	pdaf_sc_visual_tag_3 PDAF pixel tagging option for normal rows. 00: no tag. 01: weak tag. 10: strong tag Legal values: [0, 2].	N	N
	5:4	0x0000	pdaf_sc_visual_tag_2 PDAF pixel tagging option for PDAF bottom rows. 00: No tag. 01: Weak tag. 10: Strong tag Legal values: [0, 2].	N	N
	3:2	0x0001	pdaf_sc_visual_tag_1 pdaf_pixel tagging option for pdaf rows. 00: No tag. 01: Weak tag. 10: Strong tag Legal values: [0, 2].	N	N
	1:0	0x0000	pdaf_sc_visual_tag_0 PDAF pixel tagging option for pdaf top rows. 00: no tag. 01: weak tag. 10: strong tag Legal values: [0, 2].	N	N
R12988 (R0x32BC)	**15:0**	**0x0000**	**pdaf_dc_th_abs (R/W)**		
	15:10	X	Reserved		
	9:0	0x0000	pdaf_sc_th_abs PDAF 1ddc absolute threshold Legal values: [0, 1023].	N	N
R12990 (R0x32BE)	**15:0**	**0x0000**	**pdaf_dc_th_rel (R/W)**		
	15:8	X	Reserved		
	7:0	0x0000	pdaf_sc_th_rel PDAF 1ddc relative threshold Legal values: [0, 255].	N	N
R12992 (R0x32C0)	**15:0**	**0x0000**	**pdaf_dc_diff_factor (R/W)**		
	pdaf 1ddc difference factor Legal values: [0, 31].				
R12994 (R0x32C2)	**15:0**	**0x0000**	**pdaf_dma_start (R/W)**		
	index of pdaf memory start address Legal values: [0, 8191].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12996 (R0x32C4)	**15:0**	**0x0000**	**pdaf_dma_size (R/W)**		
	number of pdaf data being sent out Legal values: [0, 3888].				
R12998 (R0x32C6)	**15:0**	**0x0000**	**pdaf_dma_y (R/W)**		
	15	X	Reserved		
	14:8	0x0000	pdaf_dma_ny number of pdaf rows being sent out Legal values: [0, 127].	N	N
	7	X	Reserved		
	6:0	0x0000	pdaf_dma_y0 index to the first pdaf row being sent out Legal values: [0, 127].	N	N
R13000 (R0x32C8)	**15:0**	**0x085C**	**pdaf_seq_start (R/W)**		
	pdaf odp_seuqencer start Legal values: [0, 65535].				
R13002 (R0x32CA)	**15:0**	**0x0486**	**pdaf_odp_llength (R/W)**		
	pdaf odp_line length Legal values: [0, 65535].				
R13008 (R0x32D0)	**15:0**	**0x0000**	**pe_param_addr (R/W)**		
	pdaf PE parameter address Legal values: [0, 65535].				
R13012 (R0x32D4)	**15:0**	**0x0000**	**pe_param_value (R/W)**		
	pdaf PE parameter value Legal values: [0, 65535].				
R13106 (R0x3332)	**15:0**	**0x0000**	**read_mode2 (R/W)**		
	15:12	0x0000	extent_readout_mode 0000: normal xxx1: unityskip3dig, aka goproskip3 0010: unitybin3dig, aka goprobin3 0100: unitysum3 0110: unitybin3 1000: xbin2dig 1010: invalid 1100: unitysum3skip3 1110: unitybin3skip3 Writes are synchronized to frame boundaries. Legal values: [0, 15].	Y	N
	11:0	X	Reserved		
R13120 (R0x3340)	**15:0**	**0x0000**	**lp_ctx_ctrl (R/W)**		
	15:1	X	Reserved		
	0	0x0000	low_power_ctx Low power control. When set, chip goes to standby mode after sending 1 frame and goes to streaming mode after low_power_cnt * EXTCLK time.	N	N
R13122 (R0x3342)	**15:0**	**0x0000**	**lp_ctx_cnth (R/W)**		
	15:0	0x0000	low_power_cnth High-byte of the count. When low_power_ctx bit is enabled, the chip goes to standby mode after sending 1frame and goes to streaming mode after low_power_cnt * EXTCLK time. Legal values: [0, 65535].	N	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
Lens shading registers (R0x3600– R0x3726) should only be written during standby or vertical blanking time.					
R13124 (R0x3344)	**15:0**	**0x0000**	**lp_ctx_cntl (R/W)**		
	15:0	0x0000	low_power_cntl Low-byte of the count. When low_power_ctx bit is enabled, the chip goes to standby mode after sending 1frame and goes to streaming mode after low_power_cnt * EXTCLK time. Legal values: [0, 65535].	N	N
R13824 (R0x3600)	**15:0**	**0x0000**	**p_gr_p0q0 (R/W)**		
	P0 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13826 (R0x3602)	**15:0**	**0x0000**	**p_gr_p0q1 (R/W)**		
	P0 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13828 (R0x3604)	**15:0**	**0x0000**	**p_gr_p0q2 (R/W)**		
	P0 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13830 (R0x3606)	**15:0**	**0x0000**	**p_gr_p0q3 (R/W)**		
	P0 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13832 (R0x3608)	**15:0**	**0x0000**	**p_gr_p0q4 (R/W)**		
	P0 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13834 (R0x360A)	**15:0**	**0x0000**	**p_rd_p0q0 (R/W)**		
	P0 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13836 (R0x360C)	**15:0**	**0x0000**	**p_rd_p0q1 (R/W)**		
	P0 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13838 (R0x360E)	**15:0**	**0x0000**	**p_rd_p0q2 (R/W)**		
	P0 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13840 (R0x3610)	**15:0**	**0x0000**	**p_rd_p0q3 (R/W)**		
	P0 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13842 (R0x3612)	**15:0**	**0x0000**	**p_rd_p0q4 (R/W)**		
	P0 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13844 (R0x3614)	**15:0**	**0x0000**	**p_bl_p0q0 (R/W)**		
	P0 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13846 (R0x3616)	**15:0**	**0x0000**	**p_bl_p0q1 (R/W)**		
	P0 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13848 (R0x3618)	**15:0**	**0x0000**	**p_bl_p0q2 (R/W)**		
	P0 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13850 (R0x361A)	**15:0**	**0x0000**	**p_bl_p0q3 (R/W)**		
	P0 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13852 (R0x361C)	**15:0**	**0x0000**	**p_bl_p0q4 (R/W)**		
	P0 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13854 (R0x361E)	**15:0**	**0x0000**	**p_gb_p0q0 (R/W)**		
	P0 coefficient for Q0 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13856 (R0x3620)	**15:0**	**0x0000**	**p_gb_p0q1 (R/W)**		
	P0 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13858 (R0x3622)	**15:0**	**0x0000**	**p_gb_p0q2 (R/W)**		
	P0 coefficient for Q2 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13860 (R0x3624)	**15:0**	**0x0000**	**p_gb_p0q3 (R/W)**		
	P0 coefficient for Q3 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13862 (R0x3626)	**15:0**	**0x0000**	**p_gb_p0q4 (R/W)**		
	P0 coefficient for Q4 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13888 (R0x3640)	**15:0**	**0x0000**	**p_gr_p1q0 (R/W)**		
	P1 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13890 (R0x3642)	**15:0**	**0x0000**	**p_gr_p1q1 (R/W)**		
	P1 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13892 (R0x3644)	**15:0**	**0x0000**	**p_gr_p1q2 (R/W)**		
	P1 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13894 (R0x3646)	**15:0**	**0x0000**	**p_gr_p1q3 (R/W)**		
	P1 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13896 (R0x3648)	**15:0**	**0x0000**	**p_gr_p1q4 (R/W)**		
	P1 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13898 (R0x364A)	**15:0**	**0x0000**	**p_rd_p1q0 (R/W)**		
	P1 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13900 (R0x364C)	15:0	0x0000	p_rd_p1q1 (R/W)		
	P1 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13902 (R0x364E)	15:0	0x0000	p_rd_p1q2 (R/W)		
	P1 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13904 (R0x3650)	15:0	0x0000	p_rd_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13906 (R0x3652)	15:0	0x0000	p_rd_p1q4 (R/W)	N	N
	P1 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13908 (R0x3654)	15:0	0x0000	p_bl_p1q0 (R/W)	N	N
	P1 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13910 (R0x3656)	15:0	0x0000	p_bl_p1q1 (R/W)		
	P1 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13912 (R0x3658)	15:0	0x0000	p_bl_p1q2 (R/W)	N	N
	P1 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13914 (R0x365A)	15:0	0x0000	p_bl_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13916 (R0x365C)	15:0	0x0000	p_bl_p1q4 (R/W)	N	N
	P1 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13918 (R0x365E)	15:0	0x0000	p_gb_p1q0 (R/W)	N	N
	P1 coefficient for Q0 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13920 (R0x3660)	15:0	0x0000	p_gb_p1q1 (R/W)		
	P1 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13922 (R0x3662)	15:0	0x0000	p_gb_p1q2 (R/W)		
	P1 coefficient for Q2 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13924 (R0x3664)	15:0	0x0000	p_gb_p1q3 (R/W)		
	P1 coefficient for Q3 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13926 (R0x3666)	15:0	0x0000	p_gb_p1q4 (R/W)		
	P1 coefficient for Q4 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13952 (R0x3680)	15:0	0x0000	p_gr_p2q0 (R/W)		
	P2 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13954 (R0x3682)	15:0	0x0000	p_gr_p2q1 (R/W)		
	P2 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13956 (R0x3684)	15:0	0x0000	p_gr_p2q2 (R/W)		
	P2 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13958 (R0x3686)	15:0	0x0000	p_gr_p2q3 (R/W)		
	P2 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13960 (R0x3688)	15:0	0x0000	p_gr_p2q4 (R/W)		
	P2 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R13962 (R0x368A)	15:0	0x0000	p_rd_p2q0 (R/W)		
	P2 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13964 (R0x368C)	15:0	0x0000	p_rd_p2q1 (R/W)	N	N
	P2 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13966 (R0x368E)	15:0	0x0000	p_rd_p2q2 (R/W)	N	N
	P2 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13968 (R0x3690)	15:0	0x0000	p_rd_p2q3 (R/W)	N	N
	P2 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13970 (R0x3692)	15:0	0x0000	p_rd_p2q4 (R/W)	N	N
	P2 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R13972 (R0x3694)	15:0	0x0000	p_bl_p2q0 (R/W)	N	N
	P2 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13974 (R0x3696)	15:0	0x0000	p_bl_p2q1 (R/W)	N	N
	P2 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13976 (R0x3698)	15:0	0x0000	p_bl_p2q2 (R/W)	N	N
	P2 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13978 (R0x369A)	15:0	0x0000	p_bl_p2q3 (R/W)	N	N
	P2 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13980 (R0x369C)	15:0	0x0000	p_bl_p2q4 (R/W)	N	N
	P2 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R13982 (R0x369E)	15:0	0x0000	p_gb_p2q0 (R/W)	N	N
	P2 coefficient for Q0 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13984 (R0x36A0)	15:0	0x0000	p_gb_p2q1 (R/W)	N	N
	P2 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13986 (R0x36A2)	15:0	0x0000	p_gb_p2q2 (R/W)	N	N
	P2 coefficient for Q2 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13988 (R0x36A4)	15:0	0x0000	p_gb_p2q3 (R/W)	N	N
	P2 coefficient for Q3 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R13990 (R0x36A6)	15:0	0x0000	p_gb_p2q4 (R/W)	N	N
	P2 coefficient for Q4 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14016 (R0x36C0)	15:0	0x0000	p_gr_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14018 (R0x36C2)	15:0	0x0000	p_gr_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14020 (R0x36C4)	15:0	0x0000	p_gr_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14022 (R0x36C6)	15:0	0x0000	p_gr_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14024 (R0x36C8)	15:0	0x0000	p_gr_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14026 (R0x36CA)	15:0	0x0000	p_rd_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14028 (R0x36CC)	15:0	0x0000	p_rd_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14030 (R0x36CE)	15:0	0x0000	p_rd_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14032 (R0x36D0)	15:0	0x0000	p_rd_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14034 (R0x36D2)	15:0	0x0000	p_rd_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14036 (R0x36D4)	15:0	0x0000	p_bl_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14038 (R0x36D6)	15:0	0x0000	p_bl_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14040 (R0x36D8)	15:0	0x0000	p_bl_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14042 (R0x36DA)	15:0	0x0000	p_bl_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14044 (R0x36DC)	15:0	0x0000	p_bl_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14046 (R0x36DE)	15:0	0x0000	p_gb_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14048 (R0x36E0)	15:0	0x0000	p_gb_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14050 (R0x36E2)	15:0	0x0000	p_gb_p3q2 (R/W)	N	N
	P3 coefficient for Q2 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14052 (R0x36E4)	15:0	0x0000	p_gb_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14054 (R0x36E6)	15:0	0x0000	p_gb_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14080 (R0x3700)	15:0	0x0000	p_gr_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14082 (R0x3702)	15:0	0x0000	p_gr_p4q1 (R/W)	N	N
	P4 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14084 (R0x3704)	**15:0**	**0x0000**	**p_gr_p4q2 (R/W)**	**N**	**N**
	P4 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14086 (R0x3706)	**15:0**	**0x0000**	**p_gr_p4q3 (R/W)**	**N**	**N**
	P4 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14088 (R0x3708)	**15:0**	**0x0000**	**p_gr_p4q4 (R/W)**	**N**	**N**
	P4 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels. Legal values: [0, 65535].				
R14090 (R0x370A)	**15:0**	**0x0000**	**p_rd_p4q0 (R/W)**	**N**	**N**
	P4 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14092 (R0x370C)	**15:0**	**0x0000**	**p_rd_p4q1 (R/W)**	**N**	**N**
	P4 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14094 (R0x370E)	**15:0**	**0x0000**	**p_rd_p4q2 (R/W)**	**N**	**N**
	P4 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14096 (R0x3710)	**15:0**	**0x0000**	**p_rd_p4q3 (R/W)**	**N**	**N**
	P4 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14098 (R0x3712)	**15:0**	**0x0000**	**p_rd_p4q4 (R/W)**	**N**	**N**
	P4 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels. Legal values: [0, 65535].				
R14100 (R0x3714)	**15:0**	**0x0000**	**p_bl_p4q0 (R/W)**	**N**	**N**
	P4 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14102 (R0x3716)	**15:0**	**0x0000**	**p_bl_p4q1 (R/W)**	**N**	**N**
	P4 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14104 (R0x3718)	**15:0**	**0x0000**	**p_bl_p4q2 (R/W)**	**N**	**N**
	P4 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14106 (R0x371A)	**15:0**	**0x0000**	**p_bl_p4q3 (R/W)**	**N**	**N**
	P4 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14108 (R0x371C)	**15:0**	**0x0000**	**p_bl_p4q4 (R/W)**	**N**	**N**
	P4 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels. Legal values: [0, 65535].				
R14110 (R0x371E)	**15:0**	**0x0000**	**p_gb_p4q0 (R/W)**	**N**	**N**
	P4 coefficient for Q0 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14112 (R0x3720)	**15:0**	**0x0000**	**p_gb_p4q1 (R/W)**	**N**	**N**
	P4 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14114 (R0x3722)	**15:0**	**0x0000**	**p_gb_p4q2 (R/W)**	**N**	**N**
	P4 coefficient for Q2 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14116 (R0x3724)	**15:0**	**0x0000**	**p_gb_p4q3 (R/W)**	**N**	**N**
	P4 coefficient for Q3 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14118 (R0x3726)	**15:0**	**0x0000**	**p_gb_p4q4 (R/W)**	**N**	**N**
	P4 coefficient for Q4 for Gb. P_Gb_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels. Legal values: [0, 65535].				
R14208 (R0x3780)	**15:0**	**0x0000**	**poly_sc_enable (R/W)**	**N**	**N**
	When set, len shading correction will generate polynomial function and correct stream of pixels. When not set, the function will bypass data.				
R14210 (R0x3782)	**15:0**	**0x0B4F**	**poly_origin_c (R/W)**	**N**	**N**
	15:13	X	Reserved		
	12:0	0x0B4F	origin_c Center column of the image for polynomial function Legal values: [0, 5791].	N	N
R14212 (R0x3784)	**15:0**	**0x0877**	**poly_origin_r (R/W)**	**N**	**N**
	15:13	X	Reserved		
	12:0	0x0877	origin_r Center row of the image for polynomial function Legal values: [0, 5791].	N	N
R14272 (R0x37C0)	**15:0**	**0x0000**	**p_gr_q5 (R/W)**	**Y**	**N**
	Parameter for parabolic roll-off algorithm for greenR pixels. Writes are synchronized to frame boundaries. Legal values: [0, 65535].				
R14274 (R0x37C2)	**15:0**	**0x0000**	**p_rd_q5 (R/W)**	**Y**	**N**
	Parameter for parabolic roll-off algorithm for red pixels. Writes are synchronized to frame boundaries. Legal values: [0, 65535].				
R14276 (R0x37C4)	**15:0**	**0x0000**	**p_bl_q5 (R/W)**	**Y**	**N**
	Parameter for parabolic roll-off algorithm for blue pixels. Writes are synchronized to frame boundaries. Legal values: [0, 65535].				
R14278 (R0x37C6)	**15:0**	**0x0000**	**p_gb_q5 (R/W)**	**Y**	**N**
	Parameter for parabolic roll-off algorithm for greenB pixels. Writes are synchronized to frame boundaries. Legal values: [0, 65535].				
R14336 (R0x3800)	**15:0**	**0x0000**	**otpm_data_000 (R/W)**	**N**	**N**
	OTPM_DATA_000 Data for OTPM automatic read and write sequences. After an OTPM automatic read sequence, read data is presented in the OTPM_DATA_* registers. Before performing an OTPM automatic write (programming) sequence, the data to be written is presented in the OTPM_DATA_* registers. These registers cannot be accessed when the system is in soft standby (writes will be ignored and reads will return 0). Legal values: [0, 65535].				
R14338 (R0x3802)	**15:0**	**0x0000**	**otpm_data_001 (R/W)**	**N**	**N**
	OTPM_DATA_001 Legal values: [0, 65535].				
R14340 (R0x3804)	**15:0**	**0x0000**	**otpm_data_002 (R/W)**	**N**	**N**
	OTPM_DATA_002 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14342 (R0x3806)	**15:0**	**0x0000**	**otpm_data_003 (R/W)**	**N**	**N**
	OTPM_DATA_003 Legal values: [0, 65535].				
R14344 (R0x3808)	**15:0**	**0x0000**	**otpm_data_004 (R/W)**	**N**	**N**
	OTPM_DATA_004 Legal values: [0, 65535].				
R14346 (R0x380A)	**15:0**	**0x0000**	**otpm_data_005 (R/W)**	**N**	**N**
	OTPM_DATA_005 Legal values: [0, 65535].				
R14348 (R0x380C)	**15:0**	**0x0000**	**otpm_data_006 (R/W)**	**N**	**N**
	OTPM_DATA_006 Legal values: [0, 65535].				
R14350 (R0x380E)	**15:0**	**0x0000**	**otpm_data_007 (R/W)**	**N**	**N**
	OTPM_DATA_007 Legal values: [0, 65535].				
R14352 (R0x3810)	**15:0**	**0x0000**	**otpm_data_008 (R/W)**	**N**	**N**
	OTPM_DATA_008 Legal values: [0, 65535].				
R14354 (R0x3812)	**15:0**	**0x0000**	**otpm_data_009 (R/W)**	**N**	**N**
	OTPM_DATA_009 Legal values: [0, 65535].				
R14356 (R0x3814)	**15:0**	**0x0000**	**otpm_data_010 (R/W)**	**N**	**N**
	OTPM_DATA_010 Legal values: [0, 65535].				
R14358 (R0x3816)	**15:0**	**0x0000**	**otpm_data_011 (R/W)**	**N**	**N**
	OTPM_DATA_011 Legal values: [0, 65535].				
R14360 (R0x3818)	**15:0**	**0x0000**	**otpm_data_012 (R/W)**	**N**	**N**
	OTPM_DATA_012 Legal values: [0, 65535].				
R14362 (R0x381A)	**15:0**	**0x0000**	**otpm_data_013 (R/W)**	**N**	**N**
	OTPM_DATA_013 Legal values: [0, 65535].				
R14364 (R0x381C)	**15:0**	**0x0000**	**otpm_data_014 (R/W)**	**N**	**N**
	OTPM_DATA_014 Legal values: [0, 65535].				
R14366 (R0x381E)	**15:0**	**0x0000**	**otpm_data_015 (R/W)**	**N**	**N**
	OTPM_DATA_015 Legal values: [0, 65535].				
R14368 (R0x3820)	**15:0**	**0x0000**	**otpm_data_016 (R/W)**	**N**	**N**
	OTPM_DATA_016 Legal values: [0, 65535].				
R14370 (R0x3822)	**15:0**	**0x0000**	**otpm_data_017 (R/W)**	**N**	**N**
	OTPM_DATA_017 Legal values: [0, 65535].				
R14372 (R0x3824)	**15:0**	**0x0000**	**otpm_data_018 (R/W)**	**N**	**N**
	OTPM_DATA_018 Legal values: [0, 65535].				
R14374 (R0x3826)	**15:0**	**0x0000**	**otpm_data_019 (R/W)**	**N**	**N**
	OTPM_DATA_019 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14376 (R0x3828)	**15:0**	**0x0000**	**otpm_data_020 (R/W)**	**N**	**N**
	OTPM_DATA_020 Legal values: [0, 65535].				
R14378 (R0x382A)	**15:0**	**0x0000**	**otpm_data_021 (R/W)**	**N**	**N**
	OTPM_DATA_021 Legal values: [0, 65535].				
R14380 (R0x382C)	**15:0**	**0x0000**	**otpm_data_022 (R/W)**	**N**	**N**
	OTPM_DATA_022 Legal values: [0, 65535].				
R14382 (R0x382E)	**15:0**	**0x0000**	**otpm_data_023 (R/W)**	**N**	**N**
	OTPM_DATA_023 Legal values: [0, 65535].				
R14384 (R0x3830)	**15:0**	**0x0000**	**otpm_data_024 (R/W)**	**N**	**N**
	OTPM_DATA_024 Legal values: [0, 65535].				
R14386 (R0x3832)	**15:0**	**0x0000**	**otpm_data_025 (R/W)**	**N**	**N**
	OTPM_DATA_025 Legal values: [0, 65535].				
R14388 (R0x3834)	**15:0**	**0x0000**	**otpm_data_026 (R/W)**	**N**	**N**
	OTPM_DATA_026 Legal values: [0, 65535].				
R14390 (R0x3836)	**15:0**	**0x0000**	**otpm_data_027 (R/W)**	**N**	**N**
	OTPM_DATA_027 Legal values: [0, 65535].				
R14392 (R0x3838)	**15:0**	**0x0000**	**otpm_data_028 (R/W)**	**N**	**N**
	OTPM_DATA_028 Legal values: [0, 65535].				
R14394 (R0x383A)	**15:0**	**0x0000**	**otpm_data_029 (R/W)**	**N**	**N**
	OTPM_DATA_029 Legal values: [0, 65535].				
R14396 (R0x383C)	**15:0**	**0x0000**	**otpm_data_030 (R/W)**	**N**	**N**
	OTPM_DATA_030 Legal values: [0, 65535].				
R14398 (R0x383E)	**15:0**	**0x0000**	**otpm_data_031 (R/W)**	**N**	**N**
	OTPM_DATA_031 Legal values: [0, 65535].				
R14400 (R0x3840)	**15:0**	**0x0000**	**otpm_data_032 (R/W)**	**N**	**N**
	OTPM_DATA_032 Legal values: [0, 65535].				
R14402 (R0x3842)	**15:0**	**0x0000**	**otpm_data_033 (R/W)**	**N**	**N**
	OTPM_DATA_033 Legal values: [0, 65535].				
R14404 (R0x3844)	**15:0**	**0x0000**	**otpm_data_034 (R/W)**	**N**	**N**
	OTPM_DATA_034 Legal values: [0, 65535].				
R14406 (R0x3846)	**15:0**	**0x0000**	**otpm_data_035 (R/W)**	**N**	**N**
	OTPM_DATA_035 Legal values: [0, 65535].				
R14408 (R0x3848)	**15:0**	**0x0000**	**otpm_data_036 (R/W)**	**N**	**N**
	OTPM_DATA_036 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14410 (R0x384A)	**15:0**	**0x0000**	**otpm_data_037 (R/W)**	**N**	**N**
	OTPM_DATA_037 Legal values: [0, 65535].				
R14412 (R0x384C)	**15:0**	**0x0000**	**otpm_data_038 (R/W)**	**N**	**N**
	OTPM_DATA_038 Legal values: [0, 65535].				
R14414 (R0x384E)	**15:0**	**0x0000**	**otpm_data_039 (R/W)**	**N**	**N**
	OTPM_DATA_039 Legal values: [0, 65535].				
R14416 (R0x3850)	**15:0**	**0x0000**	**otpm_data_040 (R/W)**		
	OTPM_DATA_040 Legal values: [0, 65535].				
R14418 (R0x3852)	**15:0**	**0x0000**	**otpm_data_041 (R/W)**		
	OTPM_DATA_041 Legal values: [0, 65535].				
R14420 (R0x3854)	**15:0**	**0x0000**	**otpm_data_042 (R/W)**	**N**	**N**
	OTPM_DATA_042 Legal values: [0, 65535].				
R14422 (R0x3856)	**15:0**	**0x0000**	**otpm_data_043 (R/W)**	**N**	**N**
	OTPM_DATA_043 Legal values: [0, 65535].				
R14424 (R0x3858)	**15:0**	**0x0000**	**otpm_data_044 (R/W)**	**N**	**N**
	OTPM_DATA_044 Legal values: [0, 65535].				
R14426 (R0x385A)	**15:0**	**0x0000**	**otpm_data_045 (R/W)**	**N**	**N**
	OTPM_DATA_045 Legal values: [0, 65535].				
R14428 (R0x385C)	**15:0**	**0x0000**	**otpm_data_046 (R/W)**	**N**	**N**
	OTPM_DATA_046 Legal values: [0, 65535].				
R14430 (R0x385E)	**15:0**	**0x0000**	**otpm_data_047 (R/W)**	**N**	**N**
	OTPM_DATA_047 Legal values: [0, 65535].				
R14432 (R0x3860)	**15:0**	**0x0000**	**otpm_data_048 (R/W)**	**N**	**N**
	OTPM_DATA_048 Legal values: [0, 65535].				
R14434 (R0x3862)	**15:0**	**0x0000**	**otpm_data_049 (R/W)**	**N**	**N**
	OTPM_DATA_049 Legal values: [0, 65535].				
R14436 (R0x3864)	**15:0**	**0x0000**	**otpm_data_050 (R/W)**	**N**	**N**
	OTPM_DATA_050 Legal values: [0, 65535].				
R14438 (R0x3866)	**15:0**	**0x0000**	**otpm_data_051 (R/W)**	**N**	**N**
	OTPM_DATA_051 Legal values: [0, 65535].				
R14440 (R0x3868)	**15:0**	**0x0000**	**otpm_data_052 (R/W)**	**N**	**N**
	OTPM_DATA_052 Legal values: [0, 65535].				
R14442 (R0x386A)	**15:0**	**0x0000**	**otpm_data_053 (R/W)**	**N**	**N**
	OTPM_DATA_053 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14444 (R0x386C)	**15:0**	**0x0000**	**otpm_data_054 (R/W)**	**N**	**N**
	OTPM_DATA_054 Legal values: [0, 65535].				
R14446 (R0x386E)	**15:0**	**0x0000**	**otpm_data_055 (R/W)**	**N**	**N**
	OTPM_DATA_055 Legal values: [0, 65535].				
R14448 (R0x3870)	**15:0**	**0x0000**	**otpm_data_056 (R/W)**	**N**	**N**
	OTPM_DATA_056 Legal values: [0, 65535].				
R14450 (R0x3872)	**15:0**	**0x0000**	**otpm_data_057 (R/W)**	**N**	**N**
	OTPM_DATA_057 Legal values: [0, 65535].				
R14452 (R0x3874)	**15:0**	**0x0000**	**otpm_data_058 (R/W)**	**N**	**N**
	OTPM_DATA_058 Legal values: [0, 65535].				
R14454 (R0x3876)	**15:0**	**0x0000**	**otpm_data_059 (R/W)**	**N**	**N**
	OTPM_DATA_059 Legal values: [0, 65535].				
R14456 (R0x3878)	**15:0**	**0x0000**	**otpm_data_060 (R/W)**	**N**	**N**
	OTPM_DATA_060 Legal values: [0, 65535].				
R14458 (R0x387A)	**15:0**	**0x0000**	**otpm_data_061 (R/W)**	**N**	**N**
	OTPM_DATA_061 Legal values: [0, 65535].				
R14460 (R0x387C)	**15:0**	**0x0000**	**otpm_data_062 (R/W)**	**N**	**N**
	OTPM_DATA_062 Legal values: [0, 65535].				
R14462 (R0x387E)	**15:0**	**0x0000**	**otpm_data_063 (R/W)**	**N**	**N**
	OTPM_DATA_063 Legal values: [0, 65535].				
R14464 (R0x3880)	**15:0**	**0x0000**	**otpm_data_064 (R/W)**	**N**	**N**
	OTPM_DATA_064 Legal values: [0, 65535].				
R14466 (R0x3882)	**15:0**	**0x0000**	**otpm_data_065 (R/W)**	**N**	**N**
	OTPM_DATA_065 Legal values: [0, 65535].				
R14468 (R0x3884)	**15:0**	**0x0000**	**otpm_data_066 (R/W)**	**N**	**N**
	OTPM_DATA_066 Legal values: [0, 65535].				
R14470 (R0x3886)	**15:0**	**0x0000**	**otpm_data_067 (R/W)**	**N**	**N**
	OTPM_DATA_067 Legal values: [0, 65535].				
R14472 (R0x3888)	**15:0**	**0x0000**	**otpm_data_068 (R/W)**	**N**	**N**
	OTPM_DATA_068 Legal values: [0, 65535].				
R14474 (R0x388A)	**15:0**	**0x0000**	**otpm_data_069 (R/W)**	**N**	**N**
	OTPM_DATA_069 Legal values: [0, 65535].				
R14476 (R0x388C)	**15:0**	**0x0000**	**otpm_data_070 (R/W)**	**N**	**N**
	OTPM_DATA_070 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14478 (R0x388E)	**15:0**	**0x0000**	**otpm_data_071 (R/W)**	**N**	**N**
	OTPM_DATA_071 Legal values: [0, 65535].				
R14480 (R0x3890	**15:0**	**0x0000**	**otpm_data_072 (R/W)**	**N**	**N**
	OTPM_DATA_072 Legal values: [0, 65535].				
R14482 (R0x3892)	**15:0**	**0x0000**	**otpm_data_073 (R/W)**	**N**	**N**
	OTPM_DATA_073 Legal values: [0, 65535].				
R14484 (R0x3894)	**15:0**	**0x0000**	**otpm_data_074 (R/W)**	**N**	**N**
	OTPM_DATA_074 Legal values: [0, 65535].				
R14486 (R0x3896)	**15:0**	**0x0000**	**otpm_data_075 (R/W)**	**N**	**N**
	OTPM_DATA_075 Legal values: [0, 65535].				
R14488 (R0x3898)	**15:0**	**0x0000**	**otpm_data_076 (R/W)**	**N**	**N**
	OTPM_DATA_076 Legal values: [0, 65535].				
R14490 (R0x389A)	**15:0**	**0x0000**	**otpm_data_077 (R/W)**	**N**	**N**
	OTPM_DATA_077 Legal values: [0, 65535].				
R14492 (R0x389C)	**15:0**	**0x0000**	**otpm_data_078 (R/W)**	**N**	**N**
	OTPM_DATA_078 Legal values: [0, 65535].				
R14494 (R0x389E)	**15:0**	**0x0000**	**otpm_data_079 (R/W)**	**N**	**N**
	OTPM_DATA_079 Legal values: [0, 65535].				
R14496 (R0x38A0)	**15:0**	**0x0000**	**otpm_data_080 (R/W)**	**N**	**N**
	OTPM_DATA_080 Legal values: [0, 65535].				
R14498 (R0x38A2)	**15:0**	**0x0000**	**otpm_data_081 (R/W)**	**N**	**N**
	OTPM_DATA_081 Legal values: [0, 65535].				
R14500 (R0x38A4)	**15:0**	**0x0000**	**otpm_data_082 (R/W)**	**N**	**N**
	OTPM_DATA_082 Legal values: [0, 65535].				
R14502 (R0x38A6)	**15:0**	**0x0000**	**otpm_data_083 (R/W)**	**N**	**N**
	OTPM_DATA_083 Legal values: [0, 65535].				
R14504 (R0x38A8)	**15:0**	**0x0000**	**otpm_data_084 (R/W)**	**N**	**N**
	OTPM_DATA_084 Legal values: [0, 65535].				
R14506 (R0x38AA)	**15:0**	**0x0000**	**otpm_data_085 (R/W)**	**N**	**N**
	OTPM_DATA_085 Legal values: [0, 65535].				
R14508 (R0x38AC)	**15:0**	**0x0000**	**otpm_data_086 (R/W)**	**N**	**N**
	OTPM_DATA_086 Legal values: [0, 65535].				
R14510 (R0x38AE)	**15:0**	**0x0000**	**otpm_data_087 (R/W)**	**N**	**N**
	OTPM_DATA_087 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14512 (R0x38B0)	**15:0**	**0x0000**	**otpm_data_088 (R/W)**	**N**	**N**
	OTPM_DATA_088 Legal values: [0, 65535].				
R14514 (R0x38B2)	**15:0**	**0x0000**	**otpm_data_089 (R/W)**	**N**	**N**
	OTPM_DATA_089 Legal values: [0, 65535].				
R14516 (R0x38B4)	**15:0**	**0x0000**	**otpm_data_090 (R/W)**	**N**	**N**
	OTPM_DATA_090 Legal values: [0, 65535].				
R14518 (R0x38B6)	**15:0**	**0x0000**	**otpm_data_091 (R/W)**	**N**	**N**
	OTPM_DATA_091 Legal values: [0, 65535].				
R14520 (R0x38B8)	**15:0**	**0x0000**	**otpm_data_092 (R/W)**	**N**	**N**
	OTPM_DATA_092 Legal values: [0, 65535].				
R14522 (R0x38BA)	**15:0**	**0x0000**	**otpm_data_093 (R/W)**	**N**	**N**
	OTPM_DATA_093 Legal values: [0, 65535].				
R14524 (R0x38BC)	**15:0**	**0x0000**	**otpm_data_094 (R/W)**	**N**	**N**
	OTPM_DATA_094 Legal values: [0, 65535].				
R14526 (R0x38BE)	**15:0**	**0x0000**	**otpm_data_095 (R/W)**	**N**	**N**
	OTPM_DATA_095 Legal values: [0, 65535].				
R14528 (R0x38C0)	**15:0**	**0x0000**	**otpm_data_096 (R/W)**	**N**	**N**
	OTPM_DATA_096 Legal values: [0, 65535].				
R14530 (R0x38C2)	**15:0**	**0x0000**	**otpm_data_097 (R/W)**	**N**	**N**
	OTPM_DATA_097 Legal values: [0, 65535].				
R14532 (R0x38C4)	**15:0**	**0x0000**	**otpm_data_098 (R/W)**	**N**	**N**
	OTPM_DATA_098 Legal values: [0, 65535].				
R14534 (R0x38C6)	**15:0**	**0x0000**	**otpm_data_099 (R/W)**	**N**	**N**
	OTPM_DATA_099 Legal values: [0, 65535].				
R14536 (R0x38C8)	**15:0**	**0x0000**	**otpm_data_100 (R/W)**	**N**	**N**
	OTPM_DATA_100 Legal values: [0, 65535].				
R14538 (R0x38CA)	**15:0**	**0x0000**	**otpm_data_101 (R/W)**	**N**	**N**
	OTPM_DATA_101 Legal values: [0, 65535].				
R14540 (R0x38CC)	**15:0**	**0x0000**	**otpm_data_102 (R/W)**	**N**	**N**
	OTPM_DATA_102 Legal values: [0, 65535].				
R14542 (R0x38CE)	**15:0**	**0x0000**	**otpm_data_103 (R/W)**	**N**	**N**
	OTPM_DATA_103 Legal values: [0, 65535].				
R14544 (R0x38D0)	**15:0**	**0x0000**	**otpm_data_104 (R/W)**	**N**	**N**
	OTPM_DATA_104 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14546 (R0x38D2)	**15:0**	**0x0000**	**otpm_data_105 (R/W)**	**N**	**N**
	OTPM_DATA_105 Legal values: [0, 65535].				
R14548 (R0x38D4)	**15:0**	**0x0000**	**otpm_data_106 (R/W)**	**N**	**N**
	OTPM_DATA_106 Legal values: [0, 65535].				
R14550 (R0x38D6)	**15:0**	**0x0000**	**otpm_data_107 (R/W)**	**N**	**N**
	OTPM_DATA_107 Legal values: [0, 65535].				
R14552 (R0x38D8)	**15:0**	**0x0000**	**otpm_data_108 (R/W)**	**N**	**N**
	OTPM_DATA_108 Legal values: [0, 65535].				
R14554 (R0x38DA)	**15:0**	**0x0000**	**otpm_data_109 (R/W)**	**N**	**N**
	OTPM_DATA_109 Legal values: [0, 65535].				
R14556 (R0x38DC)	**15:0**	**0x0000**	**otpm_data_110 (R/W)**	**N**	**N**
	OTPM_DATA_110 Legal values: [0, 65535].				
R14558 (R0x38DE)	**15:0**	**0x0000**	**otpm_data_111 (R/W)**	**N**	**N**
	OTPM_DATA_111 Legal values: [0, 65535].				
R14560 (R0x38E0)	**15:0**	**0x0000**	**otpm_data_112 (R/W)**	**N**	**N**
	OTPM_DATA_112 Legal values: [0, 65535].				
R14562 (R0x38E2)	**15:0**	**0x0000**	**otpm_data_113 (R/W)**	**N**	**N**
	OTPM_DATA_113 Legal values: [0, 65535].				
R14564 (R0x38E4)	**15:0**	**0x0000**	**otpm_data_114 (R/W)**	**N**	**N**
	OTPM_DATA_114 Legal values: [0, 65535].				
R14566 (R0x38E6)	**15:0**	**0x0000**	**otpm_data_115 (R/W)**	**N**	**N**
	OTPM_DATA_115 Legal values: [0, 65535].				
R14568 (R0x38E8)	**15:0**	**0x0000**	**otpm_data_116 (R/W)**	**N**	**N**
	OTPM_DATA_116 Legal values: [0, 65535].				
R14570 (R0x38EA)	**15:0**	**0x0000**	**otpm_data_117 (R/W)**	**N**	**N**
	OTPM_DATA_117 Legal values: [0, 65535].				
R14572 (R0x38EC)	**15:0**	**0x0000**	**otpm_data_118 (R/W)**	**N**	**N**
	OTPM_DATA_118 Legal values: [0, 65535].				
R14574 (R0x38EE)	**15:0**	**0x0000**	**otpm_data_119 (R/W)**	**N**	**N**
	OTPM_DATA_119 Legal values: [0, 65535].				
R14576 (R0x38F0)	**15:0**	**0x0000**	**otpm_data_120 (R/W)**	**N**	**N**
	OTPM_DATA_120 Legal values: [0, 65535].				
R14578 (R0x38F2)	**15:0**	**0x0000**	**otpm_data_121 (R/W)**	**N**	**N**
	OTPM_DATA_121 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14580 (R0x38F4)	**15:0**	**0x0000**	**otpm_data_122 (R/W)**	**N**	**N**
	OTPM_DATA_122 Legal values: [0, 65535].				
R14582 (R0x38F6)	**15:0**	**0x0000**	**otpm_data_123 (R/W)**	**N**	**N**
	OTPM_DATA_123 Legal values: [0, 65535].				
R14584 (R0x38F8)	**15:0**	**0x0000**	**otpm_data_124 (R/W)**	**N**	**N**
	OTPM_DATA_124 Legal values: [0, 65535].				
R14586 (R0x38FA)	**15:0**	**0x0000**	**otpm_data_125 (R/W)**	**N**	**N**
	OTPM_DATA_125 Legal values: [0, 65535].				
R14588 (R0x38FC)	**15:0**	**0x0000**	**otpm_data_126 (R/W)**	**N**	**N**
	OTPM_DATA_126 Legal values: [0, 65535].				
R14590 (R0x38FE)	**15:0**	**0x0000**	**otpm_data_127 (R/W)**	**N**	**N**
	OTPM_DATA_127 Legal values: [0, 65535].				
R14592 (R0x3900)	**15:0**	**0x0000**	**otpm_data_128 (R/W)**	**N**	**N**
	OTPM_DATA_128 Legal values: [0, 65535].				
R14594 (R0x3902)	**15:0**	**0x0000**	**otpm_data_129 (R/W)**	**N**	**N**
	OTPM_DATA_129 Legal values: [0, 65535].				
R14596 (R0x3904)	**15:0**	**0x0000**	**otpm_data_130 (R/W)**	**N**	**N**
	OTPM_DATA_130 Legal values: [0, 65535].				
R14598 (R0x3906)	**15:0**	**0x0000**	**otpm_data_131 (R/W)**	**N**	**N**
	OTPM_DATA_131 Legal values: [0, 65535].				
R14600 (R0x3908)	**15:0**	**0x0000**	**otpm_data_132 (R/W)**	**N**	**N**
	OTPM_DATA_132 Legal values: [0, 65535].				
R14602 (R0x390A)	**15:0**	**0x0000**	**otpm_data_133 (R/W)**	**N**	**N**
	OTPM_DATA_133 Legal values: [0, 65535].				
R14604 (R0x390C)	**15:0**	**0x0000**	**otpm_data_134 (R/W)**	**N**	**N**
	OTPM_DATA_134 Legal values: [0, 65535].				
R14606 (R0x390E)	**15:0**	**0x0000**	**otpm_data_135 (R/W)**	**N**	**N**
	OTPM_DATA_135 Legal values: [0, 65535].				
R14608 (R0x3910)	**15:0**	**0x0000**	**otpm_data_136 (R/W)**	**N**	**N**
	OTPM_DATA_136 Legal values: [0, 65535].				
R14610 (R0x3912)	**15:0**	**0x0000**	**otpm_data_137 (R/W)**	**N**	**N**
	OTPM_DATA_137 Legal values: [0, 65535].				
R14612 (R0x3914)	**15:0**	**0x0000**	**otpm_data_138 (R/W)**	**N**	**N**
	OTPM_DATA_138 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14614 (R0x3916)	**15:0**	**0x0000**	**otpm_data_139 (R/W)**	**N**	**N**
	OTPM_DATA_139 Legal values: [0, 65535].				
R14616 (R0x3918)	**15:0**	**0x0000**	**otpm_data_140 (R/W)**	**N**	**N**
	OTPM_DATA_140 Legal values: [0, 65535].				
R14618 (R0x391A)	**15:0**	**0x0000**	**otpm_data_141 (R/W)**	**N**	**N**
	OTPM_DATA_141 Legal values: [0, 65535].				
R14620 (R0x391C)	**15:0**	**0x0000**	**otpm_data_142 (R/W)**	**N**	**N**
	OTPM_DATA_142 Legal values: [0, 65535].				
R14622 (R0x391E)	**15:0**	**0x0000**	**otpm_data_143 (R/W)**	**N**	**N**
	OTPM_DATA_143 Legal values: [0, 65535].				
R14624 (R0x3920)	**15:0**	**0x0000**	**otpm_data_144 (R/W)**	**N**	**N**
	OTPM_DATA_144 Legal values: [0, 65535].				
R14626 (R0x3922)	**15:0**	**0x0000**	**otpm_data_145 (R/W)**	**N**	**N**
	OTPM_DATA_145 Legal values: [0, 65535].				
R14628 (R0x3924)	**15:0**	**0x0000**	**otpm_data_146 (R/W)**	**N**	**N**
	OTPM_DATA_146 Legal values: [0, 65535].				
R14630 (R0x3926)	**15:0**	**0x0000**	**otpm_data_147 (R/W)**	**N**	**N**
	OTPM_DATA_147 Legal values: [0, 65535].				
R14632 (R0x3928)	**15:0**	**0x0000**	**otpm_data_148 (R/W)**	**N**	**N**
	OTPM_DATA_148 Legal values: [0, 65535].				
R14634 (R0x392A)	**15:0**	**0x0000**	**otpm_data_149 (R/W)**	**N**	**N**
	OTPM_DATA_149 Legal values: [0, 65535].				
R14636 (R0x392C)	**15:0**	**0x0000**	**otpm_data_150 (R/W)**	**N**	**N**
	OTPM_DATA_150 Legal values: [0, 65535].				
R14638 (R0x392E)	**15:0**	**0x0000**	**otpm_data_151 (R/W)**	**N**	**N**
	OTPM_DATA_151 Legal values: [0, 65535].				
R14640 (R0x3930)	**15:0**	**0x0000**	**otpm_data_152 (R/W)**	**N**	**N**
	OTPM_DATA_152 Legal values: [0, 65535].				
R14642 (R0x3932)	**15:0**	**0x0000**	**otpm_data_153 (R/W)**	**N**	**N**
	OTPM_DATA_153 Legal values: [0, 65535].				
R14644 (R0x3934)	**15:0**	**0x0000**	**otpm_data_154 (R/W)**	**N**	**N**
	OTPM_DATA_154 Legal values: [0, 65535].				
R14646 (R0x3936)	**15:0**	**0x0000**	**otpm_data_155 (R/W)**	**N**	**N**
	OTPM_DATA_155 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14648 (R0x3938)	**15:0**	**0x0000**	**otpm_data_156 (R/W)**	**N**	**N**
	OTPM_DATA_156 Legal values: [0, 65535].				
R14650 (R0x393A)	**15:0**	**0x0000**	**otpm_data_157 (R/W)**	**N**	**N**
	OTPM_DATA_157 Legal values: [0, 65535].				
R14652 (R0x393C)	**15:0**	**0x0000**	**otpm_data_158 (R/W)**	**N**	**N**
	OTPM_DATA_158 Legal values: [0, 65535].				
R14654 (R0x393E)	**15:0**	**0x0000**	**otpm_data_159 (R/W)**	**N**	**N**
	OTPM_DATA_159 Legal values: [0, 65535].				
R14656 (R0x3940)	**15:0**	**0x0000**	**otpm_data_160 (R/W)**	**N**	**N**
	OTPM_DATA_160 Legal values: [0, 65535].				
R14658 (R0x3942)	**15:0**	**0x0000**	**otpm_data_161 (R/W)**	**N**	**N**
	OTPM_DATA_161 Legal values: [0, 65535].				
R14660 (R0x3944)	**15:0**	**0x0000**	**otpm_data_162 (R/W)**	**N**	**N**
	OTPM_DATA_162 Legal values: [0, 65535].				
R14662 (R0x3946)	**15:0**	**0x0000**	**otpm_data_163 (R/W)**	**N**	**N**
	OTPM_DATA_163 Legal values: [0, 65535].				
R14664 (R0x3948)	**15:0**	**0x0000**	**otpm_data_164 (R/W)**	**N**	**N**
	OTPM_DATA_164 Legal values: [0, 65535].				
R14666 (R0x394A)	**15:0**	**0x0000**	**otpm_data_165 (R/W)**	**N**	**N**
	OTPM_DATA_165 Legal values: [0, 65535].				
R14668 (R0x394C)	**15:0**	**0x0000**	**otpm_data_166 (R/W)**	**N**	**N**
	OTPM_DATA_166 Legal values: [0, 65535].				
R14670 (R0x394E)	**15:0**	**0x0000**	**otpm_data_167 (R/W)**	**N**	**N**
	OTPM_DATA_167 Legal values: [0, 65535].				
R14672 (R0x3950)	**15:0**	**0x0000**	**otpm_data_168 (R/W)**	**N**	**N**
	OTPM_DATA_168 Legal values: [0, 65535].				
R14674 (R0x3952)	**15:0**	**0x0000**	**otpm_data_169 (R/W)**	**N**	**N**
	OTPM_DATA_169 Legal values: [0, 65535].				
R14676 (R0x3954)	**15:0**	**0x0000**	**otpm_data_170 (R/W)**	**N**	**N**
	OTPM_DATA_170 Legal values: [0, 65535].				
R14678 (R0x3956)	**15:0**	**0x0000**	**otpm_data_171 (R/W)**	**N**	**N**
	OTPM_DATA_171 Legal values: [0, 65535].				
R14680 (R0x3958)	**15:0**	**0x0000**	**otpm_data_172 (R/W)**	**N**	**N**
	OTPM_DATA_172 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14682 (R0x395A)	**15:0**	**0x0000**	**otpm_data_173 (R/W)**	**N**	**N**
	OTPM_DATA_173 Legal values: [0, 65535].				
R14684 (R0x395C)	**15:0**	**0x0000**	**otpm_data_174 (R/W)**	**N**	**N**
	OTPM_DATA_174 Legal values: [0, 65535].				
R14686 (R0x395E)	**15:0**	**0x0000**	**otpm_data_175 (R/W)**	**N**	**N**
	OTPM_DATA_175 Legal values: [0, 65535].				
R14688 (R0x3960)	**15:0**	**0x0000**	**otpm_data_176 (R/W)**	**N**	**N**
	OTPM_DATA_176 Legal values: [0, 65535].				
R14690 (R0x3962)	**15:0**	**0x0000**	**otpm_data_177 (R/W)**	**N**	**N**
	OTPM_DATA_177 Legal values: [0, 65535].				
R14692 (R0x3964)	**15:0**	**0x0000**	**otpm_data_178 (R/W)**	**N**	**N**
	OTPM_DATA_178 Legal values: [0, 65535].				
R14694 (R0x3966)	**15:0**	**0x0000**	**otpm_data_179 (R/W)**	**N**	**N**
	OTPM_DATA_179 Legal values: [0, 65535].				
R14696 (R0x3968)	**15:0**	**0x0000**	**otpm_data_180 (R/W)**	**N**	**N**
	OTPM_DATA_180 Legal values: [0, 65535].				
R14698 (R0x396A)	**15:0**	**0x0000**	**otpm_data_181 (R/W)**	**N**	**N**
	OTPM_DATA_181 Legal values: [0, 65535].				
R14700 (R0x396C)	**15:0**	**0x0000**	**otpm_data_182 (R/W)**	**N**	**N**
	OTPM_DATA_182 Legal values: [0, 65535].				
R14702 (R0x396E)	**15:0**	**0x0000**	**otpm_data_183 (R/W)**	**N**	**N**
	OTPM_DATA_183 Legal values: [0, 65535].				
R14704 (R0x3970)	**15:0**	**0x0000**	**otpm_data_184 (R/W)**	**N**	**N**
	OTPM_DATA_184 Legal values: [0, 65535].				
R14706 (R0x3972)	**15:0**	**0x0000**	**otpm_data_185 (R/W)**	**N**	**N**
	OTPM_DATA_185 Legal values: [0, 65535].				
R14708 (R0x3974)	**15:0**	**0x0000**	**otpm_data_186 (R/W)**	**N**	**N**
	OTPM_DATA_186 Legal values: [0, 65535].				
R14710 (R0x3976)	**15:0**	**0x0000**	**otpm_data_187 (R/W)**	**N**	**N**
	OTPM_DATA_187 Legal values: [0, 65535].				
R14712 (R0x3978)	**15:0**	**0x0000**	**otpm_data_188 (R/W)**	**N**	**N**
	OTPM_DATA_188 Legal values: [0, 65535].				
R14714 (R0x397A)	**15:0**	**0x0000**	**otpm_data_189 (R/W)**	**N**	**N**
	OTPM_DATA_189 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14716 (R0x397C)	**15:0**	**0x0000**	**otpm_data_190 (R/W)**	**N**	**N**
	OTPM_DATA_190 Legal values: [0, 65535].				
R14718 (R0x397E)	**15:0**	**0x0000**	**otpm_data_191 (R/W)**	**N**	**N**
	OTPM_DATA_191 Legal values: [0, 65535].				
R14720 (R0x3980)	**15:0**	**0x0000**	**otpm_data_192 (R/W)**	**N**	**N**
	OTPM_DATA_192 Legal values: [0, 65535].				
R14722 (R0x3982)	**15:0**	**0x0000**	**otpm_data_193 (R/W)**	**N**	**N**
	OTPM_DATA_193 Legal values: [0, 65535].				
R14724 (R0x3984)	**15:0**	**0x0000**	**otpm_data_194 (R/W)**	**N**	**N**
	OTPM_DATA_194 Legal values: [0, 65535].				
R14726 (R0x3986)	**15:0**	**0x0000**	**otpm_data_195 (R/W)**	**N**	**N**
	OTPM_DATA_195 Legal values: [0, 65535].				
R14728 (R0x3988)	**15:0**	**0x0000**	**otpm_data_196 (R/W)**	**N**	**N**
	OTPM_DATA_196 Legal values: [0, 65535].				
R14730 (R0x398A)	**15:0**	**0x0000**	**otpm_data_197 (R/W)**	**N**	**N**
	OTPM_DATA_197 Legal values: [0, 65535].				
R14732 (R0x398C)	**15:0**	**0x0000**	**otpm_data_198 (R/W)**	**N**	**N**
	OTPM_DATA_198 Legal values: [0, 65535].				
R14734 (R0x398E)	**15:0**	**0x0000**	**otpm_data_199 (R/W)**	**N**	**N**
	OTPM_DATA_199 Legal values: [0, 65535].				
R14736 (R0x3990)	**15:0**	**0x0000**	**otpm_data_200 (R/W)**	**N**	**N**
	OTPM_DATA_200 Legal values: [0, 65535].				
R14738 (R0x3992)	**15:0**	**0x0000**	**otpm_data_201 (R/W)**	**N**	**N**
	OTPM_DATA_201 Legal values: [0, 65535].				
R14740 (R0x3994)	**15:0**	**0x0000**	**otpm_data_202 (R/W)**	**N**	**N**
	OTPM_DATA_202 Legal values: [0, 65535].				
R14742 (R0x3996)	**15:0**	**0x0000**	**otpm_data_203 (R/W)**	**N**	**N**
	OTPM_DATA_203 Legal values: [0, 65535].				
R14744 (R0x3998)	**15:0**	**0x0000**	**otpm_data_204 (R/W)**	**N**	**N**
	OTPM_DATA_204 Legal values: [0, 65535].				
R14746 (R0x399A)	**15:0**	**0x0000**	**otpm_data_205 (R/W)**	**N**	**N**
	OTPM_DATA_205 Legal values: [0, 65535].				
R14748 (R0x399C)	**15:0**	0x0000	**otpm_data_206 (R/W)**	N	N
	OTPM_DATA_206 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14750 (R0x399E)	**15:0**	**0x0000**	**otpm_data_207 (R/W)**	**N**	**N**
	OTPM_DATA_207 Legal values: [0, 65535].				
R14752 (R0x39A0)	**15:0**	**0x0000**	**otpm_data_208 (R/W)**	**N**	**N**
	OTPM_DATA_208 Legal values: [0, 65535].				
R14754 (R0x39A2)	**15:0**	**0x0000**	**otpm_data_209 (R/W)**	**N**	**N**
	OTPM_DATA_209 Legal values: [0, 65535].				
R14756 (R0x39A4)	**15:0**	**0x0000**	**otpm_data_210 (R/W)**	**N**	**N**
	OTPM_DATA_210 Legal values: [0, 65535].				
R14758 (R0x39A6)	**15:0**	**0x0000**	**otpm_data_211 (R/W)**	**N**	**N**
	OTPM_DATA_211 Legal values: [0, 65535].				
R14760 (R0x39A8)	**15:0**	**0x0000**	**otpm_data_212 (R/W)**	**N**	**N**
	OTPM_DATA_212 Legal values: [0, 65535].				
R14762 (R0x39AA)	**15:0**	**0x0000**	**otpm_data_213 (R/W)**	**N**	**N**
	OTPM_DATA_213 Legal values: [0, 65535].				
R14764 (R0x39AC)	**15:0**	**0x0000**	**otpm_data_214 (R/W)**	**N**	**N**
	OTPM_DATA_214 Legal values: [0, 65535].				
R14766 (R0x39AE)	**15:0**	**0x0000**	**otpm_data_215 (R/W)**	**N**	**N**
	OTPM_DATA_215 Legal values: [0, 65535].				
R14768 (R0x39B0)	**15:0**	**0x0000**	**otpm_data_216 (R/W)**	**N**	**N**
	OTPM_DATA_216 Legal values: [0, 65535].				
R14770 (R0x39B2)	**15:0**	**0x0000**	**otpm_data_217 (R/W)**	**N**	**N**
	OTPM_DATA_217 Legal values: [0, 65535].				
R14772 (R0x39B4)	**15:0**	**0x0000**	**otpm_data_218 (R/W)**	**N**	**N**
	OTPM_DATA_218 Legal values: [0, 65535].				
R14774 (R0x39B6)	**15:0**	**0x0000**	**otpm_data_219 (R/W)**	**N**	**N**
	OTPM_DATA_219 Legal values: [0, 65535].				
R14776 (R0x39B8)	**15:0**	**0x0000**	**otpm_data_220 (R/W)**	**N**	**N**
	OTPM_DATA_220 Legal values: [0, 65535].				
R14778 (R0x39BA)	**15:0**	**0x0000**	**otpm_data_221 (R/W)**	**N**	**N**
	OTPM_DATA_221 Legal values: [0, 65535].				
R14780 (R0x39BC)	**15:0**	**0x0000**	**otpm_data_222 (R/W)**	**N**	**N**
	OTPM_DATA_222 Legal values: [0, 65535].				
R14782 (R0x39BE)	**15:0**	**0x0000**	**otpm_data_223 (R/W)**	**N**	**N**
	OTPM_DATA_223 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14784 (R0x39C0)	**15:0**	**0x0000**	**otpm_data_224 (R/W)**	**N**	**N**
	OTPM_DATA_224 Legal values: [0, 65535].				
R14786 (R0x39C2)	**15:0**	**0x0000**	**otpm_data_225 (R/W)**	**N**	**N**
	OTPM_DATA_225 Legal values: [0, 65535].				
R14788 (R0x39C4)	**15:0**	**0x0000**	**otpm_data_226 (R/W)**	**N**	**N**
	OTPM_DATA_226 Legal values: [0, 65535].				
R14790 (R0x39C6)	**15:0**	**0x0000**	**otpm_data_227 (R/W)**	**N**	**N**
	OTPM_DATA_227 Legal values: [0, 65535].				
R14792 (R0x39C8)	**15:0**	**0x0000**	**otpm_data_228 (R/W)**	**N**	**N**
	OTPM_DATA_228 Legal values: [0, 65535].				
R14794 (R0x39CA)	**15:0**	**0x0000**	**otpm_data_229 (R/W)**	**N**	**N**
	OTPM_DATA_229 Legal values: [0, 65535].				
R14796 (R0x39CC)	**15:0**	**0x0000**	**otpm_data_230 (R/W)**	**N**	**N**
	OTPM_DATA_230 Legal values: [0, 65535].				
R14798 (R0x39CE)	**15:0**	**0x0000**	**otpm_data_231 (R/W)**	**N**	**N**
	OTPM_DATA_231 Legal values: [0, 65535].				
R14800 (R0x39D0)	**15:0**	**0x0000**	**otpm_data_232 (R/W)**	**N**	**N**
	OTPM_DATA_232 Legal values: [0, 65535].				
R14802 (R0x39D2)	**15:0**	**0x0000**	**otpm_data_233 (R/W)**	**N**	**N**
	OTPM_DATA_233 Legal values: [0, 65535].				
R14804 (R0x39D4)	**15:0**	**0x0000**	**otpm_data_234 (R/W)**	**N**	**N**
	OTPM_DATA_234 Legal values: [0, 65535].				
R14806 (R0x39D6)	**15:0**	**0x0000**	**otpm_data_235 (R/W)**	**N**	**N**
	OTPM_DATA_235 Legal values: [0, 65535].				
R14808 (R0x39D8)	**15:0**	**0x0000**	**otpm_data_236 (R/W)**	**N**	**N**
	OTPM_DATA_236 Legal values: [0, 65535].				
R14810 (R0x39DA)	**15:0**	**0x0000**	**otpm_data_237 (R/W)**	**N**	**N**
	OTPM_DATA_237 Legal values: [0, 65535].				
R14812 (R0x39DC)	**15:0**	**0x0000**	**otpm_data_238 (R/W)**	**N**	**N**
	OTPM_DATA_238 Legal values: [0, 65535].				
R14814 (R0x39DE)	**15:0**	**0x0000**	**otpm_data_239 (R/W)**	**N**	**N**
	OTPM_DATA_239 Legal values: [0, 65535].				
R14816 (R0x39E0)	**15:0**	**0x0000**	**otpm_data_240 (R/W)**	**N**	**N**
	OTPM_DATA_240 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14818 (R0x39E2)	**15:0**	**0x0000**	**otpm_data_241 (R/W)**	**N**	**N**
	OTPM_DATA_241 Legal values: [0, 65535].				
R14820 (R0x39E4)	**15:0**	**0x0000**	**otpm_data_242 (R/W)**	**N**	**N**
	OTPM_DATA_242 Legal values: [0, 65535].				
R14822 (R0x39E6)	**15:0**	**0x0000**	**otpm_data_243 (R/W)**	**N**	**N**
	OTPM_DATA_243 Legal values: [0, 65535].				
R14824 (R0x39E8)	**15:0**	**0x0000**	**otpm_data_244 (R/W)**	**N**	**N**
	OTPM_DATA_244 Legal values: [0, 65535].				
R14826 (R0x39EA)	**15:0**	**0x0000**	**otpm_data_245 (R/W)**	**N**	**N**
	OTPM_DATA_245 Legal values: [0, 65535].				
R14828 (R0x39EC)	**15:0**	**0x0000**	**otpm_data_246 (R/W)**	**N**	**N**
	OTPM_DATA_246 Legal values: [0, 65535].				
R14830 (R0x39EE)	**15:0**	**0x0000**	**otpm_data_247 (R/W)**	**N**	**N**
	OTPM_DATA_247 Legal values: [0, 65535].				
R14832 (R0x39F0)	**15:0**	**0x0000**	**otpm_data_248 (R/W)**	**N**	**N**
	OTPM_DATA_248 Legal values: [0, 65535].				
R14834 (R0x39F2)	**15:0**	**0x0000**	**otpm_data_249 (R/W)**	**N**	**N**
	OTPM_DATA_249 Legal values: [0, 65535].				
R14836 (R0x39F4)	**15:0**	**0x0000**	**otpm_data_250 (R/W)**	**N**	**N**
	OTPM_DATA_250 Legal values: [0, 65535].				
R14838 (R0x39F6)	**15:0**	**0x0000**	**otpm_data_251 (R/W)**	**N**	**N**
	OTPM_DATA_251 Legal values: [0, 65535].				
R14840 (R0x39F8)	**15:0**	**0x0000**	**otpm_data_252 (R/W)**	**N**	**N**
	OTPM_DATA_252 Legal values: [0, 65535].				
R14842 (R0x39FA)	**15:0**	**0x0000**	**otpm_data_253 (R/W)**	**N**	**N**
	OTPM_DATA_253 Legal values: [0, 65535].				
R14844 (R0x39FC)	**15:0**	**0x0000**	**otpm_data_254 (R/W)**	**N**	**N**
	OTPM_DATA_254 Legal values: [0, 65535].				
R14846 (R0x39FE)	**15:0**	**0x0000**	**otpm_data_255 (R/W)**	**N**	**N**
	OTPM_DATA_255 Legal values: [0, 65535].				
R14848 (R0x3A00)	**15:0**	**0x0000**	**otpm_data_256 (R/W)**	**N**	**N**
	OTPM_DATA_256 Data for OTPM automatic read and write sequences. After an OTPM automatic read sequence, read data is presented in the OTPM_DATA_* registers. Before performing an OTPM automatic write (programming) sequence, the data to be written is presented in the OTPM_DATA_* registers. These registers cannot be accessed when the system is in soft standby (writes will be ignored and reads will return 0). Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14850 (R0x3A02)	**15:0**	**0x0000**	**otpm_data_257 (R/W)**	**N**	**N**
	OTPM_DATA_257 Legal values: [0, 65535].				
R14852 (R0x3A04)	**15:0**	**0x0000**	**otpm_data_258 (R/W)**	**N**	**N**
	OTPM_DATA_258 Legal values: [0, 65535].				
R14854 (R0x3A06)	**15:0**	**0x0000**	**otpm_data_259 (R/W)**	**N**	**N**
	OTPM_DATA_259 Legal values: [0, 65535].				
R14856 (R0x3A08)	**15:0**	**0x0000**	**otpm_data_260 (R/W)**	**N**	**N**
	OTPM_DATA_260 Legal values: [0, 65535].				
R14858 (R0x3A0A)	**15:0**	**0x0000**	**otpm_data_261 (R/W)**	**N**	**N**
	OTPM_DATA_261 Legal values: [0, 65535].				
R14860 (R0x3A0C)	**15:0**	**0x0000**	**otpm_data_262 (R/W)**	**N**	**N**
	OTPM_DATA_262 Legal values: [0, 65535].				
R14862 (R0x3A0E)	**15:0**	**0x0000**	**otpm_data_263 (R/W)**	**N**	**N**
	OTPM_DATA_263 Legal values: [0, 65535].				
R14864 (R0x3A10)	**15:0**	**0x0000**	**otpm_data_264 (R/W)**	**N**	**N**
	OTPM_DATA_264 Legal values: [0, 65535].				
R14866 (R0x3A12)	**15:0**	**0x0000**	**otpm_data_265 (R/W)**	**N**	**N**
	OTPM_DATA_265 Legal values: [0, 65535].				
R14868 (R0x3A14)	**15:0**	**0x0000**	**otpm_data_266 (R/W)**	**N**	**N**
	OTPM_DATA_266 Legal values: [0, 65535].				
R14870 (R0x3A16)	**15:0**	**0x0000**	**otpm_data_267 (R/W)**	**N**	**N**
	OTPM_DATA_267 Legal values: [0, 65535].				
R14872 (R0x3A18)	**15:0**	**0x0000**	**otpm_data_268 (R/W)**	**N**	**N**
	OTPM_DATA_268 Legal values: [0, 65535].				
R14874 (R0x3A1A)	**15:0**	**0x0000**	**otpm_data_269 (R/W)**	**N**	**N**
	OTPM_DATA_269 Legal values: [0, 65535].				
R14876 (R0x3A1C)	**15:0**	**0x0000**	**otpm_data_270 (R/W)**	**N**	**N**
	OTPM_DATA_270 Legal values: [0, 65535].				
R14878 (R0x3A1E)	**15:0**	**0x0000**	**otpm_data_271 (R/W)**	**N**	**N**
	OTPM_DATA_271 Legal values: [0, 65535].				
R14880 (R0x3A20)	**15:0**	**0x0000**	**otpm_data_272 (R/W)**	**N**	**N**
	OTPM_DATA_272 Legal values: [0, 65535].				
R14882 (R0x3A22)	**15:0**	**0x0000**	**otpm_data_273 (R/W)**	**N**	**N**
	OTPM_DATA_273 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14884 (R0x3A24)	**15:0**	**0x0000**	**otpm_data_274 (R/W)**	**N**	**N**
	OTPM_DATA_274 Legal values: [0, 65535].				
R14886 (R0x3A26)	**15:0**	**0x0000**	**otpm_data_275 (R/W)**	**N**	**N**
	OTPM_DATA_275 Legal values: [0, 65535].				
R14888 (R0x3A28)	**15:0**	**0x0000**	**otpm_data_276 (R/W)**	**N**	**N**
	OTPM_DATA_276 Legal values: [0, 65535].				
R14890 (R0x3A2A)	**15:0**	**0x0000**	**otpm_data_277 (R/W)**	**N**	**N**
	OTPM_DATA_277 Legal values: [0, 65535].				
R14892 (R0x3A2C)	**15:0**	**0x0000**	**otpm_data_278 (R/W)**	**N**	**N**
	OTPM_DATA_278 Legal values: [0, 65535].				
R14894 (R0x3A2E)	**15:0**	**0x0000**	**otpm_data_279 (R/W)**	**N**	**N**
	OTPM_DATA_279 Legal values: [0, 65535].				
R14896 (R0x3A30)	**15:0**	**0x0000**	**otpm_data_280 (R/W)**	**N**	**N**
	OTPM_DATA_280 Legal values: [0, 65535].				
R14898 (R0x3A32)	**15:0**	**0x0000**	**otpm_data_281 (R/W)**	**N**	**N**
	OTPM_DATA_281 Legal values: [0, 65535].				
R14900 (R0x3A34)	**15:0**	**0x0000**	**otpm_data_282 (R/W)**	**N**	**N**
	OTPM_DATA_282 Legal values: [0, 65535].				
R14902 (R0x3A36)	**15:0**	**0x0000**	**otpm_data_283 (R/W)**	**N**	**N**
	OTPM_DATA_283 Legal values: [0, 65535].				
R14904 (R0x3A38)	**15:0**	**0x0000**	**otpm_data_284 (R/W)**	**N**	**N**
	OTPM_DATA_284 Legal values: [0, 65535].				
R14906 (R0x3A3A)	**15:0**	**0x0000**	**otpm_data_285 (R/W)**	**N**	**N**
	OTPM_DATA_285 Legal values: [0, 65535].				
R14908 (R0x3A3C)	**15:0**	**0x0000**	**otpm_data_286 (R/W)**	**N**	**N**
	OTPM_DATA_286 Legal values: [0, 65535].				
R14910 (R0x3A3E)	**15:0**	**0x0000**	**otpm_data_287 (R/W)**	**N**	**N**
	OTPM_DATA_287 Legal values: [0, 65535].				
R14912 (R0x3A40)	**15:0**	**0x0000**	**otpm_data_288 (R/W)**	**N**	**N**
	OTPM_DATA_288 Legal values: [0, 65535].				
R14914 (R0x3A42)	**15:0**	**0x0000**	**otpm_data_289 (R/W)**	**N**	**N**
	OTPM_DATA_289 Legal values: [0, 65535].				
R14916 (R0x3A44)	**15:0**	**0x0000**	**otpm_data_290 (R/W)**	**N**	**N**
	OTPM_DATA_290 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14918 (R0x3A46)	**15:0**	**0x0000**	**otpm_data_291 (R/W)**	**N**	**N**
	OTPM_DATA_291 Legal values: [0, 65535].				
R14920 (R0x3A48)	**15:0**	**0x0000**	**otpm_data_292 (R/W)**	**N**	**N**
	OTPM_DATA_292 Legal values: [0, 65535].				
R14922 (R0x3A4A)	**15:0**	**0x0000**	**otpm_data_293 (R/W)**	**N**	**N**
	OTPM_DATA_293 Legal values: [0, 65535].				
R14924 (R0x3A4C)	**15:0**	**0x0000**	**otpm_data_294 (R/W)**	**N**	**N**
	OTPM_DATA_294 Legal values: [0, 65535].				
R14926 (R0x3A4E)	**15:0**	**0x0000**	**otpm_data_295 (R/W)**	**N**	**N**
	OTPM_DATA_295 Legal values: [0, 65535].				
R14928 (R0x3A50)	**15:0**	**0x0000**	**otpm_data_296 (R/W)**	**N**	**N**
	OTPM_DATA_296 Legal values: [0, 65535].				
R14930 (R0x3A52)	**15:0**	**0x0000**	**otpm_data_297 (R/W)**	**N**	**N**
	OTPM_DATA_297 Legal values: [0, 65535].				
R14932 (R0x3A54)	**15:0**	**0x0000**	**otpm_data_298 (R/W)**	**N**	**N**
	OTPM_DATA_298 Legal values: [0, 65535].				
R14934 (R0x3A56)	**15:0**	**0x0000**	**otpm_data_299 (R/W)**	**N**	**N**
	OTPM_DATA_299 Legal values: [0, 65535].				
R14936 (R0x3A58)	**15:0**	**0x0000**	**otpm_data_300 (R/W)**	**N**	**N**
	OTPM_DATA_300 Legal values: [0, 65535].				
R14938 (R0x3A5A)	**15:0**	**0x0000**	**otpm_data_301 (R/W)**	**N**	**N**
	OTPM_DATA_301 Legal values: [0, 65535].				
R14940 (R0x3A5C)	**15:0**	**0x0000**	**otpm_data_302 (R/W)**	**N**	**N**
	OTPM_DATA_302 Legal values: [0, 65535].				
R14942 (R0x3A5E)	**15:0**	**0x0000**	**otpm_data_303 (R/W)**	**N**	**N**
	OTPM_DATA_303 Legal values: [0, 65535].				
R14944 (R0x3A60)	**15:0**	**0x0000**	**otpm_data_304 (R/W)**	**N**	**N**
	OTPM_DATA_304 Legal values: [0, 65535].				
R14946 (R0x3A62)	**15:0**	**0x0000**	**otpm_data_305 (R/W)**	**N**	**N**
	OTPM_DATA_305 Legal values: [0, 65535].				
R14948 (R0x3A64)	**15:0**	**0x0000**	**otpm_data_306 (R/W)**	**N**	**N**
	OTPM_DATA_306 Legal values: [0, 65535].				
R14950 (R0x3A66)	**15:0**	**0x0000**	**otpm_data_307 (R/W)**	**N**	**N**
	OTPM_DATA_307 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14952 (R0x3A68)	**15:0**	**0x0000**	**otpm_data_308 (R/W)**	**N**	**N**
	OTPM_DATA_308 Legal values: [0, 65535].				
R14954 (R0x3A6A)	**15:0**	**0x0000**	**otpm_data_309 (R/W)**	**N**	**N**
	OTPM_DATA_309 Legal values: [0, 65535].				
R14956 (R0x3A6C)	**15:0**	**0x0000**	**otpm_data_310 (R/W)**	**N**	**N**
	OTPM_DATA_310 Legal values: [0, 65535].				
R14958 (R0x3A6E)	**15:0**	**0x0000**	**otpm_data_311 (R/W)**	**N**	**N**
	OTPM_DATA_311 Legal values: [0, 65535].				
R14960 (R0x3A70)	**15:0**	**0x0000**	**otpm_data_312 (R/W)**	**N**	**N**
	OTPM_DATA_312 Legal values: [0, 65535].				
R14962 (R0x3A72)	**15:0**	**0x0000**	**otpm_data_313 (R/W)**	**N**	**N**
	OTPM_DATA_313 Legal values: [0, 65535].				
R14964 (R0x3A74)	**15:0**	**0x0000**	**otpm_data_314 (R/W)**	**N**	**N**
	OTPM_DATA_314 Legal values: [0, 65535].				
R14966 (R0x3A76)	**15:0**	**0x0000**	**otpm_data_315 (R/W)**	**N**	**N**
	OTPM_DATA_315 Legal values: [0, 65535].				
R14968 (R0x3A78)	**15:0**	**0x0000**	**otpm_data_316 (R/W)**	**N**	**N**
	OTPM_DATA_316 Legal values: [0, 65535].				
R14970 (R0x3A7A)	**15:0**	**0x0000**	**otpm_data_317 (R/W)**	**N**	**N**
	OTPM_DATA_317 Legal values: [0, 65535].				
R14972 (R0x3A7C)	**15:0**	**0x0000**	**otpm_data_318 (R/W)**	**N**	**N**
	OTPM_DATA_318 Legal values: [0, 65535].				
R14974 (R0x3A7E)	**15:0**	**0x0000**	**otpm_data_319 (R/W)**	**N**	**N**
	OTPM_DATA_319 Legal values: [0, 65535].				
R14976 (R0x3A80)	**15:0**	**0x0000**	**otpm_data_320 (R/W)**	**N**	**N**
	OTPM_DATA_320 Legal values: [0, 65535].				
R14978 (R0x3A82)	**15:0**	**0x0000**	**otpm_data_321 (R/W)**	**N**	**N**
	OTPM_DATA_321 Legal values: [0, 65535].				
R14980 (R0x3A84)	**15:0**	**0x0000**	**otpm_data_322 (R/W)**	**N**	**N**
	OTPM_DATA_322 Legal values: [0, 65535].				
R14982 (R0x3A86)	**15:0**	**0x0000**	**otpm_data_323 (R/W)**	**N**	**N**
	OTPM_DATA_323 Legal values: [0, 65535].				
R14984 (R0x3A88)	**15:0**	**0x0000**	**otpm_data_324 (R/W)**	**N**	**N**
	OTPM_DATA_324 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14986 (R0x3A8A)	**15:0**	**0x0000**	**otpm_data_325 (R/W)**	**N**	**N**
	OTPM_DATA_325 Legal values: [0, 65535].				
R14988 (R0x3A8C)	**15:0**	**0x0000**	**otpm_data_326 (R/W)**	**N**	**N**
	OTPM_DATA_326 Legal values: [0, 65535].				
R14990 (R0x3A8E)	**15:0**	**0x0000**	**otpm_data_327 (R/W)**	**N**	**N**
	OTPM_DATA_327 Legal values: [0, 65535].				
R14992 (R0x3A90)	**15:0**	**0x0000**	**otpm_data_328 (R/W)**	**N**	**N**
	OTPM_DATA_328 Legal values: [0, 65535].				
R14994 (R0x3A92)	**15:0**	**0x0000**	**otpm_data_329 (R/W)**	**N**	**N**
	OTPM_DATA_329 Legal values: [0, 65535].				
R14996 (R0x3A94)	**15:0**	**0x0000**	**otpm_data_330 (R/W)**	**N**	**N**
	OTPM_DATA_330 Legal values: [0, 65535].				
R14998 (R0x3A96)	**15:0**	**0x0000**	**otpm_data_331 (R/W)**	**N**	**N**
	OTPM_DATA_331 Legal values: [0, 65535].				
R15000 (R0x3A98)	**15:0**	**0x0000**	**otpm_data_332 (R/W)**	**N**	**N**
	OTPM_DATA_332 Legal values: [0, 65535].				
R15002 (R0x3A9A)	**15:0**	**0x0000**	**otpm_data_333 (R/W)**	**N**	**N**
	OTPM_DATA_333 Legal values: [0, 65535].				
R15004 (R0x3A9C)	**15:0**	**0x0000**	**otpm_data_334 (R/W)**	**N**	**N**
	OTPM_DATA_334 Legal values: [0, 65535].				
R15006 (R0x3A9E)	**15:0**	**0x0000**	**otpm_data_335 (R/W)**	**N**	**N**
	OTPM_DATA_335 Legal values: [0, 65535].				
R15008 (R0x3AA0)	**15:0**	**0x0000**	**otpm_data_336 (R/W)**	**N**	**N**
	OTPM_DATA_336 Legal values: [0, 65535].				
R15010 (R0x3AA2)	**15:0**	**0x0000**	**otpm_data_337 (R/W)**	**N**	**N**
	OTPM_DATA_337 Legal values: [0, 65535].				
R15012 (R0x3AA4)	**15:0**	**0x0000**	**otpm_data_338 (R/W)**	**N**	**N**
	OTPM_DATA_338 Legal values: [0, 65535].				
R15014 (R0x3AA6)	**15:0**	**0x0000**	**otpm_data_339 (R/W)**	**N**	**N**
	OTPM_DATA_339 Legal values: [0, 65535].				
R15016 (R0x3AA8)	**15:0**	**0x0000**	**otpm_data_340 (R/W)**	**N**	**N**
	OTPM_DATA_340 Legal values: [0, 65535].				
R15018 (R0x3AAA)	**15:0**	**0x0000**	**otpm_data_341 (R/W)**	**N**	**N**
	OTPM_DATA_341 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15020 (R0x3AAC)	**15:0**	**0x0000**	**otpm_data_342 (R/W)**	**N**	**N**
	OTPM_DATA_342 Legal values: [0, 65535].				
R15022 (R0x3AAE)	**15:0**	**0x0000**	**otpm_data_343 (R/W)**	**N**	**N**
	OTPM_DATA_343 Legal values: [0, 65535].				
R15024 (R0x3AB0)	**15:0**	**0x0000**	**otpm_data_344 (R/W)**	**N**	**N**
	OTPM_DATA_344 Legal values: [0, 65535].				
R15026 (R0x3AB2)	**15:0**	**0x0000**	**otpm_data_345 (R/W)**	**N**	**N**
	OTPM_DATA_345 Legal values: [0, 65535].				
R15028 (R0x3AB4)	**15:0**	**0x0000**	**otpm_data_346 (R/W)**	**N**	**N**
	OTPM_DATA_346 Legal values: [0, 65535].				
R15030 (R0x3AB6)	**15:0**	**0x0000**	**otpm_data_347 (R/W)**	**N**	**N**
	OTPM_DATA_347 Legal values: [0, 65535].				
R15032 (R0x3AB8)	**15:0**	**0x0000**	**otpm_data_348 (R/W)**	**N**	**N**
	OTPM_DATA_348 Legal values: [0, 65535].				
R15034 (R0x3ABA)	**15:0**	**0x0000**	**otpm_data_349 (R/W)**	**N**	**N**
	OTPM_DATA_349 Legal values: [0, 65535].				
R15036 (R0x3ABC)	**15:0**	**0x0000**	**otpm_data_350 (R/W)**	**N**	**N**
	OTPM_DATA_350 Legal values: [0, 65535].				
R15038 (R0x3ABE)	**15:0**	**0x0000**	**otpm_data_351 (R/W)**	**N**	**N**
	OTPM_DATA_351 Legal values: [0, 65535].				
R15040 (R0x3AC0)	**15:0**	**0x0000**	**otpm_data_352 (R/W)**	**N**	**N**
	OTPM_DATA_352 Legal values: [0, 65535].				
R15042 (R0x3AC2)	**15:0**	**0x0000**	**otpm_data_353 (R/W)**	**N**	**N**
	OTPM_DATA_353 Legal values: [0, 65535].				
R15044 (R0x3AC4)	**15:0**	**0x0000**	**otpm_data_354 (R/W)**	**N**	**N**
	OTPM_DATA_354 Legal values: [0, 65535].				
R15046 (R0x3AC6)	**15:0**	**0x0000**	**otpm_data_355 (R/W)**	**N**	**N**
	OTPM_DATA_355 Legal values: [0, 65535].				
R15048 (R0x3AC8)	**15:0**	**0x0000**	**otpm_data_356 (R/W)**	**N**	**N**
	OTPM_DATA_356 Legal values: [0, 65535].				
R15050 (R0x3ACA)	**15:0**	**0x0000**	**otpm_data_357 (R/W)**	**N**	**N**
	OTPM_DATA_357 Legal values: [0, 65535].				
R15052 (R0x3ACC)	**15:0**	**0x0000**	**otpm_data_358 (R/W)**	**N**	**N**
	OTPM_DATA_358 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15054 (R0x3ACE)	**15:0**	**0x0000**	**otpm_data_359 (R/W)**	**N**	**N**
	OTPM_DATA_359 Legal values: [0, 65535].				
R15056 (R0x3AD0)	**15:0**	**0x0000**	**otpm_data_360 (R/W)**	**N**	**N**
	OTPM_DATA_360 Legal values: [0, 65535].				
R15058 (R0x3AD2)	**15:0**	**0x0000**	**otpm_data_361 (R/W)**	**N**	**N**
	OTPM_DATA_361 Legal values: [0, 65535].				
R15060 (R0x3AD4)	**15:0**	**0x0000**	**otpm_data_362 (R/W)**	**N**	**N**
	OTPM_DATA_362 Legal values: [0, 65535].				
R15062 (R0x3AD6)	**15:0**	**0x0000**	**otpm_data_363 (R/W)**	**N**	**N**
	OTPM_DATA_363 Legal values: [0, 65535].				
R15064 (R0x3AD8)	**15:0**	**0x0000**	**otpm_data_364 (R/W)**	**N**	**N**
	OTPM_DATA_364 Legal values: [0, 65535].				
R15066 (R0x3ADA)	**15:0**	**0x0000**	**otpm_data_365 (R/W)**	**N**	**N**
	OTPM_DATA_365 Legal values: [0, 65535].				
R15068 (R0x3ADC)	**15:0**	**0x0000**	**otpm_data_366 (R/W)**	**N**	**N**
	OTPM_DATA_366 Legal values: [0, 65535].				
R15070 (R0x3ADE)	**15:0**	**0x0000**	**otpm_data_367 (R/W)**	**N**	**N**
	OTPM_DATA_367 Legal values: [0, 65535].				
R15072 (R0x3AE0)	**15:0**	**0x0000**	**otpm_data_368 (R/W)**	**N**	**N**
	OTPM_DATA_368 Legal values: [0, 65535].				
R15074 (R0x3AE2)	**15:0**	**0x0000**	**otpm_data_369 (R/W)**	**N**	**N**
	OTPM_DATA_369 Legal values: [0, 65535].				
R15076 (R0x3AE4)	**15:0**	**0x0000**	**otpm_data_370 (R/W)**	**N**	**N**
	OTPM_DATA_370 Legal values: [0, 65535].				
R15078 (R0x3AE6)	**15:0**	**0x0000**	**otpm_data_371 (R/W)**	**N**	**N**
	OTPM_DATA_371 Legal values: [0, 65535].				
R15080 (R0x3AE8)	**15:0**	**0x0000**	**otpm_data_372 (R/W)**	**N**	**N**
	OTPM_DATA_372 Legal values: [0, 65535].				
R15082 (R0x3AEA)	**15:0**	**0x0000**	**otpm_data_373 (R/W)**	**N**	**N**
	OTPM_DATA_373 Legal values: [0, 65535].				
R15084 (R0x3AEC)	**15:0**	**0x0000**	**otpm_data_374 (R/W)**	**N**	**N**
	OTPM_DATA_374 Legal values: [0, 65535].				
R15086 (R0x3AEE)	**15:0**	**0x0000**	**otpm_data_375 (R/W)**	**N**	**N**
	OTPM_DATA_375 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15088 (R0x3AF0)	**15:0**	**0x0000**	**otpm_data_376 (R/W)**	**N**	**N**
	OTPM_DATA_376 Legal values: [0, 65535].				
R15090 (R0x3AF2)	**15:0**	**0x0000**	**otpm_data_377 (R/W)**	**N**	**N**
	OTPM_DATA_377 Legal values: [0, 65535].				
R15092 (R0x3AF4)	**15:0**	**0x0000**	**otpm_data_378 (R/W)**	**N**	**N**
	OTPM_DATA_378 Legal values: [0, 65535].				
R15094 (R0x3AF6)	**15:0**	**0x0000**	**otpm_data_379 (R/W)**	**N**	**N**
	OTPM_DATA_379 Legal values: [0, 65535].				
R15096 (R0x3AF8)	**15:0**	**0x0000**	**otpm_data_380 (R/W)**	**N**	**N**
	OTPM_DATA_380 Legal values: [0, 65535].				
R15098 (R0x3AFA)	**15:0**	**0x0000**	**otpm_data_381 (R/W)**	**N**	**N**
	OTPM_DATA_381 Legal values: [0, 65535].				
R15100 (R0x3AFC)	**15:0**	**0x0000**	**otpm_data_382 (R/W)**	**N**	**N**
	OTPM_DATA_382 Legal values: [0, 65535].				
R15102 (R0x3AFE)	**15:0**	**0x0000**	**otpm_data_383 (R/W)**	**N**	**N**
	OTPM_DATA_383 Legal values: [0, 65535].				
R15104 (R0x3B00)	**15:0**	**0x0000**	**otpm_data_384 (R/W)**	**N**	**N**
	OTPM_DATA_384 Legal values: [0, 65535].				
R15106 (R0x3B02)	**15:0**	**0x0000**	**otpm_data_385 (R/W)**	**N**	**N**
	OTPM_DATA_385 Legal values: [0, 65535].				
R15108 (R0x3B04)	**15:0**	**0x0000**	**otpm_data_386 (R/W)**	**N**	**N**
	OTPM_DATA_386 Legal values: [0, 65535].				
R15110 (R0x3B06)	**15:0**	**0x0000**	**otpm_data_387 (R/W)**	**N**	**N**
	OTPM_DATA_387 Legal values: [0, 65535].				
R15112 (R0x3B08)	**15:0**	**0x0000**	**otpm_data_388 (R/W)**	**N**	**N**
	OTPM_DATA_388 Legal values: [0, 65535].				
R15114 (R0x3B0A)	**15:0**	**0x0000**	**otpm_data_389 (R/W)**	**N**	**N**
	OTPM_DATA_389 Legal values: [0, 65535].				
R15116 (R0x3B0C)	**15:0**	**0x0000**	**otpm_data_390 (R/W)**	**N**	**N**
	OTPM_DATA_390 Legal values: [0, 65535].				
R15118 (R0x3B0E)	**15:0**	**0x0000**	**otpm_data_391 (R/W)**	**N**	**N**
	OTPM_DATA_391 Legal values: [0, 65535].				
R15120 (R0x3B10)	**15:0**	**0x0000**	**otpm_data_392 (R/W)**	**N**	**N**
	OTPM_DATA_392 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15122 (R0x3B12)	**15:0**	**0x0000**	**otpm_data_393 (R/W)**	**N**	**N**
	OTPM_DATA_393 Legal values: [0, 65535].				
R15124 (R0x3B14)	**15:0**	**0x0000**	**otpm_data_394 (R/W)**	**N**	**N**
	OTPM_DATA_394 Legal values: [0, 65535].				
R15126 (R0x3B16)	**15:0**	**0x0000**	**otpm_data_395 (R/W)**	**N**	**N**
	OTPM_DATA_395 Legal values: [0, 65535].				
R15128 R0x3B18)	**15:0**	**0x0000**	**otpm_data_396 (R/W)**	**N**	**N**
	OTPM_DATA_396 Legal values: [0, 65535].				
R15130 (R0x3B1A)	**15:0**	**0x0000**	**otpm_data_397 (R/W)**	**N**	**N**
	OTPM_DATA_397 Legal values: [0, 65535].				
R15132 (R0x3B1C)	**15:0**	**0x0000**	**otpm_data_398 (R/W)**	**N**	**N**
	OTPM_DATA_398 Legal values: [0, 65535].				
R15134 (R0x3B1E)	**15:0**	**0x0000**	**otpm_data_399 (R/W)**	**N**	**N**
	OTPM_DATA_399 Legal values: [0, 65535].				
R15136 (R0x3B20)	**15:0**	**0x0000**	**otpm_data_400 (R/W)**	**N**	**N**
	OTPM_DATA_400 Legal values: [0, 65535].				
R15138 (R0x3B22)	**15:0**	**0x0000**	**otpm_data_401 (R/W)**	**N**	**N**
	OTPM_DATA_401 Legal values: [0, 65535].				
R15140 (R0x3B24)	**15:0**	**0x0000**	**otpm_data_402 (R/W)**	**N**	**N**
	OTPM_DATA_402 Legal values: [0, 65535].				
R15142 (R0x3B26)	**15:0**	**0x0000**	**otpm_data_403 (R/W)**	**N**	**N**
	OTPM_DATA_403 Legal values: [0, 65535].				
R15144 (R0x3B28)	**15:0**	**0x0000**	**otpm_data_404 (R/W)**	**N**	**N**
	OTPM_DATA_404 Legal values: [0, 65535].				
R15146 (R0x3B2A)	**15:0**	**0x0000**	**otpm_data_405 (R/W)**	**N**	**N**
	OTPM_DATA_405 Legal values: [0, 65535].				
R15148 (R0x3B2C)	**15:0**	**0x0000**	**otpm_data_406 (R/W)**	**N**	**N**
	OTPM_DATA_406 Legal values: [0, 65535].				
R15150 (R0x3B2E)	**15:0**	**0x0000**	**otpm_data_407 (R/W)**	**N**	**N**
	OTPM_DATA_407 Legal values: [0, 65535].				
R15152 (R0x3B30)	**15:0**	**0x0000**	**otpm_data_408 (R/W)**	**N**	**N**
	OTPM_DATA_408 Legal values: [0, 65535].				
R15154 (R0x3B32)	**15:0**	**0x0000**	**otpm_data_409 (R/W)**	**N**	**N**
	OTPM_DATA_409 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15156 (R0x3B34)	**15:0**	**0x0000**	**otpm_data_410 (R/W)**	**N**	**N**
	OTPM_DATA_410 Legal values: [0, 65535].				
R15158 (R0x3B36)	**15:0**	**0x0000**	**otpm_data_411 (R/W)**	**N**	**N**
	OTPM_DATA_411 Legal values: [0, 65535].				
R15160 (R0x3B38)	**15:0**	**0x0000**	**otpm_data_412 (R/W)**	**N**	**N**
	OTPM_DATA_412 Legal values: [0, 65535].				
R15162 (R0x3B3A)	**15:0**	**0x0000**	**otpm_data_413 (R/W)**	**N**	**N**
	OTPM_DATA_413 Legal values: [0, 65535].				
R15164 (R0x3B3C)	**15:0**	**0x0000**	**otpm_data_414 (R/W)**	**N**	**N**
	OTPM_DATA_414 Legal values: [0, 65535].				
R15166 (R0x3B3E)	**15:0**	**0x0000**	**otpm_data_415 (R/W)**	**N**	**N**
	OTPM_DATA_415 Legal values: [0, 65535].				
R15168 (R0x3B40)	**15:0**	**0x0000**	**otpm_data_416 (R/W)**	**N**	**N**
	OTPM_DATA_416 Legal values: [0, 65535].				
R15170 (R0x3B42)	**15:0**	**0x0000**	**otpm_data_417 (R/W)**	**N**	**N**
	OTPM_DATA_417 Legal values: [0, 65535].				
R15172 (R0x3B44)	**15:0**	**0x0000**	**otpm_data_418 (R/W)**	**N**	**N**
	OTPM_DATA_418 Legal values: [0, 65535].				
R15174 (R0x3B46)	**15:0**	**0x0000**	**otpm_data_419 (R/W)**	**N**	**N**
	OTPM_DATA_419 Legal values: [0, 65535].				
R15176 (R0x3B48)	**15:0**	**0x0000**	**otpm_data_420 (R/W)**	**N**	**N**
	OTPM_DATA_420 Legal values: [0, 65535].				
R15178 (R0x3B4A)	**15:0**	**0x0000**	**otpm_data_421 (R/W)**	**N**	**N**
	OTPM_DATA_421 Legal values: [0, 65535].				
R15180 (R0x3B4C)	**15:0**	**0x0000**	**otpm_data_422 (R/W)**	**N**	**N**
	OTPM_DATA_422 Legal values: [0, 65535].				
R15182 (R0x3B4E)	**15:0**	**0x0000**	**otpm_data_423 (R/W)**	**N**	**N**
	OTPM_DATA_423 Legal values: [0, 65535].				
R15184 (R0x3B50)	**15:0**	**0x0000**	**otpm_data_424 (R/W)**	**N**	**N**
	OTPM_DATA_424 Legal values: [0, 65535].				
R15186 (R0x3B52)	**15:0**	**0x0000**	**otpm_data_425 (R/W)**	**N**	**N**
	OTPM_DATA_425 Legal values: [0, 65535].				
R15188 (R0x3B54)	**15:0**	**0x0000**	**otpm_data_426 (R/W)**	**N**	**N**
	OTPM_DATA_426 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15190 (R0x3B56)	**15:0**	**0x0000**	**otpm_data_427 (R/W)**	**N**	**N**
	OTPM_DATA_427 Legal values: [0, 65535].				
R15192 (R0x3B58)	**15:0**	**0x0000**	**otpm_data_428 (R/W)**	**N**	**N**
	OTPM_DATA_428 Legal values: [0, 65535].				
R15194 (R0x3B5A)	**15:0**	**0x0000**	**otpm_data_429 (R/W)**	**N**	**N**
	OTPM_DATA_429 Legal values: [0, 65535].				
R15196 (R0x3B5C)	**15:0**	**0x0000**	**otpm_data_430 (R/W)**	**N**	**N**
	OTPM_DATA_430 Legal values: [0, 65535].				
R15198 (R0x3B5E)	**15:0**	**0x0000**	**otpm_data_431 (R/W)**	**N**	**N**
	OTPM_DATA_431 Legal values: [0, 65535].				
R15200 (R0x3B60)	**15:0**	**0x0000**	**otpm_data_432 (R/W)**	**N**	**N**
	OTPM_DATA_432 Legal values: [0, 65535].				
R15202 (R0x3B62)	**15:0**	**0x0000**	**otpm_data_433 (R/W)**	**N**	**N**
	OTPM_DATA_433 Legal values: [0, 65535].				
R15204 (R0x3B64)	**15:0**	**0x0000**	**otpm_data_434 (R/W)**	**N**	**N**
	OTPM_DATA_434 Legal values: [0, 65535].				
R15206 (R0x3B66)	**15:0**	**0x0000**	**otpm_data_435 (R/W)**	**N**	**N**
	OTPM_DATA_435 Legal values: [0, 65535].				
R15208 (R0x3B68)	**15:0**	**0x0000**	**otpm_data_436 (R/W)**	**N**	**N**
	OTPM_DATA_436 Legal values: [0, 65535].				
R15210 (R0x3B6A)	**15:0**	**0x0000**	**otpm_data_437 (R/W)**	**N**	**N**
	OTPM_DATA_437 Legal values: [0, 65535].				
R15212 (R0x3B6C)	**15:0**	**0x0000**	**otpm_data_438 (R/W)**	**N**	**N**
	OTPM_DATA_438 Legal values: [0, 65535].				
R15214 (R0x3B6E)	**15:0**	**0x0000**	**otpm_data_439 (R/W)**	**N**	**N**
	OTPM_DATA_439 Legal values: [0, 65535].				
(R15216 R0x3B70)	**15:0**	**0x0000**	**otpm_data_440 (R/W)**	**N**	**N**
	OTPM_DATA_440 Legal values: [0, 65535].				
R15218 (R0x3B72)	**15:0**	**0x0000**	**otpm_data_441 (R/W)**	**N**	**N**
	OTPM_DATA_441 Legal values: [0, 65535].				
R15220 (R0x3B74)	**15:0**	**0x0000**	**otpm_data_442 (R/W)**	**N**	**N**
	OTPM_DATA_442 Legal values: [0, 65535].				
R15222 (R0x3B76)	**15:0**	**0x0000**	**otpm_data_443 (R/W)**	**N**	**N**
	OTPM_DATA_443 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15224 (R0x3B78)	**15:0**	**0x0000**	**otpm_data_444 (R/W)**	**N**	**N**
	OTPM_DATA_444 Legal values: [0, 65535].				
R15226 (R0x3B7A)	**15:0**	**0x0000**	**otpm_data_445 (R/W)**	**N**	**N**
	OTPM_DATA_445 Legal values: [0, 65535].				
R15228 (R0x3B7C)	**15:0**	**0x0000**	**otpm_data_446 (R/W)**	**N**	**N**
	OTPM_DATA_446 Legal values: [0, 65535].				
R15230 (R0x3B7E)	**15:0**	**0x0000**	**otpm_data_447 (R/W)**	**N**	**N**
	OTPM_DATA_447 Legal values: [0, 65535].				
R15232 (R0x3B80)	**15:0**	**0x0000**	**otpm_data_448 (R/W)**	**N**	**N**
	OTPM_DATA_448 Legal values: [0, 65535].				
R15234 (R0x3B82)	**15:0**	**0x0000**	**otpm_data_449 (R/W)**	**N**	**N**
	OTPM_DATA_449 Legal values: [0, 65535].				
R15236 (R0x3B84)	**15:0**	**0x0000**	**otpm_data_450 (R/W)**	**N**	**N**
	OTPM_DATA_450 Legal values: [0, 65535].				
R15238 (R0x3B86)	**15:0**	**0x0000**	**otpm_data_451 (R/W)**	**N**	**N**
	OTPM_DATA_451 Legal values: [0, 65535].				
R15240 (R0x3B88)	**15:0**	**0x0000**	**otpm_data_452 (R/W)**	**N**	**N**
	OTPM_DATA_452 Legal values: [0, 65535].				
R15242 (R0x3B8A)	**15:0**	**0x0000**	**otpm_data_453 (R/W)**	**N**	**N**
	OTPM_DATA_453 Legal values: [0, 65535].				
R15244 (R0x3B8C)	**15:0**	**0x0000**	**otpm_data_454 (R/W)**	**N**	**N**
	OTPM_DATA_454 Legal values: [0, 65535].				
R15246 (R0x3B8E)	**15:0**	**0x0000**	**otpm_data_455 (R/W)**	**N**	**N**
	OTPM_DATA_455 Legal values: [0, 65535].				
R15248 (R0x3B90)	**15:0**	**0x0000**	**otpm_data_456 (R/W)**	**N**	**N**
	OTPM_DATA_456 Legal values: [0, 65535].				
R15250 (R0x3B92)	**15:0**	**0x0000**	**otpm_data_457 (R/W)**	**N**	**N**
	OTPM_DATA_457 Legal values: [0, 65535].				
R15252 (R0x3B94)	**15:0**	**0x0000**	**otpm_data_458 (R/W)**	**N**	**N**
	OTPM_DATA_458 Legal values: [0, 65535].				
R15254 (R0x3B96)	**15:0**	**0x0000**	**otpm_data_459 (R/W)**	**N**	**N**
	OTPM_DATA_459 Legal values: [0, 65535].				
R15256 (R0x3B98)	**15:0**	**0x0000**	**otpm_data_460 (R/W)**	**N**	**N**
	OTPM_DATA_460 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15258 (R0x3B9A)	**15:0**	**0x0000**	**otpm_data_461 (R/W)**	**N**	**N**
	OTPM_DATA_461 Legal values: [0, 65535].				
R15260 (R0x3B9C)	**15:0**	**0x0000**	**otpm_data_462 (R/W)**	**N**	**N**
	OTPM_DATA_462 Legal values: [0, 65535].				
R15262 (R0x3B9E)	**15:0**	**0x0000**	**otpm_data_463 (R/W)**	**N**	**N**
	OTPM_DATA_463 Legal values: [0, 65535].				
R15264 (R0x3BA0)	**15:0**	**0x0000**	**otpm_data_464 (R/W)**	**N**	**N**
	OTPM_DATA_464 Legal values: [0, 65535].				
R15266 (R0x3BA2)	**15:0**	**0x0000**	**otpm_data_465 (R/W)**	**N**	**N**
	OTPM_DATA_465 Legal values: [0, 65535].				
R15268 (R0x3BA4)	**15:0**	**0x0000**	**otpm_data_466 (R/W)**	**N**	**N**
	OTPM_DATA_466 Legal values: [0, 65535].				
R15270 (R0x3BA6)	**15:0**	**0x0000**	**otpm_data_467 (R/W)**	**N**	**N**
	OTPM_DATA_467 Legal values: [0, 65535].				
R15272 (R0x3BA8)	**15:0**	**0x0000**	**otpm_data_468 (R/W)**	**N**	**N**
	OTPM_DATA_468 Legal values: [0, 65535].				
R15274 (R0x3BAA)	**15:0**	**0x0000**	**otpm_data_469 (R/W)**	**N**	**N**
	OTPM_DATA_469 Legal values: [0, 65535].				
R15276 (R0x3BAC)	**15:0**	**0x0000**	**otpm_data_470 (R/W)**	**N**	**N**
	OTPM_DATA_470 Legal values: [0, 65535].				
R15278 (R0x3BAE)	**15:0**	**0x0000**	**otpm_data_471 (R/W)**	**N**	**N**
	OTPM_DATA_471 Legal values: [0, 65535].				
R15280 (R0x3BB0)	**15:0**	**0x0000**	**otpm_data_472 (R/W)**	**N**	**N**
	OTPM_DATA_472 Legal values: [0, 65535].				
R15282 (R0x3BB2)	**15:0**	**0x0000**	**otpm_data_473 (R/W)**	**N**	**N**
	OTPM_DATA_473 Legal values: [0, 65535].				
R15284 (R0x3BB4)	**15:0**	**0x0000**	**otpm_data_474 (R/W)**	**N**	**N**
	OTPM_DATA_474 Legal values: [0, 65535].				
R15286 (R0x3BB6)	**15:0**	**0x0000**	**otpm_data_475 (R/W)**	**N**	**N**
	OTPM_DATA_475 Legal values: [0, 65535].				
R15288 (R0x3BB8)	**15:0**	**0x0000**	**otpm_data_476 (R/W)**	**N**	**N**
	OTPM_DATA_476 Legal values: [0, 65535].				
R15290 (R0x3BBA)	**15:0**	**0x0000**	**otpm_data_477 (R/W)**	**N**	**N**
	OTPM_DATA_477 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15292 (R0x3BBC)	**15:0**	**0x0000**	**otpm_data_478 (R/W)**	**N**	**N**
	OTPM_DATA_478 Legal values: [0, 65535].				
R15294 (R0x3BBE)	**15:0**	**0x0000**	**otpm_data_479 (R/W)**	**N**	**N**
	OTPM_DATA_479 Legal values: [0, 65535].				
R15296 (R0x3BC0)	**15:0**	**0x0000**	**otpm_data_480 (R/W)**	**N**	**N**
	OTPM_DATA_480 Legal values: [0, 65535].				
R15298 (R0x3BC2)	**15:0**	**0x0000**	**otpm_data_481 (R/W)**	**N**	**N**
	OTPM_DATA_481 Legal values: [0, 65535].				
R15300 (R0x3BC4)	**15:0**	**0x0000**	**otpm_data_482 (R/W)**	**N**	**N**
	OTPM_DATA_482 Legal values: [0, 65535].				
R15302 (R0x3BC6)	**15:0**	**0x0000**	**otpm_data_483 (R/W)**	**N**	**N**
	OTPM_DATA_483 Legal values: [0, 65535].				
R15304 (R0x3BC8)	**15:0**	**0x0000**	**otpm_data_484 (R/W)**	**N**	**N**
	OTPM_DATA_484 Legal values: [0, 65535].				
R15306 (R0x3BCA)	**15:0**	**0x0000**	**otpm_data_485 (R/W)**	**N**	**N**
	OTPM_DATA_485 Legal values: [0, 65535].				
R15308 (R0x3BCC)	**15:0**	**0x0000**	**otpm_data_486 (R/W)**	**N**	**N**
	OTPM_DATA_486 Legal values: [0, 65535].				
R15310 (R0x3BCE)	**15:0**	**0x0000**	**otpm_data_487 (R/W)**	**N**	**N**
	OTPM_DATA_487 Legal values: [0, 65535].				
R15312 (R0x3BD0)	**15:0**	**0x0000**	**otpm_data_488 (R/W)**	**N**	**N**
	OTPM_DATA_488 Legal values: [0, 65535].				
R15314 (R0x3BD2)	**15:0**	**0x0000**	**otpm_data_489 (R/W)**	**N**	**N**
	OTPM_DATA_489 Legal values: [0, 65535].				
R15316 (R0x3BD4)	**15:0**	**0x0000**	**otpm_data_490 (R/W)**	**N**	**N**
	OTPM_DATA_490 Legal values: [0, 65535].				
R15318 (R0x3BD6)	**15:0**	**0x0000**	**otpm_data_491 (R/W)**	**N**	**N**
	OTPM_DATA_491 Legal values: [0, 65535].				
R15320 (R0x3BD8)	**15:0**	**0x0000**	**otpm_data_492 (R/W)**	**N**	**N**
	OTPM_DATA_492 Legal values: [0, 65535].				
R15322 (R0x3BDA)	**15:0**	**0x0000**	**otpm_data_493 (R/W)**	**N**	**N**
	OTPM_DATA_493 Legal values: [0, 65535].				
R15324 (R0x3BDC)	**15:0**	**0x0000**	**otpm_data_494 (R/W)**	**N**	**N**
	OTPM_DATA_494 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R15326 (R0x3BDE)	**15:0**	**0x0000**	**otpm_data_495 (R/W)**	**N**	**N**
	OTPM_DATA_495 Legal values: [0, 65535].				
R15328 (R0x3BE0)	**15:0**	**0x0000**	**otpm_data_496 (R/W)**	**N**	**N**
	OTPM_DATA_496 Legal values: [0, 65535].				
R15330 (R0x3BE2)	**15:0**	**0x0000**	**otpm_data_497 (R/W)**	**N**	**N**
	OTPM_DATA_497 Legal values: [0, 65535].				
R15332 (R0x3BE4)	**15:0**	**0x0000**	**otpm_data_498 (R/W)**	**N**	**N**
	OTPM_DATA_498 Legal values: [0, 65535].				
R15334 (R0x3BE6)	**15:0**	**0x0000**	**otpm_data_499 (R/W)**	**N**	**N**
	OTPM_DATA_499 Legal values: [0, 65535].				
R15336 (R0x3BE8)	**15:0**	**0x0000**	**otpm_data_500 (R/W)**	**N**	**N**
	OTPM_DATA_500 Legal values: [0, 65535].				
R15338 (R0x3BEA)	**15:0**	**0x0000**	**otpm_data_501 (R/W)**	**N**	**N**
	OTPM_DATA_501 Legal values: [0, 65535].				
R15340 (R0x3BEC)	**15:0**	**0x0000**	**otpm_data_502 (R/W)**	**N**	**N**
	OTPM_DATA_502 Legal values: [0, 65535].				
R15342 (R0x3BEE)	**15:0**	**0x0000**	**otpm_data_503 (R/W)**	**N**	**N**
	OTPM_DATA_503 Legal values: [0, 65535].				
R15344 (R0x3BF0)	**15:0**	**0x0000**	**otpm_data_504 (R/W)**	**N**	**N**
	OTPM_DATA_504 Legal values: [0, 65535].				
R15346 (R0x3BF2)	**15:0**	**0x0000**	**otpm_data_505 (R/W)**	**N**	**N**
	OTPM_DATA_505 Legal values: [0, 65535].				
R15348 (R0x3BF4)	**15:0**	**0x0000**	**otpm_data_506 (R/W)**	**N**	**N**
	OTPM_DATA_506 Legal values: [0, 65535].				
R15350 (R0x3BF6)	**15:0**	**0x0000**	**otpm_data_507 (R/W)**	**N**	**N**
	OTPM_DATA_507 Legal values: [0, 65535].				
R15352 (R0x3BF8)	**15:0**	**0x0000**	**otpm_data_508 (R/W)**	**N**	**N**
	OTPM_DATA_508 Legal values: [0, 65535].				
R15354 (R0x3BFA)	**15:0**	**0x0000**	**otpm_data_509 (R/W)**	**N**	**N**
	OTPM_DATA_509 Legal values: [0, 65535].				
R15356 (R0x3BFC)	**15:0**	**0x0000**	**otpm_data_510 (R/W)**	**N**	**N**
	OTPM_DATA_510 Legal values: [0, 65535].				
R15358 (R0x3BFE)	**15:0**	**0x0000**	**otpm_data_511 (R/W)**	**N**	**N**
	OTPM_DATA_511 Legal values: [0, 65535].				

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R16160 (R0x3F20)	**15:0**	**0x0008**	**gth_control (R/W)**	**N**	**N**
	15:12	X	Reserved		
	11	0x0000	clip_en_fdoc Clip function enable during fine digital correction rows 0: disable 1: enable	N	N
	10	0x0000	limit_en_fdoc Limit function enable during fine digital correction rows 0: disable 1: enable	N	N
	9	0x0000	th_en_fdoc Threshold filter function enable during fine digital correction rows 0: disable 1: enable	N	N
	8:6	X	Reserved		
	5	0x0000	clip_en_rtn Clip function enable during row noise correction columns 0: disable 1: enable	N	N
	4	0x0000	limit_en_rtn Limit function enable during row noise correction columns 0: disable 1: enable	N	N
	3	0x0001	th_en_rtn Threshold filter function enable during row noise correction columns 0: disable 1: enable	N	N
	2:1	X	Reserved		
	0	0x0001	th_en_blk Threshold filter function enable during blk rows 0: disable 1: enable	N	N
R16168 (R0x3F28)	**15:0**	**0x0000**	**gth_clip_rtn (R/W)**	**N**	**N**
	15:8	0x0000	clip_th_top_rtn Highest clip value for clip function during row noise correction columns Legal values: [0, 255].	N	N
	7:0	0x0000	clip_th_bot_rtn Lowest clip value for clip function during row noise correction columns Legal values: [0, 255].	N	N
R16186 (R0x3F3A)	**15:0**	**0x0080**	**analog_control8 (R/W)**	**N**	**N**
	15:8	X	Reserved		
	7	0x0001	Reserved		
	6:0	0x0000	pixel_transfer_time Specify the pulse width of do_transfer Writes are synchronized to frame boundaries. Legal values: [0, 127].	Y	N

Table 6. MANUFACTURER SPECIFIC (continued)

Register Dec (Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R16188 (R0x3F3C)	**15:0**	**0x0003**	**analog_control9 (R/W)**	**N**	**N**
	15:4	X	Reserved		
	3	0x0000	row_sf_bin4 Enable source follower row bin4 Writes are synchronized to frame boundaries.	Y	N
	2	X	Reserved		
	1:0	0x0003	ana_blocks_enable 2'b00: ana block always on 2'b01: ana block on during frame valid 2'b10: ana block on during line valid (sample, shutter and transfer) 2'b11: dynamic power control during integration time and readout Writes are synchronized to frame boundaries. Legal values: [0, 3].	Y	N

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