

Vertical Timing Optimization for Interline CCD Image Sensors



ON Semiconductor®

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APPLICATION NOTE

Introduction

This application note applies to the ON Semiconductor Interline CCD Image Sensors listed in Table 1.

On these Interline CCDs a “speed-up” structure has been incorporated to increase the frame rate. If the vertical clock pulses are not properly aligned, then these CCDs are vulnerable to a vertical striping effect. This effect is especially noticeable in a flat field image near saturation. The artifact can be eliminated by careful adjustment of the vertical clock edge alignment as described in this note.

Below is an example of vertical stripes found in the KAI-11002 Image Sensor, where there are 16 pixels between the alternating column intensities. The top portion of the image was cropped and zoomed out (50%) for illustration purposes.

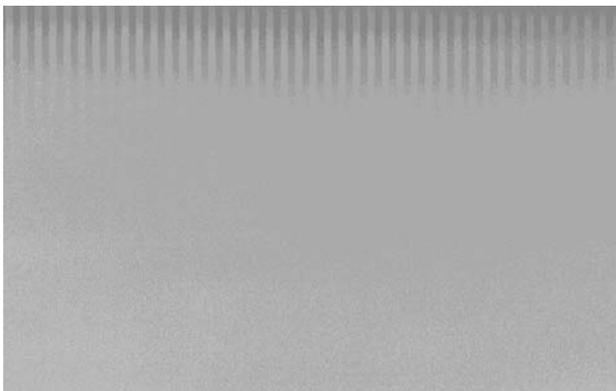


Figure 1. Example of Vertical Stripes

The spacing between stripes depends on the details of the sensor design. Please refer to the following table:

Table 1. NUMBER OF PIXELS BETWEEN STRIPES

Sensor	Spacing
KAI-0340	20 pixels ^[1] / 10 pixels ^[2]
KAI-1003	16 pixels
KAI-01150	40 pixels
KAI-2001	24 pixels
KAI-2020	24 pixels
KAI-02050	40 pixels
KAI-2093	16 pixels
KAI-02150	40 pixels
KAI-02170	40 pixels
KAI-4011	8 pixels / 16 pixels
KAI-4021	8 pixels / 16 pixels
KAI-04022	8 pixels / 16 pixels
KAI-04050	40 pixels
KAI-04070	40 pixels
KAI-08050	40 pixels
KAI-11002	16 pixels
KAI-16000	8 pixels
KAI-16050	40 pixels
KAI-16070	40 pixels
KAI-29050	40 pixels

1. Every 20 pixels for full resolution readout mode.
2. Every 10 pixels for sub-window readout mode.

There are two cases of stripes in images:

1. Stripes run equally throughout (top-bottom) image or
2. Stripes are visible primarily in the top or bottom of image (as in Figure 1).

Depending on where the stripes appear, this will help indicate where in the timing to focus on:

For case 1, top-bottom of image, the misaligned edges are most likely in the line timing.

For case 2, top and/or bottom of image, the misaligned edges are most likely in the frame timing.

Vertical Clock Edge Alignment Suggestions

For troubleshooting purposes, it is useful to capture flat-field images to solve this issue.

The most common solution to eliminate the vertical stripes is by trial and error adjustments to the vertical clock (V1, V2) edge positions. In general, the transition edges are desired close to coincident. A rising edge can come slightly before a falling edge, but if the opposite is true, these bars will likely appear (see Figure 2).

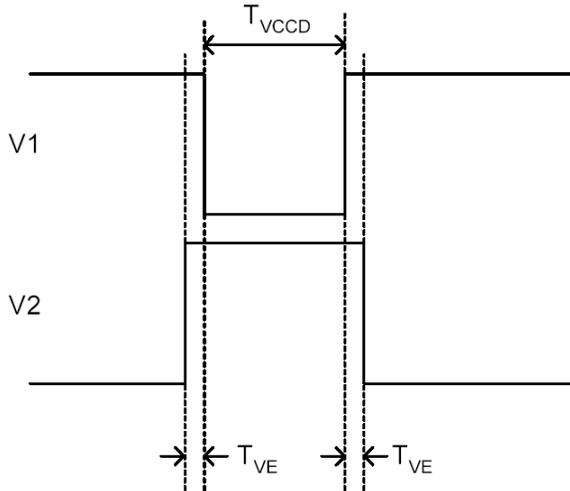


Figure 2. Example Line Timing Alignment

Please note that KAI-xxx50s and KAI-xxx70s are 4 phase vertical ccd image sensors where the photodiode to vertical ccd gate is controlled via V1 VCCD phase, as opposed to other interline CCDs (listed in Table 1) that are implementing 2 phase vertical CCD where V2 VCCD phase is controlling the photodiode to vertical ccd gate.

Also the crossing point recommendation may be different from sensor: for KAI-xxx50 and KAI-xxx70 sensors the recommended point is between 75% and 100%; refer to the device performance specification for more detail information.

It is also best practice to have the clock cross points as symmetrical as possible, as shown in Figure 3 at 50% signal amplitude.

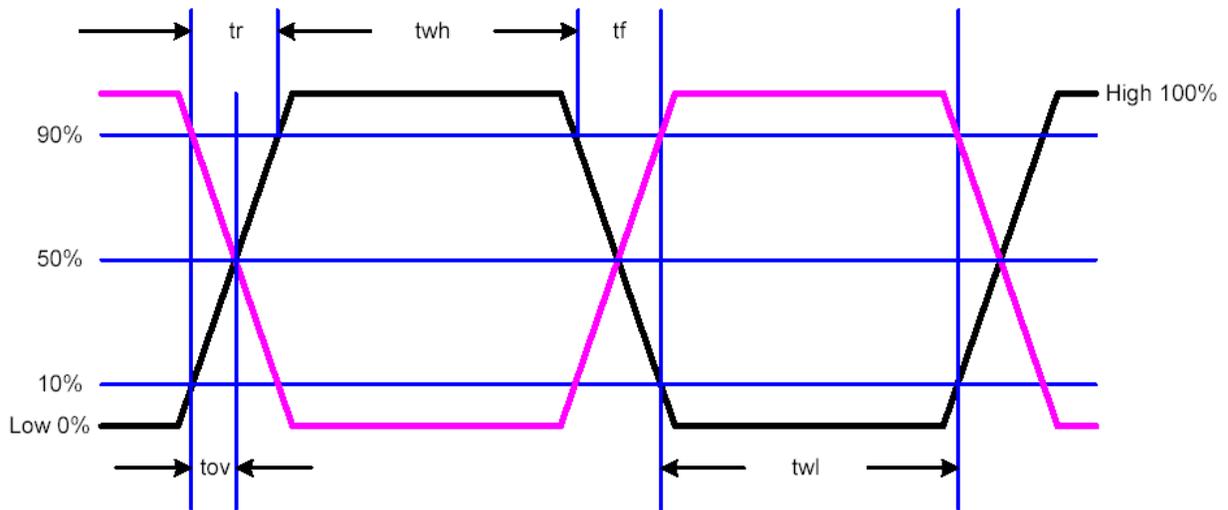


Figure 3. Symmetrical Cross Points on Timing Clocks

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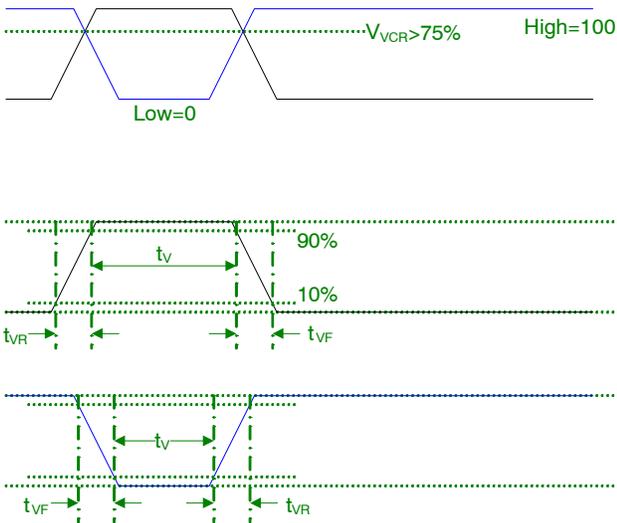


Figure 4. Symmetrical Crossing Point above 75% on Timing Clocks for KAI-xxx50 and KAI-xxx70 Image Sensors

Sometimes, a misaligned V1/V2 clock edge is accompanied by a spike on the VSUB signal. The following are suggested steps:

1. Look at V1, V2 and VSUB on an oscilloscope simultaneously.
2. Look at V1/V2 edge alignment during a row transfer, look for spikes on any of the 3 signals and adjust edge placement to eliminate.
3. Look at V1/V2 edge alignment during the frame timing (photodiode transfer) and do the same as step 2.
4. Also look at V1 and V2 where the clocks turn off and then back on for the horizontal read out. Make sure there are no glitches or spikes.
5. Look at V1, V2 and VSUB during the electronic shutter pulse and make sure there are no spikes or ringing.

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Examples of Vertical Clock Edge Alignments

We add here some examples of Vertical Clock edge alignments, during the line transfer timing, and the relative image artifacts, for a KAI-02150 interline CCD; the same considerations can be applied to all KAI-xxx50 and KAI-xxx70 series.

The image sensor was operated with Truesense Imaging evaluation hardware (please refer to Truesense Imaging web

site for more information) and set for reaching the linear saturation around 3000 ADU (Analog to Digital Units in Digital Numbers); the CCD output signal was then controlled, using a variable light source (LED), to achieve about 2800 ADU (close to linear saturation) then images and VCLOCK wave forms were plotted at different VCLOCK crossing points.

At 0% crossing point:

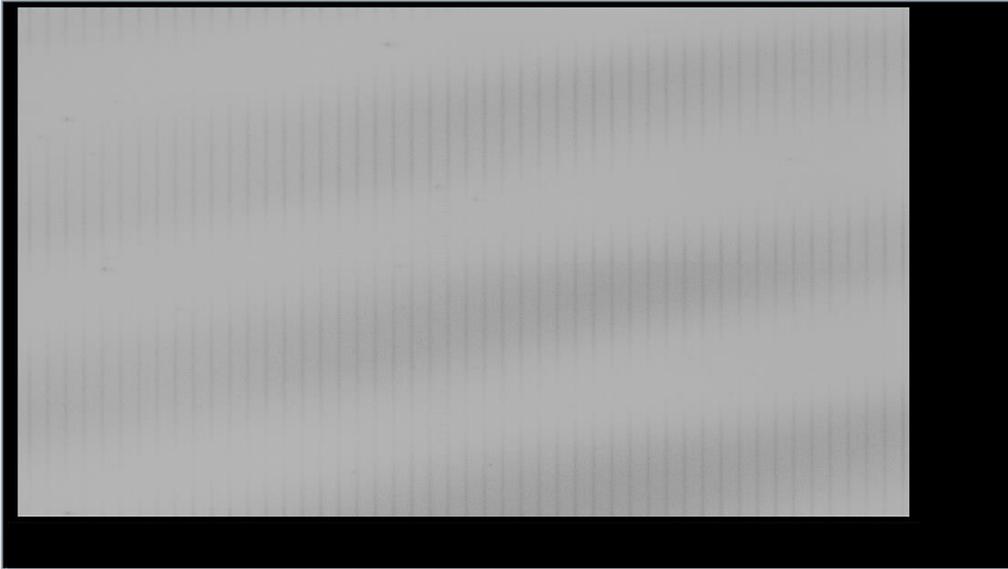


Figure 5. Image from KAI-02150 at 0% Crossing

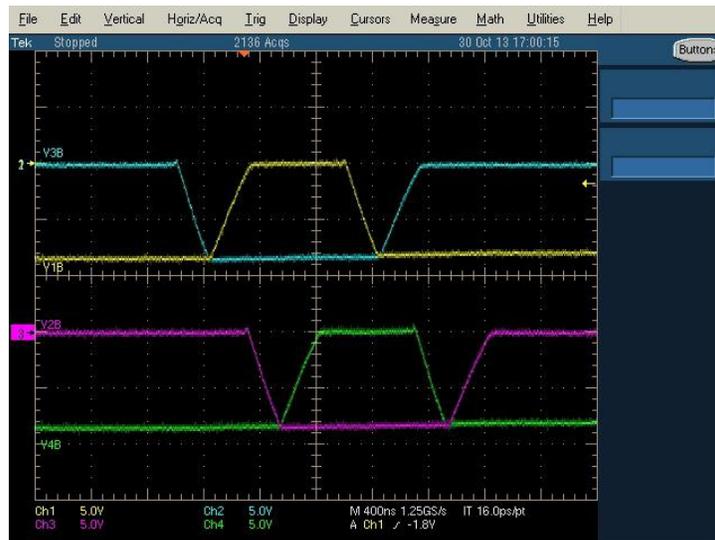


Figure 6. KAI-02150 VCLK Line Transfer Plot at 0% Crossing

At 75% crossing point:



Figure 7. Image from KAI-02150 at 75% Crossing

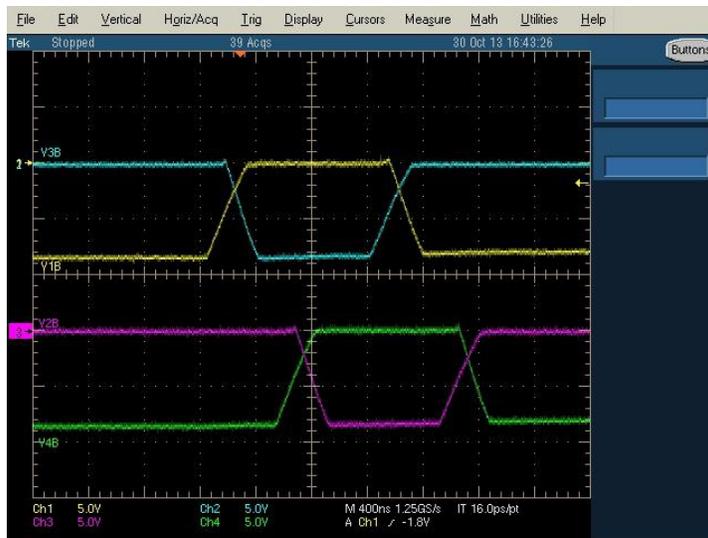


Figure 8. KAI-02150 VCLK Line Transfer Plot at 75% Crossing

Please note in Figure 5 the vertical striping running from top to bottom, the vertical bands are repeating every 40 columns.

In Figure 7 the stripes are removed due to better vertical clock edge alignment (refer to Figure 6 and Figure 8).

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