AND9187/D

Binning Mode Operation for Full Frame CCD Sensors

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APPLICATION NOTE

Introduction

This application note is intended to describe two methods for operating 20 μm and 24 μm Pixel Full Frame CCD sensors when binning is desired. The note gives a detailed explanation of both methods and associated performance issues.

The applicable CCD sensors include:

- KAF 0261 (20 μm × 20 μm Pixels)
- KAF 1001 (24 μm × 24 μm Pixels)
- KAF 4301 (24 μm × 24 μm Pixels)

Sensor Operation

Image Acquisition

An electronic representation of an image is formed from a CCD image sensor when incident photons falling on the CCD active area create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each photo gate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength.

After the CCD has been illuminated, the charge accumulated in the pixel sites is clocked out of the sensor in a two-step process. When operating in a normal, or non-binning, mode, a single line (row) of charge is first shifted out of the vertical CCD array and into the horizontal CCD register in parallel. The line of charge is then serially shifted toward the floating diffusion (FD) output node by the horizontal register. Before reaching the floating diffusion node the charge passes over the last cell of the horizontal register known as the transfer gate which consists of the H21 and H22 clock gate inputs. These gates are separate from the rest of the horizontal register and direct the charge to the desired output node. Each pixel's charge is then converted into a voltage and is sensed off chip. After the CCD output signal has been sampled by the system electronics, the charge on the floating diffusion is removed via the Reset Drain (VRD) by action of the Reset Clock (ϕR). The floating diffusion is reset to the potential applied to VRD. This is repeated for all succeeding pixels in the line, and lines in the array (See Figure 1).

Vertical Register Operation

Binning Vertically

When operating the CCD sensor in vertical binning mode, two or more lines of charge are combined together in the horizontal CCD register, before the horizontal clocks begin to shift the charge towards the floating diffusion output node. This charge is shifted to the output, pixel by pixel, in a manner identical to normal operation. In order to accomplish row-summation, the horizontal register is designed with a significantly larger capacity than the vertical register so that more than one row can be combined and read out.

In normal mode operation the Vertical Clocks V1 and V2 shift lines of charge into the horizontal CCD register in parallel, while H1 is held high and H2 is held low. The clocking sequence is shown in Figure 2. On the rising edge of V2, the line of charge in the last Vertical CCD line is transported into the Horizontal CCD register.

When operating the CCD in a binning mode, an additional sequence of the V1 and V2 clocks is repeated for as many times as the binning mode dictates before beginning to clock the charge out of the horizontal CCD register. A vertical register timing scheme for binning 2 rows is shown in Figure 3. Two lines of charge would be transported onto the Horizontal CCD register.

Horizontal Register Operation

Standard Horizontal Operation

The floating diffusion is the structure on CCDs that exists between the input of the on-chip amplifier and last phase of the horizontal register. This structure is responsible for summing the electrons from each pixel and presenting it as a voltage to the input gate of the output amplifier. The reference voltage, or "zero state" of the floating diffusion, is set to VRD when the Reset clock goes high. This effectively sets the offset voltage of the output video. The output video stays at this voltage until H22 or H21 pulses low (H1 subsequently moves high) forcing a new packet of electrons onto the floating diffusion. H22 and H21 act as steering versions of the H2 register. Electrically separated from H2, H21 and H22 are used to select which output amplifier will be used to read voltages from the device. If a low gain operation is desired, H21 is chosen to mimic H2, and H22 is set slightly more negative than H21-Low. In this mode all charge is transferred to the floating diffusion that is attached to the low gain amplifier (amp1). For high gain operation the roles of H21 and H22 are reversed from the above description. Normal mode horizontal clocking is shown below in Figure 4.

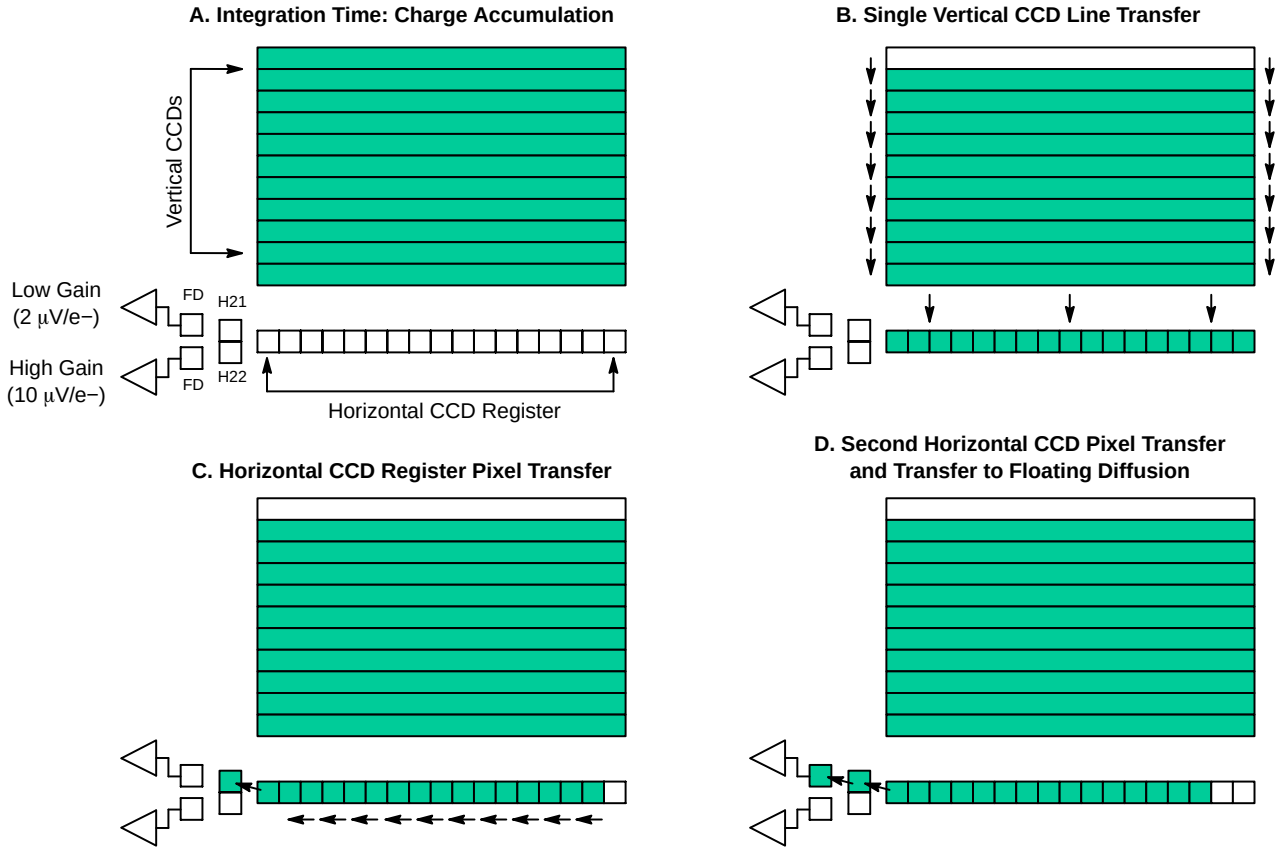

Figure 1. Normal Readout through Low Gain Output

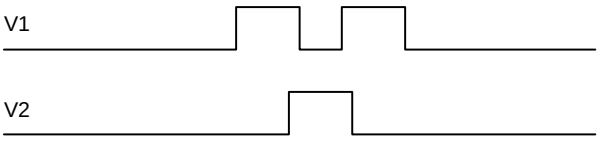

Figure 2. Normal Vertical Clock Timing

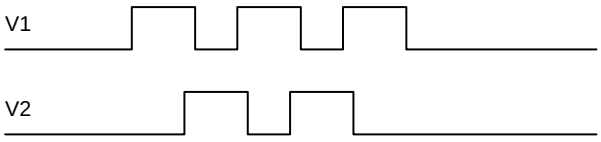

Figure 3. Vertical Timing to Combine Two Lines

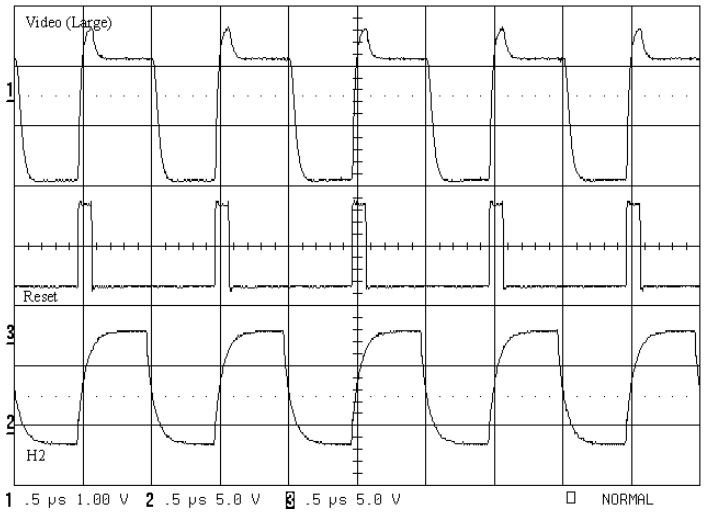

Figure 4. Normal Pixel Rate Timing

Horizontal Binning

General Principal of Horizontal Binning

In order to operate in horizontal binning mode, charge from the horizontal register must be summed at or before the input of the output amplifier. On the 20 μm and 24 μm pixel devices there are two ways to accomplish this. One method is to sum the charge on the floating diffusion by sending the reset pulse every other pixel period. This method of binning may be implemented on every Full Frame CCD. The other method is to sum charge on the H21 or H22 transfer gates, effectively using them as a summing gate. The later method allows the clamp and sample pulses to be temporally identical to normal mode timing, allowing for a noise performance that is more comparable to normal mode operation.

Horizontal Binning On to the Floating Diffusion

CCD Timing for horizontal binning operation where charge is to be collected on the floating diffusion is similar to the standard method of clocking with the exception of the reset clock. For charge to be collected on the floating diffusion, rather than resetting the FD back to VRD every cycle, charge is allowed to accumulate for as many cycles as desired. Figure 7 shows the reset clocking required to bin two columns on the floating diffusion. Note that video signal mirrors the H2 clock in its appearance for low signal operation but the effect is much less when larger signals are being read out). This is because the H2 signal capacitively couples into the output. Although visible in the waveform, this does not affect the amount of signal being read by the output amplifier. Figure 5 and Figure 6 also show the positions of clamp and sample pulses. From these figures it can be observed that the sample pulse is nearly 3/4 of a binned period from the clamp pulse. This decreases the effective sampling frequency of the CDS (Correlated Double Sampling circuit) and may lead toward increased temporal noise in some systems.

Horizontal Binning with Transfer Gates

In order to reduce noise susceptibility when binning horizontally, many CCD designs will have a binning gate or “binning well”. This is a single cell of the horizontal register located at the output end of the register that is electrically separated from the rest of the horizontal register. This separation allows for it to be clocked independent of the rest of the register and enables charge to be summed within the cell before it is transferred to the floating diffusion. Large pixel devices have a similar signal phase gate of the horizontal register that is electrically isolated from the rest of the register. This gate is the transfer gate, H21 or H22. The primary function of this gate is to steer charge to one of the two on-chip output amplifiers. In normal mode operation for high gain performance H22 is clocked identically to H2 while H21 is held low. Likewise, for standard low gain operation H21 is clocked identically to H2 while H22 is held low. Charge is accumulated in the transfer gate when it is in a high state and shifted when the signal moves more negative. In order to accumulate charge on the H21 or H22 transfer gate, (H21 is typically used since the low gain amplifier has a higher dynamic range) negative going phases of H21 or H22 are removed for each cycle that binning is desired. The benefit of this method of operation is that charge is transferred once onto the floating diffusion during 1/2 of the standard pixel period. The time between clamp and sample pulses with this mode is the same as in normal operation allowing for the same noise performance calculations to apply in binning mode that applied in standard mode. Figure 8 through Figure 10 shows the timing modifications and resulting video. H22 is assumed to be held at a DC state that is more negative than H21-Low, and all timing that is not shown in the figures is unaltered. The caveat to this method of binning is that the capacity of the horizontal register is appreciably less than the capacity of the low gain output amplifier. When binning on the floating diffusion the only charge limit is the output amplifier and the electrostatic potentials surrounding the floating diffusion. Conversely, when binning on the transfer gate the primary limiting factor is the capacity of the summing gate (same as horizontal register). In the case of the 24 μm and 20 μm pixel CCD devices, the charge capacity of the summing gate is less than that of the floating diffusion and output amplifier (See Figure 13).

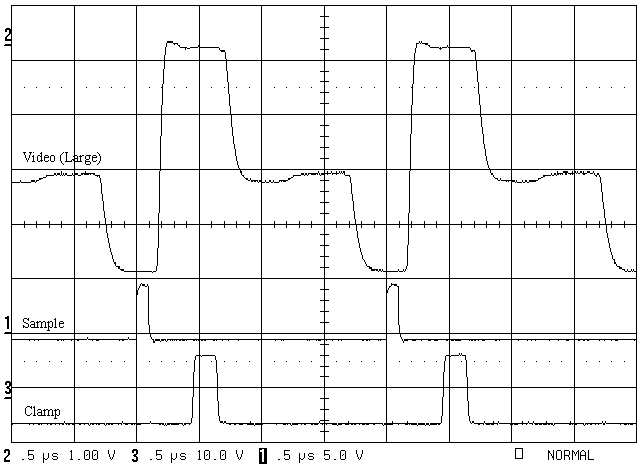

Figure 5. Two Columns Combined (Binned) on to the Floating Diffusion Large Signal

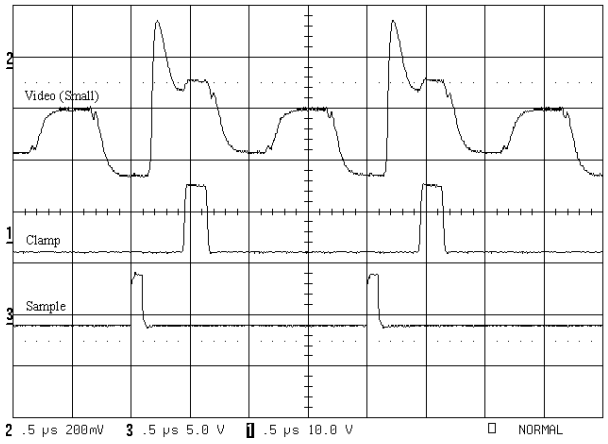

Figure 6. Two Columns Combined (Binned) on to the Floating Diffusion (Small Signal)

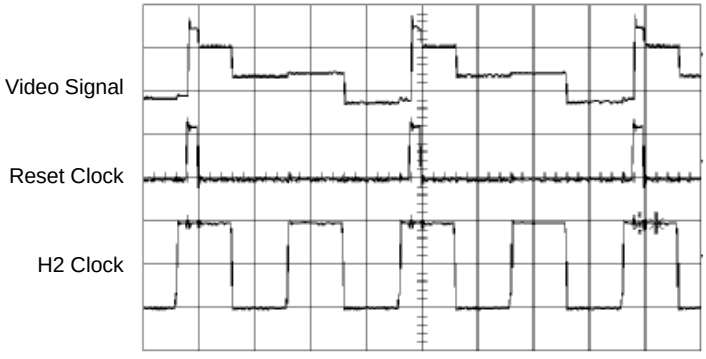

Figure 7. Reset Timing for Two Columns Combined (Binned) on to the Floating Diffusion (Small Signal)

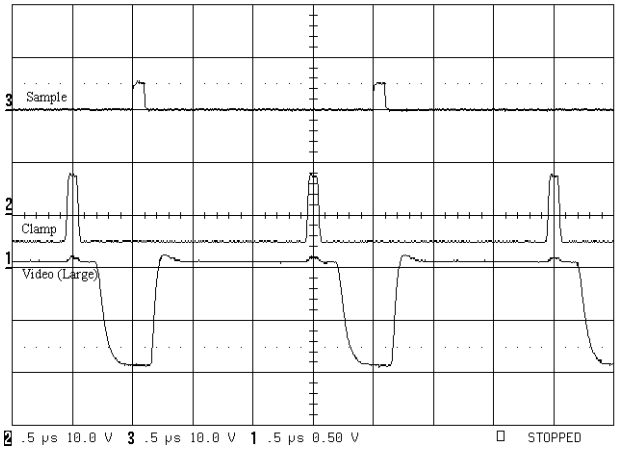

Figure 8. Two Columns Binned on to H21 (Sample/Clamp/Vid)

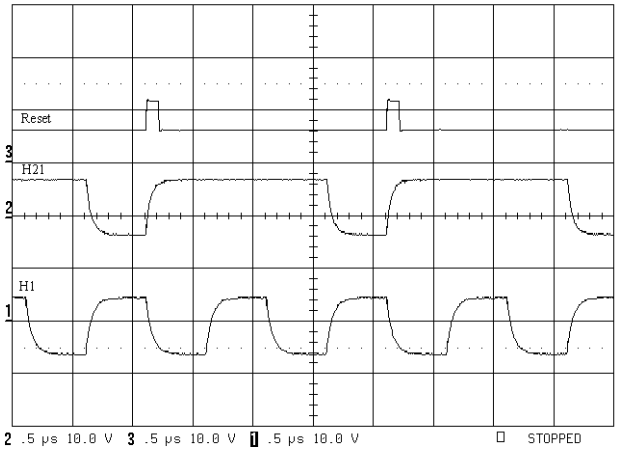

Figure 9. Two Columns Binned on to H21 (H1, H21, Reset)

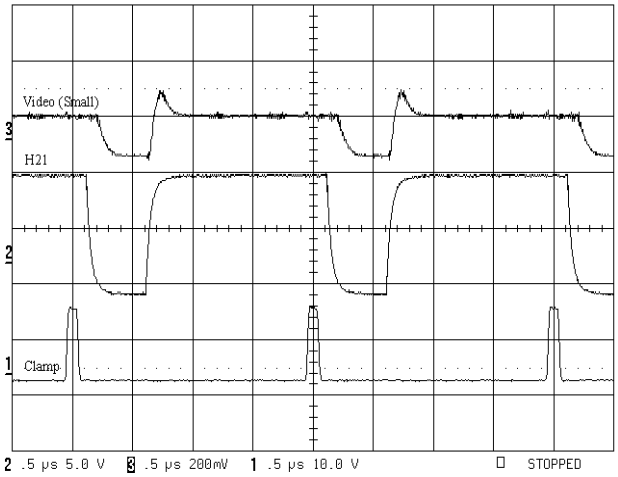

Figure 10. Two Columns Binned on to H21 (Video, H21, Clamp Clock)

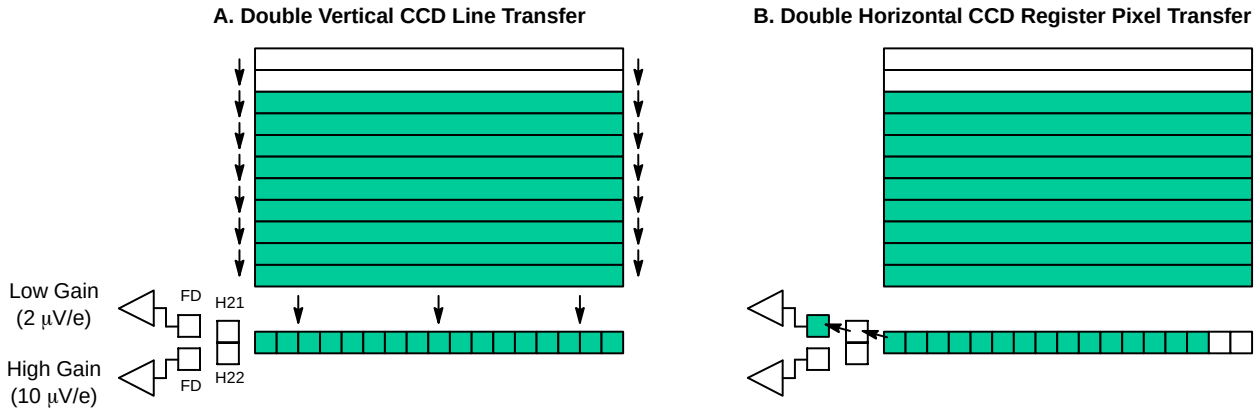

Figure 11. Charge Transport: 2×2 Binning on Floating Diffusion Using Low Gain (2 μV/electron) Output

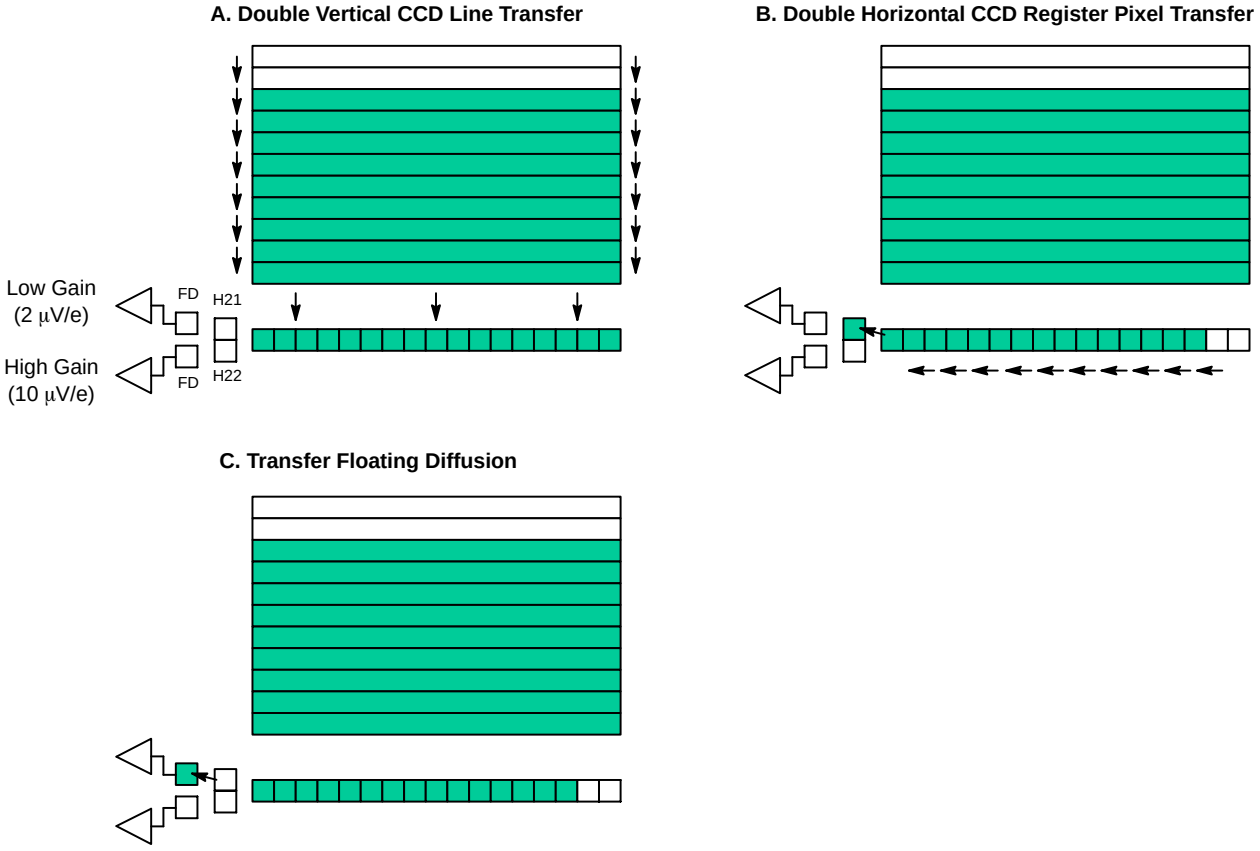

Figure 12. Charge Transport: 2×2 Binning on Transfer Gate (H21) Using Low Gain (2 μV/electron) Output

PIXEL SATURATION

Nominal CCD Settings

The 20 μm and 24 μm pixel devices have saturation levels that vary according to the mode of CCD operation. See Figure 13 for details. When operating a 24 μm Pixel KAF-Series CCD through the high gain output amplifier with the nominal settings as dictated in the Device Specifications Sheet, the output amplifier will fail first at 200,000 electrons. The full dynamic range of these devices operating in normal mode can be achieved using the low gain output amplifier. In normal mode operation using the low gain output amplifier, the first CCD structure to reach capacity as illumination is increased are the vertical registers. When this occurs streaks and column defects will appear in the image as individual vertical registers saturate. With 24 μm pixel devices this occurs at an exposure of approximately 650,000 electrons. Figure 13 shows the charge capacity measurement using the Variance vs. Mean technique. This technique leverages the Poisson behavior of photon noise (shot noise). According to this behavior the shot noise component of the variance must equal the mean where the units of measure are electrons squared and electrons respectively. Since shot noise is the only noise component that increases with increasing signal, the slope of a Mean vs. Variance plot is always equal to 1.0 as long as the CCD and signal processing electronics are operating properly. This relationship is only true if both the mean and standard deviation are plotted in electrons. If the units are not plotted in electrons, the slope of the non-electron units curve will provide a system conversion factor to electrons. When an element or elements of a CCD begin to fail due to saturation the first sign of failure is a deviation from the mean variance relationship. Saturation causes charge to blend with adjacent pixels, forces charge to leak to adjacent structures, or quantizes the conversion of charges packets. In any case, saturation causes the measured Mean vs. Variance data to fall away from the ideal slope of 1.0. The mean value at which the deviation begins to increase with increasing signal is the charge capacity of the CCD under those particular operating conditions. Through the use of this plotting technique under various operating conditions and modes, different internal structures within the CCD can be made to fail according to the Mean vs. Variance plot. In this method, charge capacities for the various structures within a CCD can be determined.

Large pixel CCDs may operate in binning mode on both the low gain and high gain outputs. However, binning on the high gain output will not increase the maximum output signal since the amplifier itself saturates at 2 volts. However, the high gain amplifier may be used in combination with a binning mode clocking scheme when maximum sensitivity is desired with relatively low noise. With this configuration, any bright points or hot spots in the image that produce more than 200,000 electrons inside the CCD will be absorbed by the excess dynamic range of the vertical and horizontal registers and will be clipped by the output amplifier without affecting the rest of the image. This method of operation uses the dynamic range of the internal CCD structures as a means of blooming suppression.

The horizontal registers in ON Semiconductor scientific CCDs are designed to have nearly twice the electron capacity per cell as the vertical registers. This allows for binning in the vertical direction of 2 rows without saturation of the horizontal register. In 24 μm pixel devices the horizontal register has a charge capacity of 1,100,000 electrons, while the vertical registers have a capacity of 650,000 electrons.

When binning 2 vertical by 2 horizontal the charge capacity in terms of the structural limits of the main horizontal and vertical registers should be 2,200,000 electrons for a 24 μm pixel device. This is slightly larger than the maximum achievable capacity through the low gain amplifier when binning 2×2 on the floating diffusion, which has a maximum linear capacity of 1.9 million electrons. Therefore, the effective capacity of the CCD as a whole is 1.9 million electrons. However, this does allow for a well-balanced binning of nearly 4 volts of signal. On the other hand, if the transfer gate is used for binning instead of the floating diffusion, the maximum attainable charge output will be cut to 1.1 million electrons since the transfer gate is merely a small section for the horizontal register.

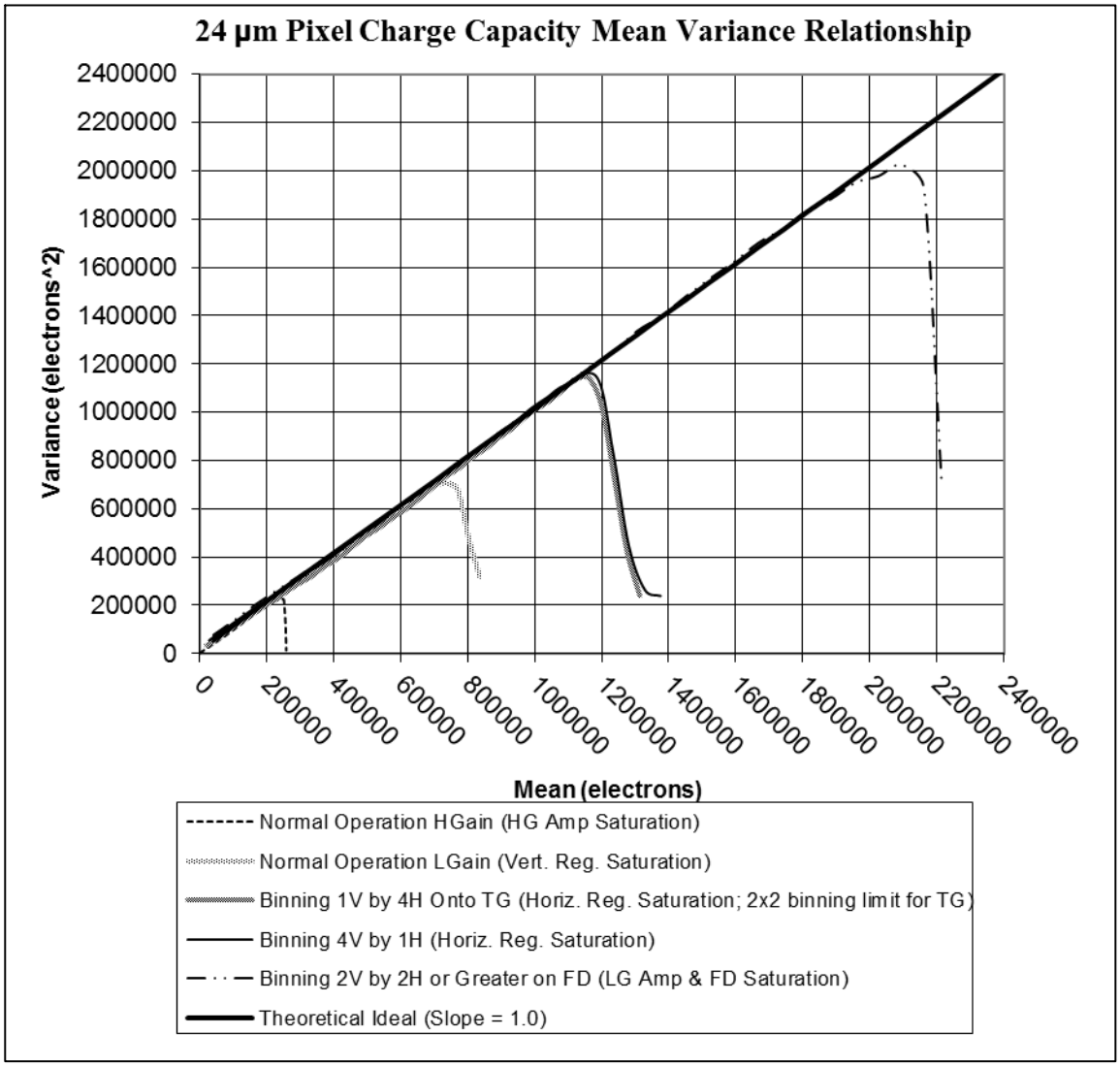

Figure 13. Mean-Variance Plot Showing Charge Capacities of Various Structures Using a 24 µm Pixel Device in Various Modes

Table 1. CHARGE CAPACITY FOR 20 µm PIXEL

Region	Capacity in Thousands of Electrons	Low Gain (2 µV/e−) Output	High Gain (10 µV/e−) Output
Charge Capacity of a Single Pixel (Vertical CCD Register Capacity)	650	1.3 V	2 V (Saturated)
Horizontal CCD Capacity (Including H21/H22)	1100	2.2 V	2 V (Saturated)
Low Gain Amplifier and Floating Diffusion Capacity (Table 1&2 Settings)	1900	3.8 V	2 V (Saturated)
Low Gain Amplifier and Floating Diffusion Capacity at Nominal (KAF Specification) Settings	1080	2.16 V	2 V (Saturated)
High Gain Amplifier and Floating Diffusion Capacity	200	N/A	2 V

Adjusted CCD Settings

Figure 14 shows the Floating Diffusion charge capacity just before saturation with the sensor being operated in 2×2 Binning mode at the nominal values according to the device specification.

The floating diffusion output node capacity depends on several variables, namely VRD, VOG and the Reset clock. At the nominal settings suggested in the CCD performance specifications, the output node capacity, Qtot, is about the same as the Horizontal CCD capacity. In order to increase the charge capacity, Qtot, of the floating diffusion output node, the floating diffusion well depth must be increased. This is achieved by making VOG less positive and making VRD more positive. The low level of the Reset clock must also be made less positive.

When adjusting VRD more positive to 13.5 V, VDD must be moved to 17 V to maintain a linear behavior throughout a 3.8 V dynamic range. In addition, VOG should be moved less positive to 3 V and the low level of the Reset clock voltage swing should be lowered to 4 V. These changes allow for a floating diffusion charge capacity of 1,900,000 electrons on 24 μm pixel devices.

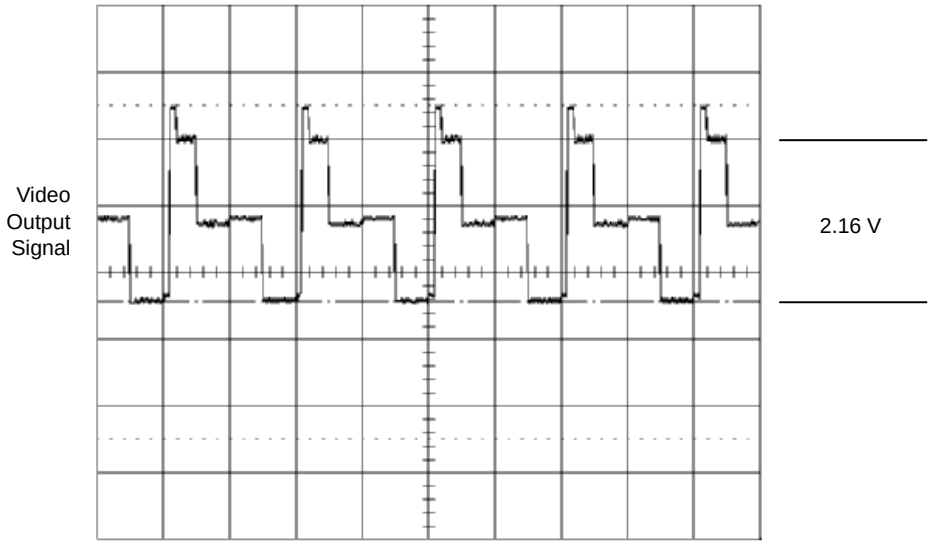

Figure 14. Floating Diffusion Charge Capacity (Nominal Settings)

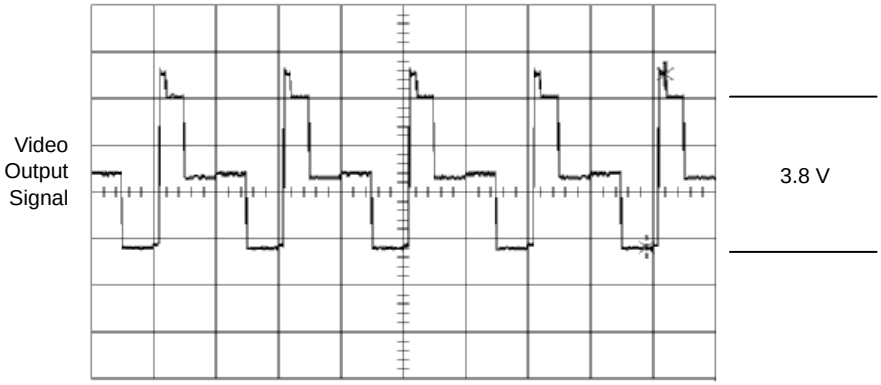

Figure 15. Floating Diffusion Capacity after VRD, VOG, Reset Adjustments

SATURATED VIDEO OUTPUT SIGNAL

When operating a CCD in binning mode, particularly when using the floating diffusion, saturation can occur earlier than expected. This section outlines various early-saturation symptoms and methods for solving the problem.

Charge is dumped onto the Floating Diffusion (FD) on the falling edge of H2. If enough electrons are present, they can flow back over the output gate if VOG is set too positive. Figure 16 illustrates the effect this has on the video output: because the image sensor has been uniformly illuminated, the second step should be same as the first, but due to saturation, the first step is very large but the second is reduced by the VOG resulting in a much smaller step .

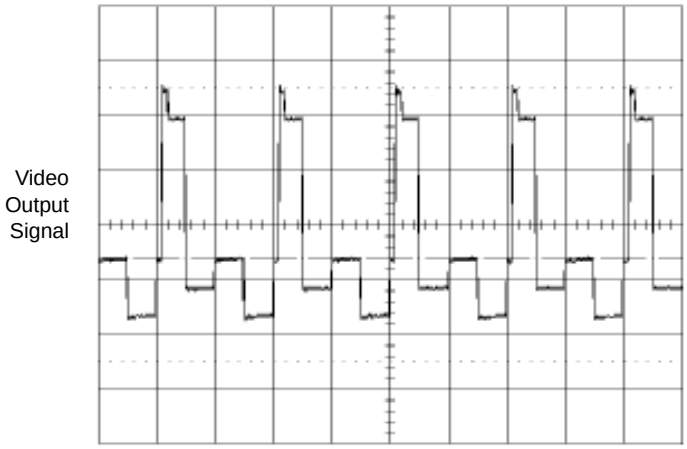

Figure 16. Output Video when Charge Flows Back Over the Output Gate

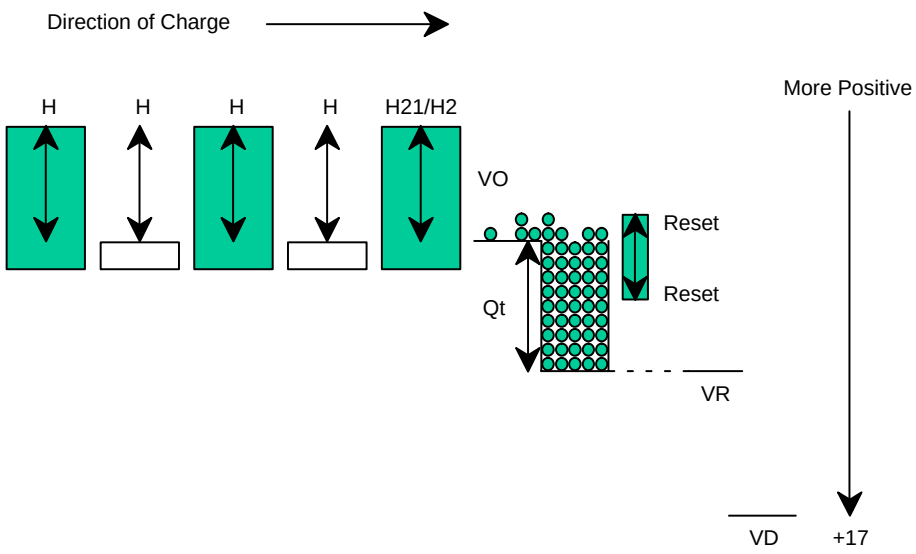

Figure 17. Charge Flowing Back over VOG when the Floating Diffusion Capacity is Reached

Another problem that can occur if enough electrons are present is that they can flow over the Reset Gate if the low level of the Reset clock is not set low enough. Figure 18 illustrates the effect this has on the video output. Because the sensor is being uniformly illuminated, each of the two steps (pixels) in the waveform should be approximately equal. The floating diffusion output node is saturated however, and electrons are being lost over the Reset Gate, and the second step can be seen to be less than the first step (See Figure 19).

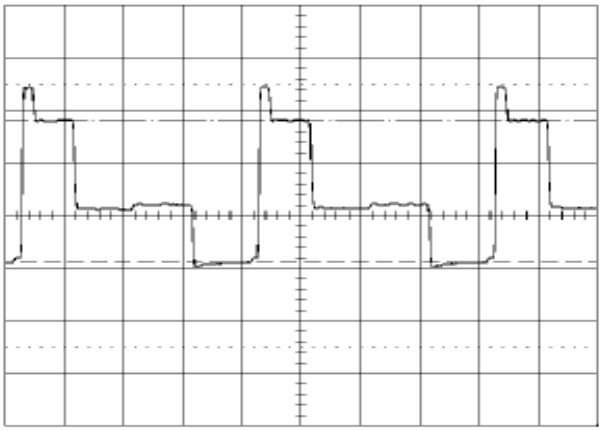

Figure 18. Charge Lost Over the Reset Gate

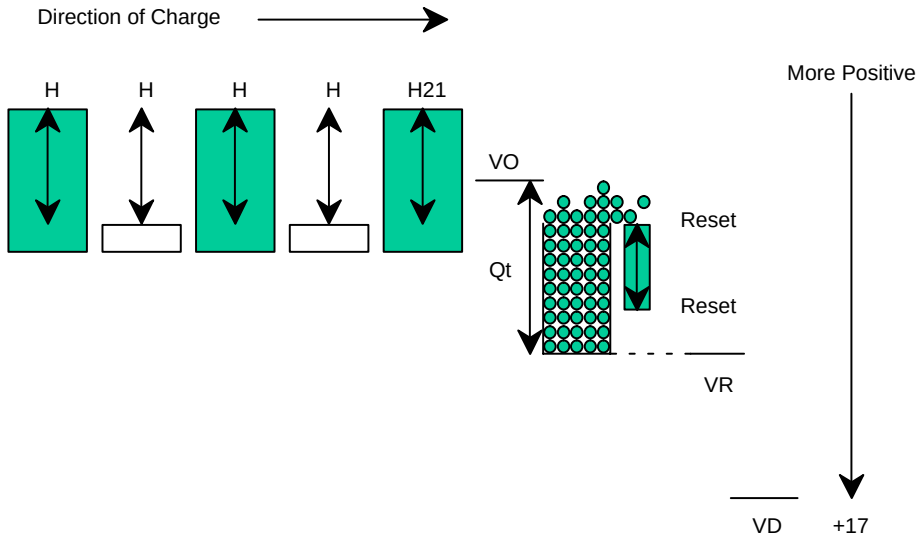

Figure 19. Charge Lost Over the Reset Gate

BIAS RECOMMENDATIONS WHEN BINNING

Based on the discussion presented in the last section, the standard operating voltages may be modified to create a larger output amplifier capacity. The tolerance on these voltages is reduced and may have to be adjusted for each individual sensor.

The recommended CCD settings for operating 24 μm Pixel Full Frame CCD sensors in binning applications are shown below. Bold type indicates possible deviation from the nominal setting in the Device Performance Specifications.

Table 2. DC OPERATING RECOMMENDATIONS FOR BINNING OPERATION

Input Pin/s	DC Voltage (V)
VRD	13.5
VSS	2
VDD	17
VSUB	0
VOG	4
LOD/GAURD	10

Table 3. AC OPERATING RECOMMENDATIONS FOR BINNING OPERATION

Input Pin/s	Low Voltage (V)	High Voltage (V)
V1	−9	1
V2	−9	1
H1	−2	8
H2	−2	8
H21	−3	8
H22	−3.5	−3.5
Reset	4	10

SUMMARY

ON Semiconductor large pixel CCDs may be operated in binning by binning on the floating diffusion or by binning on the transfer gate. In addition to the timing requirements of the specific binning mode operation bias voltages need to be adjusted in order to achieve the maximum charge capacity at the output. The mode of operation and the output amplifier to be used may be determined by the demands for CCD sensitivity, noise, and dynamic range. While binning on the transfer gate provides for potential noise advantages over binning on the floating diffusion, the method has limited charge capacity compared to using the FD. In general large pixel CCDs provides the user with a high level of flexibility that allows each Image Sensor to be tailored to meet the needs of many applications.

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