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An Introduction to LDO Early Warning Function

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APPLICATION NOTE

Abstract

In today's world of high speed, high power processors, new demands have been placed on the power source regulator. One example is the need to inform the processor in advance of an impending drop in supply voltage below a critical value. A common supervisory feature found in automotive LDOs is the Reset signal. When the input voltage is disconnected or lower than minimum operating voltage, the output voltage of regulator will decreases below the reset function threshold and the LDO activates a processor reset output. When an unanticipated Reset signal is received by the processor, important data is often lost because it has no time to save that data.

This application note describes in detail the LDO Early Warning feature, which prevents the aforementioned loss of data by monitoring the input voltage and warning the processor in advance of an impending condition where a Reset signal will occur.

Introduction

Low−dropout ("LDO") series regulators are often selected to power microprocessor (μP) devices in critical systems. LDO devices designed for these applications typically include a logic−level Reset output to interface with the processor. When the regulator output voltage is within tolerance limits, the Reset output will be high. When the output voltage falls below a preset or user−programmed level, either due to overload or low input voltage, the Reset output is asserted low. Often, assertion of the Reset output is delayed by interposing a timer between the comparator and output. The delay timer provides immunity to transient events that will not pose a threat to the system. Figure 1 depicts the block diagram and operating input−output waveforms of a basic LDO series regulator with Reset function.

Despite the control advantages afforded by LDO devices with integrated Reset functions, they may not protect the system against all potential consequences of loss or interruption of the regulator input voltage. If the input voltage drops below the minimum level required to maintain the output in regulation, an unanticipated Reset output state change can occur, which may reset the processor before critical data has been saved and/or benign system conditions established.

Figure 2 represents a graphical depiction of this scenario. LDO input voltage, output voltage, and Reset output (RO) are all plotted as a function of time during an input voltage ramp down. As input voltage decays, three distinct operational regions are encountered:

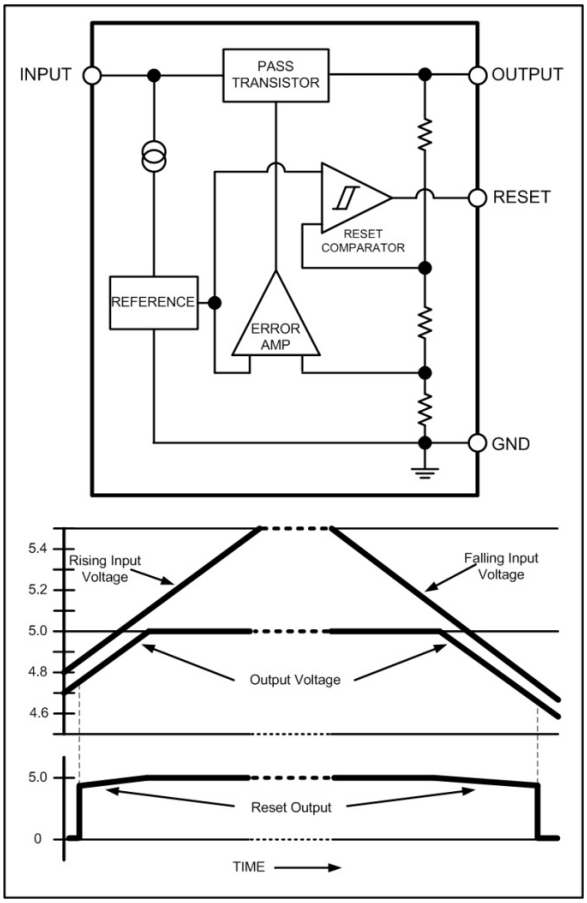


Figure 1. Basic LDO with Reset

Regulation region. Here, the input−output differential voltage ($V_{IN} - V_{OUT}$) exceeds the LDO maximum dropout voltage and Vout is relatively independent of Vin.

Pre−dropout region. This region, which begins approximately where the decaying input−output differential voltage crosses the LDO maximum dropout voltage, is characterized by degraded line regulation. Vout may remain within the specified tolerance band, but exhibits a marked V_{IN} dependence.

Dropout region. From this point onward, the LDO is in dropout and Vout falls in lockstep with decaying V_{IN}. The LDO output is no longer in regulation and RO is asserted.

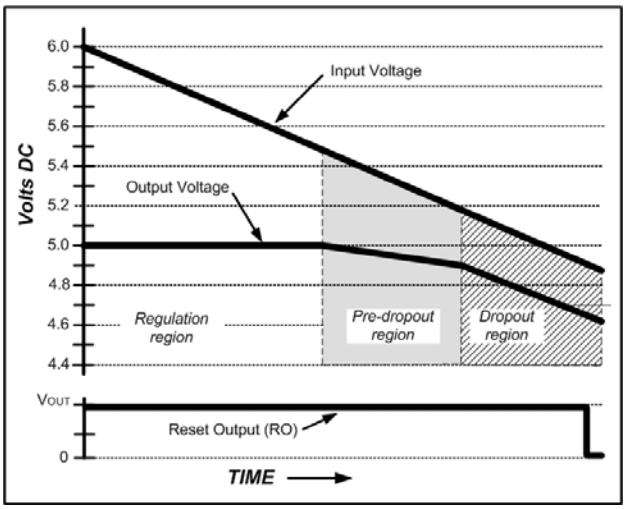


Figure 2. LDO Reaction to Decaying Input Voltage

One practical solution to this problem is the detection of V_{IN} approaching the pre−dropout region, combined with an additional logic path between LDO and processor. This logic output allows the LDO regulator to provide the host processor with early warning of an impending unplanned assertion of the Reset output.

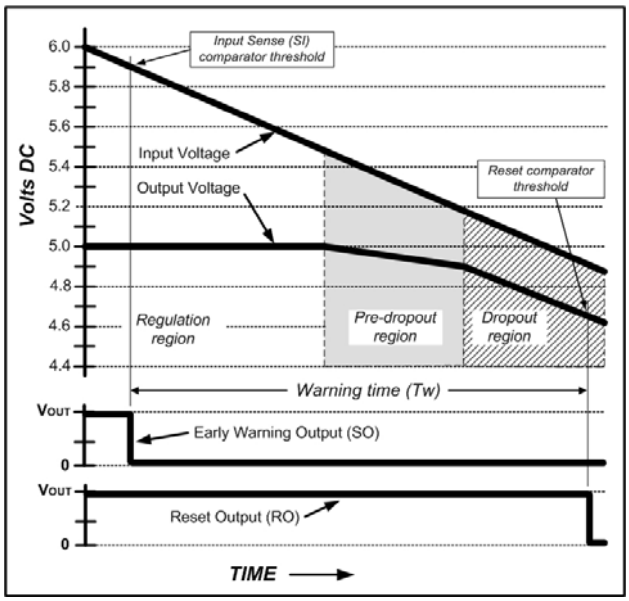
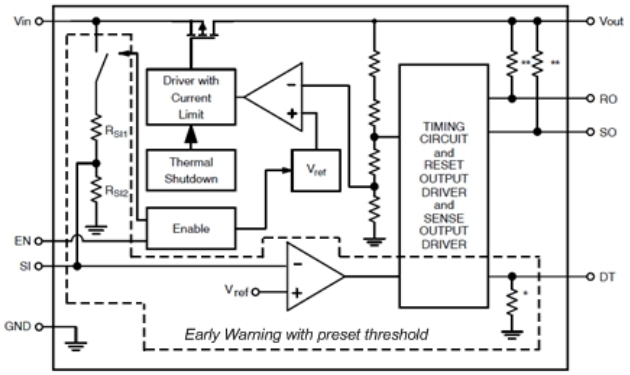


Figure 3. Early Warning Implemented by Input Voltage Detection

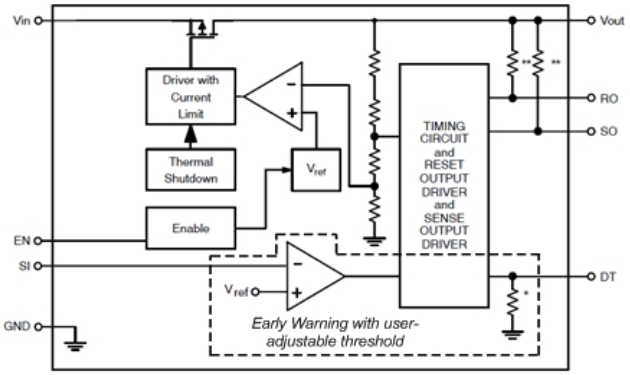
The processor can then be programmed to implement appropriate countermeasures to prevent loss of data or other undesirable consequential events. LDO regulator devices are now available with an integrated Early Warning V_{IN} monitoring function, typically consisting of a reference, comparator, and logical output driver.

Figure 3 describes the operating characteristics of this feature during decay on the regulator input voltage, Vin. For this example, the input voltage sense (early warning) output SO is designed to change state as V_{IN} crosses 5.9 V, and the Reset output (RO) is designed to change state when the regulator output voltage crosses 4.65 V. The consequential Warning time (labeled Twarning) is a direct function of the difference between the SI and Reset thresholds, and an inverse function of the rate of regulator input voltage decay.

Figures 4a and 4b depict simplified block diagrams of an LDO regulator product family with integral early warning function, the NCV8667. In both figures, the elements that comprise the early warning function are outlined by a dashed line. The early warning input pin is labeled SI (sense in) and the early warning output logic−level pin is labeled SO (sense out).



(4a)



(4b)

Figure 4. LDO Devices Incorporating an Early Warning Function

The regulator of Figure 4a includes an internal resistor divider to scale the input sense (SI) threshold, whereas the regulator of Figure 4b does not. With the latter device, an external resistor divider is required to set the threshold. The internal divider resistance of 1 MΩ can achieve a lower quiescent current contribution than practical values of precision external resistors, and is switched out when the regulator is not enabled, markedly reducing standby current.

New EW resistor divider idea

Consider Adjustable Early Warning Threshold option where is the EW threshold is adjusted by external EW resistor divider as shown in Figure 5. The values for R_{SI1} and R_{SI2} are selected for a typical threshold (i.e. 1.25 V) on the SI pin according to eq.1 and eq.2 where $V_{in\_EW(th)}$ is demanded value of input voltage at which Early Warning signal has to be generated. The higher the values of resistors R_{SI1} and R_{SI2} are, the lower is current flowing through the resistor divider. Because the divider is put outside the chip more quiescent current flows from the battery. The values of resistors are usually limited to few hundreds of kilohms (i.e. 200 kΩ or 250 kΩ).

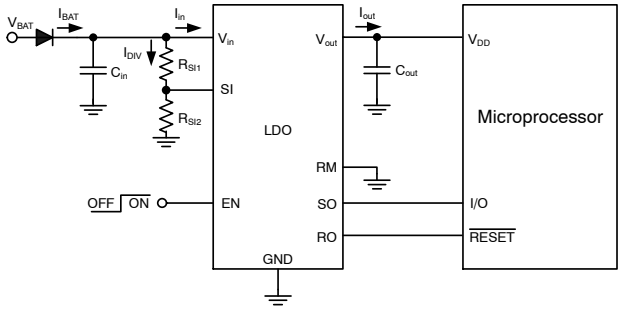


Figure 5. An LDO with External EW Divider

$$V_{in\_EW(th)\_Low} = 1.25\left(1 + \frac{R_{SI1}}{R_{SI2}}\right) \quad \text{(eq. 1)}$$

$$R_{SI1} = R_{SI2}\left(\frac{V_{in\_EW(th)\_Low}}{1.25} - 1\right) \quad \text{(eq. 2)}$$

The benefit of internal EW resistor divider is shown in following example. There is an LDO with external EW divider shown in Figure 5 and NCV8667 with internal EW divider shown in Figure 6.

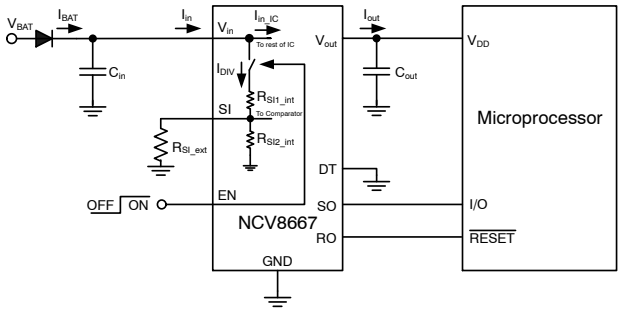


Figure 6. NCV8667 with Internal EW Divider

Application Quiescent Current Reduction

If $V_{in\_EW\_th}$ is required to be set to 5.9 V using an Ultra Low I_q LDO with external EW resistor divider then:

R_{SI1} = 200 kΩ R_{SI2} = 51 kΩ

$I_{BAT} = I_{DIV} + I_{in}$ = 52.6 μA + 28 μA = 80.6 μA

* I_{DIV} is current flowing through external EW resistor divider, I_q is quiescent current of an LDO

The advantage of an internal (on chip) EW resistor divider is that these resistor values can be significantly higher than external resistors and hence, lower quiescent current from batter. In the NCV8667/69 family the total internal EW divider resistance value is 1 MΩ (i.e. R_{SI_int1} = 480 kΩ and R_{SI_int2} = 520 kΩ).

If $V_{in\_EW\_th}$ is required to be set to 5.9 V using NCV8667 with internal EW divider only one external resistor R_{SI_ext} is required:

R_{SI_ext} = 150 kΩ

$I_{BAT} = I_{in} = I_{DIV} + I_{in\_IC}^{*}$ = 50.6 μA

* I_{DIV} includes current flowing through EW resistor divider including also R_{SI_ext} current, I_{in_IC} is quiescent current of the rest of IC @Vin = 13.2 V

The quiescent current from battery is 30 μA lower when the EW resistors are internal comparded to when they are external.

Application Shutdown Current Reduction

Quiescent current savings become more apparent in shutdown mode. During shutdown, the internal EW resistor divider of the NCV8667 is disconnected from battery via an internal switch.

$I_{BAT} = I_{DIV} + I_{DIS}$ = 52.6 μA + 1 μA = 53.6 μA

* I_{DIV} is current flowing through external EW resistor divider, I_{DIS} is shutdown current of an LDO

In case of NCV8667 there is no current flowing through the EW resistor divider because it is disconnected from supply by an internal switch and then:

$I_{BAT} = I_{DIV} + I_{DIS}$ = 0 μA + 1 μA = 1 μA

* I_{DIV} is current flowing through internal EW resistor divider (~0 μA in shutdown mode), I_{DIS} is shutdown current

The difference is 52.6 μA which is significant reduction of battery current in shutdown mode.

Setting EW threshold using R_{SI_ext}

Preset Early Warning Threshold options can be adjusted externally using R_{SI_ext} resistor connected between input monitor SI and GND as shown in Figure 6. The value for R_{SI_ext} is recommended to be selected in range from 50 kΩ to 250 kΩ and the voltage of EW threshold can be set according to Figure 7. The higher the R_{SI_ext} resistance is the lower the overall Quiescent Current of the application (see Figure 8) is. General formulas for calculation of $V_{in\_EW(th)\_L}$ and R_{SI_ext} for selected preset Early Warning options are described by eq.3 and eq.4.

$$V_{in\_EW(th)\_Low} = 1.1\left(1 + \frac{R_{SI1} \times \left(R_{SI2} + R_{SI\_ext}\right)}{R_{SI2} \times R_{SI\_ext}}\right) + 0.25 \quad \text{(eq. 3)}$$

$$R_{SI\_ext} = 1.1\left(\frac{R_{SI1} \times R_{SI2}}{R_{SI2} \times V_{in\_EW(th)\_Low} - 0.25) - 1.1 \times 10^{6}}\right) \quad \text{(eq. 4)}$$

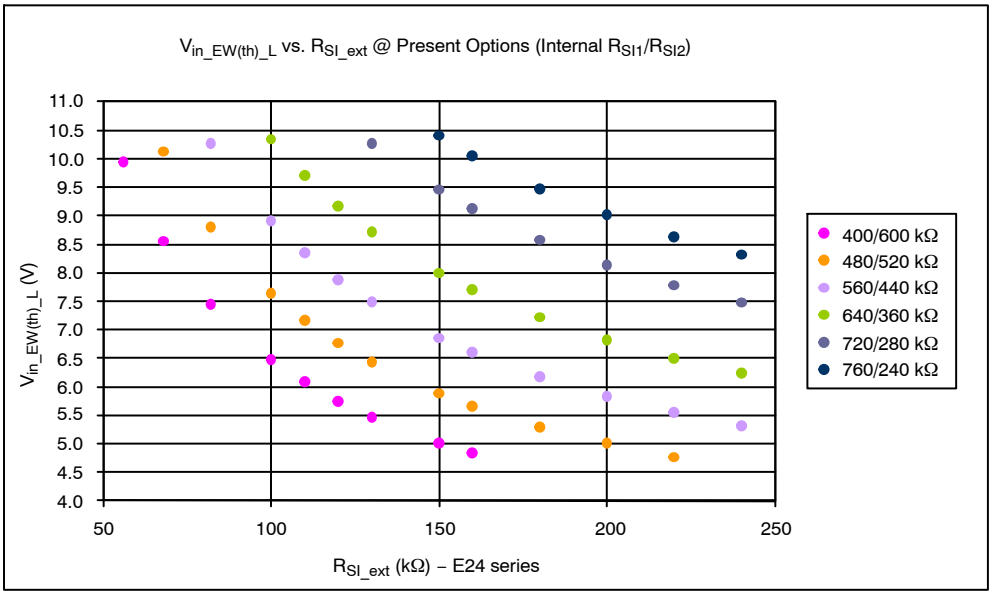


Figure 7. Input Voltage EW Threshold Low vs. R_{SI_ext} (calculated using E24 series)

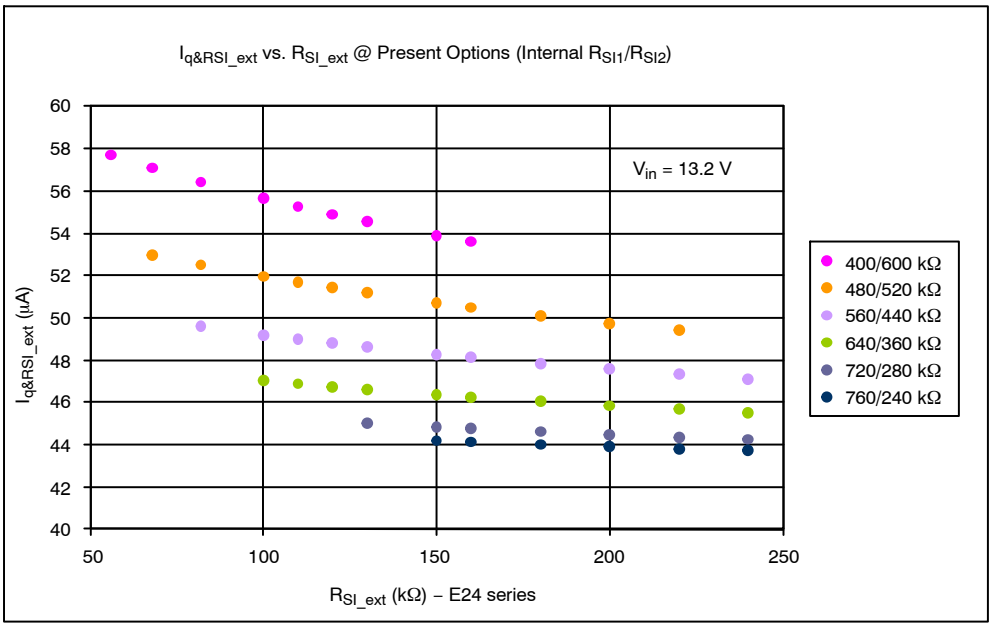


Figure 8. Quiescent Current vs. R_{SI_ext} (calculated using E24 series)

$T_{warning}$ Calculation

The EW function can be used for checking minimum supply voltage required for reliable operation of the NCV8667. An on−chip comparator is available to provide the special signal to microprocessor. If the battery is decreasing (e.g. supply connector disconnection) the uP receives the information via SO signal which can be processed by dedicated DI pin of the uP. EW topology is illustrated in Figure 9.

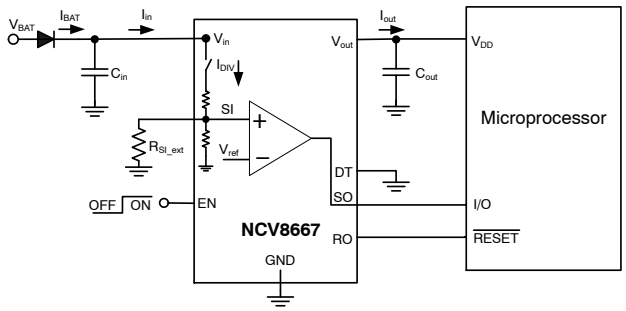


Figure 9. Early Warning Application Circuit

The early warning function compares a voltage defined by the user to an internal reference voltage (i.e. 1.25 V). Therefore the supervised voltage has to be scaled down by external or internal voltage divider in order to compare it. The timing of EW is shown in Figure 10.

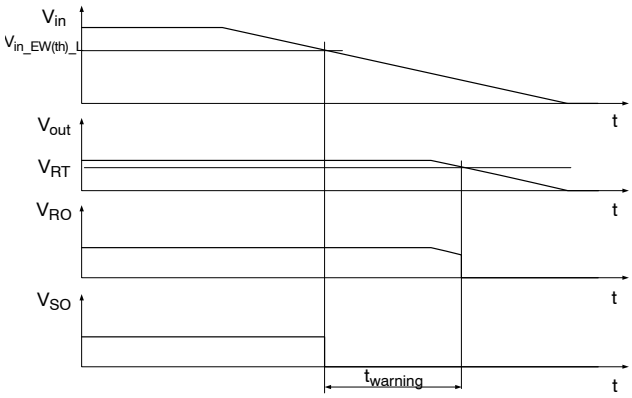


Figure 10. Early Warning Timing

When the input voltage decreases below preset EW threshold then SO output goes low. The input voltage drops continuously further and when output voltage decreases below reset threshold then RO output goes low as well causing uP reset. The time between assuring SO Low and RO Low is called $T_{warning}$ and provides to uP time to finish necessary tasks before ressiting. $T_{warning}$ time can be calculated by eq.5.

$$T_{warning} = \frac{\left(V_{in\_EW(th)\_Low} - V1\right).Cin}{Iout} + \frac{Ln\left(\frac{Vrt - V1 + IoutR - \frac{I}{Cout}}{\frac{1}{Cout}\left(\frac{Iout(RCout-1)}{RCout}\right)}\right)}{-\frac{Cin+Cout}{RCinCout}}$$

(eq. 5)

More details related to $T_{warning}$ calculation are shown in the Appendix 1. The $T_{warning}$ time depends on input and output capacitors values, EW threshold value and output load current. For better understanding see simplified schematic in Figure 11.

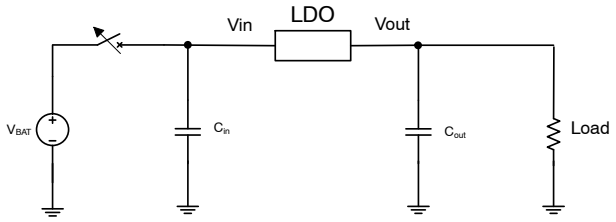


Figure 11. Simplified Schematic for $T_{warning}$ Calculation

Operating Conditions:

V_{in} = 13.2 V
$V_{EW\_th\_l}$ = 5.89 V
V_{rt} = 4.65 V
C_{in} = 4.7 μF
C_{out} = 1 μF
I_{out} = 10 mA

Using eq.5 for calculation the $T_{warning}$ is 890 ms.

For determination of $T_{warning}$ also PSpice model of NCV8667[2] can be used. The schematic and simulation results for $T_{warning}$ can be seen in Figure 12 and Figure 13.

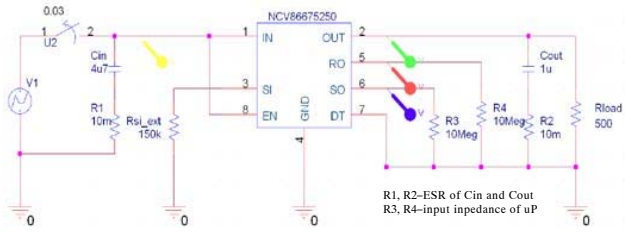


Figure 12. Simplified Schematic for $T_{warning}$ Calculation

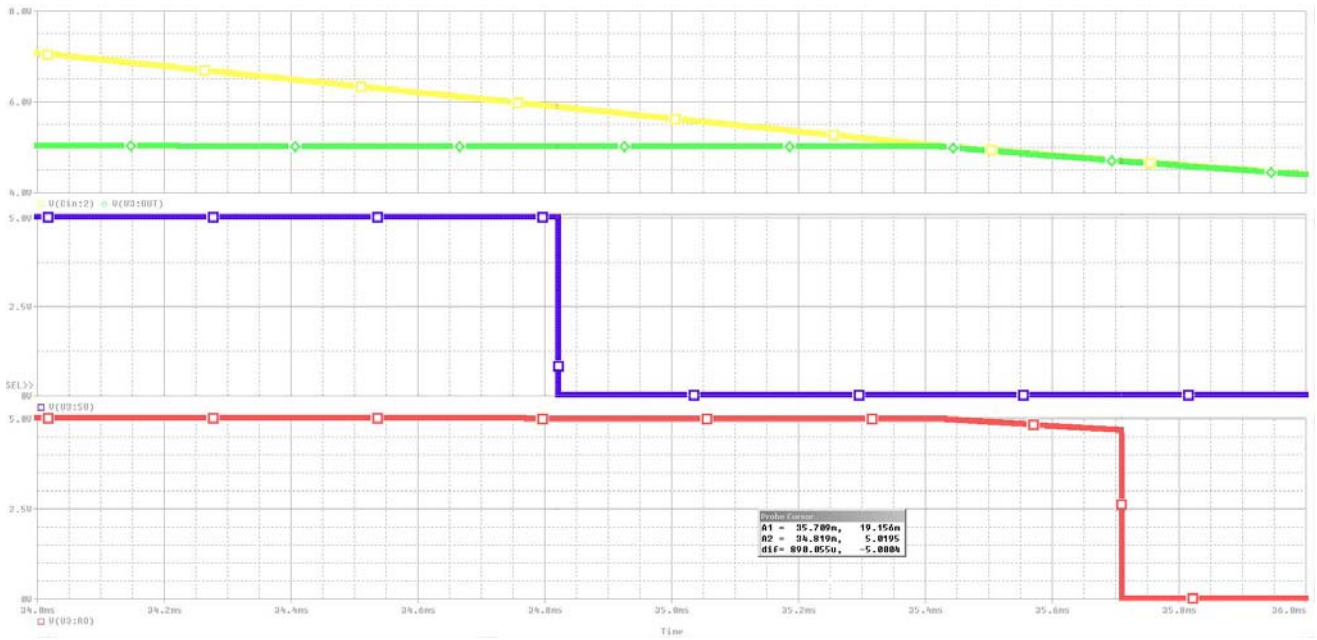


Figure 13. PSpice Simulation Results for $T_{warning}$

Conclusion

The NCV8667/69 families bring significant reduction of both quiescent and shutdown currents in the battery supplied applications, and hence, enable longer battery life thanks to unique idea of internal EW resistor divider and internal disconnect switch.

The EW threshold can be adjusted with just one external resistor which saves number of components required for EW function and space on PCB.

Reference:

1. NCV8667 datasheet
http://www.onsemi.com/pub_link/Collateral/NCV8667−D.PDF
2. PSpice model
http://www.onsemi.com/PowerSolutions/supportDoc.do?type=models&rpn=NCV8667

APPENDIX 1: CALCULATION OF $T_{warning}$

Schematic:

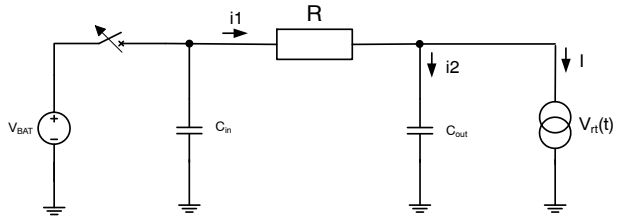


Figure 14.

Step 1: Regulation and Pre−dropout region

$\Delta V = V_{in\_EW(th)\_Low} - V_1$ (Input voltage before dropout)

Then $V_1 = V_{out} + V_{DO}$

$t1 = \Delta V \cdot C_{in}/I$

And $I = I_{out} + I_q$

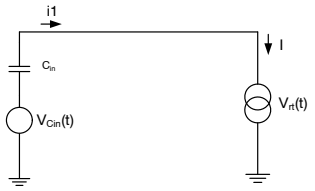


Figure 15.

$$t1 = \frac{\left(V_{in\_EW(th)\_Low} - V1\right).Cin}{I}$$

Step 2: Dropout region

$\Delta V = 5.3\ V - V_{rt}$ (typ. 4.75 V)

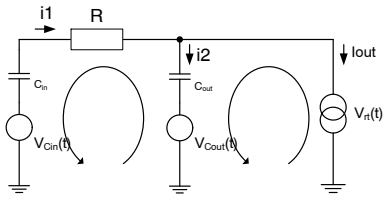


Figure 16.

$V_{Cin}(0) = V1$

$V_{Cout}(0) = V1 - IR$

$Iout = i1 + i2$

$$1.\quad i1(p)R + \frac{i1(p)}{pCin} + \frac{V1}{p} - \frac{V1}{p} + \frac{IR}{p} - \frac{i2(p)}{pCout} = 0,$$

$$i2(p) = Iout - i1(p)$$

$$i1(p)\left(R + \frac{1}{pCin} + \frac{1}{pCout}\right) + Iout\left(\frac{R}{p} - \frac{1}{pCout}\right) = 0$$

$$i1(p)\left(R + \frac{1}{pCin} + \frac{1}{pCout}\right) + Iout\left(\frac{R}{p} - \frac{1}{pCout}\right) = 0 \Rightarrow$$

$$i1(p) = \frac{-\ Iout(RCout - 1)}{RCout\left(p + \frac{Cin + Cout}{RCinCout}\right)}$$

$$\frac{1}{p + a} \leftrightarrow e^{-at}$$

$$i1(t) = \frac{-\ Iout(RCout - 1)}{RCout}\ e^{\frac{Cin + Cout}{RCinCout}t2}$$

$$i2(t) = Iout - i1(t)$$

$$2.\quad \frac{1}{pCout}\ i2(p) + \frac{V1}{p} - \frac{IR}{p} - \frac{Vrt}{p} = 0 \Rightarrow$$

$$Vrt(t) = \frac{1}{Cout}\ i2(t) + u1(t) - IoutR$$

$$Vrt(t) = \frac{1}{Cout}\left(I - \frac{-\ Iout(RCout - 1)}{RCout}\ e^{\frac{Cin + Cout}{RCinCout}t2}\right) + V1(t)$$

$$\frac{Vrt - V1 + IoutR - \frac{1}{Cout}}{\frac{1}{Cout}\left(\frac{Iout(RCout - 1)}{RCout}\right)} = e^{\frac{Cin + Cout}{RCinCout}t} \Rightarrow t2$$

$$\frac{Ln\left(\frac{Vrt - V1 + IoutR - \frac{1}{Cout}}{\frac{1}{Cout}\left(\frac{Iout\ (RCout - 1)}{RCout}\right)}\right)}{\frac{Cin + Cout}{RCinCout}} = t2$$

$$T_{warning} = t1 + t2$$

$$T_{warning} = \frac{\left(V_{in\_EW(th)\_Low} - V1\right).Cin}{Iout} + \frac{Ln\left(\frac{Vrt - V1 + IoutR - \frac{I}{Cout}}{\frac{1}{Cout}\left(\frac{Iout(RCout - 1)}{RCout}\right)}\right)}{-\ \frac{Cin + Cout}{RCinCout}}$$

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