SEPIC Converter Analysis and Design

AND90136/D

Introduction

The single-ended primary-inductor converter (SEPIC) is a type of DC/DC converter that allows the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input. The SEPIC converter is controlled by the duty cycle of the main switch Q1.

Like other DC–DC switch-mode power supply converters, the SEPIC exchanges energy between inductors and capacitors to convert from one voltage to another voltage. Typical applications for a SEPIC regulator are [1]:

- Battery-operated equipment and handheld devices
- NiMH chargers
- LED lighting applications
- DC power supplies having a wide range of input voltages

Any boost controller (External FET) or converter (Internal FET) can be used to control a SEPIC regulator. We will focus on a SEPIC controller for the rest of this document. In figure (1) we have represented the SEPIC controller with separate inductors, however these inductors can be coupled inductors (see Appendix A). A simplified schematic for a SEPIC regulator is shown in figure (1).

![Figure 1. SEPIC Converter](image)

When transistor Q1 is conducting, the input inductor L1 is charged by the input voltage $V_{in}$. Inductor L2 takes energy from the coupling capacitor Ccp. The output current to the load is supplied by capacitor Cout. The simplified schematic while Q1 is conducting (ON state) is shown below in figure (2).

![Figure 2. SEPIC Converter during ON State](image)
Depicted below in figure (3) is the simplified schematic when transistor Q1 is off. When the main switch Q1 is off, the diode is conducting and inductor L1 charges the coupling capacitor Ccp. The currents through inductor L1 and inductor L2 provide current to the output capacitor Cout and the load.

Figure 3. SEPIC Converter during OFF State

Figure 4. Steady State Waveforms for a SEPIC Converter in CCM Mode. $v_{Q1}$ is the Drain to Source ($V_{DS}$) of Transistor Q1.
**Duty Cycle**

The voltage across inductor L1 (assuming no Ohmic losses in the inductor) is shown below in figure (5):

![Figure 5. Voltage across Inductor L1](https://via.placeholder.com/150)

Applying Volt–Second balance on inductor L1 we arrive at:

\[
\frac{1}{T_{sw}} \left[ \int_{0}^{DT_{sw}} V_{in} dt + \int_{DT_{sw}}^{T_{sw}} (V_{in} - V_{Ccp} - V_{D} - V_{out}) dt \right] = 0
\]

\[
= DT_{sw}V_{in} + (1 - D)T_{sw}(V_{in} - V_{Ccp} - V_{D} - V_{out}) \quad (\text{eq. 1})
\]

Given that the average voltage across inductors L1 and L2 equals 0, the average voltage across the coupling capacitor \(V_{Ccp} = V_{in}\). Replacing \(V_{Ccp}\) with \(V_{in}\) in equation (1) yields:

\[
DV_{in} + (1 - D)(-V_{D} - V_{out}) = 0
\]

Therefore:

\[
\frac{D}{1 - D} = \frac{V_{out} + V_{D}}{V_{in}}
\]

Or:

\[
D = \frac{V_{out} + V_{D}}{V_{in} + V_{out} + V_{D}}
\]

Where \(V_{D}\) is the diode forward voltage. From equation (3) we notice that the maximum duty cycle occurs at \(V_{in}\) and the minimum duty cycle occurs at \(V_{in,max}\). If we ignore the diode drop, we arrive at the ideal duty cycle for the regulator:

\[
D_{ideal} = \frac{V_{out}}{V_{in} + V_{out}}
\]

**Relationship between Input and Output Current**

![Figure 6. Capacitor Ccp, Currents](https://via.placeholder.com/150)
When Q1 is conducting, the coupling capacitor C\text{cp} discharges through L2 therefore the capacitor current varies from \( -I_{L2,\text{valley}} \) to \( -I_{L2,\text{peak}} \) as shown in figure (6). Similarly, when Q1 is off and the diode is conducting, the current through the coupling capacitor C\text{cp} varies from \( I_{L1,\text{peak}} \) to \( I_{L1,\text{valley}} \) as shown in figure (6). Applying Ampere second balance on capacitor C\text{cp} yields:

\[
\frac{1}{T_{\text{sw}}} \left[ \int_{0}^{T_{\text{sw}}} -\left( I_{L2,\text{valley}} + \frac{di_{L2}}{dt} (t - 0) \right) dt + \int_{T_{\text{sw}}}^{T_{\text{sw}}} \left( I_{L1,\text{peak}} - \frac{di_{L1}}{dt} (t - DT_{\text{sw}}) \right) dt \right] = 0
\]

\[
= \frac{1}{T_{\text{sw}}} \left[ \int_{0}^{T_{\text{sw}}} -\left( I_{L2,\text{valley}} + \frac{V_{\text{in}}}{L_2} \right) dt + \int_{T_{\text{sw}}}^{T_{\text{sw}}} \left( I_{L1,\text{peak}} - \frac{V_{\text{out}}}{L_1} (t - DT_{\text{sw}}) \right) dt \right]
\]

\[
= \frac{1}{T_{\text{sw}}} \left[ \int_{0}^{T_{\text{sw}}} -\left( I_{L2,\text{valley}} + \frac{V_{\text{in}}}{L_2} \right) dt + \int_{T_{\text{sw}}}^{T_{\text{sw}}} \left( I_{L1,\text{peak}} + \frac{V_{\text{in}} + V_{\text{out}} DT_{\text{sw}}}{L_1} - \frac{D}{1 - D} \frac{V_{\text{in}}}{L_1} (t - DT_{\text{sw}}) \right) dt \right]
\]

\[
= -DT_{\text{sw}} \left( I_{L2,\text{valley}} + \frac{V_{\text{in}} + V_{\text{out}} DT_{\text{sw}}}{2L_2} \right) + (1 - D)T_{\text{sw}} \left( I_{L1,\text{valley}} + \frac{V_{\text{in}} + V_{\text{out}} DT_{\text{sw}}}{2L_1} \right)
\]

\[
= -DT_{\text{sw}} \left( I_{L2,\text{valley}} + \frac{I_{L1,\text{p2p}}}{2} \right) + (1 - D)T_{\text{sw}} \left( I_{L1,\text{valley}} + \frac{I_{L1,\text{p2p}}}{2} \right)
\]

(eq. 5)

Where \( I_{L1,\text{p2p}} \) is the peak to peak inductor current.

From equation (5), \( \left( I_{L2,\text{valley}} + \frac{I_{L1,\text{p2p}}}{2} \right) \) is equal to the average current through inductor L2 (\( I_{L2} \)). Following the same approach for inductor L1 we conclude that \( \left( I_{L1,\text{valley}} + \frac{I_{L1,\text{p2p}}}{2} \right) \) is the average current through inductor L1 (\( I_{L1} \)). Therefore:

\[
-I_{L2} + (1 - D)I_{L1} = 0
\]

\[
\frac{I_{L1}}{I_{L2}} = \frac{D}{1 - D}
\]

(eq. 6)

At this point we have found a relationship between the average inductor currents. Assuming 100% efficiency we arrive at the following expression:

\[
\begin{align*}
V_{\text{out}} &= V_{\text{in}} \\
\frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{I_{L1}}{I_{\text{out}}} = \frac{I_{L1}}{I_{L2}} = \frac{D_{\text{ideal}}}{1 - D_{\text{ideal}}} \quad \text{(eq. 7)}
\end{align*}
\]

Using equation (2) and (7) the relationship between the average input and output currents can be expressed as:

\[
I_{\text{in}} = \frac{D_{\text{ideal}}}{1 - D_{\text{ideal}}} \quad I_{\text{out}} \quad \text{and} \quad \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{I_{\text{out}}}{V_{\text{in}}} \quad \text{(eq. 8)}
\]

**Inductor selection**

When Q1 is conducting, the voltage across the inductor L1 equals:

\[
v_{L1} = L_1 \frac{di_{L1}}{dt}
\]

(eq. 9)

Where \( f_{\text{sw}} \) is the switching frequency of the regulator and is defined as:

\[
f_{\text{sw}} = \frac{1}{T_{\text{sw}}}
\]

(eq. 14)

To design the SEPIC regulator we need to define the maximum allowed ripple in the inductors. A good rule of thumb is to use 20% to 40% of the input current. Assuming the allowed ripple through both inductors is 20% we arrive at the following expression:

\[
\Delta I_L = I_{L1,\text{p2p}} = I_{\text{in}} \times 20\%
\]

(eq. 15)
Solving equation (15) in terms of the output current $I_{out}$ yields:

$$\Delta I_L = I_{out} \frac{V_{out}}{V_{in(min)}} \times 20\%$$  \hspace{1cm} (eq. 16)

Using equation (13), the inductor value can be calculated as:

$$L_1 = L_2 = L = \frac{V_{in(min)}}{\Delta I_{fsw}} D_{max}$$  \hspace{1cm} (eq. 17)

If inductors L1 and L2 are coupled inductors, the value of the inductance required is half of what would be needed should there be two separate inductors [2]. Therefore, for coupled inductors the value of inductance required is given by:

$$L_{1a} = L_{1b} = \frac{V_{in(min)}}{2 \Delta I_{LS}} D_{max}$$  \hspace{1cm} (eq. 18)

The peak current in inductor L1 can be expressed as:

$$I_{L1,peak} = I_L + \frac{\Delta I_L}{2}$$  \hspace{1cm} (eq. 19)

$$= I_{in} + \frac{\Delta I}{2}$$

$$= \frac{I_{out} D_{max}}{1 - D_{max}} + \frac{\Delta I_L}{2}$$

$$= \frac{I_{out} D_{max}}{1 - D_{max}} \times \left(1 + \frac{20\%}{2}\right)$$  \hspace{1cm} (eq. 20)

Or in terms of the input and output voltages:

$$I_{L1,peak} = \frac{V_{out} + V_D}{V_{in(min)}} \times \left(1 + \frac{20\%}{2}\right)$$  \hspace{1cm} (eq. 21)

After some algebraic manipulation, the equation for the RMS current is given by:

$$I_{Q1, rms} = \sqrt{\frac{1}{T_{sw}}} \int_0^{T_{sw}} i_{Q1}(t) \, dt$$

$$= \sqrt{(I_{L1,peak} + I_{L2,peak})^2 D_{max} + (I_{L1,peak} + I_{L2,peak})^2}$$

$$\sqrt{2 V_D L_{2max} D_{max} T_{sw} + V_{2in(min)}^2} \frac{4 D_{max}^3 T_{sw}^2}{3}$$  \hspace{1cm} (eq. 29)

Though less accurate, for a quick, back of the envelope calculation, we can ignore the second summand in the expression above which yields:

$$I_{Q1, rms} = \sqrt{D_{max} \left[ \frac{1}{1 - D_{max}} I_{out}^2 \right] + \frac{1}{3} V_{in(min)}^2 \frac{1}{L^2} \frac{1}{D_{sw}}}$$  \hspace{1cm} (eq. 30)

The power losses in the transistor Q1 can be divided into two categories:

1. Conduction Losses
2. Switching or overlap Losses

The total power losses in transistor Q1 are equal to:

$$P_{Q1} = P_{cond} + P_{sw}$$  \hspace{1cm} (eq. 33)

The conduction losses in the transistor is given by:

$$P_{cond} = \frac{I_{Q1, rms}^2 R_{DS(on)} D_{max}}{2}$$  \hspace{1cm} (eq. 34)

The switching losses are approximately equal to,

$$P_{sw} = \frac{1}{2} V_D I_{Q1, peak}(t_{rise} + t_{fall}) f_{sw}$$  \hspace{1cm} (eq. 35)
When Q1 is off, the voltage from drain to source can be calculated using a KVL:
\[ V_{DS} = V_{Ccp} + V_D + V_{out} \] (eq. 36)

Given,
\[ V_{Ccp} = V_{in(max)} \]

Equation (36) can be expressed as,
\[ P_{sw} = \frac{1}{2} (V_{in(max)} + V_D + V_{out}) |Q_{1,peak}| (\tau_{rise} + \tau_{fall}) f_{sw} \] (eq. 38)

Where \( \tau_{rise} \) & \( \tau_{fall} \) are the rise and fall of the gate of Q1 and can be calculated as,
\[ \tau_{rise} = \frac{Q_{gd}}{I_{src}} \] (eq. 39)
\[ \tau_{fall} = \frac{Q_{gd}}{I_{sink}} \] (eq. 40)

\( Q_{gd} \) is the MOSFET Miller plateau voltage gate charge, and \( I_{src} \) and \( I_{sink} \) are the source and sink currents of the gate driver respectively. The \( r_{DS(on)} \) is typically found in the datasheet and should be selected at maximum junction temperature. To ensure proper operation, the selected MOSFET must have:

1. Breakdown voltage > \( V_{in(max)} + V_D + V_{out} \)
2. Continuous current capability > \( I_{Q1(rms)} \)
3. Maximum junction temperature \( T_{j(max)} > P_{Q1} x R_{Q1A} + T_{ambient} \)
4. \( V_{GS} > \) Gate drive voltage

It is important to mention that if a SEPIC converter is used (internal FET) \( I_{Q1(rms)} \) will be the maximum current through the device.

\[ I_{Ccp,rms,max} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_{Ccp}^2(t) \, dt} \] (eq. 45)

For simplicity we have assumed the average current through the inductors. The RMS current can now be expressed as:
\[ I_{Cp, rms, max} = \sqrt{\frac{D_{max}}{1 - D_{max}} \left( \frac{1 - D_{max}}{T_{sw}} \right)} \] (eq. 46)

Employing equation (6), the expression above can be simplified to:
\[ I_{Cp, rms, max} = \frac{I_{out}}{\sqrt{\frac{D_{max}}{1 - D_{max}}}} \] (eq. 47)

Or in terms of the input and output voltages:
\[ I_{Cp, rms, max} = \frac{V_{out} + V_D}{V_{in(min)}} \] (eq. 48)

Diode Selection
To ensure proper operation and avoid damaging the diode, the diode selected must be able to withstand reverse voltages equal to:
\[ V_R = V_{in(max)} + V_{out(max)} \] (eq. 41)

The peak current through the diode is equal to the peak current of transistor Q1 so the diode must be able to handle:
\[ I_{D(peak)} = I_{Q1,peak} = I_{L1,peak} + I_{L2,peak} \] (eq. 42)

There’s also an average current that the diode must be able to withstand:
\[ I_D = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_d(t) \, dt \] (eq. 43)

Last but not least, the conduction loss in the diode is equal to the diode average current times the forward voltage drop in the diode therefore the diode package must be able to dissipate up to:
\[ P_D = I_D V_D (1 - D_{max}) = I_{out} V_D \] (eq. 44)

To improve efficiency (or reduce losses in the diode) a diode with a low forward voltage is recommended. Schottky diodes are a good candidate due to their low forward voltage.

In summary, for proper operation the selected diode must have:

1. Reverse voltage capability ≥ \( V_{in(max)} + V_{out(max)} \)
2. Peak current capability ≥ \( I_{Q1(peak)} \)
3. Average current capability ≥ \( I_D \)
4. Maximum junction temperature \( T_{j(max)} > P_D x R_{Q1A} + T_{ambient} \)

Coupling Capacitor Selection
To calculate the amount of RMS that coupling capacitor \( C_{cp} \) must withstand, we need to calculate the RMS current in the capacitor. The RMS current can be calculated as [3]:
\[ I_{Cp, rms, max} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_{Ccp}^2(t) \, dt + \int_0^{T_{sw}} i_{Ccp}^2(t) \, dt} \] (eq. 45)

The coupling capacitor must be able to handle voltages equal to:
\[ V_{in(max)} \]

The peak-to-peak voltage across the capacitor can be calculated as:
\[ \Delta V_{c_{cp}} = \frac{1}{C_{cp}} \int_0^{T_{sw}} i_d(t) \, dt = \frac{I_{in}(1 - D_{max}) T_{sw}}{C_{cp}} \]
\[ = \frac{I_{out} (1 - D_{max}) T_{sw}}{C_{cp}} \]
\[ = I_{out} D_{max} \frac{f_{sw}}{C_{cp} f_{sw}} \] (eq. 49)
The ripple across the coupling capacitor $C_{cp}$ is determined by its capacitance and its equivalent series resistance (ESR). Assuming a linear relationship between the two sources of ripple we arrive at:

$$\Delta V_{C_{cp}} \leq \frac{i_{out}D_{max}}{C_{cp}f_{sw}} + \text{ESR} \times \max(l_{L1,\text{peak}}, l_{L2,\text{peak}})$$

Thus, the coupling capacitor can be calculated as:

$$C_{cp} \geq \frac{i_{out}D_{max}}{\Delta V_{C_{cp}}f_{sw}} \quad \text{(eq. 50)}$$

Similarly, the maximum ESR can be calculated as:

$$\text{ESR} \leq \frac{\Delta V_{C_{cp}}}{\max(l_{L1,\text{peak}}, l_{L2,\text{peak}})} \quad \text{(eq. 51)}$$

It is recommended to use a ceramic capacitor to keep the ESR losses as small as possible.

**Output Capacitor Selection**

Looking at figure (4), when transistor Q1 is conducting, the current through the output capacitor equals $i_{out}$ since the capacitor is the only element providing current to the output. When transistor Q1 is off the current through the $C_{out}$ is the sum of the inductors $L_1$ and $L_2$ current minus the load current. Assuming average currents for simplicity, the output capacitor RMS current can be expressed as:

$$i_{C_{out},\text{rms,max}} = \sqrt{\frac{1}{T_{sw}} \left[ \int_{0}^{DT_{sw}} i_{out}^2 \, dt + \int_{DT_{sw}}^{T_{sw}} (l_{L1} + l_{L2} - i_{out})^2 \, dt \right]} \quad \text{(eq. 52)}$$

From equation (7) $i_{out} = i_{L2}$ therefore

$$i_{C_{out},\text{rms,max}} = i_{C_{cp},\text{rms,max}} = \sqrt{\frac{1}{T_{sw}} \left[ \int_{0}^{DT_{sw}} l_{L2}^2 \, dt + \int_{DT_{sw}}^{T_{sw}} l_{L1}^2 \, dt \right]} \quad \text{(eq. 53)}$$

Or in terms of the input and output voltages:

$$i_{out} = \sqrt{\frac{V_{out}^2 + V_{D}}{V_{in_{\text{min}}}}} \quad \text{(eq. 54)}$$

The ripple across the output capacitor $C_{out}$, is determined by its capacitance and its equivalent series resistance (ESR). Assuming a linear relationship between the two sources of ripple we arrive at:

$$\Delta V_{C_{out}} \leq \frac{i_{out}D_{max}}{C_{out}f_{sw}} + \text{ESR} \times (l_{L1,\text{peak}} + l_{L2,\text{peak}})$$

Thus, the output capacitor can be calculated as:

$$C_{out} \geq \frac{i_{out}D_{max}}{\Delta V_{C_{out}}f_{sw}} \quad \text{(eq. 55)}$$

Similarly, the maximum ESR can be calculated as:

$$\text{ESR} \leq \frac{\Delta V_{C_{out}}}{l_{L1,\text{peak}} + l_{L2,\text{peak}}} \quad \text{(eq. 56)}$$

It is recommended to use a ceramic capacitor to keep the losses small.

**Input Capacitor**

The input capacitor sees moderately low RMS current thanks to the input inductor. The RMS current in the input capacitor is given by:

$$i_{C_{in},\text{rms}} = \frac{\Delta l_{i}}{\sqrt{12}} \quad \text{(eq. 57)}$$
Design Example
Input voltage: 3.75 – 9.0 V
Output voltage: 5.5 V
Output current: 1.25 A
Frequency: 2 MHz
Assuming a diode drop of 0.5 V
Temperature: 85°C
Device selected onsemi NCV898031

Figure 7. Simplified Application Schematic (Simulation Test Bench)

Step 1: Calculate the Duty Cycle
\[ D_{\text{max}} = \frac{V_{\text{out}} + V_D}{V_{\text{in(min)}} + V_{\text{out}} + V_D} = \frac{5.5 + 0.5}{3.75 + 5.5 + 0.5} = 0.6154 \]
\[ D_{\text{min}} = \frac{V_{\text{out}} + V_D}{V_{\text{in(max)}} + V_{\text{out}} + V_D} = \frac{5.5 + 0.5}{9.0 + 5.5 + 0.5} = 0.4 \]

Step 2: Inductor Selection
Calculate the inductor ripple current:
\[ \Delta I_L = I_{\text{out}} \times 20\% \]
\[ = 1.25 \times \frac{5.5}{3.75} \times 20\% = 0.3667 \text{ A} \]
Now the inductance L1 and L2 can be calculated:
\[ L_1 = L_2 = L = \frac{V_{\text{in(min)}}}{\Delta I_L f_{\text{sw}}} D_{\text{max}} \]
\[ = \frac{3.75}{0.3667 \times 2e6} \times 0.6154 = 3.1469 \mu\text{H} \]

Wurth Elektronik 7447783033: 3.3 μH, 4.1 A, and 18 mΩ is selected for L1 and L2. Based on the inductor selected, we can calculate the actual inductor ripple as:
\[ \Delta I_L = \frac{V_{\text{in(min)}}}{V_{\text{out}}} D_{\text{max}} = 0.3497 \text{ A} \]
\[ \text{Ripple} = \frac{\Delta I_L}{I_{\text{out}}} \times 100 = 19.07\% \]

The peak L1 current can be calculated as:
\[ I_{L1,\text{peak}} = I_{\text{out}} \times \left( \frac{V_{\text{out}} + V_D}{V_{\text{in(min)}}} \right) \times \left( 1 + \frac{19.07\%}{2} \right) \]
\[ = 1.25 \times \frac{5.5 + 0.5}{3.57} \times \left( 1 + \frac{19\%}{2} \right) = 2.1907 \text{ A} \]

And the peak L2 current can be calculated as:
\[ I_{L2,\text{peak}} = I_{\text{out}} \times \left( 1 + \frac{19.07\%}{2} \right) \]
\[ = 1.25 \times \left( 1 + \frac{19\%}{2} \right) = 1.3692 \text{ A} \]
Step 3. Power MOSFET Selection

The peak current through the MOSFET equals:

\[ I_{Q1,peak} = I_{L1,peak} + I_{L2,peak} = 2.1907 + 1.3692 = 3.5599 \, \text{A} \]

Calculate the rms current through the MOSFET:

\[
I_{Q1(rms)} = \sqrt{\frac{D_{\text{max}}}{1 - D_{\text{min}}} \left( \frac{1}{3} I_{Q1,peak}^2 + \frac{1}{3} I_{V_{\text{in}(\text{min})}}^2 \frac{1}{L^2} \frac{D_{\text{max}}^2}{F_{\text{sw}}} \right)}
\]

\[
= \sqrt{0.6154 \times \left( \frac{1}{1 - 0.6154} \times 1.25 \times \frac{3.75^2}{3} + \frac{1}{3.36 - 6^2} \times \frac{0.6154^2}{2e6^2} \right)}
\]

\[ = 2.5544 \, \text{A} \]

Breakdown voltage:

\[ V_{\text{BDSS}} > V_{\text{in}(\text{max})} + V_{\text{out}} + V_D \]

\[ > 9 + 5.5 + 0.5 \]

\[ > 15 \, \text{V} \]

Assuming an \( r_{DS(\text{ON})} \) of 10 mΩ, the conduction power dissipation can be calculated:

\[
P_{\text{cond}} = \frac{I_{Q1,peak}^2 \cdot r_{DS(\text{ON})}}{D_{\text{max}}}
\]

\[ = 2.5544^2 \times 10e^{-3} \times 0.6154 = 40.2 \, \text{mW} \]

Similarly, assuming a \( r_{\text{rise}} \) & \( r_{\text{fall}} \) of 10 ns each, the switching power loss can be calculated:

\[
P_{\text{sw}} = \frac{1}{2} \cdot (V_{\text{out}} + V_D + V_{\text{in}(\text{max})}) \cdot I_{Q1,peak} \cdot (r_{\text{rise}} + r_{\text{fall}}) \cdot f_{\text{sw}}
\]

\[ = \frac{1}{2} \times 15 \times 3.5599 \times (10e^{-9} + 10e^{-9}) \times 2e6 = 1.0680 \, \text{W} \]

Now the total power dissipation can be calculated:

\[
P_{Q1} = P_{\text{cond}} + P_{\text{sw}}
\]

\[ = 40.2e^{-3} + 1.0680 = 1.0811 \, \text{W} \]

\[ V_{\text{GS}} \] has to be greater than the gate drive voltage for NCV898031 which is equal to 6.3 (typ). The onsemi MOSFET NTTFS5C471NL N-Channel, 40 V, 12 A, 9 mΩ was selected using onsemi Product Recommendation Tool+. For NTTFS5C471NL, the \( R_{\text{DUA}} = 50 \, \text{°C/W} \) and the \( T_{j(\text{max})} = 175 \, \text{°C} \) therefore

\[
T_{j(\text{max})} > P_{Q1} \times R_{\text{DUA}} + T_{\text{ambient}}
\]

\[ 175 > 1.0811 \times 50 + 85 \]

\[ 175^\circ \text{C} > 140.4^\circ \text{C} \]

Step 4: Diode Selection

The peak current for the diode is equal to:

\[ I_{D,peak} = I_{Q1,peak} = I_{L1,peak} + I_{L2,peak} = 2.1907 + 1.3692 = 3.5599 \, \text{A} \]

The reverse voltage for the diode equals:

\[ V_{\text{Vin(max)}} + V_{\text{out(max)}} = 9.0 + 5.5 = 14.5 \, \text{V} \]

The average current for the diode equals:

\[
I_D = \frac{I_{\text{out}}}{1 - D_{\text{min}}} = \frac{1.25}{1 - 0.4} = 2.0833 \, \text{A}
\]

At \( I_D = 2 \, \text{A} \) (@ 100°C), the forward diode drop \( V_D \approx 0.35 \), therefore the power dissipated in the diode equals:

\[
P_D = I_D \cdot V_D
\]

\[ = 1.25 \times 0.35 = 0.4375 \, \text{W} \]

The onsemi Diode MBRS320T3G, Schottky Power Rectifier, Surface Mount, 3.0 A, 20 V is selected. For the selected diode the \( R_{\text{DUA}} = 30 \, \text{°C/W} \)

\[
T_{j(\text{max})} > P_D \times R_{\text{DUA}} + T_{\text{ambient}}
\]

\[ 150 > 0.4375 \times 30 + 85 = 98.125 \]

\[ 150^\circ \text{C} > 103.75^\circ \text{C} \]

Step 5: SEPIC Coupling Capacitor Selection

The RMS current through the capacitor is given by:

\[
I_{\text{Ccp(rms)}} = I_{\text{out}} \sqrt{\frac{V_{\text{out}} + V_D}{V_{\text{in(min)}}}}
\]

\[ = 1.25 \sqrt{\frac{5.5 + 0.5}{3.75}} = 1.5811 \, \text{A} \]

For 5% ripple, the minimum capacitance can be calculated as:

\[
C_{\text{Ccp}} = \frac{I_{\text{out}} \cdot D_{\text{max}}}{0.05 \times V_{\text{in(min)}} \cdot f_{\text{sw}}}
\]

\[ \geq \frac{1.25 \times 0.6154}{0.05 \times 3.75 \times 2e6} \geq 2.05 \, \mu\text{F} \]

Wurth Elektronik 885012209026 3.3 \mu\text{F}, 25 V, and 3.69 mΩ @ 2 MHz is selected for Ccp. Given we have selected a ceramic capacitor with low ESR, we will ignore the ESR requirement.

It may become necessary to place an RC damping network in parallel with the coupling capacitor if the resonance is within ~1 decade of the closed-loop crossover frequency. The capacitance of the damping capacitor should be ~5 times that of the coupling capacitor. The optimal damping resistance (including the ESR of the damping capacitor) is calculated as:

\[
R_{\text{damping}} = \frac{L1 + L2}{\sqrt{C_{\text{Ccp}}}}
\]

Step 6: Output Capacitor Selection

The RMS current through the capacitor is given by:

\[
I_{\text{Out,rms}} = I_{\text{out}} \sqrt{\frac{V_{\text{out}} + V_D}{V_{\text{in,min}}}}
\]

\[
= 1.25 \sqrt{\frac{5.5 + 0.5}{3.75}} = 1.5811 \text{ A}
\]

For 2% ripple, the minimum capacitance can be calculated as:

\[
C_{\text{Out}} \geq \frac{I_{\text{out}} D_{\text{max}}}{0.02 \times V_{\text{out}} \text{sw}}
\]

\[
\geq \frac{1.25 \times 0.6154}{0.02 \times 5.5 \times 2e6} \geq 3.4965 \mu\text{F}
\]

Wurth Elektronik 885012208068 4.7 \( \mu \text{F} \), 25 \( \text{V} \), and 3.73 \( \text{m\Omega} \) @ 2 MHz is selected for \( C_{\text{out}} \). Given we have selected a ceramic capacitor with low ESR, we will ignore the ESR requirement.

Step 7: Input Capacitor Selection

The RMS current through the input capacitor is given by

\[
Wurth \ Elektronik \ 885012208068 \ 4.7 \ \mu\text{F}, \ 25 \ \text{V}, \ \text{and} \ 3.73 \ \text{m\Omega} \ @ \ 2 \ \text{MHz} \ is \ selected \ for \ \text{Cin}.
\]

Selecting the input capacitor needs special considerations such as:

\[
I_{\text{Cin,rms}} = \frac{\Delta I_L}{\sqrt{12}}
\]

\[
= \frac{0.3497}{\sqrt{12}} = 0.1 \text{ A}
\]

- Electromagnetic Interference (EMI). An EMI filter might be needed to mitigate EMI.
- Negative impedance of the converter. Negative impedance can lead to oscillations.

These items must be addressed in the physical circuit thus it lies beyond the scope of this application report.

Simulation Results

To corroborate our analytical waveforms and ensure proper operation, simulations where carried out using the NCV898031 SIMPLIS model and the schematic in figure (7) for the following conditions:

- Input voltage: 6.0 V
- Output voltage: 5.5 V
- Output current: 1.25 A
- Frequency: 2 MHz

Figure 8. Transient Simulation Results
There are also more average models that can be downloaded to simulate the loop response of the circuit and measure the stability of the design. All the models can be found on the product page for NCV898031 under the technical Documentation & Design Resources:

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**Resources:**

1. Find the best product for your application using onsemi Product Recommendation Tool+ (PRT+)
2. Simulate the performance for your regulator using onsemi WebDesigner+ (WD+)

**References:**


Appendix A

Using coupled inductors leads to a design with better integration, less components, and lower inductance requirement when compared to using two separate inductors. One issue with coupled inductors is that it’s harder to find high power off-the-shelf coupled inductors as compared to single inductors.