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Revolutionizing Analog to Digital Conversion

NCD9801x 12−bit SAR ADC

AND90121/D

Prepared by: **Bryson Barney**
Mixed Signal Applications Engineer

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APPLICATION NOTE

Abstract

The NCD9801x ADC is a differential 12−bit resolution successive approximation register analog−to−digital converter unlike any other SAR ADC available on the market. It uses an innovative design to keep a low input capacitance of 2 pF, easily besting the typical SAR ADC input capacitance. The analog power consumption of the NCD9801x converter can reach nano−Watt levels during conversion and can be scaled dynamically based on the clock rate. These two unique traits allow designers to utilize the NCD9801x in design applications that have previously been unachievable.

Low Power Performance

The NCD9801x ADC has the unique benefit of dynamically controlled power consumption. To get the maximum sampling rate of 2 MSPS, the SPI clock (SCLK) runs at 32 MHz, putting the analog current consumption at 100 μA. Current consumption decreases in a linear fashion with decreased SCLK rates as shown in the plot below.

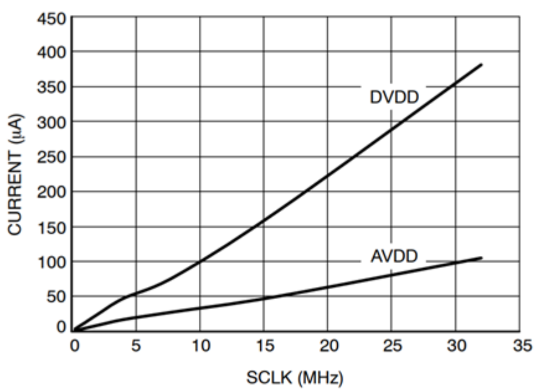

Figure 1. Current versus SCLK Frequency

When there is no activity on SCLK, the current consumption floor is an impressive 4 nA. A standard coil cell Li−Ion battery provides 40 mAh. Theoretically this could power the NCD9801 in standby mode for 1,000 years. Using a sampling rate of 512 samples per second (SCLK = 8.2 kHz), then the same coin Li−Ion battery would power the analog supply for 80 years, which is beyond the shelf life of the battery. This makes the NCD9801x friendly for energy harvesting applications where small amounts of energy can be stored on a capacitor that is then used to power the converter.

Low Input Capacitance

Typical SAR ADC designs utilize a capacitive distribution array to sample and subdivide the input voltage against a reference voltage to facilitate the analog to digital conversion. The better the matching between the capacitors in this array, the better the accuracy of the ADC. To achieve better accuracy, larger front−end capacitors are typically used in a SAR ADC. The accuracy of the ADC is improved with higher input capacitance. However, a larger input capacitance requires larger current drive at the ADC input, usually in the form of an external buffer amplifier.

The NCD9801x uses an innovative calibrated capacitance array that allows it to maintain 12−bit resolution and accuracy while keeping the input capacitance to an impressive 2 pF. This input capacitance is far lower than typical SAR ADC input capacitance. With a 2 pF input capacitance, a signal source with a 1 MHz sine wave only needs to provide 4 μA to charge the input capacitance. If the sampling rate is reduced to 512 samples per second (per the previous example) the drive of the signal source only needs to be 1.8 nA.

The end result is that both the ultra−low dynamically adjustable analog power and the low input capacitance differentiate the NCD9801x from other low−power SAR ADCs of similar resolution, size and cost. The table below shows a comparison highlighting key metrics for comparable ADCs.

Manufacturer	ON	Analog Devices	Texas Instruments	Maxim	Linear Technology
Device	NCD98010/1	AD7091	ADS7044	MAX11108	LTC2365
Resolution	12 bits	12 bits	12 bits	12 bits	12 bits
Max Sample Rate	2 MSPS	1 MSPS	1 MSPS	3 MSPS	1 MSPS
DNL	+/- 1 lsb	+/- 0.9 lsb	+/- 1 lsb	+/- 1 lsb	+/- 1 lsb
INL	+/- 1 lsb	+/- 1 lsb	+/- 1 lsb	+/- 1 lsb	+/- 1 lsb
SNR	68dB	68 dB	72 dB	73 dB	73 dB
SINAD	68dB	68 dB	71 dB	72 dB	72 dB
THD	-83dB	-86 dB	-85 dB	-85 dB	-86 dB
Supply Range	1.8 to 3.6 V	2.09 to 5.25 V	1.65 to 3.6 V	2.2 to 3.6 V	2.35 to 3.6 V
Current	50uA/MSPS** @ 3V	367uA/MSPS* @ 3V	300uA/MSPS** @ 3V	660uA/MSPS* @ 3.6 V	866uA/MSPS* @ 3V
Single-Ended or Differential	Diff.	S.E.	Diff.	S.E.	S.E.
Serial or Parallel Interface	SPI	SPI	SPI	SPI	SPI
Input Cap	2pF	7pF	15 pF	20 pF	20 pF
Package Size	1.5x1.5	2x2	1.5x1.5	2.1x1.6	3x1.5
Power Difference when compared to ON Semiconductor NCD98010		4.9 times	4 times	8.8 times	11.5 times

*Typical, **Max

Highly Differentiated

Figure 2.

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The NCD9801x is offered in a 1.5 mm x 1.5 mm package, allowing it to fit into tiny places.

Untapped Applications

The low input capacitance and low power capabilities of the NCD9801x device make it perfect for a number of applications. In typical sensor applications, a buffer between the sensor and the ADC input is required to charge the input capacitance of the ADC. Given an input with the appropriate voltage range, the buffer can be omitted saving power, cost, and space.

The example below shows a balanced resistor bridge where one of the resistances is a sensor whose resistance changes with the sensed environment. Deviations in the sensor resistance from the balanced resistor network will show up at the ADC inputs as a differential signal for digitization. Since the bridge may be higher in impedance, the low input capacitance of the NCD9801x is a big advantage.

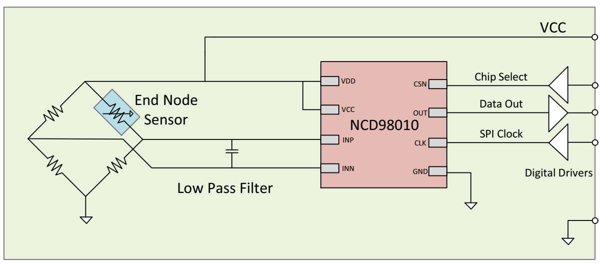

Figure 3.

Remote Sensor Applications

Remote sensing applications usually have low power / small foot print requirements. Quite often such systems are battery operated and difficult to access. The NCD9801x power profile removes the need to access the system for long periods of time given the enormous battery life potential.

The NCD9801x is also a good fit for applications dependent on energy harvesting via mechanical vibration, acoustics, solar energy, heat transfer, electromagnetic energy, or otherwise. Below is an example of a strain gauge that uses energy harvesting to monitor structural integrity at key points in a building's structure. The gauge and the piezo−electric stack move together in the event of lateral movement. The strain on the piezo stack powers the system long enough to charge capacitors and provide power to an SOC radio, which gets samples of the strain reading and transmits it to an accessible external receiver.

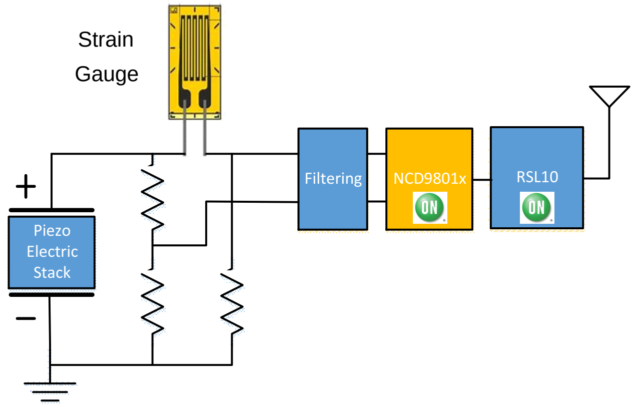

Figure 4.

Other wired applications benefit from the NDC9801x by placing it local to the end node sensor, with the wired SPI interface going out to a more accessible easier to power processor.

NCD9801x used in a Wakeup System

Wakeup systems are an increasingly popular use of low−power electronics. Wakeup systems lie "dormant" consuming less power than the leakage of a battery cell, waiting for a very specific event, signaled or environmental. If that event occurs, then the wakeup system enables more powerful processing to make decisions and take actions. Examples of such systems include room occupancy sensors, remote rare−event data collection, and wearables that track external stimuli.

Low Cost Systems (cost down the MCU)

The NCD9801x can be paired with low−cost, low resource MCU's with the intention of reducing the space and cost of the overall system. If the processor only needs to get ADC samples, then it can be reduced to only a simple Logic Gate Array (FPGA or CPLD) programmed to drive the SPI interface and perform an action based on the resulting samples. One low−power FPGA could support many NCD9801x ADC's in different locations. Many MCU's have 12−bit ADC modules on−board, however, the power consumed by those internal ADC's is difficult to constrain. Having an external NCD9801 allows the application to cost down to a simpler, lower power MCU. The MCU would no longer be required to have an onboard ADC module, opening the door to lower cost MCU options, while maintaining the capability to get 12−bit differential high speed analog to digital conversion. This could be applied to smart phone hardware peripherals, tablets, wireless headphones, wearables, and battery operated medical equipment.

Conclusion

The NCD9801x device is revolutionizing the role and utility of analog−to−digital conversion. Take your design to the next level with the benefits of the NCD9801x by accomplishing more with a smaller power budget.

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