

# Paralleling Power MOSFETs for Switching Applications

## AND90108/D

### Introduction

In high current applications, a beneficial characteristic of power MOSFETs is the ability to parallel devices to increase current conduction and power switching capacity. Numerous authors have treated this topic in the open technical literature [1–7] as well as manufacturer's application notes [8] and data books [11]. The reader is guided to these references for very fine in-depth treatment in addition to this application note.

The fundamental consideration when designing a system to employ parallel MOSFETs is to maintain balance among the device junction temperatures and to keep all within the maximum rating of the device as given in the manufacturer's data sheet, e.g., [9]. As is well-known, safe and reliable operation of the MOSFET is a function of its thermal state, which in turn is determined by the coupled interaction of device losses and the thermal management system while operating according the usage profile of the application. Total losses consist of conduction and switching losses, which are driven primarily by the magnitude of the drain current and switching frequency. However, many factors contribute to how well such losses are shared by the paralleled MOSFETs, both statically and dynamically [1, 5, 7].

Equal sharing of current and losses among devices is important in all of the modes in which MOSFETs may operate, including:

- Fully “on” during static conditions
- Switching transients (turn-on and turn-off) and pulsed conditions
- “Linear mode” (more precisely, “saturation mode”) operation

This application note provides guidance on how safely to operate power MOSFETs in parallel in switching applications. For more general guidance, refer to [7, 8, & 11].

### Key Take-Aways for Paralleling MOSFETs

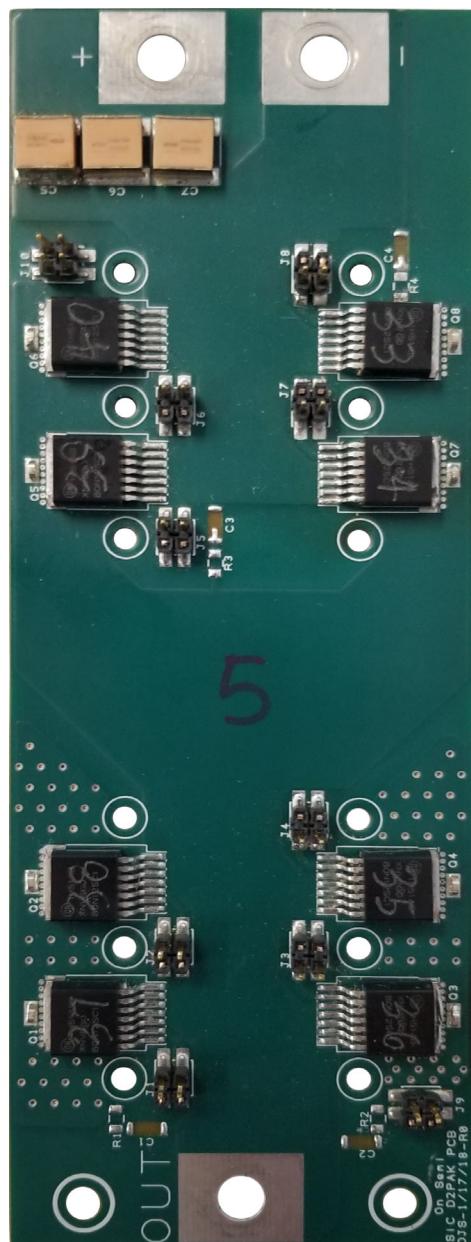
- Successful paralleling of MOSFETs is *achievable* and is routinely done without extraordinary or costly measures by careful layout and circuit design.
- Thermal mismatch will exacerbate parameter mismatch issues and is best addressed by using a common heatsink for all paralleled MOSFETs comprising the switch.
- Control stray circuit elements, especially inductance, by balanced and compact circuit layout.
- Switch as fast as possible while watching for EMI issues (ringing) and keeping common source inductance for all MOSFETs as balanced and minimal as possible to keep dynamic current sharing as even as possible.
- Use a dedicated, distributed gate resistor for each MOSFET, closely coupled to the device terminal, to provide damping (decoupling) of any gate oscillations that may arise in the low impedance loops between the Cgd of devices.



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### APPLICATION NOTE



**Figure 1. Example Half-Bridge Test PCB with 4 Paralleled D2PAK-7L Silicon-Carbide MOSFETs per Switch**

- Avoid the costly practice of matching parameters (binning) and rely on good circuit board layout and nominal device selection to give some margin in allowable switching and conduction losses.
- Avoid extra gate circuitry such as external capacitance and Zener diodes for protection as these tend to slow down switching and induce oscillations, leading to higher switching losses and greater imbalance from MOSFET to MOSFET.
- When evaluating avalanche operation, e.g. during high current, high speed switching, keep avalanche current at or below what can be handled by a single MOSFET since avalanche current sharing during very short transients is difficult to ensure, likely resulting in the die with lowest BAV taking most or all of the avalanche energy.

#### Static Current Sharing Design Considerations

Although increasing junction temperature raises the on resistance and the conduction losses of the power MOSFET, definite benefits are attributable to the positive temperature coefficient of  $R_{DS(on)}$ . If a portion of the chip begins to hog current, the localized temperature will increase, causing a corresponding increase in the  $R_{DS(on)}$  of that portion of the chip, and current will shift away to the cooler, less active, portions of the die. This trait accounts for the tendency of the device to share current over the entire surface of the die's active region. Because current crowding and hot-spotting are eliminated under normal operating conditions, there is no need to de-rate power MOSFETs to guard against secondary breakdown. The argument supporting current sharing within a device, due to the positive temperature coefficient of  $R_{DS(on)}$ , is easily extended to the case of paralleled devices. As within a single device with some imbalance in  $R_{DS(on)}$  over the die's active area, an imbalance or mismatch of  $R_{DS(on)}$  between devices will cause an initial current loading imbalance between devices. The resulting rise in junction temperature and on-resistance of the device with the lowest  $R_{DS(on)}$  will decrease that device's drain current and will establish a more equal distribution of the total load current in all paralleled devices.

While this tendency is definitely observable and beneficial, its influence on the degree of current sharing is often overstated. In the power MOSFET, the current sharing mechanism is not triggered simply by high junction temperature, but by the difference in  $T_J$  between the low and high  $R_{DS(on)}$  devices. Due to the generally small thermal coefficient of  $R_{DS(on)}$ , a substantial difference in junction temperature would need to develop to drive a reasonable level of current sharing.

Since the ultimate concern is for optimum reliability, the emphasis should not be placed on obtaining large deltas in  $T_J$  to force a greater degree of current sharing; rather, the effort should be focused on decreasing  $T_J$  of the hottest device. This is accomplished by close thermal coupling of the paralleled devices, provided that the total heat sinking capability is not compromised by doing so. This will tend to

minimize the differences in both case and junction temperature. Before a worst case example of these concepts can be examined, some knowledge of the range of the variation of  $R_{DS(on)}$  within production devices must be obtained.

Invariably (from any manufacturer) there will be at least a slight mismatch in paralleled MOSFET's  $R_{DS(on)}$ , even at the same current and case temperature, due to process and manufacturing variation, leading to individual drain current imbalance. The worst case situation is obviously the paralleling of devices with the widest possible variation in  $R_{DS(on)}$ . A representative example of variation in  $R_{DS(on)}$  taken from final test data on more than 1500 samples of a given part number is shown in Figures 2 and 3.

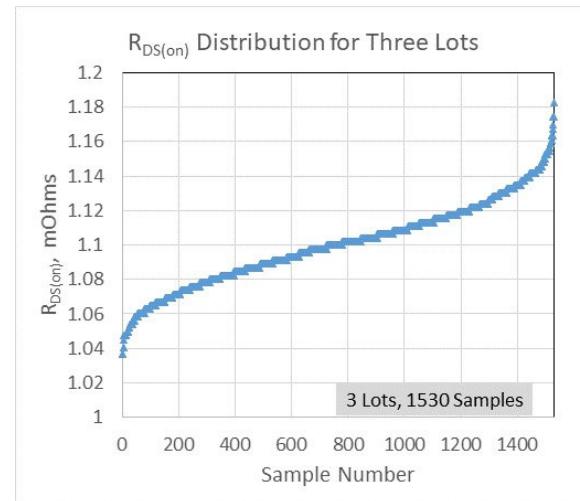


Figure 2. Representative Variation Trend

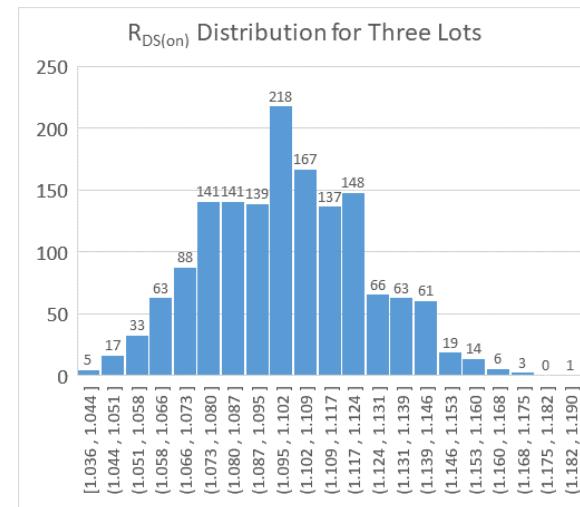


Figure 3. Representative Variation Distribution

Table 1 shows the min, max, median, and delta from this dataset, as well as the data sheet entries for the same part [10]. As is frequently the case, data sheet values for min and max are significantly wider than what is found within

normal process variation, and the user may be prudent to make use of the data sheet information for added margin in his design. From this information, one will have to design for a worst case  $R_{DS(on)}$  mismatch in the range of 15 to 25%.

**Table 1. REPRESENTATIVE VARIATION LIMITS OF  $R_{DS(ON)}$**

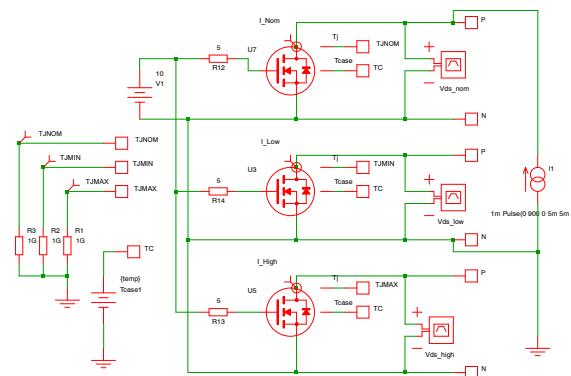
$R_{DS(on)}$ , mΩ	Final Test	Data Sheet
Max	1.183	1.4
Typ (Median)	1.100	1.1
Min	1.036	n/a
Delta (max-min)	0.147	0.3
Percent Variation	13.4%	27.3%

$R_{DS(on)}$  is dependent on the junction temperature,  $T_J$ . The strength of this dependency varies by technology. For example, from 25°C to  $T_{J(max)}$ , low and medium voltage trench silicon MOSFETs may vary by a factor of 1.75, while high voltage super junction MOSFETs may vary by a factor of 2.2, and silicon-carbide MOSFETs may only vary by a factor of 1.2.  $I_D$  is determined by the application operating point and  $T_J$  is a result of the power dissipation and thermal impedance, thus strongly dependent upon  $R_{DS(on)}$ . The quality of heat sinking and thermal coupling between devices also affects  $I_D$  and  $T_J$ . These interdependent relationships make an analytical attempt to determine the degree of current sharing between several devices with a given  $R_{DS(on)}$  mismatch a challenging task. Appendix A of Reference [11] provides an excellent guide to such an analysis, and Reference [9] provides a similar guide for an iterative solution. However, instead of these venerable classical methods, given the wide availability of circuit simulation software, a simple process to evaluate current mismatch due to  $R_{DS(on)}$  variability is shown here.

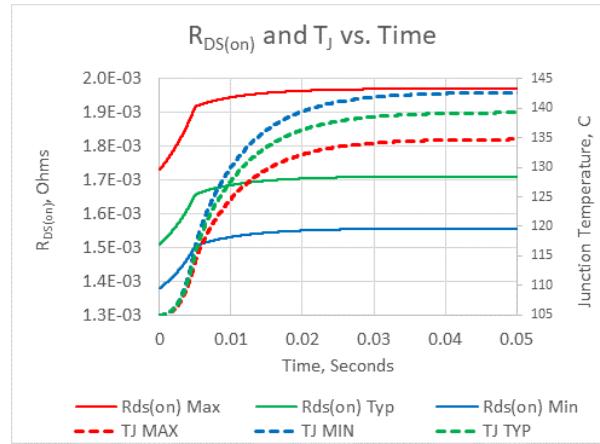
Figure 4 shows a simple simulation schematic of three devices in parallel that can be used to evaluate the impact of temperature rise and  $R_{DS(on)}$  variation on the evolution of drain current sharing among three MOSFETs with max, typical, and min (assumed from final test data)  $R_{DS(on)}$  values. The circuit is idealized in that all parallel paths have exactly the same gate voltage and no other parasitic circuit elements that would govern current balance. We have assumed here that the case temperature is held constant at 105°C. The fixed and equal case temperature boundary conditions illustrate solely the effect of on resistance variation across manufacturing variability and junction temperature. The model includes internal thermal network for the package ( $R_{θJC} \sim 0.89$  C/W). One can see by examining Figure 6 that the imbalance in current is approximately 23% of the nominal 300 A (~70 A), and a thermal imbalance also exists, with a maximum variation of 8°C, as seen in Figure 5. Yet, there is no increasing thermal imbalance. It is also obvious that the on resistance difference is not sufficient to force the currents to balance

more evenly over time. This simulation was run for a target of 300 A per device, which is the max  $I_D$  value from the data sheet [9].

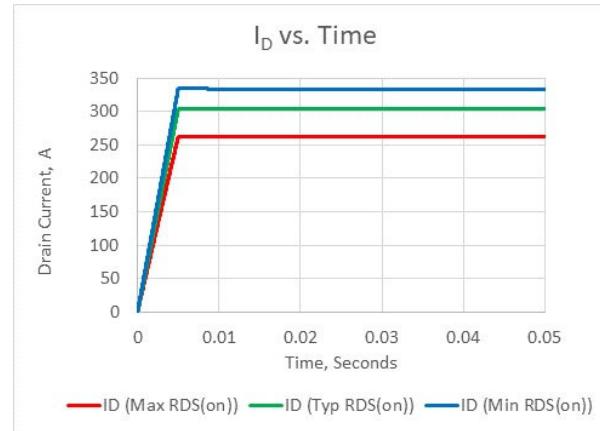
In the prior exercise, we looked at on resistance variation in isolation. Now we examine the case where thermal impedance from case to ambient is included.



**Figure 4. Idealized On Resistance Variation Circuit**



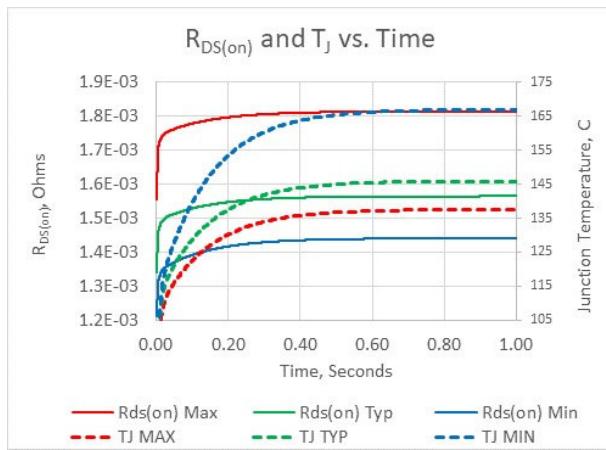
**Figure 5. Idealized On Resistance Temperature Imbalance**



**Figure 6. Idealized On Resistance Current Imbalance**

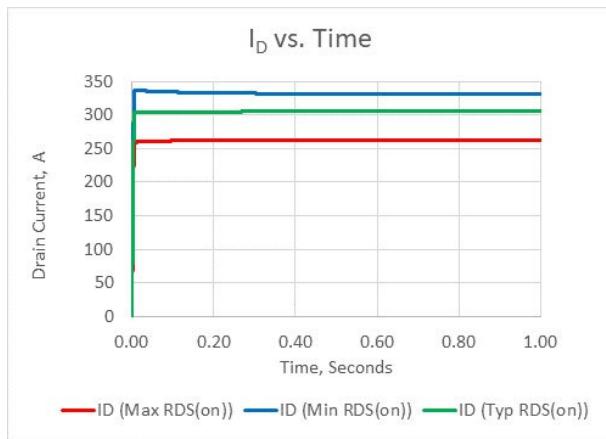
Let us assume as an example a very good cooling system that provides only an additional 0.2 K/W thermal resistance nominally, case to ambient, but has some variation due to assembly or other issues such that one device has 50% higher thermal resistance. For simulation brevity, let us assume a 120 ms thermal time constant for a simple 1<sup>st</sup> order thermal network ( $R_\theta = 200 \text{ m}$ ,  $C_\theta = 600 \text{ m}$ , nominal). To keep the operating conditions approximately the same as the first simulation, we will assume ambient temperature is 85°C.

Figure 7 shows the case where the lowest  $R_{DS(on)}$  device happens to be mounted on the cooling system with the increased  $R_\theta$ , thus the device which carries the highest current is also receiving the worst cooling. We see a significantly higher junction temperature on this device, and we see a greater spread in temperature.



**Figure 7.  $R_\theta$  and  $R_{DS(on)}$  Variation:  $R_{DS(on)}$  and  $T_J$  Result**

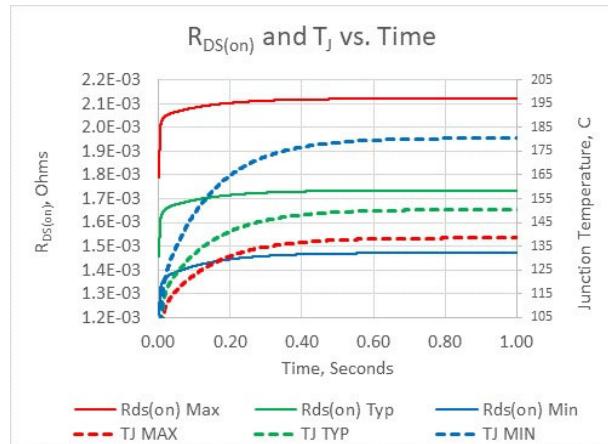
Figure 7 shows that the spread in  $R_{DS(on)}$  and junction temperatures has increased to about 0.4 mΩ (about 24% of nominal) and 30°C, up from 8°C. However, even with the larger delta between devices, we do not see an increasing thermal imbalance developing.



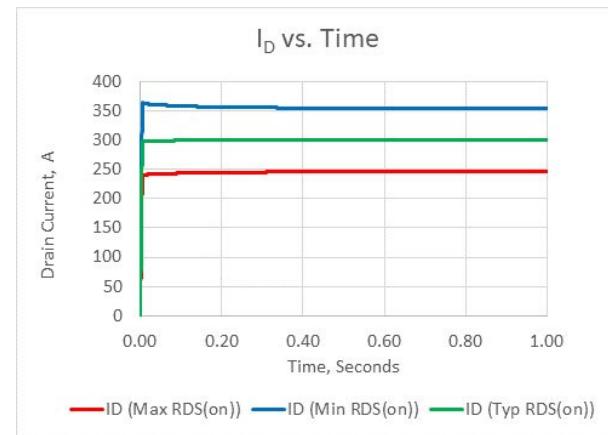
**Figure 8.  $R_\theta$  and  $R_{DS(on)}$  Variation: Current Imbalance**

We now add a difference in gate voltage to see the further impact on imbalances in current and junction temperature. For example, we reduce the gate voltage on the typical and maximum  $R_{DS(on)}$  parts by 10% to 9 V while maintaining  $V_{GS} = 10 \text{ V}$  on the low  $R_{DS(on)}$  part / high  $R_\theta$  part, with the intention to force even more current through this device.

Figures 9 and 10 present the results for this case for  $R_{DS(on)}$ , junction temperature, and  $I_D$  variation. As expected the reduced  $V_{GS}$  on two parts forces a larger current imbalance, higher junction temperature, worse current sharing.



**Figure 9.  $R_\theta$ ,  $R_{DS(on)}$  &  $V_{GS}$  Variation:  $R_{DS(on)}$  and  $T_J$  Result**



**Figure 10.  $R_\theta$  and  $R_{DS(on)}$  Variation: Current Imbalance**

Table 2 shows a summary of the steady state variation for these three cases just studied, representing the static imbalance condition.

**Table 2. SUMMARY OF STEADY STATE RESULTS ACROSS ALL VARIATIONS – STATIC IMBALANCE CASE**

Varied Value	None	R <sub>DS(on)</sub>			R <sub>θ</sub> +50%			V <sub>GS</sub> -10%		
		Max	Typ	Min	Max	Typ	Min	Max	Typ	Min
I <sub>D</sub>	300	263	303	334	263	305	337	246	300	363
R <sub>DS(ON)</sub> , mΩ	1.71	1.97	1.71	1.56	1.81	1.56	1.44	2.12	1.74	1.47
T <sub>J</sub> , C	138	135	139	143	138	146	167	138	150	181
P <sub>D</sub> , W	154	137	157	173	126	146	158	128	157	185

While reviewing Table 2, recall that each new variation added after the R<sub>DS(on)</sub> was additional to the R<sub>DS(on)</sub> variation, and was applied to the same of the three parts in parallel, namely the one with minimum R<sub>DS(on)</sub>, thus carrying maximum current.

#### Dynamic Current Sharing Design Considerations

The dynamic current sharing case refers to the normal switching of the MOSFETs, such as that found in a PWM motor control or dc–dc converter application. This is the most commonly encountered dynamic situation affecting normal design choices for paralleling MOSFETs. Some comments will be made later regarding avalanche and short circuit conditions.

Power MOSFETs will share current reasonably well with simple and efficient gate–drive circuitry. The issues of greatest concern to those interested in dynamic current sharing of paralleled MOSFETs are:

- Device parameters that influence dynamic current sharing.
- Variation of pertinent device parameters from lot to lot.
- The effects of switching speed on dynamic current sharing.
- The requirements and effects of circuit layout.
- The possibility of self-induced oscillations.

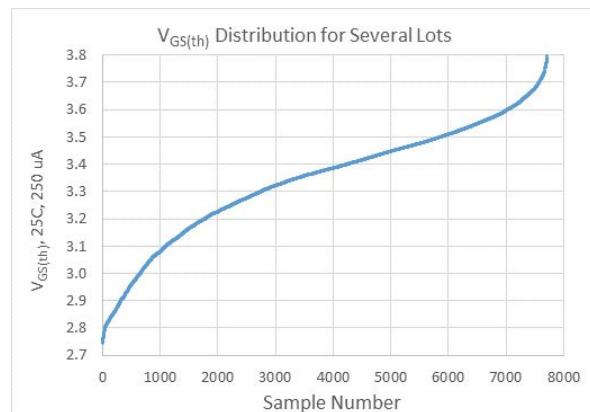
#### Device Parameters That Influence Dynamic Current Sharing

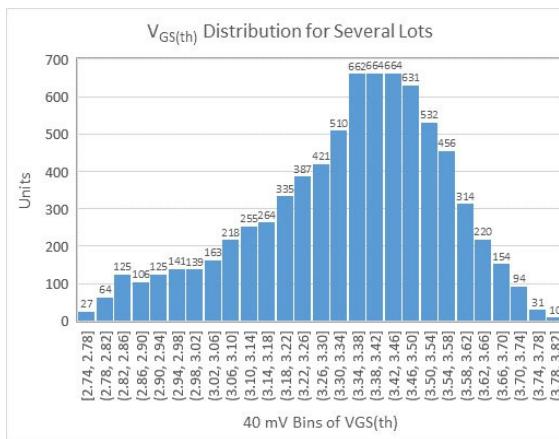
The device parameters that influence the degree of dynamic current sharing are the inter-related transconductance, gate–source threshold voltage V<sub>GS(th)</sub>, input capacitance, and on-resistance R<sub>DS(on)</sub>. However, the device characteristic that may be most useful to predict how well paralleled MOSFETs will current share during switching is the transconductance curve, i.e., the relationship between the drain current and the gate–source voltage. To obtain optimum current distribution during turn-on and turn-off, the ideal situation is to have all gate–source voltages rising (or falling) simultaneously on devices with identical transconductance curves. This idealization would ensure that as the devices switch through the active region, all would share current evenly.

As was done for static imbalance cases, we will use circuit simulation of three parts in parallel to illustrate the dynamic imbalances that can occur during switching. As readers will be aware, there are numerous contributors to specific switching waveform behavior. Obvious ones are the gate resistor, gate driver IC properties, device properties (and their intrinsic variability), stray parasitic circuit elements associated with PCB and DC link filters and bus work, local capacitor banks' specific part details, gate and drain protection circuitry such as Zener diodes, etc. Additionally, for test data, even the errors associated with high quality test instrumentation can contribute significantly to uncertainty in results. Therefore, with respect to evaluating dynamic current sharing and associated safe operation of the MOSFETs in parallel, it is not practical to include all such contributing elements in this analysis.

#### Variation of Pertinent Device Parameters

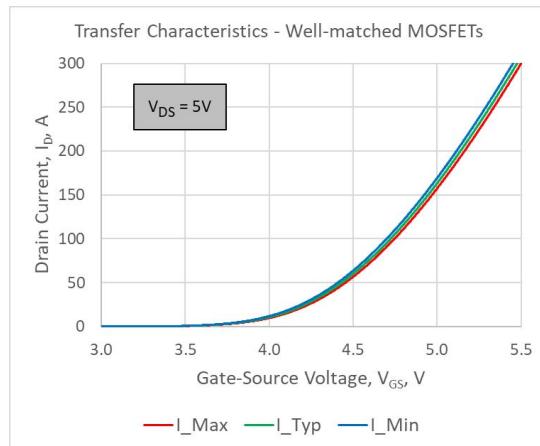
To begin, let us examine a representative set of final test data that shows variation in V<sub>GS(th)</sub>. Transconductance, V<sub>GS(th)</sub>, and R<sub>DS(on)</sub> are closely coupled parameters, so examining V<sub>GS(th)</sub> is a simple parameter to look at. Figures 11 and 12 show the variation and the distribution of ~7500 samples of a particular large die, 80 V trench MOSFET.

**Figure 11. Variation of V<sub>GS(th)</sub>**



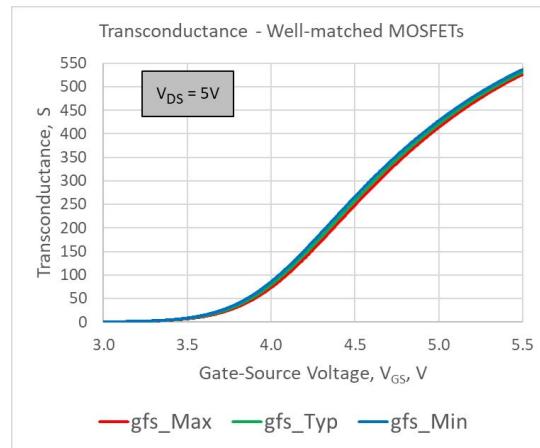
**Figure 12. Distribution of  $V_{GS(th)}$  Across ~7500 Samples**

As a representative part from the same technology, we can expect the distribution of our 80 V MOSFET [9] to exhibit similar variation. So, using an adjustable circuit model for our part, we can set up a simulation with three parts that exhibit  $V_{GS(th)}$  values that are only about  $\pm 20$  mV different from the nominal 3 V at 250  $\mu$ A. The resulting transfer characteristic and transconductance curves (at  $T_J = 25^\circ\text{C}$ ) are shown in Figures 13 and 14. As seen, the curves are very closely aligned. For example, at  $V_{GS} = 5.25$  V and  $V_{DS} = 5$  V, the drain current values are 224 A, 231 A, and 238 A, for max, typ, and min  $V_{GS(th)}$  parts, respectively. Likewise, transconductances at the same gate and drain voltages are 477 S, 483 S, and 489 S, for max, typ, and min  $V_{GS(th)}$  parts. This current level of about 200 A was chosen because later we will examine dynamic current balance while switching this level of drain current in the three paralleled parts.



**Figure 13. Transfer Characteristic Well-Matched Parts**

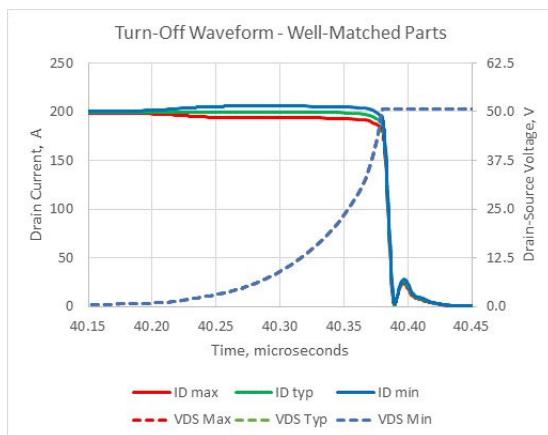
With these models, we can examine switching waveforms during turn-on and turn-off to see how well current is shared, using an idealized circuit initially with no parasitic elements external to the package (that is, no additional drain or common source inductance, identical gate voltage). For a nominal 200 A drain current, Figures 15 and 16 illustrate the dynamic behavior of this well-matched set of parts switching in parallel.



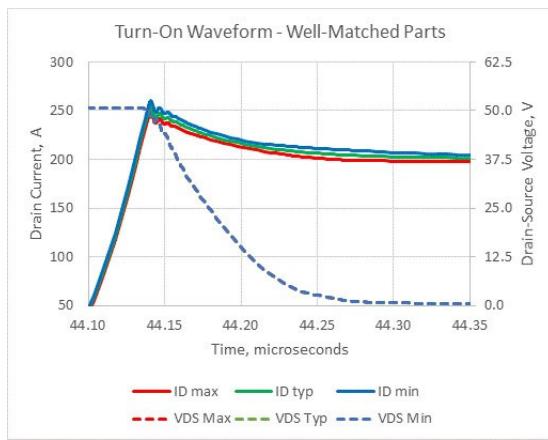
**Figure 14. Transconductance of Well-Matched Parts**

As seen in Figures 15 and 16, the device with the highest threshold voltage, “max”, is the first to begin turning off and the last to begin turning on, thereby conducting less current. As “max” current reduces during turn off, the remaining two devices are still “on” and experience an increase in their current. As can be seen by close inspection of Figure 15, the “min” part accepts the larger amount of this increase because it remains at a higher conductance, for the given gate voltage. The reverse of this process is evident in Figure 16.

By examining the minor differences in the current waveforms in Figures 15 and 16, one would expect very minor differences in accumulated energy during the switching events, and consequently minimal difference in junction temperature. In fact, not shown here but confirmed in simulation,  $E_{OFF}$  was different by only 40  $\mu$ J out of 485  $\mu$ J (typical), while  $E_{ON}$  was different by only 75  $\mu$ J out of 835  $\mu$ J (typical), per die, at this 200 A nominal switching event. Likewise, with the case temperature fixed at 105°C, at the end of both switching events, typical temperature rise was < 1°C and the delta from min to max was only < 0.1°C.



**Figure 15. Turn-Off at 200A – Well-Matched Parts**



**Figure 16. Turn-On at 200A – Well-Matched Parts**

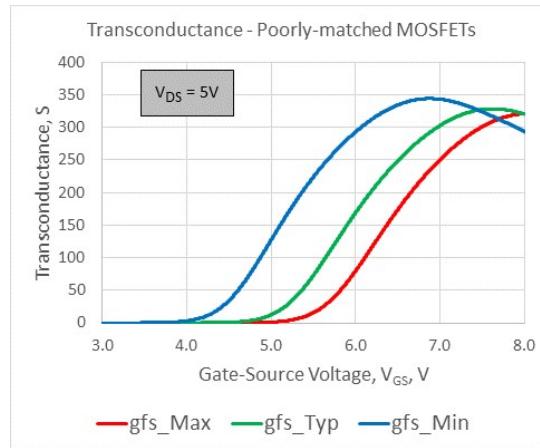
Seeing the relatively good current sharing of well-matched parts, we now look what happens in the worst case for the spread represented in Figure 11. We now set the MOSFET models in simulation to exhibit 25°C, 250 mA min, typical, and max  $V_{GS(th)}$  of 2.75 V, 3.4 V, and 3.8 V, respectively, and repeat the simulation. These results are shown in Figures 17 to 20.

Referring to Figures 19 and 20, we can see that the switching currents are quite unbalanced, differing by ~300 A from the max to min, while the typical device remains at 200 A. Since this is a relatively brief transient of ~400 ns, there is not a significant impact on temperature of the devices, but there will develop an unbalance of average switching loss over time, which will produce a temperature offset eventually, depending on the system thermal impedance. The reader is reminded that, while the transconductance variation is large here and is realistically possible for parts taken from various production lots, the

external power circuitry is still very much idealized, in that there is no drain inductance or common source inductance. As will be seen, some common source inductance has a beneficial effect for current balancing.



**Figure 17. Transfer Characteristic Poorly-Matched Parts**



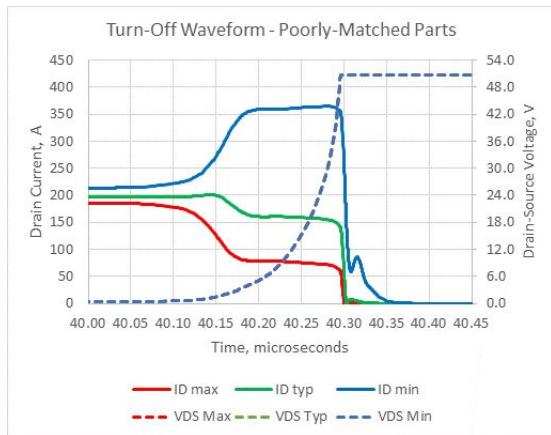
**Figure 18. Transconductance of Poorly-Matched Parts**

Table 3 provides a summary comparison of switching energy and effect on total switching losses and junction temperature rise  $\delta T_J$  for these initial cases with idealized external circuits free of parasitic inductance. We can see that for the same high performance heatsink described above for the static imbalance, here the well-matched parts yield differences in total switching energy ( $E_{SW}$ ) of about 120  $\mu J$ , which at 10 kHz switching in a MOSFET inverter would correspond to less than 1°C variation in junction temperature. The rather large current difference shown for

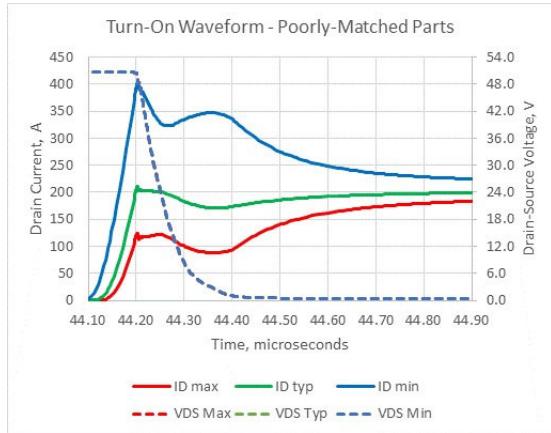
the poorly matched parts would yield about 2000  $\mu\text{J}$  difference, and about  $11^\circ\text{C}$  junction temperature variance.

**Table 3. SUMMARY RESULTS LONG TERM**

Variable	Well-Matched Parts			Poorly-Matched Parts		
	Min	Typ	Max	Min	Typ	Max
Eon, $\mu\text{J}$	850	810	770	1840	900	490
Eoff, $\mu\text{J}$	511	491	471	896	339	156
Esw, $\mu\text{J}$	1360	1301	1241	2736	1239	646
fsw, kHz	10	10	10	10	10	10
P <sub>SW</sub> , Avg W	6.8	6.5	6.2	13.7	6.2	3.23
$\delta T_J$ , $^\circ\text{C}$	7.4	7.1	6.8	14.9	6.8	3.5



**Figure 19. Turn-Off at 200A – Poorly-Matched Parts**



**Figure 20. Turn-On at 200A – Poorly-Matched Parts**

With respect to this idealized situation of the external circuit having no significant parasitic inductances, we can see that even large differences in mismatched transconductance that yields a large current mismatch during the switching transients, the net effect on total losses, while measurable, have a relatively minimal impact on thermal imbalance.

#### The Requirements and Effects of Circuit Layout

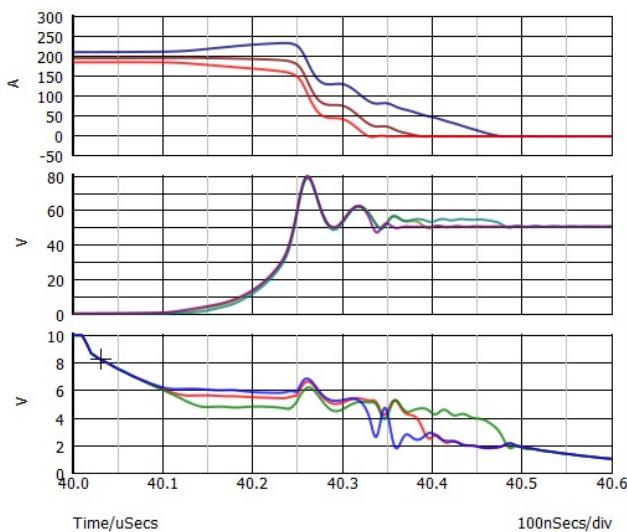
Even with identically matched devices, dynamic current sharing between MOSFETs will be poor if an asymmetrical circuit layout is used. Obviously, if the gate drives are different, unequal rates of gate-source voltage rise and fall can cause unsynchronized switching and even device failure in extreme cases. As the switching speeds of these devices are increased, the designer's perception as to what may constitute an important parasitic circuit element must change. When approaching the maximum switching speeds of power MOSFETs, even small variations in lead length may influence their paralleled switching performance. Unequal source wiring inductances are especially deleterious.

It is good design practice to minimize these inductances to keep EMI and  $V_{DS}$  overshoot issues under control. However, the presence particularly of common source inductance (inductance in the high current path of the source connection that is common with the gate loop) can be beneficial for current sharing, but must be balanced with overall system performance and as similar as possible for all paralleled MOSFETs.

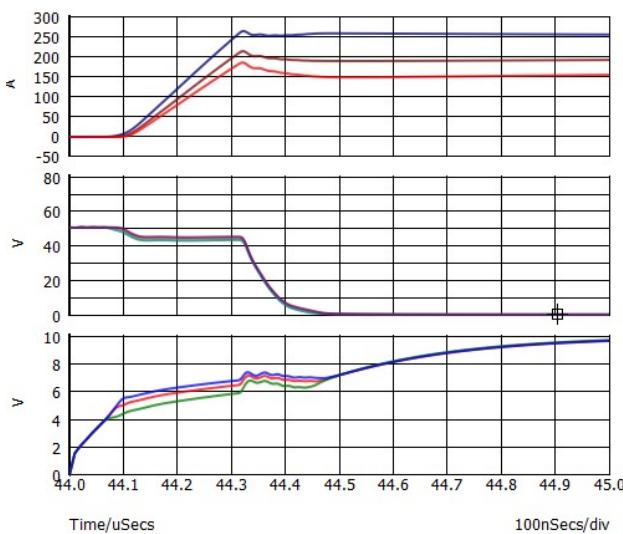
A modest 6 nH total split evenly between drain and source legs yeilds a significant improvement in the dynamic current imbalance, as seen in Figures 20 and 21. During turn off from 200 A nominal for each part, we now have less than 100 A difference from min to max. We begin to see overshoot voltage as expected in the drain circuit, but no avalanche is yet encountered.

Note in Figures 21 and 22, the red current trace is  $I_{D(\max)}$  and the blue current trace is  $I_{D(\min)}$ , while the blue  $V_{GS}$  trace is  $V_{GS(\max)}$  and the green  $V_{GS}$  trace is  $V_{GS(\min)}$ .

Table 4 shows a summary for these conditions of adding stray inductance for the case of poorly-matched parts. As seen in this table, losses increase compared to the ideal external circuit with poorly-matched parts, shown in Table 3. However, losses and temperature rise are more balanced in steady state. In this simulation,  $\delta T_J$  difference is only  $\sim 7^\circ\text{C}$ .



**Figure 21. Simulation Output with Stray Inductance, Poorly-Matched Parts – Turn Off Event**



**Figure 22. Simulation Output with Stray Inductance, Poorly-Matched Parts – Turn Off Event**

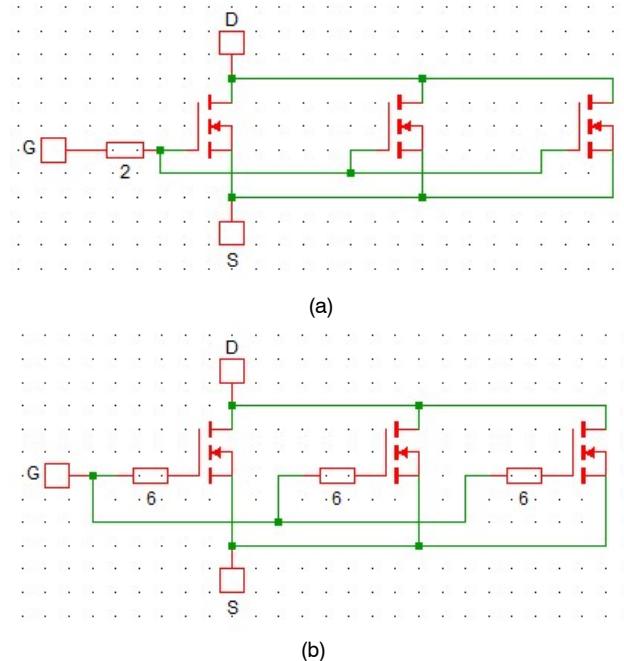
**Table 4. SUMMARY RESULTS – STRAY INDUCTANCE INCLUDED WITH POORLY-MATCHED PARTS**

Variable	Min	Typ	Max
Eon, $\mu$ J	1459	864	630
Eoff, $\mu$ J	1773	1448	1258
Esw, $\mu$ J	3232	2312	1888
fsw, kHz	10	10	10
Psw, Avg W	16.2	11.6	9.4
$\delta T_j$ , °C	17.6	12.6	10.3

#### *The Requirements and Effects of Circuit Layout*

Coupled oscillations in the gate and drain circuits may become objectionable or dangerous to the power MOSFETs if the gates are driven from a single common gate node. For example, assume one wishes to drive each of three

MOSFETs in parallel with a total of  $2\ \Omega$  gate resistance, as illustrated in Figure 23 (a). An underdamped RLC circuit is then formed by the three MOSFETs' C<sub>GD</sub>, C<sub>GS</sub>, parasitic L<sub>D</sub>, and parasitic L<sub>S</sub>, with minimal damping resistance. An equivalent distributed gate resistance network is shown in Figure 23 (b), with each MOSFET having an associated  $6\ \Omega$  gate resistor. These two configurations will give equivalent switching speed, but the distributed network will provide more damping during the switching events.



**Figure 23. (a) Single Gate Resistor  
(b) Distributed Gate Resistors**

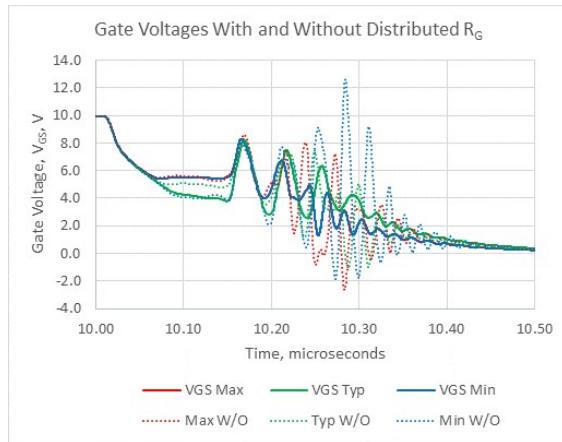
Continuing with our previous condition where the min, typical, and max V<sub>GS(th)</sub> samples are selected and paralleled together, we can compare the relative gate and drain circuit stability in simulation. The results are presented for the same 200 A drain current switching event as previously.

Figures 24 and 25 show the gate voltage waveforms for each MOSFET with and without the distributed gate resistors. In these figures, the dotted traces are without the distributed gate resistor but with equivalent single driving node gate resistance of  $2\ \Omega$ , and the solid lines are with distributed  $6\ \Omega$  gate resistors.

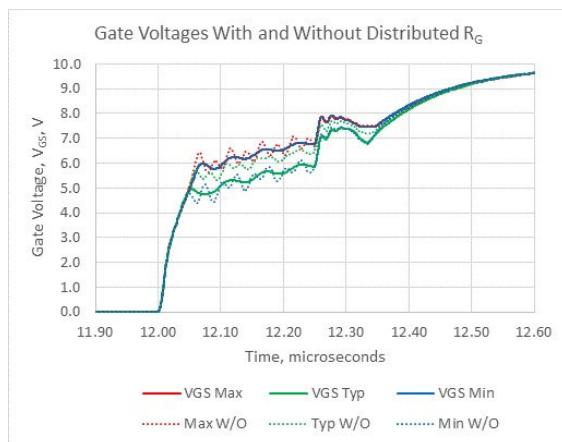
Initial gate oscillations for this high speed switching case are difficult to avoid, due to the midpoint dV/dt and Miller capacitance. However, the following numerous cycles of oscillations in gate voltage can be damped with the distributed resistance as the RLC circuit responds to the initial switching impulse and reverse recovery transient of the opposite switch body diode.

Because the combined distributed gate resistances are equivalent in value to a single lumped gate resistor, the switching time constant remains the same, and the losses are

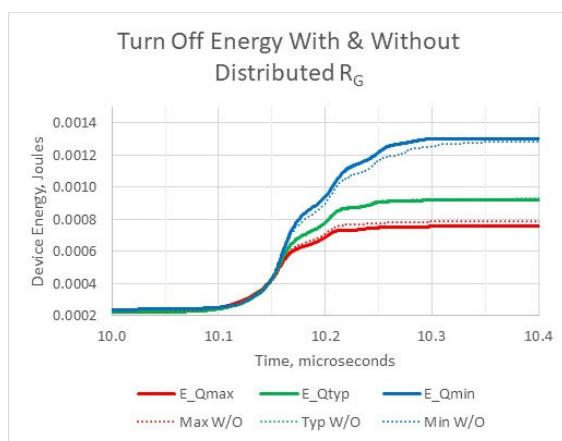
not impacted significantly, but as can be seen especially in Figure 24, the gate oscillations are under much better control. As an example, Figure 26 shows the energy lost during the turn-off event.



**Figure 24. Gate Voltages for Turn Off with and without Distributed Gate Resistors.**



**Figure 25. Gate Voltages for Turn On with and without Distributed Gate Resistors**



**Figure 26. Turn-Off Energy with and without Distributed Gate Resistors**

With respect to gate resistor selection, it is also worth noting that for most high current applications (e.g., motor drives) where paralleling is commonly used, switching frequency is relatively low (in the range of 5–15 kHz). Here, conduction losses are so dominant that increasing gate resistance to reduce gate oscillations does not have a significant impact on total losses, since switching losses remain relatively low.

For the final determination of what level of current sharing is necessary for successful application, designers will need to explore the techniques described here and to consider how best to optimize circuit layout, switching speed, device margin, and thermal management. This involves making sure that the worst case operating conditions can be handled in steady state and in harsh transient conditions, not solely the instantaneous losses and peak currents reached. Using the techniques described here will help the designers arrive at a successful solution.

#### A Few Words on Short Circuit Withstand Time and Avalanche

With the increased application power MOSFETs to high power systems such as Belt Starter Generator for 48 V vehicle electrification and electric vehicle traction drives, increased attention is being paid to short circuit withstand time (SCWT). With these applications the state of the art is being advanced and fundamental tradeoffs are being examined. Especially with respect to very low  $R_{DS(on)}$  silicon MOSFETs ( $\leq 0.5 \text{ m}\Omega$ ) and very high speed silicon-carbide MOSFETs, the very features that make them attractive for these applications make for difficulty in handling short circuit conditions and also increase the likelihood of experiencing avalanche.

To minimize switching and conduction losses, packages with extremely low stray inductance and small, efficient footprints are being developed. These lead to the ability, with tightly coupled DC link capacitor banks, to develop thousands of amps of short circuit (SC) current within 1 to 2 microseconds. This is often less time than is necessary to detect an overcurrent condition and apply safe turn-off measures! Then, even with the low inductance package and board design,  $di/dt$  is so high during turn off that avalanche is likely to occur.

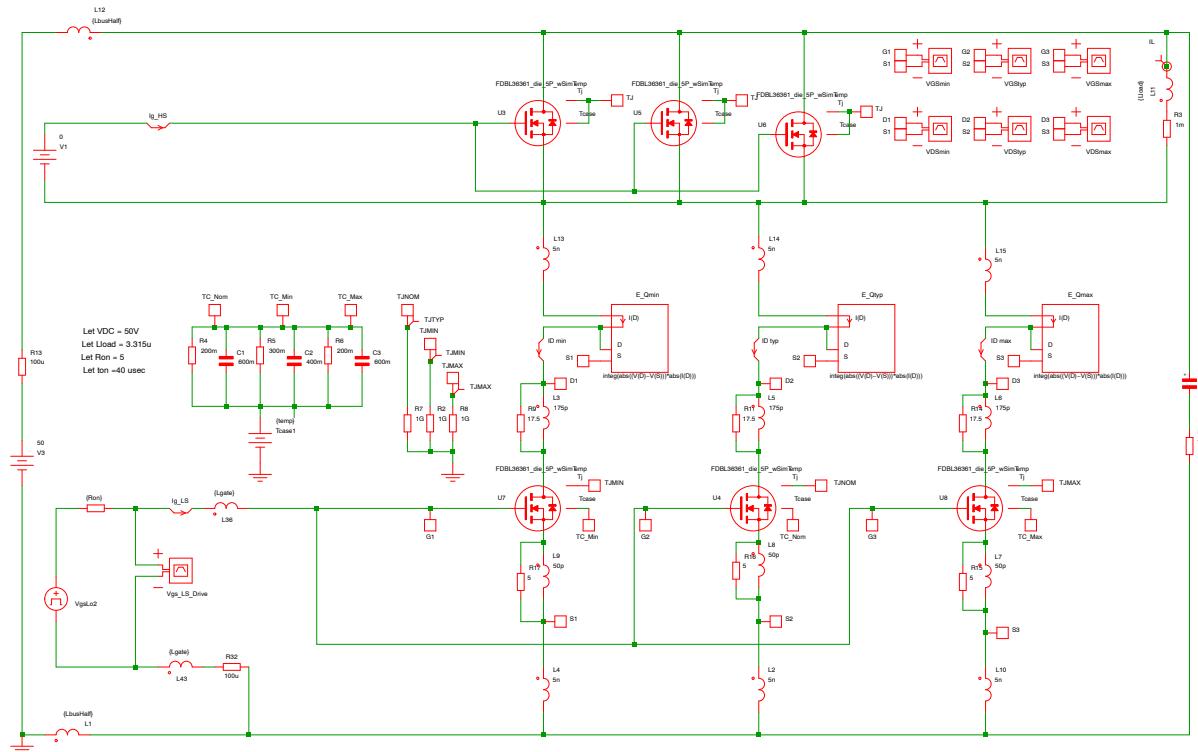
Two recommendations are clear: include an optimized amount of common source inductance to provide negative gate voltage feedback during high  $di/dt$  events in order to limit current, and consider alternatives to “desaturation detection” techniques for overcurrent and SC fault detection. Otherwise, with very low resistance, fast switches, there may be instances when it is impossible to recover from a short circuit event.

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APPENDIX A



## **Figure 27. Appendix A**

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