

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.



ON Semiconductor®

www.onsemi.com

Key Steps to Design a Multimode PFC Stage Using the NCP1655

Overview

This paper describes the key steps and provides the main equations useful for the rapid design of a multimode PFC stage driven by the NCP1655. This application note illustrates this process through the following practical 500 W, universal-mains application:

- Maximum Output Power: 500 W
- Input Voltage Range: from 90 V rms to 265 V rms
- Regulation Output Voltage: 390 V
- CCM Frequency: 65 kHz
- Clamp Frequency: 130 kHz

Introduction

The NCP1655 is a multimode controller. Practically, it transitions from one conduction mode to another depending on the line/load conditions for an optimized efficiency over the entire operating range. Housed in a SO-9 package, the circuit further incorporates the features necessary for robust and compact PFC stages, with a minimal number of external components. NCP1655 functions make it the ideal candidate in systems where cost-effectiveness, reliability, low stand-by power, high efficiency ratios over the load range and near-unity power factor are key parameters:

- Multimode Capability.

As detailed in the next section, the NCP1655 selects the operating mode (continuous, critical or discontinuous conduction mode) as a function of the inductor current cycle duration for an optimized operation over the line/load range. In light load, frequency foldback is further engaged to maximize the efficiency. It is further possible to engage the soft-skip mode where the output voltage swings between two levels to minimize the standby losses. In addition, valley turn on of the MOSFET is provided in both the critical and discontinuous conduction modes. Note that the NCP1655 multimode algorithm closely controls the switching frequency in all circumstances (65 kHz in continuous conduction mode with jittering, between 25 kHz and 130 kHz in the other modes), hence easing EMI filtering.

- High-Voltage Capability.

The circuit features a high-voltage pin (V_S pin) to monitor the input voltage for the line-range and brownout detection circuitries. The V_S pin saves the need for external high-impedance resistors to sense the input voltage.

- Fast Line / Load Transient Compensation.

The NCP1655 incorporates a digital trans-conductance error amplifier and a digital compensation setting the low bandwidth necessary for proper line current shaping. As a result, inherently, PFC stages are slow systems and traditionally exhibit large over- and under-shoots when abrupt load or line transients occur (e.g. at start-up). The NCP1655 dramatically narrows the output voltage range. First, the controller detects over-voltage (OVP) situations and interrupts the power delivery as long as the output voltage exceeds this OVP threshold. Also, the *dynamic response enhancer* (DRE) drastically speeds-up the regulation loop when the output voltage is 4.5% below its desired level. As a matter of fact, a PFC stage provides the downstream converter with a very narrow voltage range.

- A “pfcOK” signal.

The circuit detects whether the PFC stage is in steady state or on the contrary, in a start-up or fault condition. In the first case, the “pfcOK” pin (pin 2) sources a current proportional to the feedback pin voltage and is grounded otherwise. When in high state, the external resistor to be placed between the pfcOK pin and ground forms a voltage representative of the output voltage which can be used not only to enable the downstream converter but also to provide it with a feedforward signal. On the other hand, the pfcOK pin turns low in the event of a major fault like a brown-out situation or if the bulk voltage drops too low (see BUV protection) so that, finally, the downstream converter can be optimally designed for the narrow voltage provided by the PFC stage when the pfcOK pin is high.

APPLICATION NOTE

- Safety Protections.

The NCP1655 permanently monitors the input and output voltages, the input current and the die temperature to protect the system from possible over-stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:

- ◆ Over-Current and Overstress Protections: the circuit senses the inductor current and prevents it from exceeding the programmed current limit. In addition, the circuit enters a low duty-cycle operation mode in an overstress situation, that is, when the current reaches 150% of the current limit as this can happen if the inductor saturates.
- ◆ In-rush detection: when in frequency-clamped critical conduction mode, the NCP1655 prevents the power switches from turning on in the presence of the large in-rush currents which typically take place when the power supply is plugged in.
- ◆ Under-Voltage Protection: this feature prevents operation if the feedback pin is accidentally grounded or open.
- ◆ Bulk Under-Voltage Detection (BUV): The BUV function is implemented to prevent the downstream converter from operating when the buck voltage is too low. Practically, a BUV situation is detected when the feedback pin voltage drops below 1.2 V typically
- ◆ Brown-Out Detection: the circuit detects too low levels of the input voltage and if the line sag is long enough (650 ms typically), a brown-out fault is detected and pfcOK is grounded.
- ◆ Thermal Shutdown: the circuit stops pulsing when its junction temperature exceeds 150 °C typically and resumes operation once it drops below about 100 °C (50 °C hysteresis).

Multimode Capability

The NCP1655 naturally transitions from one conduction mode to another depending on the conditions so that the operation is optimized over the line/load range:

- The circuit operates in critical conduction mode (CrM) by default. CrM is an efficient and popular mode of operation where the inductor current ramps up to twice the line instantaneous current, ramps down to zero then

immediately ramps positive again. The input current ripple is large (2 times the line instantaneous current) but the MOSFET turn-on losses are minimized. This is because, the current being at a null when the MOSFET closes, there are no reverse-recovery losses of the boost diode to worry about but also, because valley turn-on of the MOSFET can be obtained. Zero voltage switching is even possible when the input voltage is less than 50% of the output voltage.

- The CrM switching frequency is by essence variable and tends to increase near the line zero crossing and more generally at light load. The NCP1655 prevents the switching frequency from exceeding a maximum level (130 kHz typically) by generating a dead-time. This is the so-called frequency-clamped critical conduction mode (FCCrM). When the frequency is clamped, the PFC stage operates in discontinuous conduction mode (DCM) while keeping properly shaping the line current by appropriately compensating for dead-times. Even, the system can repeatedly transition between DCM and CrM with no discontinuity in operation and with no power factor degradation
- In addition, when the load further decreases, the frequency clamp level decays, thus, lowering the DCM frequency (frequency foldback). This method is an effective solution to maintain the low-power range efficiency at a high level while otherwise it would sag because of the switching losses dramatic impact. However, the minimum frequency is firmly maintained above 25 kHz to stay outside the audible range.
- In heavy-load and low-line conditions, the input current becomes high and the inductor current ripple, ΔI_L , can take too large a value, leading to an increased inductor size, excessive conduction losses and significant EMI filtering pains, if the PFC remains operated in CrM. In this case, the NCP1655 can enter the continuous conduction mode (CCM), which is more suitable in heavy load conditions.
- In very light-load conditions, the circuit can enter a soft-skip cycle mode where the output voltage swings between 103% and 98% of its nominal level. During the idle phase for which the bulk capacitor discharges, the NCP1655 consumption is minimized (250 μ A). This mode is externally set using the pfcOK or V_M pins.

AND90080/D

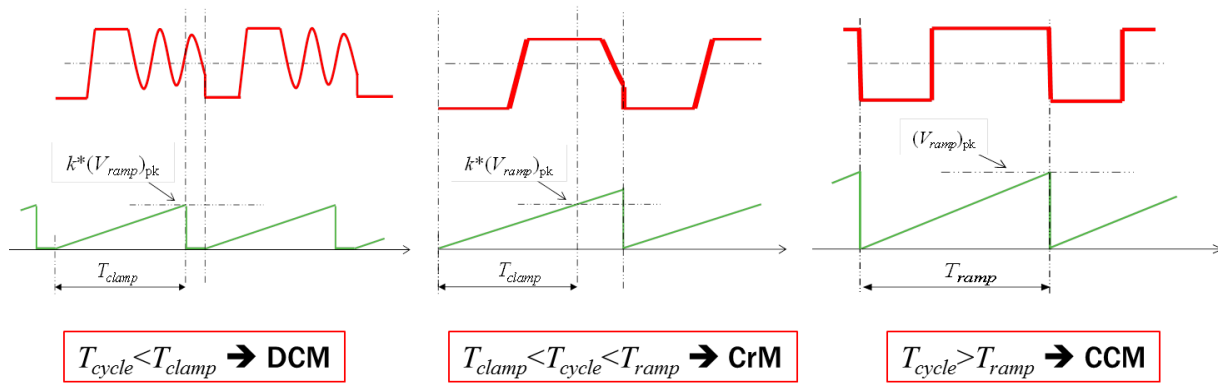


Figure 1. The Mode is Selected based on the Switching Current Duration (T_{clamp} is the DCM Period Clamp, T_{ramp} is the Switching CCM Period)

Figure 1 sketches the manner the conduction mode is selected. This is based on the duration of the inductor current cycle.

- The circuit tends to operate in critical conduction mode as long as the current switching cycle is short enough not to enter the CCM mode. However, if the current cycle happens to be shorter than the frequency–clamp period (T_{clamp} which is slightly below 8 μs leading to a 130 kHz DCM frequency), the circuit delays the next cycle until the T_{clamp} time has elapsed. Thus, the circuit enters DCM operation. The switching cycle is actually a bit longer than T_{clamp} since the next cycle is further delayed until the next valley is detected (left of Figure 1). Doing so, valley turn–on is obtained for minimized turn–on losses.
- This is the frequency–Clamped Critical conduction Mode (FCCrM) where transitions between CrM and DCM are managed cycle–by–cycle so that the circuit can transition from DCM to CrM and vice versa within a half–line cycle. Practically, DCM is more likely to occur near the line zero crossing and CrM at the top of the sinusoid. As the load further decays, current cycles become too short to cause CrM cycles and DCM operation is obtained over the entire line sinusoid. At very light load, the DCM period clamp is increased (a longer minimum switching period is forced causing frequency foldback).
- In heavy–load conditions, the circuit enters CCM when the current cycle is longer than the 112% of the CCM period (about 17 μs for a 65 kHz CCM switching frequency). The circuit cannot leave CCM on a cycle–by–cycle basis. It permanently operates in CCM until no current cycle longer than the CCM period is detected for a blanking time of several line cycles. In other words, the circuit remains in CCM over the entire half–line cycle until the load is decreased enough to recover the FCCrM mode.

The inductor value sets the power above which the circuit will enter CCM. Equation gives the CrM switching frequency at the top of the line sinusoid:

$$f_{sw} \Big|_{V_{in(t)} = \sqrt{2} \cdot V_{in,rms}} = \frac{V_{in,rms}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{2 \cdot L \cdot P_{in,avg} \cdot V_{out}} \quad (\text{eq. 1})$$

We can then compute L leading the switching frequency (at the top of the line sinusoid) to become as low as the CCM one (f_{CCM}) when the power exceeds the wished level for CCM entering ($P_{in,transition}$). Practically, 89% of f_{CCM} is actually to be targeted since the NCP1655 implements the hysteresis necessary to avoid repeated and unwanted transitions between modes:

$$L = \frac{V_{in,rms}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{2 \cdot 89\% \cdot f_{CCM} \cdot P_{in,transition} \cdot V_{out}} \quad (\text{eq. 2})$$

As an example, if we target $P_{in,transition} = 270 \text{ W}$ at low line (90 V), f_{CCM} being 65 kHz, a 175 μH inductor is to be chosen.

It comes from this that at low line (90 V rms) and with a 175 μH inductor, the system will operate in FCCrM for powers below 270 W and in CCM for powers above 270 W. Also, whatever the full load is, the maximum input current ripple to be filtered by the EMI filter is the current ripple obtained at this FCCrM–to–CCM power threshold. In other words, the inductor value can be selected so that the circuit enters CCM when the FCCrM current ripple gets too high for optimal operation.

- Selecting the power threshold for FCCrM to CCM transition

The power for transition must be considered at the lowest–line level of the application. This threshold ($(P_{in,transition})_{LL}$) is generally set in the range 300 W, that is, to a power level above which CCM is considered as the most appropriate conduction mode. However, the ratio

$(P_{in,transition})_{LL}$ over $(P_{in,avg})_{max}$ must not be too low. First, a very deep CCM operation would lead to too large an inductor. Second, if too low, the control signal range may not be sufficient to provide the full power. Practically, $(P_{in,transition})_{LL}$ over $(P_{in,avg})_{max}$ must be set to 20% or above in a wide-mains application. More flexibility is possible in a reduced line range. In any cases, the computation of the V_M pin resistor which sets the CCM gain enables to check that the selection is correct. We will see that Eq. 27 gives the maximum V_M pin resistance enabling to provide the full power ($R_{M,max}$). Eq. 29 provides the V_M pin resistance for constant-power transition ($R_{M,CP}$). ($R_{M,CP}$) must be lower than ($R_{M,max}$) for full power delivery. Even, for the sake of margin, ($R_{M,CP}$) should be set lower than ($80% * R_{M,max}$). Thus, if ($R_{M,CP}$) is higher than ($80% * R_{M,max}$), it is recommended to increase $(P_{in,transition})_{LL}$.

Design Steps

Key Specifications

We must first identify the main specification points of the PFC stage:

- f_{line} : Line frequency. 50 Hz /60 Hz applications are targeted. Practically, they are often specified in a range of 47–63 Hz and for calculations such as hold-up time, one has to factor in the lowest specified value.
- $(V_{in,rms})_{LL}$: Lowest level of the line voltage. This is the minimum rms input voltage for which the PFC stage must operate nominally. Such a level is usually 10–12% below the minimum typical voltage which could be 100 V in many countries. We will take: $(V_{in,rms})_{LL} = 90 V$. The circuit is however able to operate down to the thresholds of the NCP1655 brown-out protection:
 - ◆ $(V_{in,rms})_{boH} = V_{BO(start)} / \sqrt{2}$
 - ◆ $(V_{in,rms})_{boL} = V_{BO(stop)} / \sqrt{2}$
 Where $V_{BO(start)}$ is the line-sag and BO upper threshold (95 V typically – see data sheet) and $V_{BO(stop)}$ is the line sag and BO lower threshold (87 V typically – see data sheet), thus corresponding to the following typical rms levels: 67 V and 61 V.
- $(V_{in,rms})_{HL}$: Highest level for the line voltage. This is the maximum input rms voltage. It is usually 10% above the maximum typical voltage (240 V in many countries). We will use: $(V_{in,rms})_{HL} = 264 V$.

- $V_{out,nom}$: Nominal output voltage. This is the regulation level for the PFC output voltage (also designated as bulk voltage). $V_{out,nom}$ must be higher than $(\sqrt{2} \cdot (V_{line,rms})_{HL})$. 390 V is our target value.
- $(\Delta V_{out})_{pk-pk}$: Peak-to-peak output voltage ripple. This parameter is often specified in percentage of output voltage. It must be selected equal or lower than 8% to avoid triggering the over-voltage protection (softOVP) and/or the dynamic response enhancer (DRE) in normal operation.
- $t_{HOLD-UP}$: Hold-up time. This parameter specifies the amount of time the output will remain valid during a line dropout event. One line cycle is typically specified. This requirement requires knowing the minimum voltage on the PFC stage output necessary for proper operation of your application ($V_{out,min}$). No hold-up time will be considered here.
- P_{out} : Output power. This is the power consumed by the PFC load.
- $P_{out,max}$: Maximum output power. This is the maximum output power level, that is, 500 W in our application.
- $(P_{in,avg})_{max}$: Maximum input power. This is the maximum power which can be absorbed from the mains in normal operation. This level is typically obtained at full load, lowest line. As a starting point, we will assume an efficiency of 92% which leads to:

$$(P_{in,avg})_{max} = \frac{500}{92\%} \cong 540 W$$
- $(P_{in,transition})_{LL}$: Input power above which the circuit enters the CCM mode. This power threshold is considered at the lowest line of the application. We will set it to 270 W in our application. Note that if a power thresholds in the range of 300 W is generally a good choice, it must be set to 20% of $(P_{in,avg})_{max}$ or above. See the “CCM Duty Ratio control” section for more details.

We can now compute the value of the components shown in the generic application schematic of Figure 2.

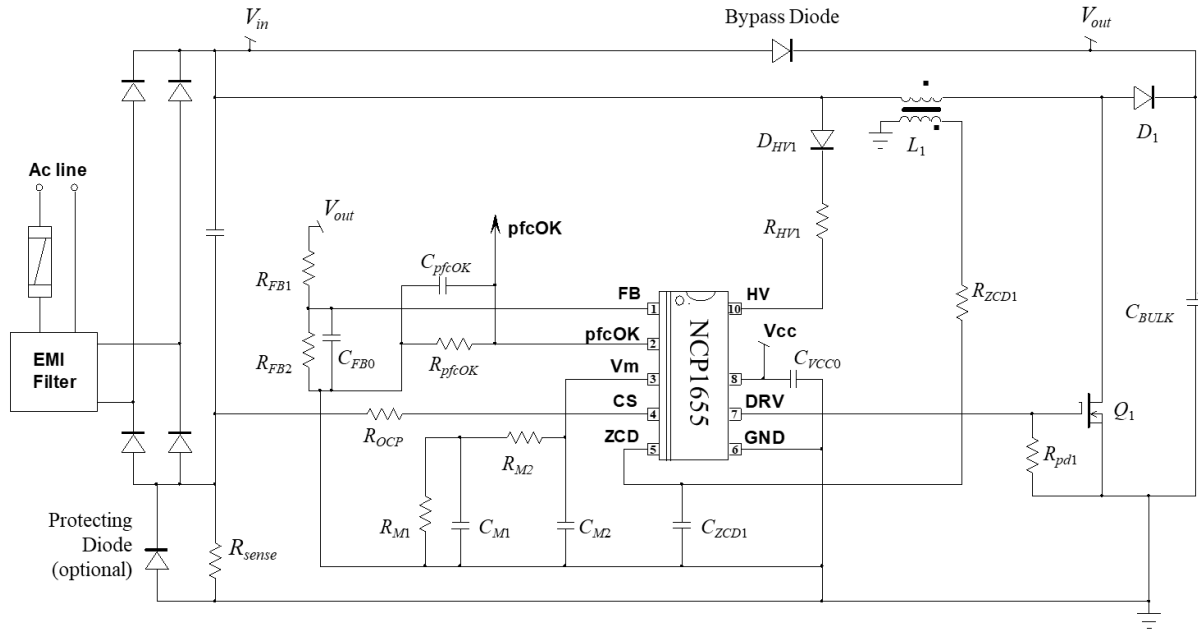


Figure 2. NCP1655 Generic Application Schematic

Inductor Selection

The inductance sets the power level above which the PFC stage enters the CCM mode of operation. Practically, The PFC stage will enter CCM when the CrM frequency drops to (65 kHz / 112%), that is, 58 kHz.

The following equation gives a good approximation of the CrM switching frequency (at the top of the sinusoid) [1]:

$$\int_{SW} = \frac{V_{in,rms}^2 \cdot (V_{out} - \sqrt{2} \cdot V_{in,rms})}{2 \cdot L \cdot P_{in,avg} \cdot V_{out}} \quad (\text{eq. 3})$$

Thus, if $(P_{in,transition})_{LL}$ is the input average power above which the circuit must enter the CCM mode at the line lowest level ($V_{in,rms} = (V_{in,rms})_{LL}$), one can deduct from the precedent equation, the inductor value necessary to meet this target:

$$L = \frac{(V_{in,rms})_{LL}^2 \cdot (V_{out} - \sqrt{2} \cdot (V_{in,rms})_{LL})}{2 \cdot (f_{SW})_{th} \cdot (P_{in,transition})_{LL} \cdot V_{out}} \quad (\text{eq. 4})$$

Where $(f_{SW})_{th}$ is the 58 kHz frequency threshold, $(V_{in,rms})_{LL}$ is the lowest-line rms voltage.

In our application, selecting 270 W for $(P_{in,transition})_{LL}$, it comes:

$$L = \frac{90^2 \cdot (390 - \sqrt{2} \cdot 90)}{2 \cdot 58 \cdot 10^3 \cdot 270 \cdot 390} \cong 175 \mu\text{H} \quad (\text{eq. 5})$$

One can show that in CCM, the current peak-to-peak ripple at the top of the sinusoid, is given by:

$$(\Delta I_L)_{PP} = \frac{V_{out} - \sqrt{2} \cdot V_{in,rms}}{L \cdot f_{CCM}} \cdot \frac{\sqrt{2} \cdot V_{in,rms}}{V_{out}} \quad (\text{eq. 6})$$

The inductor peak current will hence be:

$$I_{L,pk} = \frac{\sqrt{2} \cdot P_{in,avg}}{V_{in,rms}} + \frac{(\Delta I_L)_{PP}}{2} \quad (\text{eq. 7})$$

Combining equations (7) and (6) leads to:

$$I_{L,pk} = \frac{\sqrt{2} \cdot P_{in,avg}}{V_{in,rms}} + \left(\frac{V_{out} - \sqrt{2} \cdot V_{in,rms}}{2 \cdot L \cdot f_{CCM}} \cdot \frac{\sqrt{2} \cdot V_{in,rms}}{V_{out}} \right) \quad (\text{eq. 8})$$

Computing at the lowest line level (90 V rms), one obtains the maximum inductor current:

$$(I_{L,pk})_{max} = \frac{\sqrt{2} \cdot (P_{in,avg})_{max}}{(V_{in,rms})_{LL}} + \left(\frac{V_{out} - \sqrt{2} \cdot (V_{in,rms})_{LL}}{2 \cdot L \cdot f_{CCM}} \cdot \frac{\sqrt{2} \cdot (V_{in,rms})_{LL}}{V_{out}} \right) \quad (\text{eq. 9})$$

In our application, the maximum peak value and the lowest-line peak-to-peak ripple $((\Delta I_L)_{pp-LL})$ of the inductor current will hence be:

$$(\Delta I_L)_{pp-LL} = \frac{390 - \sqrt{2} \cdot 90}{175 \cdot 10^{-6} \cdot 65 \cdot 10^3} \cdot \frac{\sqrt{2} \cdot 90}{390} \cong 7.5 \text{ A} \quad (\text{eq. 10})$$

$$(I_{L,pk})_{max} = \frac{\sqrt{2} \cdot 540}{90} + \left(\frac{390 - \sqrt{2} \cdot 90}{2 \cdot 175 \cdot 10^{-6} \cdot 65 \cdot 10^3} \cdot \frac{\sqrt{2} \cdot 90}{390} \right) \cong 12.2 \text{ A} \quad (\text{eq. 11})$$

Finally, the following expression gives an estimate of the inductor rms current:

$$(I_{L,rms})_{max} = \sqrt{\left(\frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}}\right)^2 + \left(\frac{(V_{in,rms})_{LL}^2}{12 \cdot (L \cdot f_{CCM})^2} \cdot \left(1 - \frac{16 \sqrt{2} \cdot (V_{in,rms})_{LL}}{3\pi \cdot V_{out}} + \frac{3 \cdot (V_{in,rms})_{LL}^2}{2 \cdot V_{out}^2}\right)\right)} \cong 6.2 \text{ A} \quad (\text{eq. 12})$$

PQ3230 inductor ref. 750317557 from Würth Elektronik is selected. It exhibits an auxiliary winding ($n_{aux}/n_p=10\%$) which is used to provide the zero current detection signal necessary for valley turn on in both critical and discontinuous conduction modes.

Note that if the PFC stage was designed to remain in frequency-clamped critical conduction mode (no CCM operation), the following equations would provide the electrical specification of the inductor:

$$I_{L,max} = \frac{2\sqrt{2} \cdot (P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \quad (\text{eq. 13})$$

$$(\Delta I_L)_{pp-90V} = \frac{2\sqrt{2} \cdot (P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \quad (\text{eq. 14})$$

$$(I_{L,rms})_{max} = \frac{I_{L,max}}{\sqrt{6}} \quad (\text{eq. 15})$$

This would happen for L lower than the value by returned by Eq. 4 if the transition power ($P_{in,transition}$) was set above the maximum input power, that is, in our application, for $L < 90 \mu\text{H}$.

Current Sensing and CCM Control

The NCP1655 is designed to monitor a negative voltage proportional to the inductor current (I_L). As portrayed by Figure 3, a current sense resistor (R_{sense}) is inserted in the return path to generate a negative voltage (V_{Rsense}) proportional to I_L . The circuit uses V_{Rsense} to detect when I_L exceeds its maximum permissible level. Practically, the circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage at a null. By inserting a resistor R_{OCP} between the CS pin and R_{sense} , we adjust the current sourced by the CS pin (I_{CS}) as follows:

$$-(R_{sense} \cdot I_L) + (R_{OCP} \cdot I_{CS}) = 0 \quad (\text{eq. 16})$$

Which leads to:

$$I_{CS} = \frac{R_{sense}}{R_{OCP}} I_L \quad (\text{eq. 17})$$

In other words, the CS pin current (I_{CS}) is proportional to the inductor current. The following three protecting functions compare I_{CS} to internal current references for:

- Over current protection: if I_{CS} gets higher than internal threshold $I_{LIMIT1(LL)}$ (200 μA typically), the MOSFET immediately turns off. This is the traditional cycle-by-cycle current limitation.
- Overstress protection: if I_{CS} exceeds a second internal threshold I_{LIMIT2} which is 50% higher than I_{LIMIT1} , the circuit detects an abnormal condition. In this case, the circuit stops operation for 800 μs . This protection can trip if the inductor saturates or if its auxiliary winding is accidentally shorted. It may also help protect the circuit if the MOSFET turns on during an inrush sequence.
- Inrush current detection. When in frequency-clamped critical conduction mode, the circuit cannot restart a new cycle until I_{CS} has dropped below I_{inrush} (10 μA typically that is 5% of the maximum current threshold I_{LIMIT1}). The inrush current detector stabilizes operation by providing a rough second ZCD signal, when (during the start-up phase and at very high line for instance), the auxiliary winding voltage is too low to provide an accurate ZCD signal. It also protects the circuit by preventing operation during the inrush phase (*If an inrush sequence happens when the circuit operates, the overstress protection will trip (provided that the inrush current exceeds the overstress level) and stop operation for 800 μs . At the end of this delay, the inrush protection prevents operation until the inrush event is finished.*)

Internal current I_{CS} is also used in CCM to control the power-switch duty-ratio.

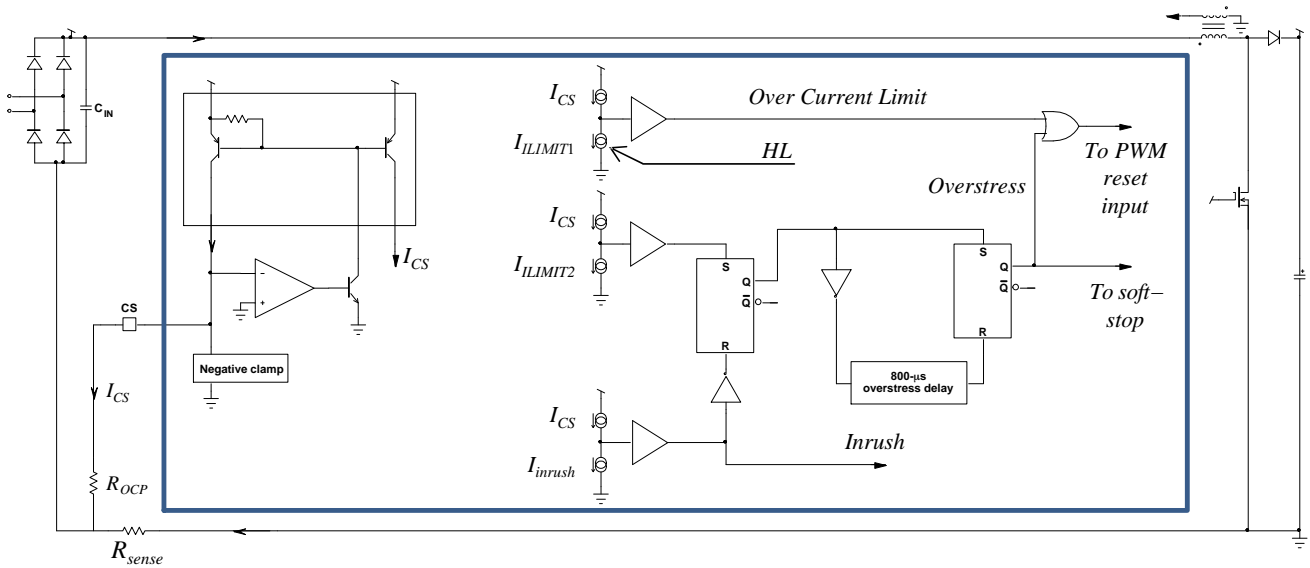


Figure 3. Current Sense Block

As we have two external components to set the current limit (R_{OCP} and R_{sense}), one can select the current sense resistance for an **optimized trade-off between losses and noise immunity**.

The following equations give an estimate of the R_{sense} maximum losses:

$$P_{R_{sense}} = R_{sense} \cdot (I_{L,rms})_{max}^2 \quad (\text{eq. 18})$$

One can choose R_{sense} as a function of its relative impact on the PFC stage efficiency at low line and full power. If α is the relative percentage of the power consumed by R_{sense} , this criterion leads to:

$$P_{R_{sense}} \leq \alpha \cdot P_{in,max} \quad (\text{eq. 19})$$

Finally:

$$R_{sense} \leq \frac{\alpha \cdot P_{in,max}}{(I_{L,rms})_{max}^2} \quad (\text{eq. 20})$$

In our application, we choose ($\alpha = 0.25\%$),

$$R_{sense} \leq \frac{0.25\% \cdot 540}{6.2^2} \cong 35 \text{ m}\Omega \quad (\text{eq. 21})$$

In practice, we will use $R_{sense} = 30 \text{ m}\Omega$ and hence, since the maximum inductor current is 12.2 A (see inductor computation):

$$R_{OCP} = \frac{R_{sense} \cdot I_{L,max}}{(I_{LIMIT1(LL)})_{min}} = \frac{30 \cdot 10^{-3} \cdot 12.2}{190 \cdot 10^{-6}} \cong 1.93 \text{ k}\Omega \quad (\text{eq. 22})$$

Where $I_{LIMIT1(LL)}$ is the guaranteed lowest value of the current limit threshold over the -40°C , 125°C range (see data sheet). In practice, one selects $R_{OCP} = 2 \text{ k}\Omega$ for availability and margin reasons.

It is wise to check that the inductor will not saturate when the maximum current is obtained taking into account I_{LIMIT1} , R_{OCP} and R_{sense} tolerances.

Since the CS pin is designed to source a current, it is not recommended to add a capacitor directly on the pin for filtering. Instead, the network of Figure 4 is actually used where the resistor R_{OCP} is split into 2 resistors R_{OCP1} and R_{OCP2} and a capacitor C_{CS} is placed between the R_{OCP1} and R_{OCP2} common node and ground. Practically, in our application, we select 1 k Ω for R_{OCP1} and R_{OCP2} and a 100 pF capacitor is implemented for C_{CS} .

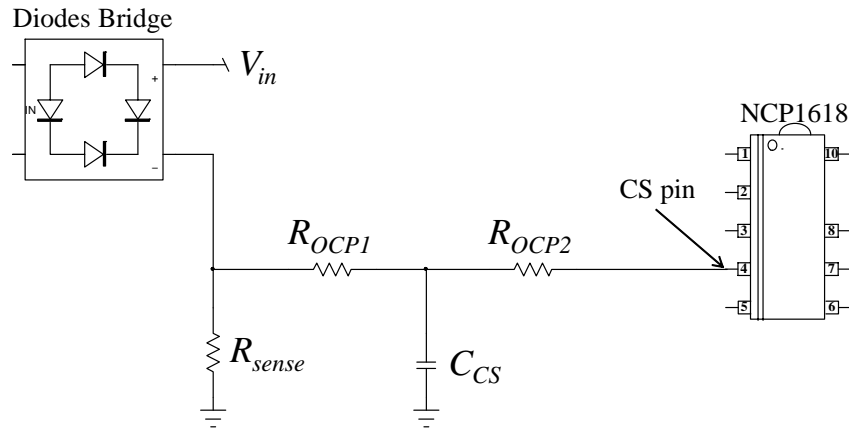


Figure 4. Filtering the CS Pin

Important notes:

- The current sense resistor sees the huge inrush current which can take place during start-up or faulty phases and must be able to sustain it in the worse conditions of the application. As shown by Figure 1, a diode can be placed across R_{sense} to divert a large part of this in-rush current. This diode is actually optional but is recommended if risks exist that the inrush stress can damage R_{sense} or if the R_{sense} voltage may become large enough to cause I_{CS} to exceed the pin max ratings. The forward voltage of the diode must be high enough not to clamp the R_{sense} voltage below the current protection levels (over-current limitation and overstress detection). The overstress threshold upper value being $330 \mu\text{A}$, the forward voltage should be higher than $(R_{OCP} * 330 \mu\text{A})$, that is, 660 mV in our case.
- The NCP1655 senses the CS pin impedance before starting operation (or before restarting operation after an interruption) and prevents MOSFET switching until it is high enough. The NCP1655 redoes it at the end of any switching cycle during which the CS pin current (I_{CS}) does not exceed the inrush level (5% of the overcurrent threshold) while the line instantaneous voltage is higher than its brown-out threshold. The circuit performs this impedance test to detect and protect the PFC stage if the CS pin is accidentally grounded. **Not to improperly detect a CS fault, R_{OCP} or $(R_{OCP1} + R_{OCP2})$ should be higher than 1.5 k Ω**

CCM Duty Ratio Control

For CCM control, the NCP1655 re-uses the proven “predictive method” scheme implemented in the NCP1653

and NCP1654 CCM PFC controllers. In other words, it directly computes the power switch on-time as a function of the inductor current. Practically, as shown by Figure 5, the V_M pin sources I_{CS} modulated by the control signal to build the CCM current information. The V_M pin signal is:

$$V_M = 0.4 \cdot R_M \cdot \frac{V_{RAMP,pk}}{V_{REGUL}} \cdot I_{CS} \quad (\text{eq. 23})$$

Where $V_{RAMP,pk}$ and R_M respectively are the peak value of the CCM PWM ramp and the V_M pin resistor value. The CCM regulation voltage (V_{REGUL}) is proportional to the regulation control signal provided by the internal regulation block ($V_{CONTROL}$) as follows for line feedforward:

- ($V_{CONTROL}$) in low-line conditions*
 - ($V_{CONTROL} / 4$) in high-line conditions*
- (*Note: The circuit detects low-line conditions if the HV pin voltage remains below 222 V for 25 ms or more (typical values – see data sheet) and it remains in low-line conditions until the HV pin voltage exceeds 236 V typically. At that moment, it enters the high-line mode.)

As detailed in the data sheet [2], this leads to the following input power expressions:

- Low-line conditions:

$$P_{in,avg} = \frac{2.5 \cdot R_{OCP} \cdot V_{in,rms}^2}{R_M \cdot R_{sense}} \cdot \frac{V_{CONTROL}}{V_{out}} \quad (\text{eq. 24})$$

- High-line conditions:

$$P_{in,avg} = \frac{0.625 \cdot R_{OCP} \cdot V_{in,rms}^2}{R_M \cdot R_{sense}} \cdot \frac{V_{CONTROL}}{V_{out}} \quad (\text{eq. 25})$$

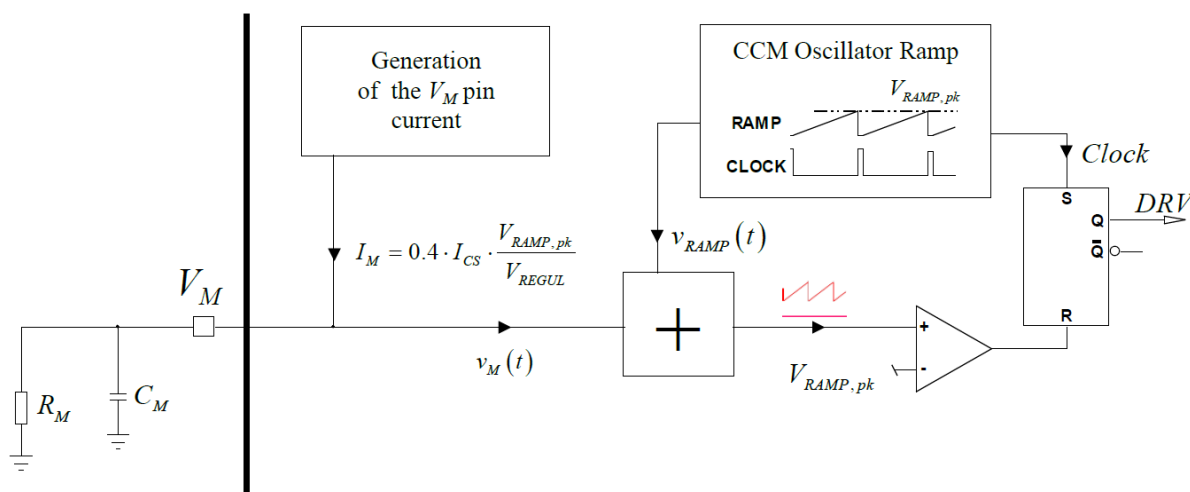


Figure 5. CCM Duty Ratio Control

As highlighted by above equations, resistor R_M adjusts the PFC stage power capability, leading to the two following R_M selection criteria:

- This resistance must be low enough for full-power

delivery: $P_{in,avg}(V_{CONTROL,max}) > \frac{P_{out,max}}{\eta}$ whatever the line magnitude is. Due to the CCM gain change in high-line conditions, we need to check that the full power can be delivered at the lowest rms voltage of both the low-line and high-line ranges:

$$R_M \leq R_{M,max} = \text{MIN} \left[\frac{2.5 \cdot R_{OCP} V_{CONTROL,max}}{(P_{in,avg})_{max} R_{sense}} \cdot \frac{(V_{in,rms})_{LL}^2}{V_{out}}, \frac{0.625 \cdot R_{OCP} V_{CONTROL,max}}{(P_{in,avg})_{max} R_{sense}} \cdot \frac{\left(\frac{V_{lineselect(LL)}}{\sqrt{2}}\right)^2}{V_{out}} \right] \quad (\text{eq. 26})$$

Where $V_{lineselect(LL)}$ is the lowest line peak voltage for high-line operation ($V_{lineselect(LL)}$ is the threshold for low-line detection – 222 V typically). Note that if the line lowest level of the application was within the high-line

range ($\sqrt{2}(V_{in,rms})_{LL} \geq V_{lineselect(LL)}$), the max value for R_M simplifies as follows:

$$R_{M,max} = \frac{0.625 \cdot R_{OCP} V_{CONTROL,max}}{(P_{in,avg})_{max} R_{sense}} \cdot \frac{(V_{in,rms})_{LL}^2}{V_{out}} \quad (\text{eq. 27})$$

- This resistance should preferably be selected so that there is no power discontinuity (constant-power transition) when the PFC stage transitions between FCCrM and CCM. In low-line conditions, $V_{CONTROL}$ is abruptly discharged to ($V_{CONTROL} / 4$) at the FCCrM to CCM transition (and charged to $4 \cdot V_{CONTROL}$ at the CCM to FCCrM transition), in order to provide a large CCM $V_{CONTROL}$ range. Due to this $V_{CONTROL}$ division by four at low line and the change in gain for feed-forward at high line (division by four), the

constant-power constraint leads to one single equation where the left side is the instantaneous power delivered in FCCrM and the right side the instantaneous power delivered in CCM just after the transition:

$$\frac{v_{in}^2(t)}{2 \cdot L \cdot f_{CCM}} \cdot \frac{V_{CONTROL}}{V_{CONTROL,max}} = 2.5 \cdot \frac{R_{OCP}}{R_M} \frac{V_{CONTROL}}{R_{sense}} \cdot \frac{v_{in}^2(t)}{V_{out}} \quad (\text{eq. 28})$$

From Eq. 28, we can deduce the following equation which provides the R_M resistance for constant–power transition:

$$R_{M,CP} = 1.25 \cdot L \cdot f_{CCM} \cdot \frac{R_{OCP}}{R_{sense}} \cdot \frac{V_{CONTROL,max}}{V_{out}} \quad (\text{eq. 29})$$

In our application, the maximum R_M value to meet the full–power delivery constraint ($R_{M,max}$) is:

$$R_{M,max} = \text{MIN} \left(\frac{2.5 \cdot 2 \cdot 10^3}{540} \cdot \frac{3.75}{0.03} \cdot \frac{90^2}{390}, \frac{0.625 \cdot 2 \cdot 10^3}{540} \cdot \frac{3.75}{0.03} \cdot \frac{157^2}{390} \right) \cong 18.3 \text{ k}\Omega \quad (\text{eq. 30})$$

The R_M value to meet the constant–power transition criterion is:

$$R_{M,CP} = 1.25 \cdot 175 \cdot 10^{-6} \cdot 65 \cdot 10^3 \cdot \frac{2 \cdot 10^3}{30 \cdot 10^{-3}} \cdot \frac{3.75}{390} \cong 9.1 \text{ k}\Omega \quad (\text{eq. 31})$$

As aforementioned, for the sake of margin, we want ($R_{M,CP}$) to be 20% below ($R_{M,max}$). This is the case here ($R_{M,CP} < 80\% \cdot R_{M,max}$). Our ($P_{in,transition}$)_{LL} selection is hence correct since with ($R_M = R_{M,CP} = 9.1 \text{ k}\Omega$), the PFC stage can provide the full power (since ($R_{M,CP}$) is less than ($80\% \cdot R_{M,max}$)) and can smoothly transition between the FCCrM and CCM modes.

Note that if ($R_{M,CP}$) was higher than ($80\% \cdot R_{M,max}$), we should increase ($P_{in,transition}$)_{LL} to be able to provide the full power and ensure a constant–power transition.

Also note that if ($R_{M,CP}$) provides the optimal value for smooth transition, a power step in the range of $\pm 50\%$ when transitioning can be managed by the circuit without a risk of erratic operation (repeated transitions between the two modes). No need hence to look for the exact computed value (as long as it remains below ($80\% \times R_{M,max}$)). In addition, a different resistance can be wished to meet some application constraints. For instance, you may want to reduce the CCM gain (using R_M closer to $R_{M,max}$) to reduce the gap between the power capability of the PFC stage and the power actually needed in your application. To that

extend, using $\left(R_M = \sqrt{0.8 \cdot R_{M,max} \cdot R_{M,CP}} \right)$ can be a good option too. In our case, we select

$\left(R_M = \sqrt{0.8 \cdot 18.3 \cdot 9.1} \cong 11 \text{ k}\Omega \right)$. A capacitor C_M is to be placed across the V_M pin to filter out the switching ripple. The time constant ($R_M \times C_M$) should be selected in the range of 100 μs , that is, sufficiently large to filter out the switching

ripple but low enough not to distort the low frequency component (that is the 100 or 120 Hz rectified sinusoid). Thus:

$$C_M \cong \frac{100 \cdot 10^{-6}}{R_M} \quad (\text{eq. 32})$$

In our application, this criterion leads to the following C_M value: 9 nF. We take the closest standard value: $C_M = 10 \text{ nF}$.

As discussed in [3], dividing the V_M resistors in two resistors as shown by Figure 2, is recommended to clean the operation at very high line where the V_M voltage is close to the threshold of the internal comparator for MOSFET turn off (3.75 V typically). If not, due to the V_M resistors inertia, the circuit may skip cycles at the top of the sinusoid.

Practically, one selects R_{M1} and R_{M2} so that the sum of them equals the computed R_M value and R_{M2} is chosen in the range of 10% of R_M . C_{M1} is computed similarly to C_M as follows:

$$C_{M1} \cong \frac{100 \cdot 10^{-6}}{R_{M1}} \quad (\text{eq. 33})$$

One can add a small capacitor C_{M2} to filter out possible surrounding noise but it must be low enough to keep a low–inertia signal across R_{M2} .

In our case, we finally opt for:

- $R_{M1} = 10 \text{ k}\Omega$
- $R_{M2} = 1 \text{ k}\Omega$
- $C_{M1} = 10 \text{ nF}$
- No C_{M2} capacitor

Power Components

Diodes Bridge

The diodes bridge is mainly selected based on the voltage it must sustain and on the power it must dissipate. [5] shows that a good approximate value of the maximum power loss is given by:

$$P_{\text{bridge}} = \frac{4\sqrt{2}}{\pi} \cdot V_f \cdot \frac{(P_{\text{out}})_{\text{max}}}{\eta} \cong 1.8 \cdot V_f \cdot \frac{500}{90} \cong 11 \cdot V_f \quad (\text{eq. 34})$$

Assuming a 0.85 V forward voltage per diode ($V_f = 0.85$ V), the bridge approximately dissipates 9.4 W. Diodes bridge GSIB1580 from Vishay is implemented. A 4.5 °C/W heatsink (SK481–50 from Fischer Elektronik) limits the temperature rise to about 45 degrees.

Boost Diode

As discussed in [6], the boost diode selection is critical in CCM applications. The diode current at its turn-off being non-zero, reverse recovery leads to dissipation in the diode and in the MOSFET. For best efficiency ratios, a SiC diode (FFSPF0865A from ON Semiconductor) is selected.

The output diode conduction losses can be roughly approximated to $(I_{\text{out,max}} \cdot V_f)$, where $I_{\text{out,max}}$ is the load maximum current and V_f the diode forward voltage. The maximum output current being nearly 1.3 A (500 W / 390 V), the diode conduction losses are roughly estimated in the range of 2.6 W (assuming $V_f = 2.0$ V – max instantaneous forward voltage @ 125°C and 8 A specified in the FFSPF0865A data sheet).

Power MOSFETs

The MOSFET is selected based on the peak voltage stress ($V_{\text{out,max}} + \text{margin}$) and on the maximum rms current flowing through it ($(I_{Q,\text{rms}})_{\text{max}}$) which can be approximated using the following equation:

$$(I_{Q,\text{rms}})_{\text{max}} \cong (I_{L,\text{rms}})_{\text{max}} \cdot \sqrt{1 - \frac{8\sqrt{2} \cdot (V_{\text{in,rms}})_{\text{LL}}}{3\pi \cdot V_{\text{out,nom}}}} \quad (\text{eq. 35})$$

In our application, Eq. 35 leads to:

$$(I_{Q,\text{rms}})_{\text{max}} \cong 6.2 \cdot \sqrt{1 - \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 390}} \cong 5.3 \text{ A} \quad (\text{eq. 36})$$

A FCPF067N65 MOSFETs from ON Semiconductor is selected, which exhibits a maximum drain-to-source on-resistance ($r_{\text{DS(on)}}$) of 67 mΩ @ 25 °C. Considering a 100% $r_{\text{DS(on)}}$ increase at high temperature, the maximum conduction losses are given by:

$$(P_{\text{cond}})_{\text{max}} \cong 200\% \cdot (r_{\text{DS(on)}})_{25^\circ\text{C}} \cdot 5.3^2 \cong 2 \cdot 0.067 \cdot 5.3^2 \cong 3.8 \text{ W} \quad (\text{eq. 37})$$

It is hard to predict MOSFET switching losses precisely. They highly depend on the diode choice, on the MOSFET drive speed and on the possible presence of some snubbing circuitry. Hence, their prediction is a tough and inaccurate exercise that will not be made in this paper. Instead, we will place the MOSFET and the boost diode on the same heat-sink and consider that as a rule of the thumb, the total power to be dissipated by the heatsink is 4% of the output power. (Note: We rather consider 6% of the output power if the diode bridge is placed on the heatsink. In a single-mains application, this figure could be halved.)

Note that to further improve the efficiency, the MOSFET opening can be accelerated using the schematic of Figure 6, where Q_1 , a small pnp transistor, amplifies the MOSFET turn off gate current.

Even better a MOSFET driver can be used to speed-up both transitions and in addition, ease the board layout by placing the driver close to the MOSFET and then minimize the loop area of the high-current traces. This is the selected approach. A small SOT23–5 FAN3100 driver is implemented in our application.

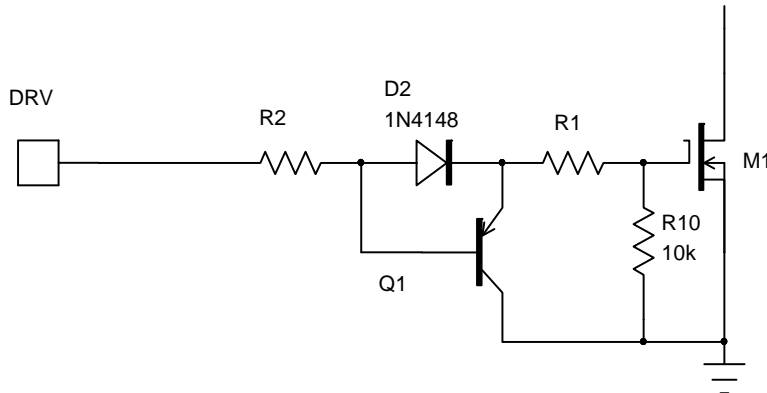


Figure 6. Q_1 Speeds Up the MOSFET Turn Off

Heatsinks

Like in [4], as a rule of thumb, one can estimate that the total power dissipated by the silicon components (diodes bridge, boost MOSFET and diode) is in the range of:

- 6% of the output power in wide-mains applications
- 3% of the output power in single-mains applications.

Such a losses budget to be dissipated by heatsinks and other cooling elements is supposed to be pessimistic. If experimental tests show that they are worse, the design and/or the components selection must be tweaked if it wished to meet an efficiency of 92% or more.

No fan is implemented in our 500 W application. It is cooled down by the heatsinks as follows:

- The diodes bridge is fitted on a 4.5 °C/W heatsink (SK481-50 from Fischer Elektronik) to limit its temperature rise to about 45 °C (about 9.4 W being dissipated)
- The two MOSFETs and the boost diodes share a second heat-sink. Assuming that as a rule of thumb, it will have to dissipate 4% of P_{out} ($4\% \cdot 500 \text{ W} \cong 20 \text{ W}$), a 2.8 °C/W heat-sink (ref. SK481-50 from Fischer Elektronik) is implemented which limits the temperature rise to about 56 °C compared to the ambient temperature.

Bulk Comparator Design

In addition to the rated voltage, the output capacitor is generally designed considering the 3 following factors:

- The maximum permissible low-frequency ripple of the output voltage. The input current and voltage being both sinusoidal, PFC stages deliver a squared sinusoidal power that matches the load power demand in average only. As a consequence, the output voltage exhibits a low frequency ripple (e.g., 120 Hz in USA) that is inherent to the PFC function.
- The rms current flowing through the bulk capacitor. Based on this computation, one must estimate the maximal permissible ESR for an acceptable heating.
- The hold-up time specification. The hold-up time is the time for which the power supply must keep providing the full power while the line is gone. The

duration of the mains interruption (hold-up time) is generally in the range of 10 or 20 ms.

The output voltage peak-to-peak ripple is given by:

$$\Delta V_{out(p-p)} = \frac{P_{out}}{2\pi \cdot f_{line} \cdot C_{bulk} \cdot V_{out,nom}} \quad (\text{eq. 38})$$

This ripple must keep lower than $\pm 4\%$ of the output voltage (8% peak-to-peak) not to trigger the DRE and OVP functions in normal operation. Thus, we can derive the bulk capacitance necessary to avoid too large a low-frequency ripple:

$$C_{bulk} \geq \frac{P_{out,max}}{2\pi \cdot (f_{line})_{min} \cdot 8\% \cdot V_{out,nom}^2} \quad (\text{eq. 39})$$

In our application, taking into account the line frequency minimum value (47 Hz), this leads to:

$$C_{bulk} \geq \frac{500}{2\pi \cdot 47 \cdot 8\% \cdot 390^2} \cong 139 \mu\text{F} \quad (\text{eq. 40})$$

The following equation gives an approximate value of the capacitor rms current:

$$I_{C(rms)} \cong \sqrt{\left((I_{L,rms})^2 \cdot \frac{8\sqrt{2} \cdot V_{in,rms}}{3\pi \cdot V_{out}} \right) - \left(\frac{P_{out}}{V_{out,nom}} \right)^2} \quad (\text{eq. 41})$$

We can derive from Eq. 41 the following estimate of the bulk capacitor maximum rms current:

$$I_{C(rms)max} \cong \sqrt{\left((6.2)^2 \cdot \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 390} \right) - \left(\frac{500}{390} \right)^2} \cong 3.0 \text{ A} \quad (\text{eq. 42})$$

Finally the following expression expresses the minimum bulk capacitance necessary to meet a specified hold-up time ($t_{hold-up}$), where $V_{out,min}$ is the minimum bulk voltage for proper operation of the downstream converter:

$$C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{hold-up}}{V_{out}^2 - V_{out,min}^2} \quad (\text{eq. 43})$$

The hold-time being not considered here, a 330 μF / 450 V capacitor (861141486022 from Wurth Elektronik) is chosen to satisfy the two other above conditions.

Powering the Circuit

The NCP1655 is ideal in applications where an external power source (provided by an auxiliary power supply or from the downstream converter) feeds the circuit. The maximum level of the V_{CC} start-up threshold (11.25 V) is low enough so that the circuit can be powered from typical

12 V voltage rails. The auxiliary source (V_{CC0} of Figure 7) is often applied through a switch which can abruptly turn on and off. Note that in this case, it is recommended to limit the V_{CC} pin dV/dt by adding a small resistor (R_1) particularly if the V_{CC} capacitor (C_1) is small. As an example, R_1 can be $22\ \Omega$ and C_1 , 220 nF.

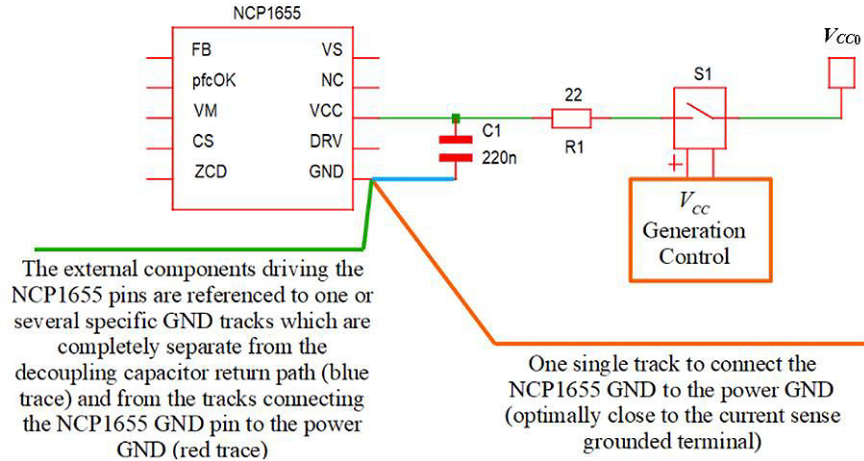


Figure 7. Powering the NCP1655

Sequencing Management

Forward or half-bridge converters take a significant advantage of a narrow input voltage range. In such applications, the PFC stage is expected to start first and to keep on as long as the power supply is plugged in, so that the downstream converter is disabled until the output of the PFC stage is nominal. The NCP1655 features a “*pfcOK*” pin to enable/disable the downstream converter. Practically, it is in high state when the PFC stage is in nominal state and low otherwise (fault or start-up condition). In particular, the *pfcOK* pin is grounded if a line brown-out or a bulk under-voltage is detected.

As aforementioned, the *pfcOK* pin is designed to control the operation of the downstream converter. It is in high state when the PFC stage is in nominal operation. On the contrary, the *pfcOK* pin is grounded when the PFC stage is in start-up phase or in a fault condition. Using the *pfcOK* signal to enable/disable it, the downstream converter can be optimally designed for the narrow voltage range nominally provided by the PFC stage in normal operation.

When in high state, the *pfcOK* pin sources a current proportional to the feedback voltage ($k \cdot V_{FB}$), where k is 10 $\mu\text{A/V}$ typically. In other words, the *pfcOK* pin typically

sources 25 μA when the FB voltage is 2.5 V (regulation level). An external resistor is to be placed between the *pfcOK* and GND pins to obtain a voltage V_{pfcOK} which is proportional to the bulk voltage and can serve as a feedforward signal for the downstream converter.

In our application, a 56 k Ω resistor is used so that the *pfcOK* voltage is ($56 \cdot 10^3 \cdot 25 \cdot 10^{-6} = 1.4\ \text{V}$) when the output voltage is nominal. A capacitor should be placed between the *pfcOK* and ground pins for decoupling. The pin should not be too much filtered not to degrade the feedforward function. A good trade-off generally consists setting the filter corner frequency about 5 times higher than the line frequency:

$$C_{pfcOK} \leq \frac{1}{10\pi \cdot R_{pfcOK} \cdot (f_{line})_{max}} \tag{eq. 44}$$

In our case, Eq. 44 leads to:

$$C_{pfcOK} \leq \frac{1}{10\pi \cdot 56 \cdot 10^3 \cdot 63} \cong 9\ \text{nF} \tag{eq. 45}$$

A 10 nF ceramic capacitor is placed between the *pfcOK* and GND pins for decoupling.

Input Voltage Sensing

The V_S pin provides access to the brownout and line range detectors. The brownout detector detects too low line levels and the line range detector determines the presence of either 110 V or 220 V ac mains. Depending on the detected input voltage range device parameters are internally adjusted to optimize the system performance. As shown by Figure 8, the V_S pin should be connected to the rectified voltage through a diode (D_{HV1}). The diode prevents the pin voltage from going below ground. A resistor in series with the diode (R_{HV1}) can be used for protection. It should be less than 20k not to alter the accuracy of the input voltage measurement.

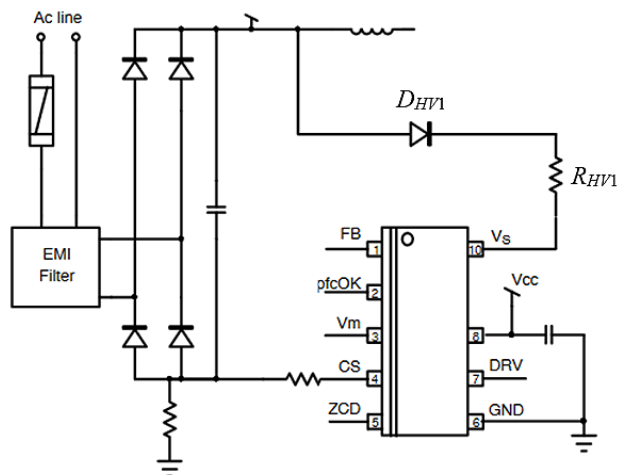


Figure 8. High-Voltage Input Connection

The brown-out protection prevents the controller from starting operation until the V_S pin voltage exceeds the upper brownout threshold, $V_{BO(start)}$, typically 95 V. The brown-out protection trips and prevents operation if the V_S pin voltage remains below the lower brownout threshold ($V_{BO(stop)}$) of 87 V typically, for the brownout timer (650 ms typically). The timer is set long enough to pass line-dropout tests. Note that when the line recovers, the circuit does not resume operation until V_{CC} is above the start-up threshold ($V_{CC(on)}$) of 10.5 V typically) so that a clean restart is obtained.

“High-line” is detected when the V_S pin exceeds the high-line select threshold, $V_{lineselect(HL)}$, typically 236 V. The controller switches back to “low-line” mode if the V_S pin voltage remains below $V_{lineselect(LL)}$ (which is 222 V typically) for the t_{line} timer delay (25 ms typically). If the controller transitions to “low-line”, it is prevented from switching back to “high-line” until the lockout timer $t_{line(lockout)}$ (typically 515 ms), expires. The line range detection circuit optimizes the operation for wide-mains applications. Practically, in “high-line”:

- The regulation bandwidth and the CCM gain are divided by 4
- The $V_{CONTROL}$ threshold below which frequency foldback starts is divided by two

Feedback Network

The output voltage of the PFC stage is externally scaled-down by a resistors divider (R_{FB1} and R_{FB2} of Figure 2) and monitored by the feed-back input (pin1). The bias current of the feedback pin is minimized (less than 500 nA) to allow the use of a high-impedance feed-back network. It is neglected in below calculations. The feedback voltage must equate the internal reference voltage ($V_{REF} = 2.5$ V) when V_{out} is nominal. In other words:

$$\frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot V_{out,nom} = V_{REF} \quad (\text{eq. 46})$$

Or:

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{out,nom}}{V_{REF}} - 1 \quad (\text{eq. 47})$$

Another constraint on the feedback resistors relates to the power R_{FB1} and R_{FB2} dissipate as they are biased by the V_{out} high-voltage rail (in the range of 390 V typically). If the impedance ($R_{FB1} + R_{FB2}$) is low, R_{FB1} and R_{FB2} can easily consume several hundreds of milliwatts and jeopardize the standby performance.

In steady-state, the feedback voltage is in the range of the 2.5 V regulation reference voltage (V_{REF}). The nominal feedback bias current can hence be defined as a function of feedback bottom resistor (R_{FB2}) as follows:

$$I_{FB} = \frac{V_{REF}}{R_{FB2}} \quad (\text{eq. 48})$$

Trade-off between losses and noise immunity dictates the choice of this resistor. Resistors up to 56 k Ω ($I_{FB} \cong 50$ μ A) generally give good results. Higher values can be considered if allowed by the board PCB layout and if the impedance remains compatible which the 250 nA sink current (500 nA max. on the -40 $^{\circ}$ C to 125 $^{\circ}$ C temperature range) built-in to ground the feedback pin and disable the driver if the pin is accidentally open. If I_{FB} is set below 50 μ A, the regulation level may be significantly impacted by the 250 nA sink current. In our application, we target a bias current in the range of 100 μ A which generally gives a good trade-off between losses and noise immunity. This criterion leads to:

$$R_{FB2} = \frac{V_{REF}}{100 \mu A} = 25 \text{ k}\Omega \quad (\text{eq. 49})$$

($R_{FB2} = 27$ k Ω) is finally selected. Following Eq. 47, R_{FB1} is given by:

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1 \right) \quad (\text{eq. 50})$$

We target a 390 V regulation level, hence:

$$R_{FB1} = 27 \text{ k}\Omega \cdot \left(\frac{390}{2.5} - 1 \right) = 4185 \text{ k}\Omega \quad (\text{eq. 51})$$

For safety reasons, several resistors should be placed in series instead of a single R_{FB1} resistor. In our application, we

choose a (1800 kΩ + 1800 kΩ + 560 kΩ) network. This selection together with ($R_{FB2} = 27 \text{ k}\Omega$) leads to:

$$V_{\text{out,nom}} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot V_{\text{REF}} = \frac{1800 + 1800 + 560 + 27}{27} \cdot 2.5 \text{ V} \cong 388 \text{ V} \quad (\text{eq. 52})$$

Zero Current Detection (ZCD)

The NCP1655 optimizes the efficiency by turning on the MOSFET at the very valley when operating in critical and discontinuous conduction modes. For this purpose, the circuit is designed to monitor the voltage of a small winding taken off of the boost inductor. This auxiliary winding (called the “zero current detector” or ZCD winding) gives a scaled version of the inductor voltage which is easily usable by the controller. The PFC stage being a boost converter, the auxiliary winding provides:

- $V_{\text{AUX}} = -\frac{N_{\text{AUX}}}{N_p} \cdot v_{\text{in}}(t)$ during the MOSFET conduction time
- $V_{\text{AUX}} = \frac{N_{\text{AUX}}}{N_p} (V_{\text{out}} - v_{\text{in}}(t))$ during the demagnetization time. This voltage used to detect the zero current detection can be small when the input voltage is nearly the output voltage.
- A voltage oscillating around zero during dead-times

The NCP1655 embeds an internal comparator to monitor such a signal. Practically, during the off-time, it compares the ZCD pin voltage to an upper threshold V_{ZCDH} (1 V typically) and to a lower threshold V_{ZCDL} (0.5 V typically) to detect falling edges of the ZCD signal, these events being indicative of the end of the demagnetization phase and/or of the valleys of the MOSFET Drain-source voltage.

The signal delivered by the auxiliary winding (V_{AUX}) hence depends on the turns ratio (N_p / N_{AUX}). Ideally, this turns ratio should be sized so that V_{AUX} exceeds the ZCD upper threshold during the demagnetization phase in all operating conditions. V_{AUX} is minimal at the top of the highest line sinusoid, leading to:

$$\frac{N_p}{N_{\text{AUX}}} \leq \frac{V_{\text{out}} - (\sqrt{2} \cdot (V_{\text{in,rms}})_{\text{HL}})}{V_{\text{ZCDH}}} \quad (\text{eq. 53})$$

With $((V_{\text{in,rms}})_{\text{HL}} = 265 \text{ V})$ and $(V_{\text{out}} = 390 \text{ V})$, (N_p / N_{AUX}) must be lower than 15. A turns ratio of 10 was selected for this design.

A resistor, R_{ZCD1} is to be added between the auxiliary winding and the ZCD pin. This resistor limits the current flowing into or out of pin 5. This current must be kept below 2 mA (sink and source). In general, the pins are the most stressed by the sink current obtained at high line. Hence, R_{ZCD1} must be selected high enough so that:

$$R_{\text{ZCD1}} \geq \frac{\frac{N_{\text{AUX}}}{N_p} \cdot \sqrt{2} \cdot (V_{\text{in,rms}})_{\text{HL}}}{I_{\text{ZCD}}} = \frac{\sqrt{2} \cdot 265}{2 \cdot 10^{-3} \cdot 10} \cong 19 \text{ k}\Omega \quad (\text{eq. 54})$$

A 27 kΩ was selected.


Note that in critical or discontinuous conduction mode, the very moment when the next drive pulse begins depends on the time constant formed by this resistor and the small parasitic capacitance of the ZCD pin. Ideally, the MOSFET must turn on when its drain-source voltage is the valley. This will minimize switching losses. A small capacitor (C_{ZCD1} of Figure 2) may have to be added on the ZCD pin to accomplish this. The C_{ZCD1} value this is best found experimentally.

Important Note: the circuit detects cases where the ZCD pin is accidentally grounded by making a test of the ZCD pin impedance whenever no falling edge of the auxiliary winding can be detected. In such a case, no DRV pulses are generated until the pin impedance is detected high enough. Not to improperly trigger the protection, the external ZCD network should be selected so that the pin impedance is above 7.5 kΩ. In above example, R_3 is 10 kΩ, which meets this criterion.

Layout and Noise Immunity Considerations

The NCP1655 is not particularly sensitive to noise. However, usual layout rules for power supply apply. Figure 7 summarizes some of them. However, let us remind the following:

- The loop area of the power train must be minimized
- Star configuration for the power ground that provides the current return path
- Star configuration for the circuit ground
- The circuit ground and the power ground should be connected by one single path
- This path should preferably connect the circuit ground to the power ground at a place that is very near the grounded terminal of the current sense resistor (R_{SENSE}).
- A ceramic capacitor (220 nF or more) should be placed between the circuit V_{CC} and GND pins, with a minimized connection length. Limit the dV/dt when applying or removing a power source to power the circuit. If necessary, add a resistor to limit the edges. See the “Powering the circuit” section.
- The components (resistors or capacitors) that program the circuit operation must be placed as close as possible to the pin they drive.
- As aforementioned, it is furthermore recommended to filter the signal applied to the FB , CS , pfcOK , V_M and ZCD pins to protect them from possible surrounding noise. It must not be excessive however not to distort the voltage sensed by these pins. See the corresponding sections for more details.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative