AND90010/D

Power Supply Sequence of LC823455 Series for Audio Applications

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APPLICATION NOTE

Introduction

This application note describes a guideline of power supply sequence for desired application.

The intended audience is customers who are developing audio applications using the LC823455 Series (called LC823455 hereafter).

BACKGROUND

LC823455 has multiple power supply terminals, which are classified into the following seven power supply groups according to their roles.

(1) Internal core power supply
(2) RTC power supply
(3) 1 V series analog power supply
(4) DAMP power supply
(5) External IO power supply
(6) 1.8 V series analog power supply
(7) 3 V series analog power supply

This application note describes power supply sequence about these power supply groups.

Power Supply Terminals

Table 1 shows the voltage requirements for the power supply terminals of LC823455 within the different power supply groups.

Table 1. POWER SUPPLY TERMINALS

Group	Symbol	Low operation (V)	High operation (V)	Note
(1) Internal core	Vdd1	0.95 − 1.155	1.05 − 1.155	
(2) RTC	VddRTC	0.765 − 0.90		(*1)
		0.90 − 1.155		
(3) 1 V series analog	VddXT1	0.95 − 1.155		For X'tal : 12 MHz, 19.2 MHz, 24MHz
	AVddPLL1	0.95 − 1.155		
	AVddPLL2	0.95 − 1.155		
	DVddUSBPHY1	0.93 − 1.1		(*2)
(4) DAMP	AVddDAMPL	0.95 − 1.65		(*3)
	AVddDAMPR	0.95 − 1.65		(*3)
(5) External IO	Vdd2	1.7 − 1.95		For 1.8 V interface
		2.7 − 3.6		For 3.3 V interface
	VddSD1	1.7 − 1.95		For 1.8 V interface
		2.7 − 3.6		For 3.3 V interface
(6) 1.8V series analog	AVddADC	1.7 − 1.95		
	AVddUSBPHY18	1.7 − 1.95		(*2)
(7) 3 V series analog	AVddUSBPHY2	3.07 − 3.6		(*2)
Internal clock frequency (For Cortex−M3, LPDSP32, AHB, APB)		max 115 MHz	max 170 MHz	

Ta = −20°C to +65°C

(*1) APB clock needs 57.5 MHz or less.
(*2) While USB is used (including USB suspend mode).
(*3) While the terminal is used not as GPO (general purpose output) but as headphone amp.

In some packages of LC823455, XTALINFO[1:0] terminal is not prepared. It is set internally in accordance with the prescribed frequency of XT1. The frequency of XT1 other than 12, 19.2, 24 MHz may cause functional error during ROM boot, because some internal clock frequencies are determined automatically according to the XTALINFO[1:0] input and connected XT1 frequency .

The Low operating condition in the table indicates that the internal clock frequency can run up to 115 MHz. In contrast, the High operating condition indicates that the internal clock frequency can run up to 170 MHz. Vdd1 is the power supply terminal of the internal digital core. If you wish to achieve low power consumption with the LC823455, it should be run in the Low operating condition with a voltage lower than 1.05 V (for example, 1.0 V) supplied to Vdd1. If you wish to achieve high performance with the LC823455, it should be run in the High operating condition with a voltage higher than 1.05 V (for example, 1.1 V) supplied to Vdd1.

VddXT1 is the power supply terminal of the X'tal oscillator and is supplied with the voltage range showed in the table – for example, 1.0 V. LC823455 may be clocked with a X'tal oscillator running at frequency of 12 MHz, 19.2 MHz, or 24 MHz. Any frequencies other than these are not permitted because they may cause functional errors during ROM boot.

There are two PLL functions. PLL1 is for system PLL and PLL2 is for audio PLL. AVddPLL1 is the power supply terminal of PLL1 and AVddPLL2 is that of PLL2. The voltage range of the power supply terminal of both PLL1 and PLL2 is the same as VddXT1 as per the table.

All the power supply terminals of LC823455 have to be supplied with their regulated voltage listed in the table even if some of the functions related to each power supply terminal are not used in your application. For example, even if RTC is not used, VddRTC has to be supplied with its regulated voltage. Even if the 12−bit ADC is not used, VddADC has to be supplied with its regulated voltage.

There are two power supply terminals in the External IO group. They can be individually supplied with two voltage levels based on the application. One is for a 1.8 V IO interface and the other is for a 3.3 V IO interface. Regarding the IO voltage selection for the Vdd2 IO group, you must control the IO18V terminal by either setting it to Low for a 3.3 V IO interface or setting it to High for a 1.8 V IO interface. In addition, the voltage level supplied to the IO18V terminal is Vdd1. Regarding the IO voltage selection for the VddSD1 IO group, you must control a register in “System Controller” described in the “System Functions User’s Manual”. For either IO group, when setting the 1.8 V IO interface, even for extremely short periods of time, you must supply not only the 3.3 V voltage range but also the voltage over the 1.8 V voltage range to each power supply terminal (Vdd2 or VddSD1).

Power Supply Sequence

The basic power supply sequence is in the order shown below (1, 2, 3). In addition, it is acceptable to simultaneously power on and off different power supply groups.

When powering on:

1. Powering on the internal power supply terminals
2. Powering on the external I/O power supply terminals
3. Providing signals to the external I/O terminals

When powering off:

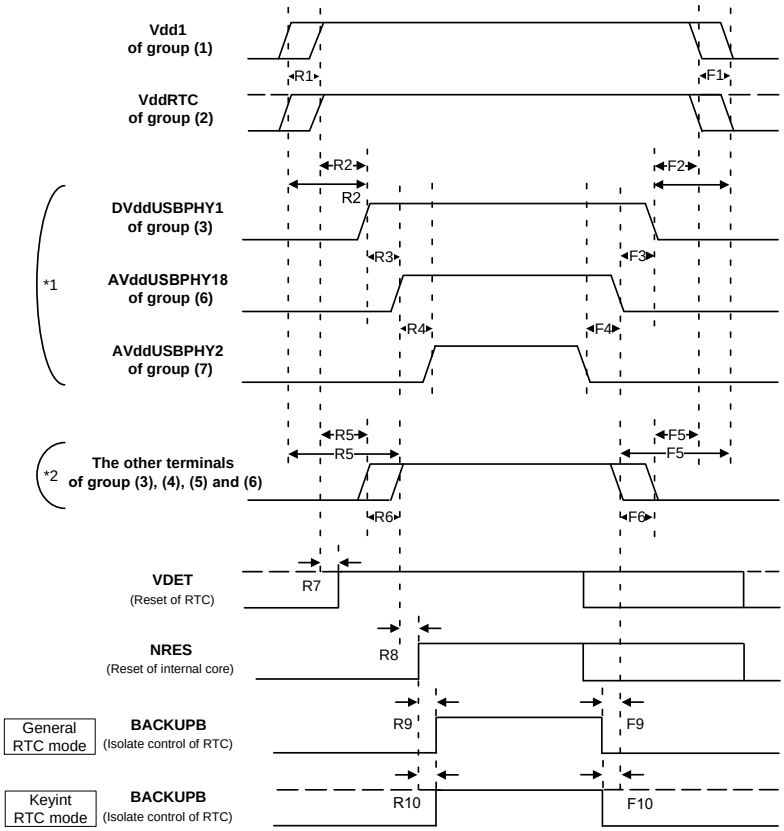
1. Removing signals from the external I/O terminals
2. Powering off the external I/O power supply terminals
3. Powering off the internal power supply terminals

Powering on the external I/O power supply terminals while the internal power supply terminals are not supplied might cause some glitches on the I/O signals and some flow of through current inside. To avoid it, the sequence above is recommended as the basic sequence.

Figure 1 shows the power supply sequence of LC823455. The Rise Time period is shown as Rn and the Fall Time period is shown as Fn in Figure 1.

Vdd1 is the internal core power supply terminal, therefore Vdd1 must be powered on first. VddRTC is the RTC power supply terminal. The RTC block may become electrically independent during General RTC mode or Keyint RTC mode. In these modes, all power domains except the RTC power domain may be powered off by controlling the external regulators while keeping the RTC timer working correctly. This requires that VddRTC is also powered on first. The timing relation between Vdd1 and VddRTC doesn’t have any constraint (R1), because VddRTC is an independent power supply terminal.

Regarding the power supply terminals (*1) related to the USB block, after powering on both Vdd1 and VddRTC, DVddUSBPHY1 has to be powered on within max 10 ms (R2). Then, AVddUSBPHY18 has to be powered on within max 10 ms (R3) after DVddUSBPHY1, and then, AVddUSBPHY2 has to be powered on within max 10 ms (R4) after AVddUSBPHY18.



Group	Symbol
(1) Internal core	Vdd1
(2) RTC	VddRTC
(3) 1 V series analog	VddXT1
	AVddPLL1
	AVddPLL2
	DVddUSBPHY1
(4) DAMP	AVddDAMPL
	AVddDAMPR
(5) External IO	Vdd2
	VddSD1
(6) 1.8V series analog	AVddADC
	AVddUSBPHY18
(7) 3 V series analog	AVddUSBPHY2

Rise Timing	Fall Timing	Min	Max
R1, R6	F1, F6	There is no constraint.	
R2, R3, R4, R5	F2, F3, F4, F5	0 ms	10 ms
R7, R8	–	400 μs	–
R9, R10	F9, F10	0 ns	–

Note: *2 shows any power supply terminals in the group (3), (4), (5) and (6) except the combination of *1.
Note: WLCSP120 doesn t have BACKUPB terminal and is fixed to Keyint RTC mode internally.

Figure 1. Power Supply Sequence

Regarding the other power supply terminals (*2) in group (3), (4), (5) and (6) except the USB power supply terminals, after powering on both Vdd1 and VddRTC, they have to be powered within max 10 ms (R5). Also, the timing relation among them doesn't have any constraint (R6).

Of course, simultaneous power supply on of R1, R2, R3, R4, R5, and R6 is acceptable.

As for powering off, the power supply terminals must be powered off according to the basic power supply sequence as shown in Figure 1 (F1, F2, F3, F4, F5, and F6).

Simultaneously powering off F1, F2, F3, F4, F5, and F6 is acceptable as well.

VDET is the reset signal of RTC and is active low. It has to be released to high level after low level is given to it for at least 400 μs after VddRTC is powered on and while it is supplied (R7).

NRES is the main reset signal of the internal core and is active low. It also has to be released to high level after low level is given to it for at least 400 μs after all power supply terminals are powered on and while they are supplied (R8).

BACKUPB is the isolate control terminal which means that all power domains except the RTC power domain can be powered off. When it is set to low, the RTC power domain is separated from the other power domains electrically. When it is at a high level, both of the domains are connected electrically.

In General RTC mode, in order to power off the power domains except RTC, you must control the timing of BACKUPB correctly as shown in Figure 1. BACKUPB must be released to a high level after NRES is released to a high level at power on (R9), and then, it must be set to a low level before any one of the power domains except RTC is powered off (F9). In other words, the power domains except RTC can be powered off while BACKUPB is set to low, and they must continue being supplied while BACKUPB is set to high.

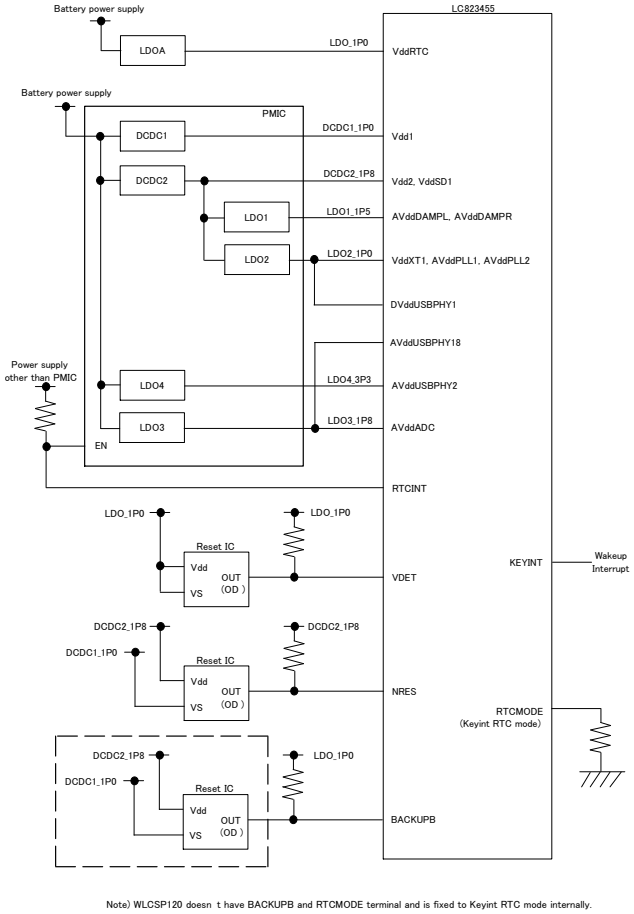
In Keyint RTC mode, LC823455 has an internal isolate control signal generated by a sequencer in the RTC block, and isolation is controlled by this internal isolate control signal as well as BACKUPB. The sequencer can control the isolation of the power domains automatically even when power supply voltage is supplied to LC823455 at first, so it is usually acceptable to tie off BACKUPB to a high level as shown with the broken line in Figure 1. However, when you need to control the isolation from outside of LC823455 with no relation to the internal sequencer, for example, over a short period of time when changing the battery while keeping RTC working precisely thanks to charged capacitors, BACKUPB must be controlled as shown with the solid line as well as General RTC mode (R10, F10).

Example of Power Supply Voltage

Table 2 shows an example of power supply voltages for LC823455. The voltage setting is suitable to the Low operating condition for low power consumption. Figure 2 shows an example of power supply structure according to Table 2 with Keyint RTC mode.

Table 2. EXAMPLE OF POWER SUPPLY VOLTAGE

Group	Symbol	Voltage (V)	Supply source	Note
(1) Internal core	Vdd1	1.0	DCDC1	
(2) RTC	VddRTC	1.0	LDOA	
(3) 1 V series analog	VddXT1	1.0	LDO2 (supplied by DCDC2)	For X'tal : 12 MHz, 19.2 MHz, 24MHz
	AVddPLL1	1.0		
	AVddPLL2	1.0		
	DVddUSBPHY1	1.0		
(4) DAMP	AVddDAMPL	1.5	LDO1 (supplied by DCDC2)	
	AVddDAMPR	1.5		
(5) External IO	Vdd2	1.8	DCDC2	For 1.8 V interface
	VddSD1	1.8		For 1.8 V interface
(6) 1.8V series analog	AVddADC	1.8	LDO3	
	AVddUSBPHY18	1.8		
(7) 3 V series analog	AVddUSBPHY2	3.3	LDO4	



Note) WLCSP120 doesn t have BACKUPB and RTCMODE terminal and is fixed to Keyint RTC mode internally.

Figure 2. Example of Power Supply Structure

In this example, two DCDC converters and five LDOs are used for the power supply terminals of LC823455. The battery is connected to DCDC1, DCDC2, LDO3, LDO4 and LDOA as a power supply source, and then DCDC2 is connected to LDO1 and LDO2 as a power supply source to save the battery current consumption as much as possible. The DCDCs and LDOs supply each voltage to the power supply terminals as shown in Table 2.

The PMIC in Figure 2 has DCDCs and LDOs other than LDOA for the RTC group (2) with an enable pin. The enable pin is controlled to power on/off by RTCINT terminal in Keyint RTC mode with a pull up resistor tied to any power supply other than the power supply that the PMIC generates.

LDOA for RTC has to continue supplying voltage to VddRTC independently in Keyint RTC mode so as to power off all the power supply terminals except VddRTC.

In Keyint RTC mode, for example, if you need to change the battery over a short time period while keeping RTC working precisely, the circuit in the rectangle surrounded by the broken outline in Figure 2 must be implemented at BACKUPB.

In contrast, if you do not need to change the battery, you do not need to implement the circuit in the rectangle surrounded by the broken outline, and it is acceptable to tie off BACKUPB with a pull− up resister to the power supply for VddRTC, or connect BACKUPB to the same signal as VDET.

Figure 3 shows an example circuit diagram where RTC is not used. If you don't use the RTC block, you may tie off the XIN32K terminal to VssRTC GND shown in Figure 3. If you use the RTC block, you must connect a 32.768 kHz Xtal oscillation circuit to the XIN32K and XOUT32K terminals. In either case, an appropriate voltage within the specified voltage range must be supplied to VddRTC.

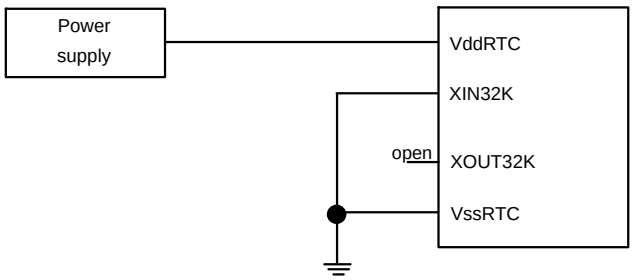


Figure 3. Example Circuit Diagram where RTC is Not Used

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