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AND90009/D

LV5980MC Step-Down Switching Regulator

Low Power Consumption and High Efficiency

ON Semiconductor®

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APPLICATION NOTE

INTRODUCTION

The LV5980MC is a fixed 370 kHz, high−output−current, Non−synchronous PWM converter that integrates a low−resistance, high−side MOSFET and a Customer Chosen, External Diode for the rectification. The LV5980MC utilizes externally compensated current mode control to provide good transient response, ease of implementation, and excellent loop stability. It regulates input voltages from 4.5 V to 23 V down to an output voltage as low as 1.235 V and is able to supply up to 3.0 A of load current. The LV5980MC includes Power Save Feature to enhance efficiency during Light Load. In low consumption mode, the device show operating current of 63 μA from VIN by shutting down unnecessary circuits.

Key Features

- Power Save Feature
- Enhanced Light Load Efficiency
- Low Consumption Mode (I_{SLEEP} 63 μA)
- High Efficiency (100 mΩ High−Side MOSFET)
- 4.5 V to 23 V Operating Input Voltage Range
- Fixed 370 kHz PWM Operation
- Pulse−by−Pulse Current Limiting
- Short Circuit Protection
- Programmable Soft Start
- Thermal Shutdown

EVALUATION BOARD PERFORMANCE SUMMARY

Parameter	Rating			Unit
	Min	Typ	Max	
Input Supply Voltage	8	15	20	V
Output Voltage	−	5	−	V
Current Limit Peak	3.5	4.7	6.2	A
Oscillatory Frequency	−	370	−	kHz

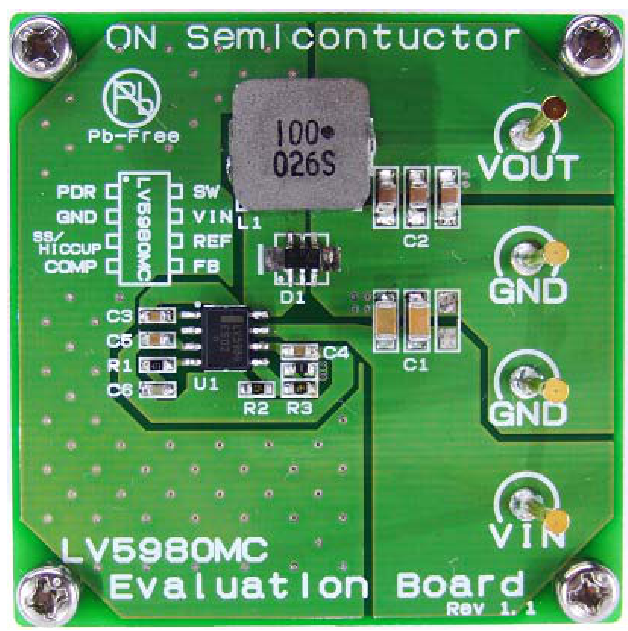

Figure 1. LV5980MC Evaluation Board

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Block Diagram

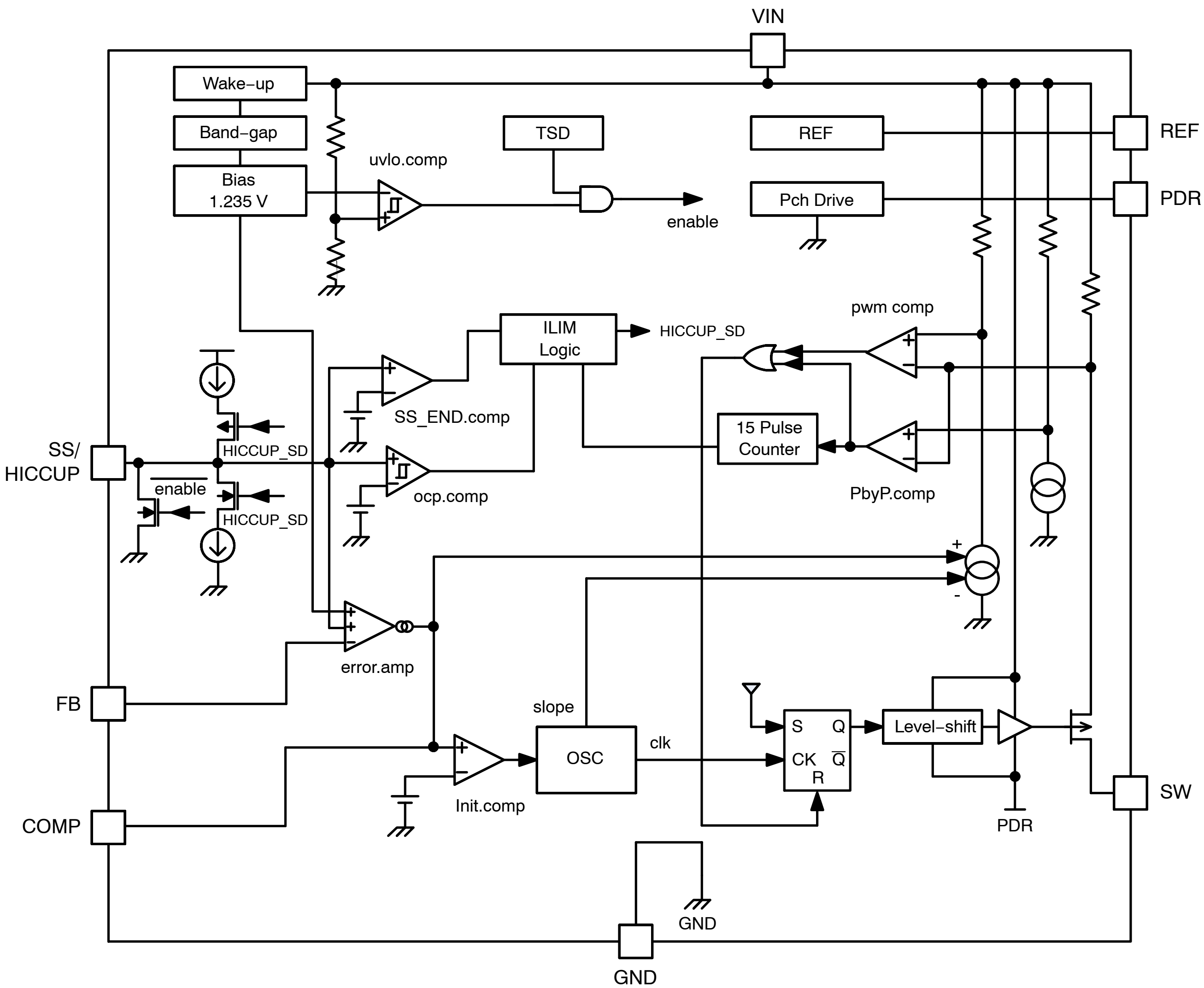


Figure 2. LV5980MC Block Diagram

Schematic

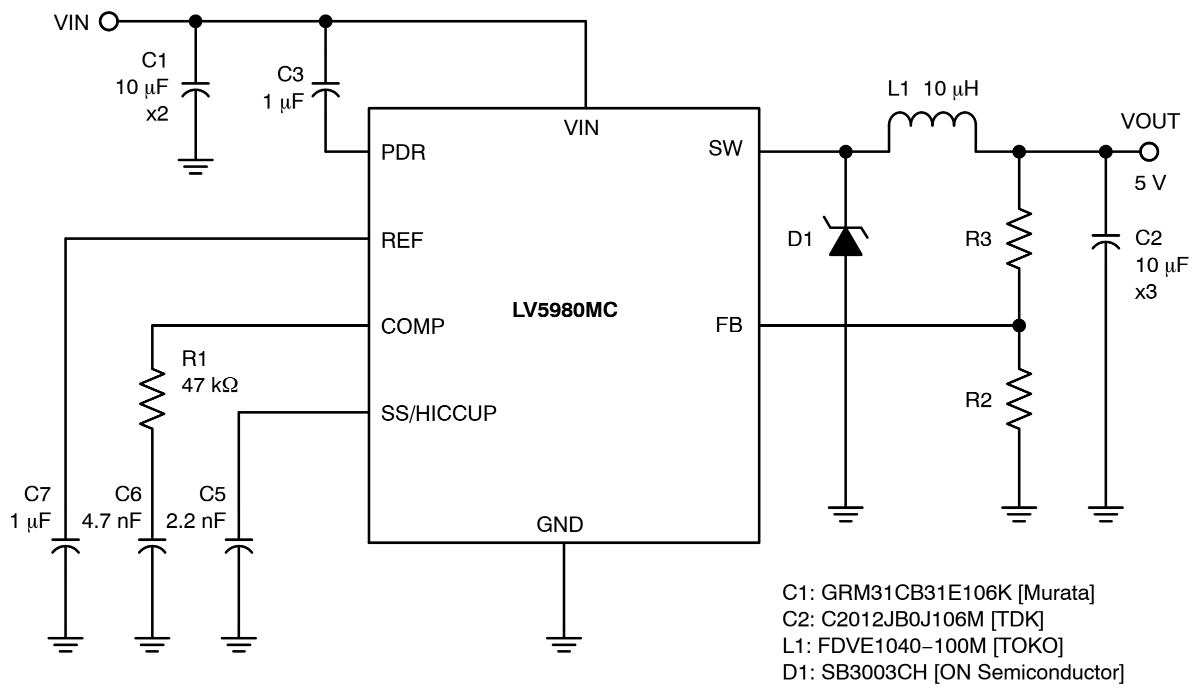


Figure 3. LV5980MC 5 V Schematic

Bill of Materials

Table 1. BILL OF MATERIALS

Designator	Manufacturer Part Number	Value	Tolerance	Qty.	Manufacturer
U1	LV5980MC	–	–	1	ON Semiconductor
L1	FDVE1040−100M	10 µH/5.2 A	10%	1	TOKO INC
R1	RK73B1JTTD473J	47 kΩ	5%	1	KOA
R2	RK73H1JTTD2203F	220 kΩ	1%	1	KOA
R3	RK73H1JTTD6803F	680 kΩ	1%	1	KOA
C1	GRM31CB31E106K	10 µF/25 A	10%	2	Murata
C2	C2012JB0J106M	10 µF/6.3 A	10%	3	TDK Corp
C3	GRM188B31E105K	1 µF/25 A	10%	1	Murata
C5	GRM188B31E105K	1 µF/25 A	10%	1	Murata
C6	GRM188B11H472K	4.7 nF/50 V	10%	1	Murata
C7	GRM188B11H222K	2.2 nF/50 V	10%	1	Murata
D1	SB3003CH	–	–	1	ON Semiconductor

IN/OUT Conditions

Table 2. IN/OUT CONDITIONS

Symbol	Function
VIN	Power Supply Input Pin
VOUT	DC/DC Converter Output Pin
GND	Ground Pin

CONNECTION DIAGRAM AND TEST SET UP DESCRIPTION

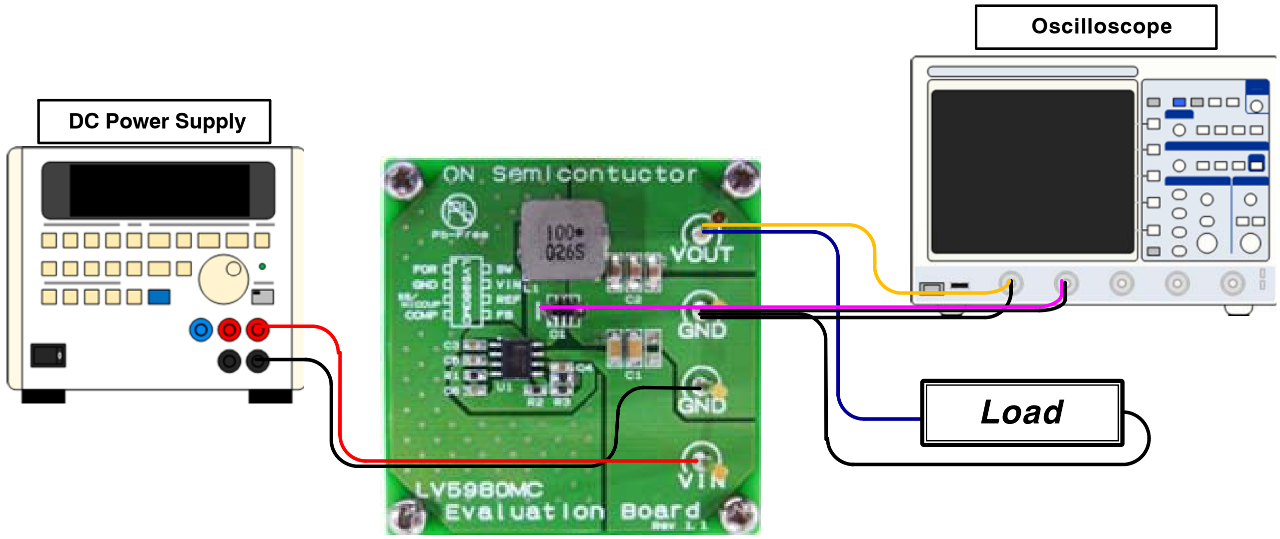


Figure 4. LV5980MC Test Set Up Diagram

Test Set Up Description

1. Connect the Load between VOUT and GND.
2. Connect the DC power supply with VIN and GND.
3. The output becomes a set voltage.

RESULTS

(Application Curves for LV5980MCGEVB at T_A = 25°C)

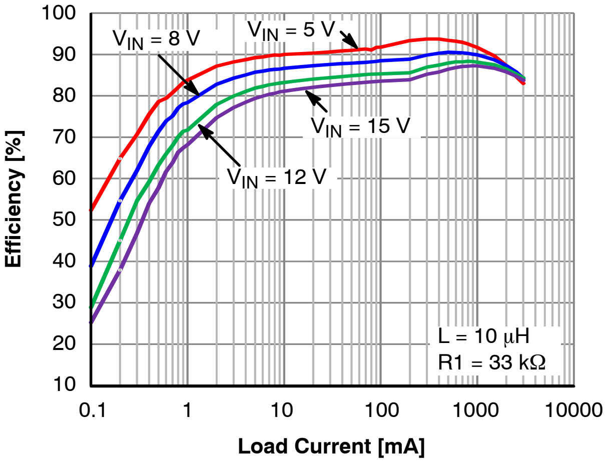


Figure 5. Efficiency/VOUT = 3.3 V

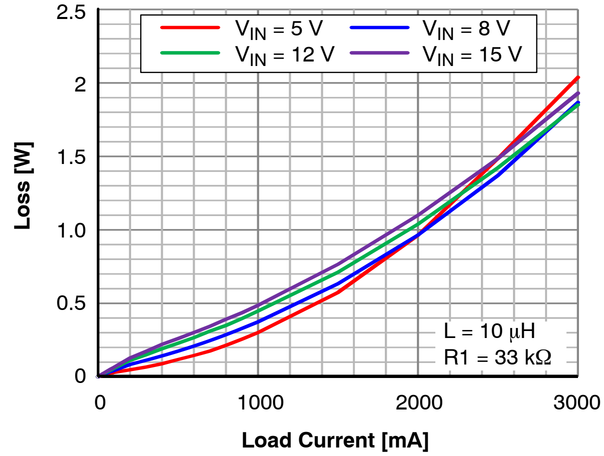


Figure 6. Loss/VOUT = 3.3 V

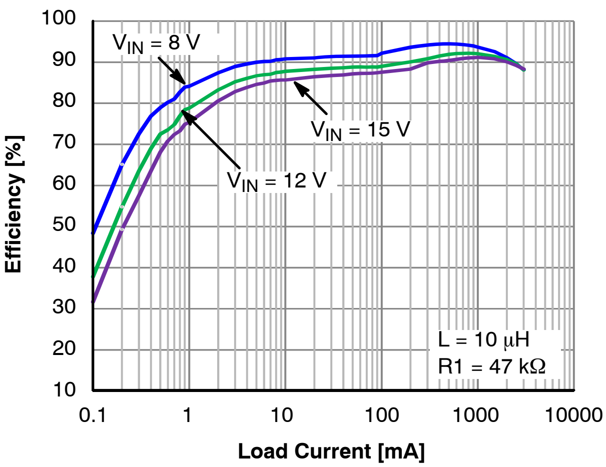


Figure 7. Efficiency/VOUT = 5 V

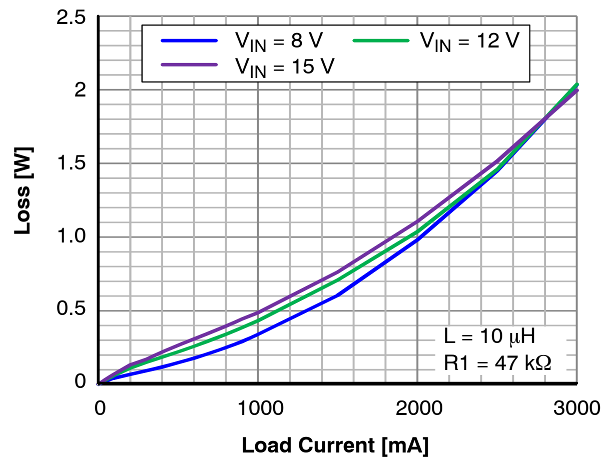


Figure 8. Loss/VOUT = 5 V

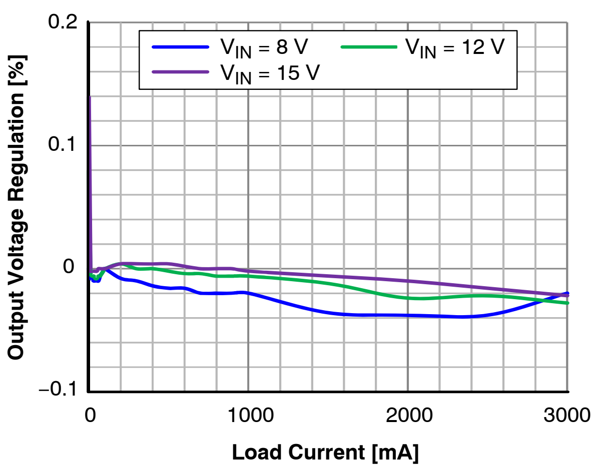


Figure 9. Load Regulation/VOUT = 5 V

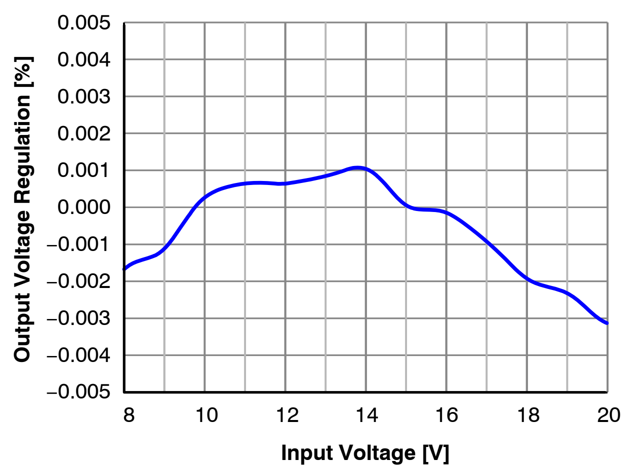


Figure 10. Line Regulation/VOUT = 5 V

RESULTS (Continued)

(Application Curves for LV5980MCGEVB at T_A = 25°C)

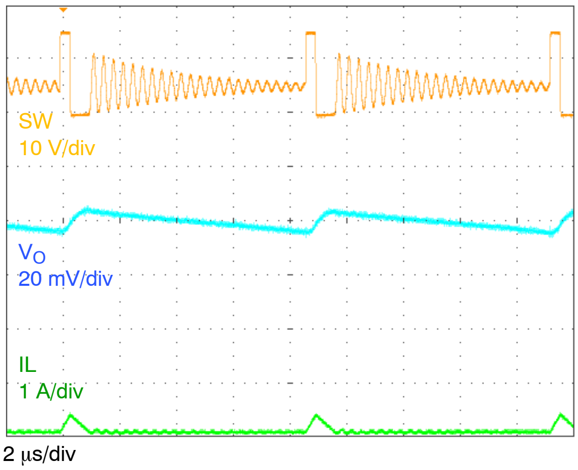


Figure 11. Output Ripple Voltage I_O = 20 mA

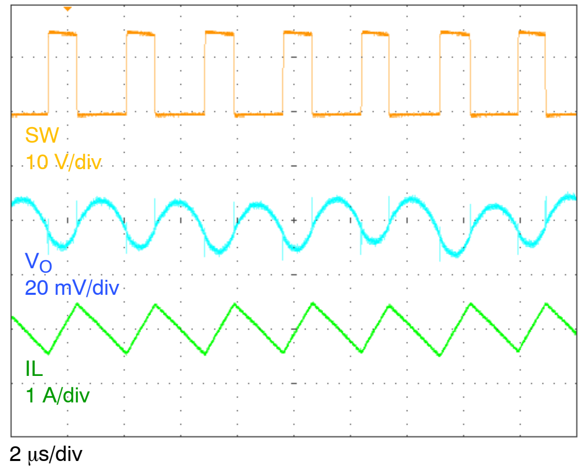


Figure 12. Output Ripple Voltage I_O = 2 A

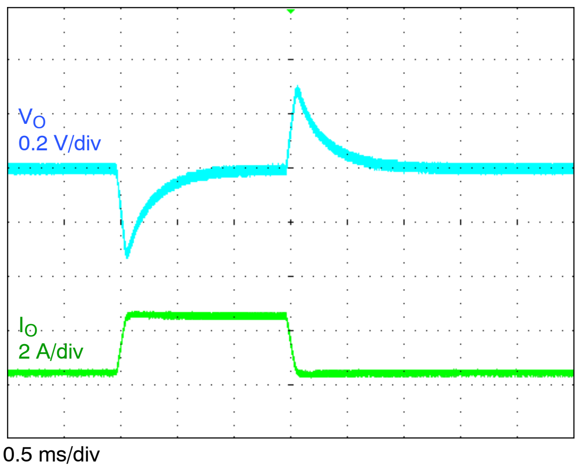


Figure 13. Load Transient Response I_{OUT} = 0.5 ⇔ 2.5 A

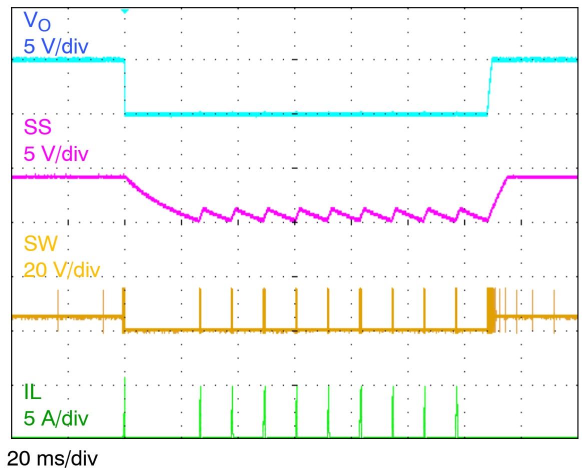


Figure 14. Short Circuit Protection

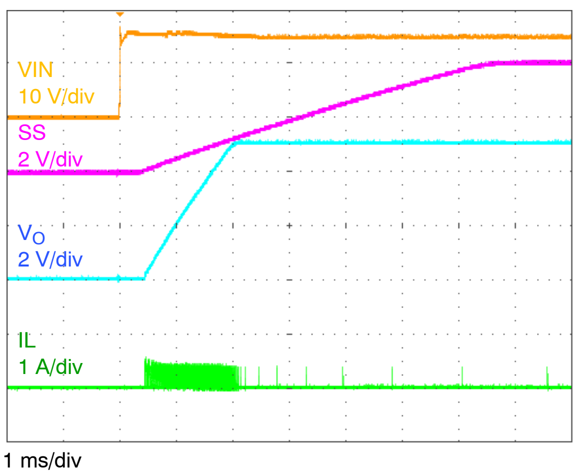


Figure 15. Start Up Sequence No Load

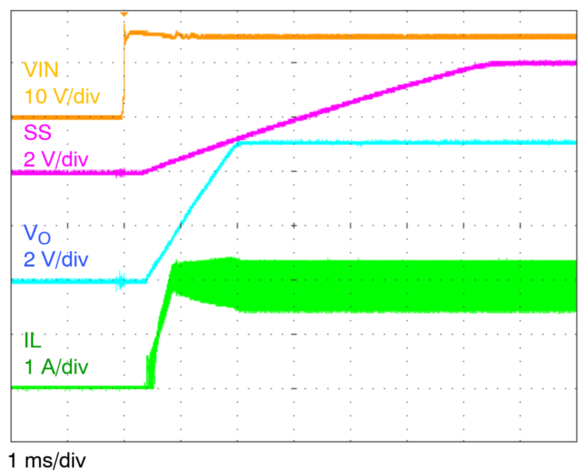


Figure 16. Start Up Sequence I_O = 2A

DETAILED DESCRPTION

Output Voltage Setting

Output voltage (V_{OUT}) is configurable by the resistance R3 between V_{OUT} and FB and the R2 between FB and GND. V_{OUT} is given by the following equation 1.

$$V_{OUT} = \left(1 + \frac{R3}{R2}\right) \cdot V_{REF} = \left(1 + \frac{R3}{R2}\right) \cdot 1.235 \quad [V] \qquad \text{(eq. 1)}$$

Soft Start

Soft start time (T_{SS}) is configurable by the capacitor (C5) between SS/HICCUP and GND. The setting value of T_{SS} is given by the equation 2.

$$T_{SS} = C5 \cdot \frac{V_{REF}}{I_{SS}} = C5 \cdot \frac{1.235}{1.8 \cdot 10^{-6}} \quad [ms] \qquad \text{(eq. 2)}$$

Hiccup Over−current Protection

Over−current limit (I_{CL}) is set to 4.7 A in the IC. When the peak value of inductor current is higher than 4.7 A for 15 consecutive times, the protection deems it as over current and stops the IC. Stop period (T_{HIC}) is defined by the discharging time of the SS/HICCUP. When SS/HICCUP is lower than 0.15 V, the IC starts up. When SS/HICCUP is higher than 0.3 V and then over current is detected, the IC stops again. And when SS/HICCUP is higher than 1.235 V, the discharge starts again. When the protection does not detect over−current status, the IC starts up again.

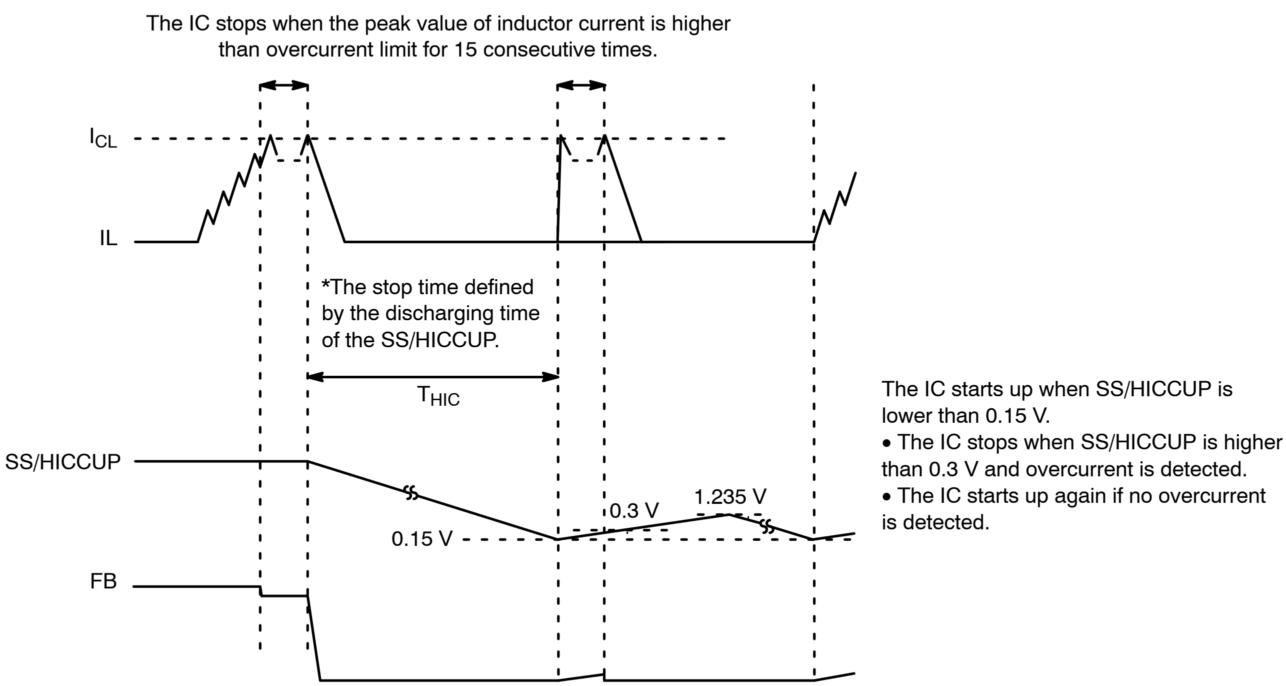


Figure 17. Hiccup Over−current Protection Time Chart

Power−save Feature

The LV5980MC has Power−saving feature (Low consumption Mode) to enhance efficiency during light load. By shutting down unnecessary circuits, operating current of the IC is minimized and high efficiency is realized. When the output load current decrease, the COMP pin voltage falls to 0.9 V and the device enters Low consumption Mode (The COMP pin is connected internally to an Init. comparator which compares with 0.9 V reference). In low consumption mode, the device show operating current of 63 μA from VIN. When the COMP pin voltage is larger than 0.9 V, IC operates in continuous Mode (PWM Mode).

DESIGN PROCEDURE

Inductor Selection

When conditions for input voltage, output voltage and ripple current are defined, the following equations 3 give inductance value.

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_R} \cdot T_{ON}$$

$$T_{ON} = \frac{1}{\left(\frac{V_{IN} - V_{OUT}}{V_{OUT} + V_F} + 1\right) \cdot F_{OSC}} \qquad \text{(eq. 3)}$$

F_{OSC} : Oscillatory Frequency
V_F : Forward Voltage of Schottky Barrier Diode
V_{IN} : Input Voltage
V_{OUT} : Output Voltage

- Inductor Current: Peak Value (I_{RP})
  Current peak value (I_{PR}) of the inductor is given by the equation 4.

$$I_{RP} = I_{OUT} + \frac{V_{IN} - V_{OUT}}{2L} \cdot T_{ON} \qquad \text{(eq. 4)}$$

  Make sure that rating current value of the inductor is higher than a peak value of ripple current.

- Inductor Current: Ripple Current (ΔI_R)
  Ripple current (ΔI_R) is given by the equation 5.

$$\Delta I_R = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} \qquad \text{(eq. 5)}$$

  When load current (I_{OUT}) is less than 1/2 of the ripple current, inductor current flows discontinuously.

Output Capacitor Selection

Make sure to use a capacitor with low impedance for switching power supply because of large ripple current flows through output capacitor.

This IC is a switching regulator which adopts current mode control method. Therefore, you can use capacitor such as ceramic capacitor and OS capacitor in which equivalent series resistance (ESR) is exceedingly small. Effective value is given by the equation 6 because the ripple current (AC) that flows through output capacitor is saw tooth wave.

$$I_{C\_OUT} = \frac{1}{2\sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{L \cdot F_{OSC} \cdot V_{IN}} \text{ [Arms]} \qquad \text{(eq. 6)}$$

Input Capacitor Selection

Ripple current flows through input capacitor which is higher than that of the output capacitors.

Therefore, caution is also required for allowable ripple current value.

The effective value of the ripple current flows through input capacitor is given by the equation 7.

$$I_{C\_IN} = \sqrt{D\,(1 - D)} \cdot I_{OUT} \text{ [Arms]}$$

$$D = \frac{T_{ON}}{T} = \frac{V_{OUT}}{V_{IN}} \qquad \text{(eq. 7)}$$

In (eq. 7), D signifies the ratio between ON/OFF period. When the value is 0.5, the ripple current is at a maximum. Make sure that the input capacitor does not exceed the allowable ripple current value given by (eq. 7). With (eq. 7), if V_{IN} = 15 V, V_{OUT} = 5 V, I_{OUT} = 1.0 A and F_{OSC} = 370 kHz, then I_{C_IN} value is about 0.471 Arms.

In the board wiring from input capacitor, V_{IN} to GND, make sure that wiring is wide enough to keep impedance low because of the current fluctuation. Make sure to connect input capacitor near output capacitor to lower voltage bound due to regeneration current. When change of load current is excessive (I_{OUT}: high → low), the power of output electric capacitor is regenerated to input capacitor. If input capacitor is small, input voltage increases. Therefore, you need to implement a large input capacitor. Regeneration power changes according to the change of output voltage, inductance of a coil and load current.

Selection of External Phase Compensation Component

This IC adopts current mode control which allows use of ceramic capacitor with low ESR and solid polymer capacitor such as OS capacitor for output capacitor with simple phase compensation. Therefore, you can design long−life and high quality step−down power supply circuit easily.

Frequency Characteristics

The frequency characteristic of this IC is constituted with the following transfer functions.

(1) Output resistance breeder : H_R
(2) Voltage gain of error amplifier : G_{VEA}
Current gain : G_{MEA}
(3) Impedance of phase compensation external element : Z_C
(4) Current sense loop gain : G_{CS}
(5) Output smoothing impedance : Z_O

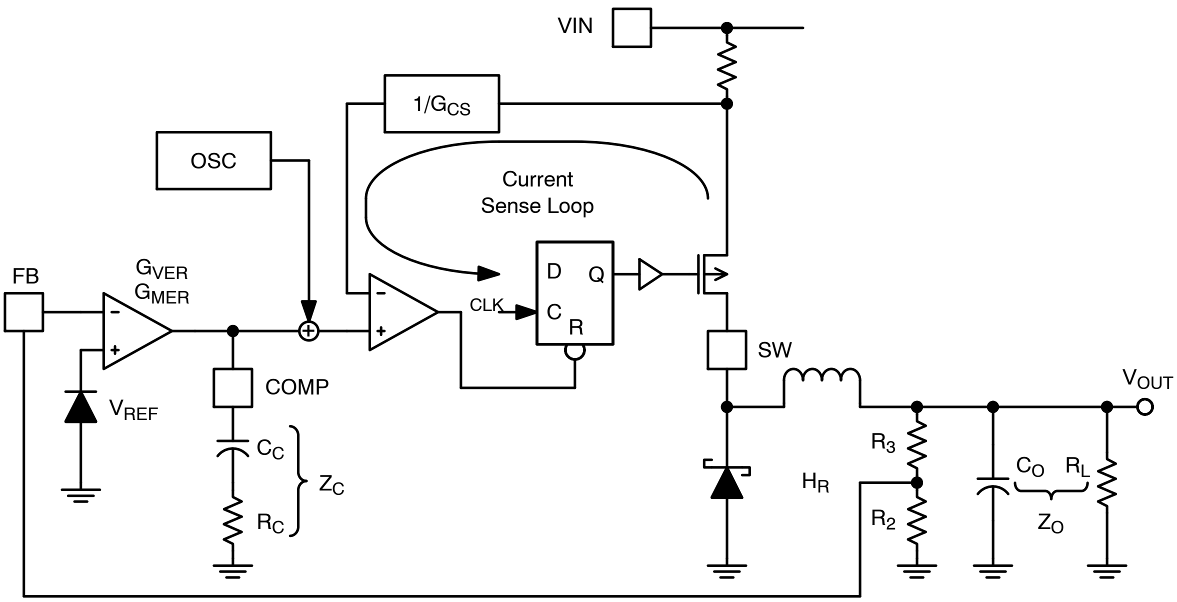


Figure 18. Compensation Network

Closed loop gain is obtained with the following formula 8.

$$G = H_R \cdot G_{MER} \cdot Z_C \cdot G_{CS} \cdot Z_O = \quad \text{(eq. 8)}$$
$$= \frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot \left(R_C + \frac{1}{sC_C}\right) \cdot G_{CS} \cdot \frac{R_L}{1 + sC_O \cdot R_L}$$

Frequency characteristics of the closed loop gain is given by pole fp1 consists of output capacitor C_O and output load resistance R_L, zero point fz consists of external capacitor C_C of the phase compensation and resistance R_C, and pole fp2 consists of output impedance Z_{ER} of error amplifier and external capacitor of phase compensation C_C as shown in formula 8. fp1, fz, fp2 are obtained with the following equations 9 to 11.

$$fp1 = \frac{1}{2\pi \cdot C_O \cdot R_L} \quad \text{(eq. 9)}$$

$$fz = \frac{1}{2\pi \cdot C_C \cdot R_C} \quad \text{(eq. 10)}$$

$$fp2 = \frac{1}{2\pi \cdot Z_{ER} \cdot C_C} \quad \text{(eq. 11)}$$

Calculation of External Phase Compensation Constant

Generally, to stabilize switching regulator, the frequency where closed loop gain is 1 (zero−cross frequency f_{ZC}) should be 1/10 of the switching frequency (or 1/5). Since the switching frequency of this IC is 370 kHz, the zero−cross frequency should be 37 kHz. Based on the above condition, we obtain the following formula 12.

$$\frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot \left(R_C + \frac{1}{sC_C}\right) \cdot G_{CS} \cdot \frac{R_L}{1 + sC_O \cdot R_L} = 1 \quad \text{(eq. 12)}$$

As for zero−cross frequency, since the impedance element of phase compensation is RC >> ($1/sC_C$), the following equation 13 is obtained.

$$\frac{V_{REF}}{V_{OUT}} \cdot G_{MER} \cdot R_C \cdot G_{CS} \cdot \frac{R_L}{1 + 2\pi \cdot f_{ZC} \cdot C_O \cdot R_L} = 1 \quad \text{(eq. 13)}$$

Phase compensation external resistance can be obtained with the following formula 14, the variation of the formula 13. Since $2\pi \cdot f_{ZC} \cdot C_O \cdot R_L >> 1$ in the equation 14, we know that the external resistance is independent of load resistance.

$$R_C = \frac{V_{OUT}}{V_{REF}} \cdot \frac{1}{G_{MER}} \cdot \frac{1}{G_{CS}} \cdot \frac{1 + 2\pi \cdot f_{ZC} \cdot C_O \cdot R_L}{R_L} \quad \text{(eq. 14)}$$

When output is 5 V and load resistance is 5 Ω (1 A load), the resistances of phase compensation are as follows.
G_{CS} = 2.7 A/V, G_{MER} = 220 μA/V, f_{ZC} = 37 kHz.

$$R_C = \frac{5}{1.235} \cdot \frac{1}{220 \cdot 10^{-6}} \cdot \frac{1}{2.7} \cdot$$
$$\cdot \frac{1 + 2 \cdot 3.14 \cdot (37 \cdot 10^{3}) \cdot (30 \cdot 10^{-6}) \cdot 5}{5} = \quad \text{(eq. 15)}$$
$$= 48.898... \cdot 10^{3} = 48.90\ [\text{k}\Omega]$$

If frequency of zero point fz and pole fp1 are in the same position, they cancel out each other. Therefore, only the pole frequency remains for frequency characteristics of the closed loop gain.

In other words, gain decreases at −20 dB/dec and phase only rotates by 90° and this allows characteristics where oscillation never occurs.

$$fp1 = fz$$
$$\frac{1}{2\pi \cdot C_O \cdot R_L} = \frac{1}{2\pi \cdot C_C \cdot R_C} \quad \text{(eq. 16)}$$
$$C_C = \frac{R_L \cdot C_O}{R_C} = \frac{5 \cdot (30 \cdot 10^{-6})}{48.9 \cdot 10^{3}} =$$
$$= 3.067... \cdot 10^{-9} = 3.07\ [\text{nF}]$$

The above shows external compensation constant obtained through ideal equations. In reality, we need to define phase constant through testing to verify constant IC operation at all temperature range, load range and input voltage range. In the evaluation board for delivery, phase compensation constants are defined based on the above constants. The zero−cross frequency required in the actual system board, in other word, transient response is adjusted by external compensation resistance. Also, if the influence of noise is significant, use of external phase compensation capacitor with higher value is recommended.

The table of compensation values is provided below.

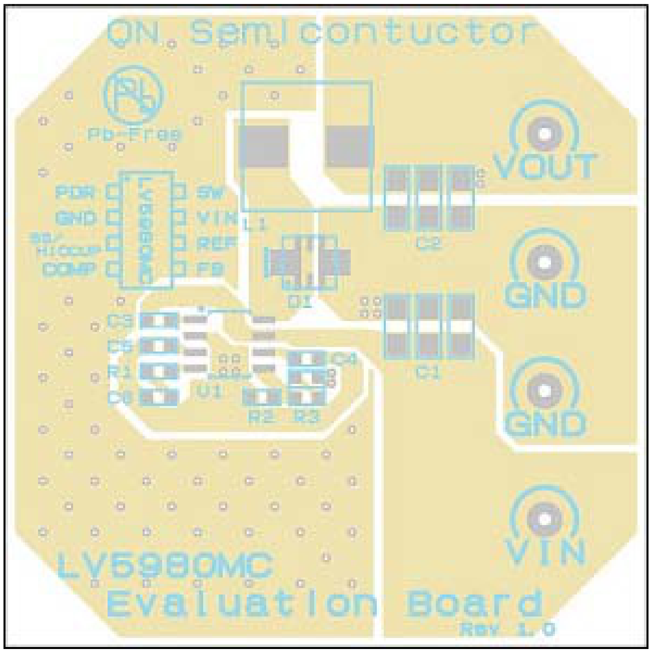
Table 3. COMPENSATION VALUES

VIN (V)	V_{OUT} (V)	L (μH)	R2 (kΩ)	R3 (kΩ)	R_C (kΩ)	C_C (nF)	C_O (μF)
8	1.235	4.7	220	0	20	3.3	30
	1.8	5.6	220	100	24	3.3	30
	3.3	6.8	180	300	33	4.7	30
	5	8.2	220	680	39	4.7	30
12	1.235	4.7	220	0	20	3.3	30
	1.8	5.6	220	100	24	3.3	30
	3.3	8.2	180	300	33	4.7	30
	5	10	220	680	39	4.7	30
	8	12	150	820	47	5.6	30*
18	1.235	5.6	220	0	20	3.3	30
	1.8	6.8	220	100	24	3.3	30
	3.3	10	180	300	33	4.7	30
	5	12	220	680	39	4.7	30
	8	15	150	820	47	5.6	30*
	15	33	82	910	51	5.6	30*

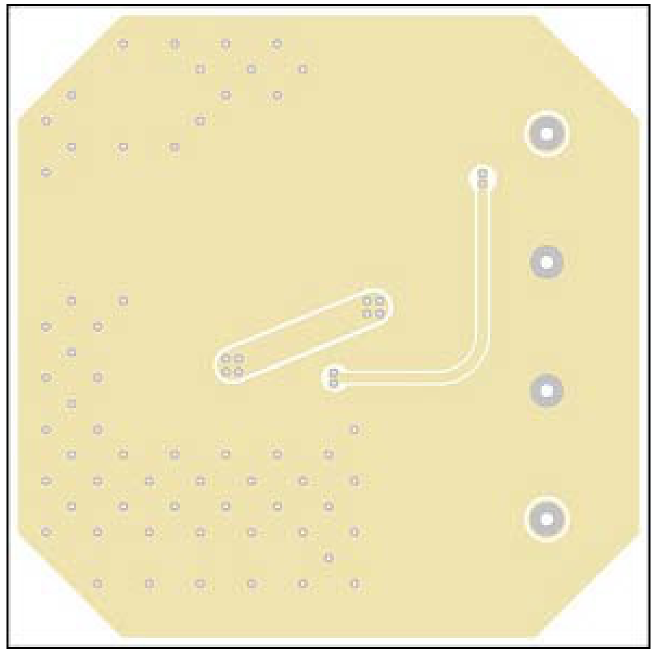
*10 μF/25 V (Murata: GRM31CB31E106K)

The zero−cross frequency required in the actual system board, in other word, transient response is adjusted by R_C. Also, if the influence of noise is significant, use of C_C with higher value is recommended.

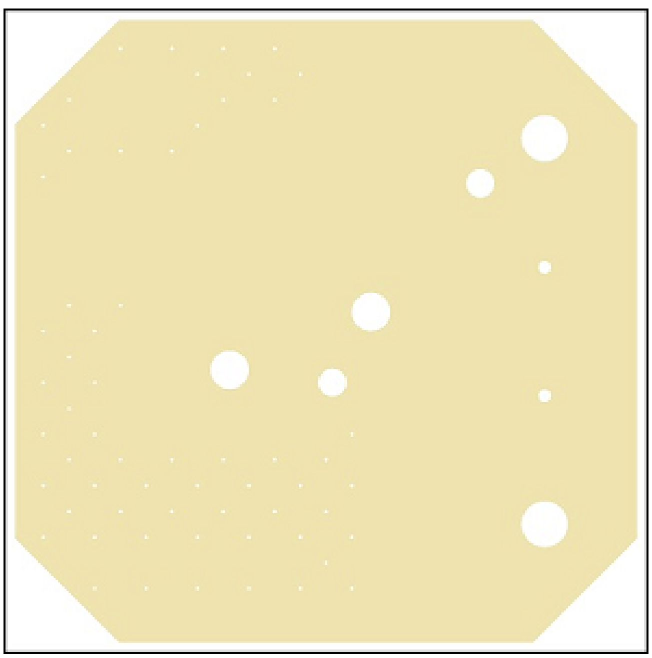
SUGGESTED CIRCUIT LAYOUT



Top−Side Layout



Bottom−Side Layout



$2^{nd}/3^{rd}$ Layout

Figure 19. 4−layer PCB with All Components on Top Side

Pattern design of the board affects the characteristics of DC−DC converter. This IC switches high current at a high speed. Therefore, if inductance element in a pattern wiring is high, it could be the cause of noise. Make sure that the pattern of the main circuit is fat and short.

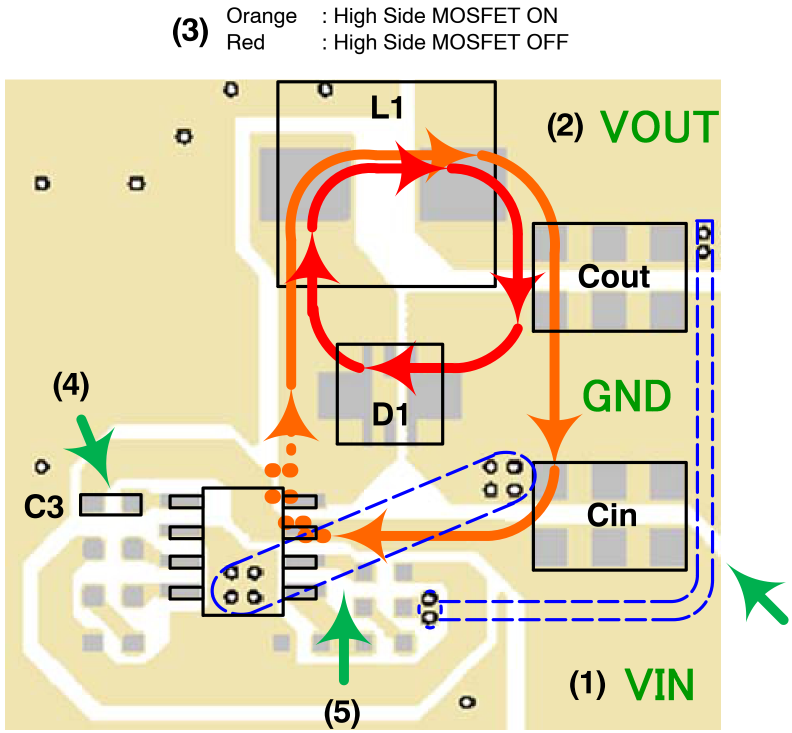


Figure 20. LV5980MCGEVB Board Layout

(1) Pattern Design of the Input Capacitor

Connect a capacitor near the IC for noise reduction between V_{IN} and the GND. The change of current is at the largest in the pattern between an input capacitor and V_{IN} as well as between GND and an input capacitor among all the main circuits. Hence make sure that the pattern is as fat and short as possible.

(2) Pattern Design of an Inductor and the Output Capacitor

High electric current flows into the choke coil and the output capacitor. Therefore this pattern should also be as fat and short as possible.

(3) Pattern Design with Current Channel into Consideration

Make sure that when High side MOSFET is ON (red arrow) and OFF (orange arrow), the two current channels runs through the same channel and an area is minimized.

(4) Pattern Design of the Capacitor between V_{IN}−PDR

Make sure that the pattern of the capacitor between V_{IN} and PDR is as short as possible.

(5) Pattern Design of the Small Signal GND

The GND of the small signal should be separated from the power GND.

(6) Pattern Design of the FB−OUT Line

Wire the line shown in red between FB and OUT to the output capacitor as near as possible. When the influence of noise is significant, use of feedback resistors R2 and R3 with lower value is recommended.

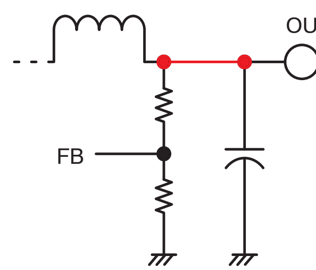


Figure 21. FB−OUT Line

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