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Basics of Clock Jitter

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APPLICATION NOTE

Introduction

This application note focuses on the different types of clock jitter. Clock jitter is deviation of a clock edge from its ideal location. Understanding clock jitter is very important in applications as it plays a key role in the timing budget in a system.

With the increasing system data rates, timing jitter has become critical in system design, as in some instances the system performance limit is determined by the system timing margin. So a good understanding of the timing jitter becomes very important in system design. Total jitter can be separated into random jitter and deterministic jitter components. We will not discuss the components of jitter in this application note. We will focus on different types of clock jitter.

Clock timing jitter can be measured in time domain and in frequency domain. Cycle−to−cycle jitter, period jitter and time interval error (TIE) jitter are measured in time domain, where as phase noise and phase jitter are measured in frequency domain. Some of the sources of jitter are thermal noise, power supply noise, ground bounce, PLL circuitry, crosstalk and reflections.

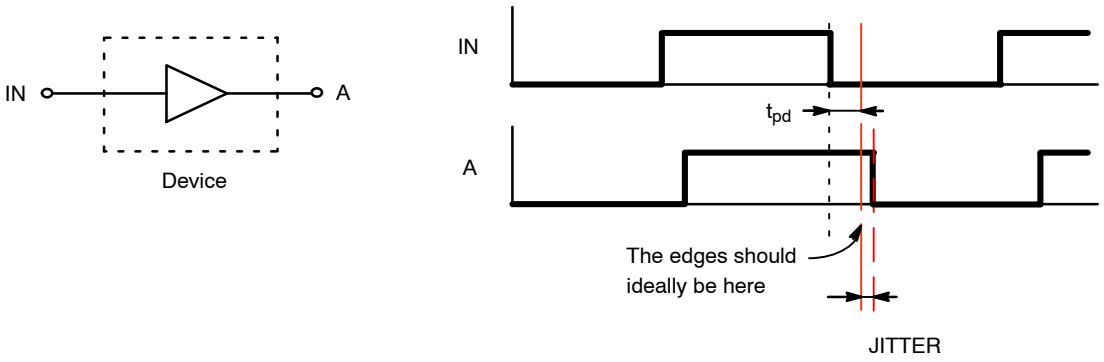

Figure 1. Examples of Clock Jitter

Different types of Clock Jitter

- *Cycle−to−cycle Jitter* − The cycle−to−cycle jitter measures the change in clock period between any two adjacent clock cycles over 1,000 clock cycles.
  - The cycle−to−cycle jitter RMS measures the standard deviation of the change in clock period measurement between any two adjacent clock cycles over 1,000 clock cycles.
  - The cycle−to−cycle jitter peak−to−peak measures the difference between minimum clock period change and maximum clock period change between any two adjacent clock cycles over 1,000 clock cycles.

The cycle−to−cycle jitter measurement is used to determine high frequency jitter in applications as it measures the jitter between two adjacent clock cycles. It is very important to have a small value of cycle to cycle jitter as it impacts the system timing margin.

- *Period Jitter* – The period jitter measures the maximum deviation of clock period of a clock cycle in the waveform over 10,000 clock cycles.
  - The period jitter RMS measures the standard deviation of the clock period measurements over 10,000 clock cycles.
  - The period jitter peak−to−peak measures the difference between minimum clock period and maximum clock period measurement over 10,000 clock cycles.

The period jitter measurement is used to determine low frequency jitter in applications as it measures the jitter by measuring the clock period deviations over 10,000 clock cycles. Period jitter is used to calculate the system timing margin. Figure 2 shows Example of Clock Period Jitter Measurement of ON Semiconductor's Programmable Clock – NB3N3020.

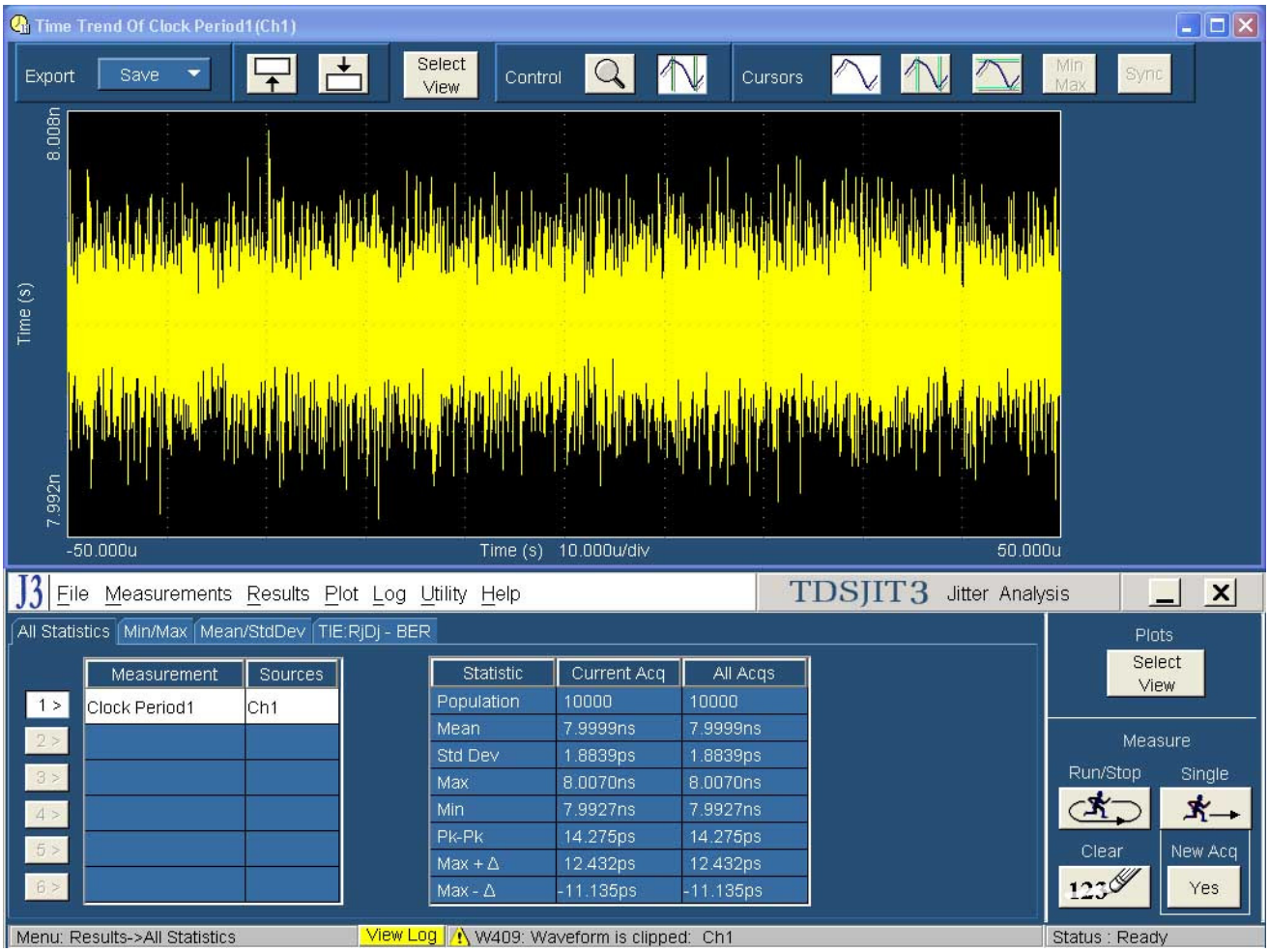

Figure 2.

- *Time Interval Error (TIE) Jitter* – The TIE jitter measures how far each active edge of the clock varies from corresponding edge of an ideal clock.
  - The TIE jitter RMS measures the standard deviation of the timing error.
  - The TIE peak−to−peak measures the difference of the minimum and maximum timing error.

The TIE jitter is important in clock and data recovery (CDR) PLLs to show if the PLL in the CDR is able to track to the incoming data stream. A large TIE jitter shows that the CDR PLL is not able to properly track the variation in the incoming data stream. Figure 3 shows Example of Time Interval Error (TIE) Jitter measurement of ON Semiconductor's Clock Synthesizer – NB3N3002.

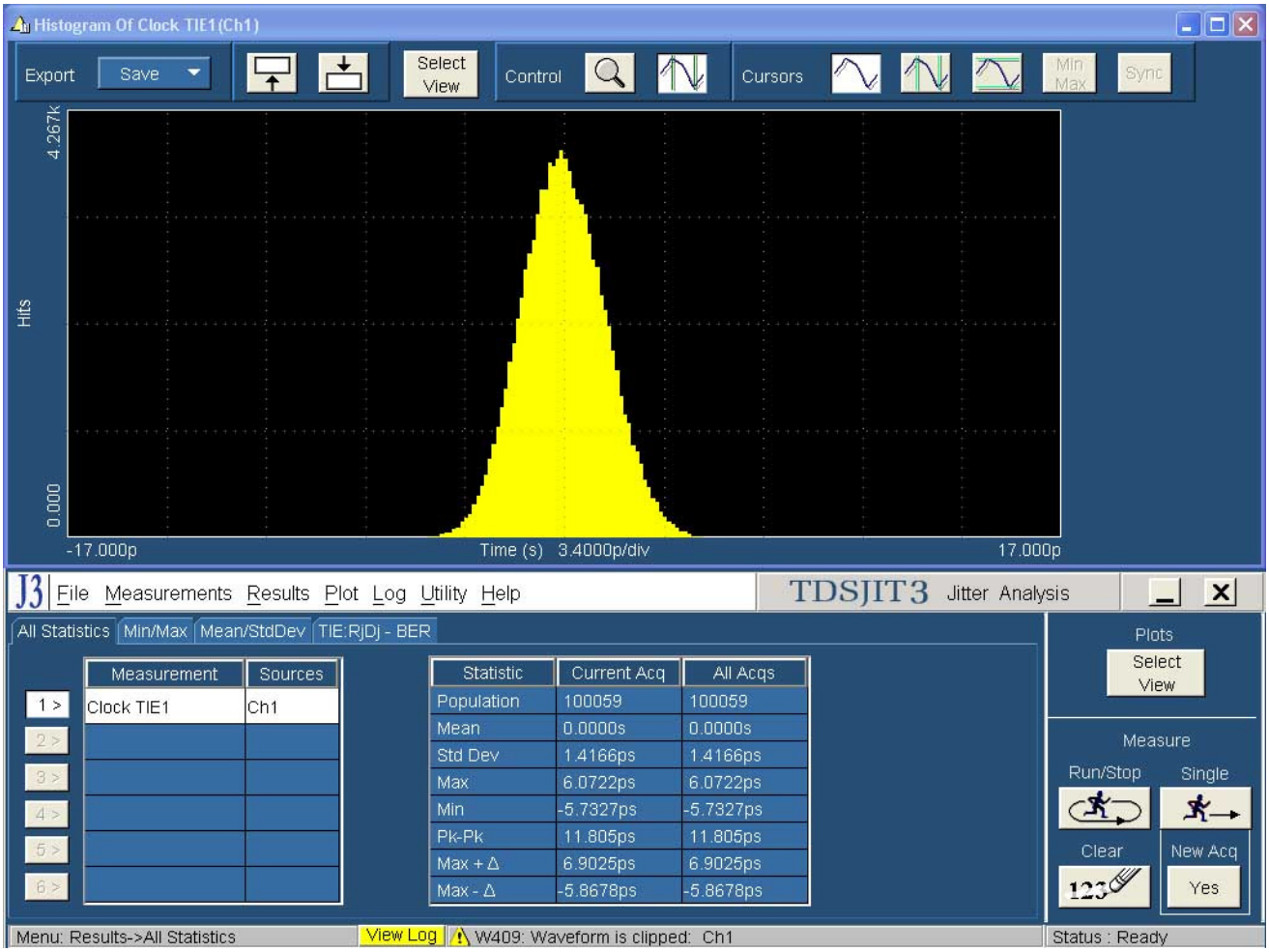

Figure 3.

• *Phase Noise* – Phase noise is measured in the frequency domain, and is a ratio of signal power to noise power normalized to a 1 Hz bandwidth at a given offset from the carrier signal.

Phase jitter is measured by integrating the phase noise across specified frequency offsets from the carrier signal. Phase jitter measures the amount of energy present in the specified frequency offsets from the carrier signal compared to the energy of the carrier signal by integrating the area under the phase noise plot. As an example, SONET uses a frequency offset of 12 kHz to 20 MHz from the carrier signal to integrate the area under the phase noise plot to measure phase jitter. Fiber Channel uses a frequency offset of 637 kHz to 10 MHz from the carrier signal to integrate the area under the phase noise plot to measure phase jitter. Figure 4 shows example of phase noise and phase jitter measurement of one of the PureEdge™ PLL devices from the crystal oscillator product family – NBXDBB018 which generates a dual frequency LVPECL output at 155.52 MHz/ 311.04 MHz meeting the jitter requirements of SONET applications.

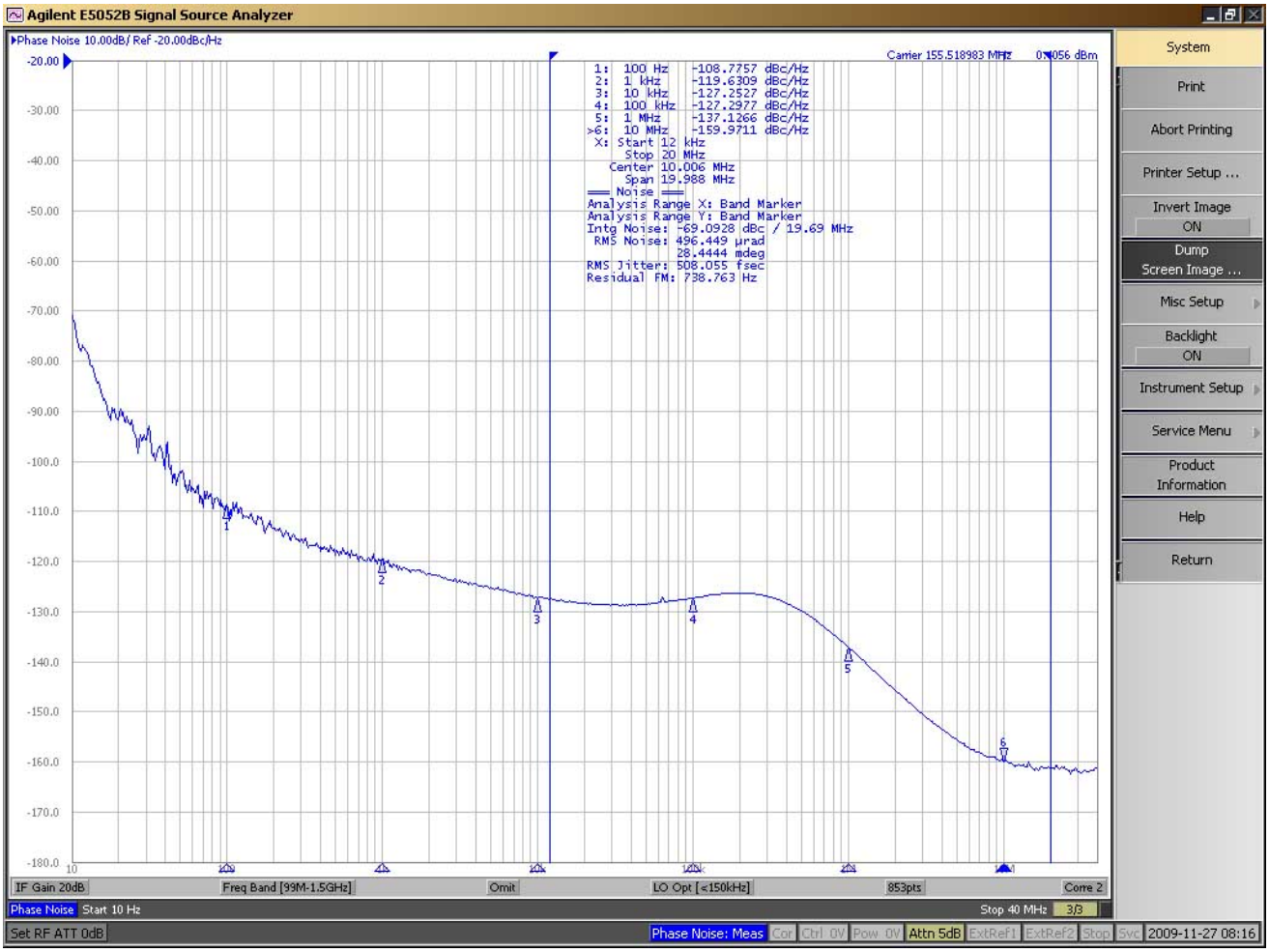

Figure 4.

Conclusion

This application note provided an introduction of clock jitter, explained the different types of clock jitter and significance of each type of clock jitter measurement. Examples of the different types of clock jitter measurements were also shown in the content above. With increasing system data rates, sometimes the system performance limit is determined by the system timing margin, hence understanding timing clock jitter is critical for system designers.

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