ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

AND8453

Loop Control Design of an ac-dc Adapter Using the NCP1250

Prepared by: Christophe Basso
ON Semiconductor

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

The NCP1250 controller lends itself very well to the design of small to moderate output power offline converters. Despite its ease of implementation and the limited number of active pins, the control loop design cannot be overlooked, especially if high volumes are at stake. To further ease the work of the design engineer, ON Semiconductor has developed on an automated design tool based on Microsoft Excel®. Rather than being a simple spreadsheet, the software plots the various ac responses based on the hardware component values and suggests a compensation scheme based on the popular TL431. Follow the steps…

A Compact Adapter

The NCP1250 includes everything needed to build a compact and robust ac−dc converter including Over Voltage Protection (OVP), Over Temperature Protection (OTP) and finally, input line Over Power Protection (OPP). Operating from a 65 kHz switching frequency, the adapter presented in Figure 1 delivers 19 V with a nominal output current capability of 3 A continuous. Please note the absence of the front−end rectifying section, purposely ignored for the sake of simplicity.

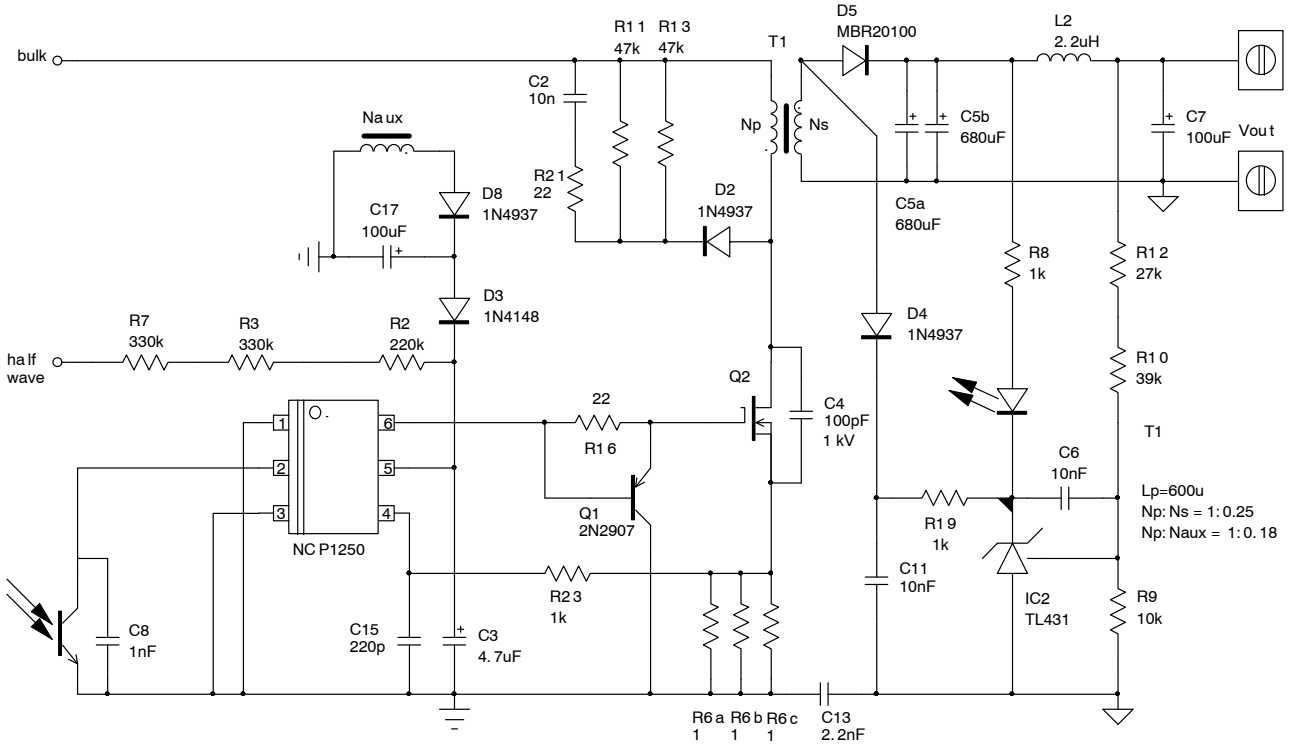

Figure 1. The 60 W Adapter Uses a Few Components Around the NCP1250 While Offering Excellent Performance

To reduce the wasted power during standby, the start−up network (R_2 R_3 and R_7) is connected to the half−wave rectified mains. Due to a high start−up level on the NCP1250, the V_{CC} capacitor C_3 can be kept small and does not hamper the power−on time. To make sure the auxiliary voltage remains alive in no−load conditions, an additional rectifier is added (D_8 and C_{17}). To improve the driving capability of the part, a small PNP transistor Q_1 has been added to allow the quick turn−off of the power MOSFET Q_2. On the secondary side, a TL431 ensures regulation and loop stability by implementing a type 2 configuration. Please note that this schematic is a simplified version of a real NCP1250−based adapter where OTP, OVP and OTP can be implemented by using a single pin, pin 3. The description is now complete and it is time to take a look at the compensation strategy.

Loop Control Design

Loop control is an often overlooked feature in the process of designing power converters. Either the designer is not an expert in the field of stability or he simply believes that a simple trial and error operation in the laboratory will save him precious minutes to finish his design earlier! Fatal error… When understood, loop control is not a difficult exercise, especially these days where a lot of tools are available. On the contrary, if a prototype converter shows an acceptable transient response on the bench at room temperature, expect this response to severely degrade as millions of converters are manufactured with different types of components. At the end, it might be very possible that the few minutes you saved from leaving loop control behind your shoulder, will turn into endless nights to solve an oscillation problem that has popped up in the production line situated far away from home.

What exactly are we talking about? Figure 2 shows the theoretical representation of a power converter delivering an output voltage V_{out}. If we neglect the perturbations brought by the output current and the input voltage, we can write the following equations:

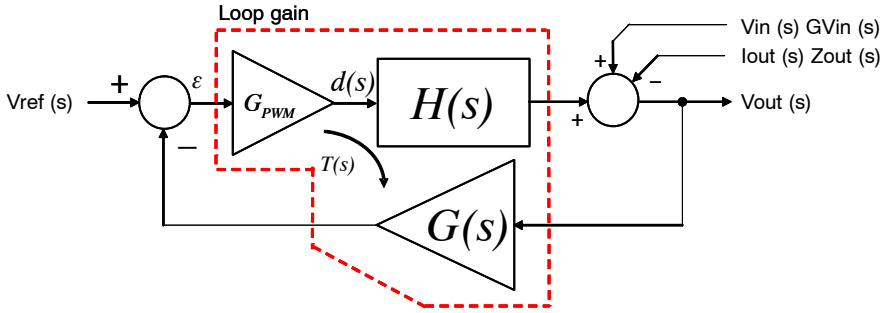

Figure 2. A Closed−Loop System Permanently Monitors a Given Variable, Usually the Output, and Makes Sure It Does Not Deviate from the Imposed Target

$$V_{out}(s) = d(s)H(s) \quad \text{(eq. 1)}$$

$$d(s) = \left[V_{ref}(s) - V_{out}(s)G(s)\right]G_{PWM} \quad \text{(eq. 2)}$$

If we substitute Equation 2 into Equation 1, we have:

$$V_{out}(s) = \left[V_{ref}(s) - V_{out}(s)G(s)\right]G_{PWM}H(s) \quad \text{(eq. 3)}$$

Re−arranging gives:

$$\frac{V_{out}(s)}{V_{ref}(s)} = \frac{G_{PWM}H(s)}{1 + G(s)G_{PWM}H(s)} = \frac{G_{PWM}H(s)}{1 + T(s)} \quad \text{(eq. 4)}$$

This expression describes the closed−loop transfer function of the converter. To ensure stability, the denominator must be different from zero. The denominator is made of the loop gain $T(s)$ added to 1. Theory tells that stability is jeopardized if $T(s)$, the loop gain, exhibits both a magnitude of 1 (or 0 dB) and an argument of −180° at a considered frequency f_c. If $T(s)$ meets these two criteria, we have an oscillator and any perturbation, like noise, will turn our system into an oscillator tuned at f_c. Oscillations will cease if the phase lag at f_c becomes less than −180° or if the gain at f_c deviates from 0 dB. To ensure stability, we have to be sure that the phase lag of $T(s)$, at a frequency where its magnitude is 0 dB, is always far from the −180° limit. The distance of argT(s) to the −180° limit is called the phase margin and is noted φ_m. Figure 3 shows an example of a converter exhibiting a crossover frequency of 6.5 kHz and a phase margin of 92°. Without entering into the details, it is possible to show that the phase margin links to the equivalent quality coefficient Q of a second−order system:

- A low phase margin implies a high quality coefficient Q and a fast ringing response: the system recovers quickly from a load step but severely overshoots. If the phase margin further degrades, the system might lose its natural damping and the ringing will turn into steady−state oscillations.
- A phase margin of 76° is equivalent to a Q of 0.5 on a second−order system featuring an origin pole and a high−frequency pole in the vicinity of the crossover frequency. It gives a quick recovery without overshoot.
- A large phase margin, greater than 90°, gives a damped system with slow recovery and no overshoot.

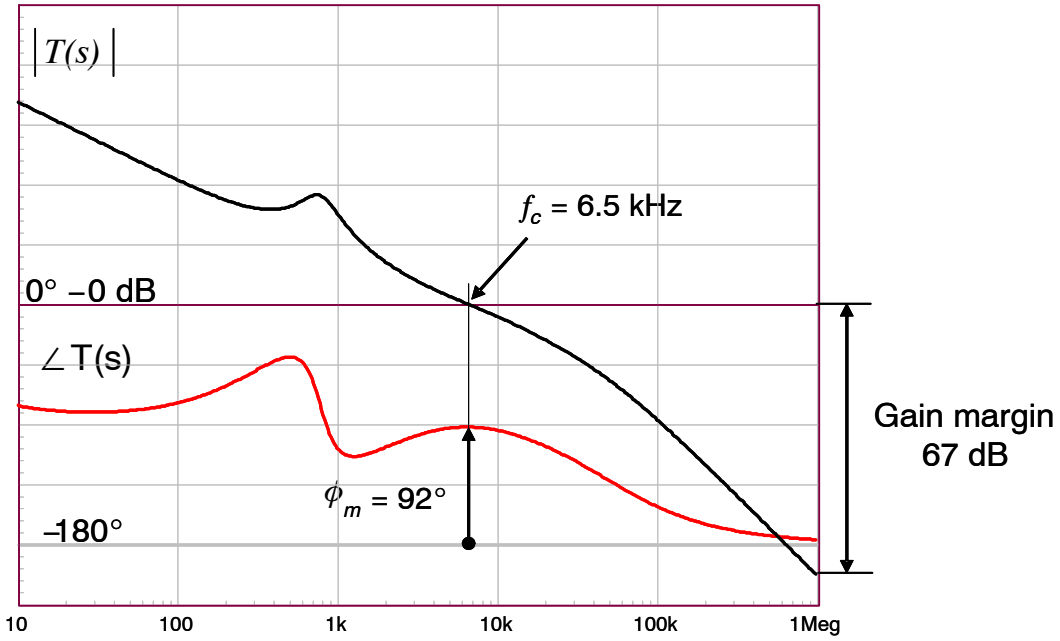

Figure 3. The Distance From the Open−Loop Gain Phase Curve at Crossover to the −180° Line is Called the Phase Margin

It is then the designer task to shape the loop gain *T(s)* so that enough phase margin is present, whatever the operating conditions are: input voltage, output current, ambient temperature and so on. You shape the loop gain by playing with the compensator elements to form *G(s)*. The compensator transfer function will thus include an origin pole (to provide a high dc gain) plus a pole/zero pair to provide local phase boost. We talk in that case of a type 2 compensator. Where to place these pole and zero is the question that often torments power supply designers. Fortunately, ON Semiconductor has developed a fully automated spreadsheet that will recommend values for you to test.

Using the Automated Software

Before using the software downloaded from Ref. [2] URL address, you must be familiar with the internal structure of the NCP1250, at least around the feedback pin. It appears in Figure 4 and shows how the feedback voltage programs the peak current setpoint of the controller. A divider by 4.2 is installed in the feedback path to provide a comfortable dynamic on the feedback signal, across the optocoupler collector−emitter space. The pull−up resistor is 16 kΩ and plays a role in the gain expression as it loads the optocoupler collector. To avoid any current runaway in fault conditions, the maximum voltage set point is limited to a precise 800 mV level. The pull−up resistor value and the internal divider ratio are parameters the software needs to compute the compensation elements. The other needed elements relate to the application schematic: the transformer and its parameters such as the primary inductance L_p and its associated turns ratio are passed to the automated spreadsheet. In our adapter, the inductance is 600 μH and the turns ratio is 1:0.25, meaning we have 4 times less turns on the secondary than on the primary. Either you enter the exact number of turns for the primary and the secondary in the spreadsheet, or you just enter 100 for the primary and 25 for the secondary. The important parameter now is the output capacitor Equivalent Series Resistor (ESR). Most of simulation errors come from a bad value used for this parameter, it is therefore important to extract it from the manufacturer data−sheet or best, characterize it on the bench. For this adapter, we have used two paralleled 680 μF capacitors from Rubycon, ZL series. Based on their data−sheet, they exhibit an ESR of 21 mΩ at room temperature which increases to 53 mΩ at low temperatures (−10°C). The high−temperature ESR is not stated and will be required to see its effect on the loop gain. We are now all set and can launch the software to see the first technical panel as it appears in Figure 5.

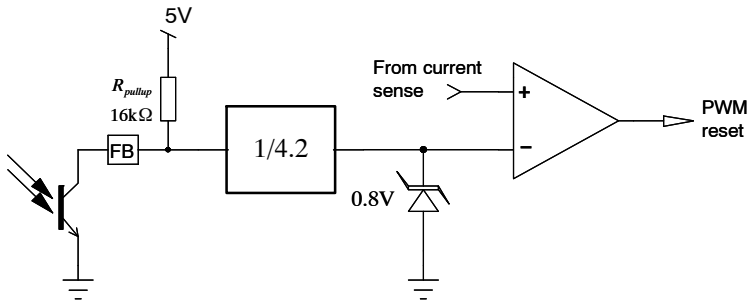

Figure 4. The Peak Current Set Point is Internally Limited to 0.8 V

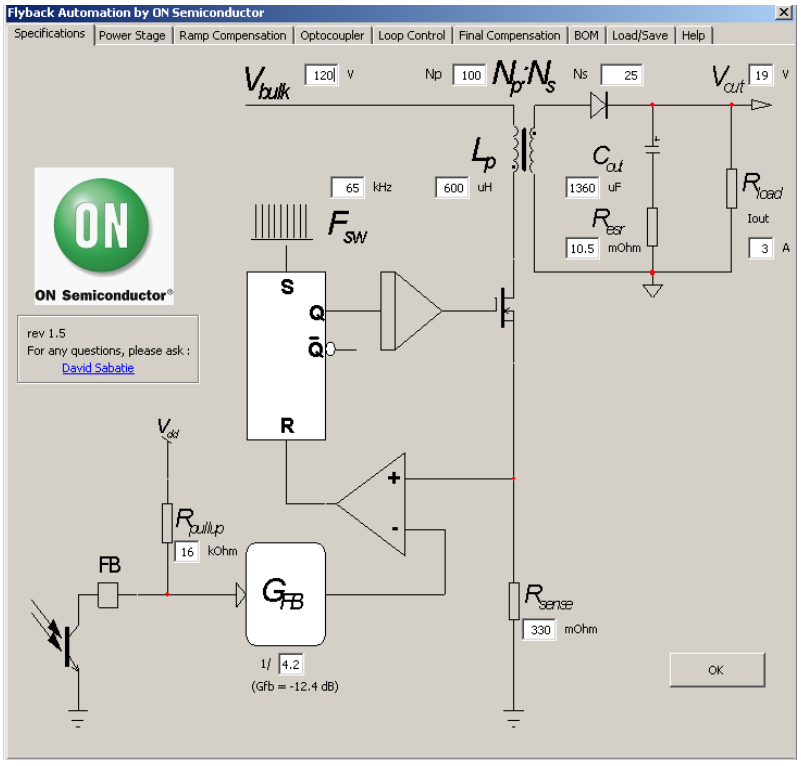

Figure 5. The Opening Panel Shows the Basic Flyback Architecture Where the Operating Parameters Must Be Entered

All fields are populated with the required numbers and the ok button can now be pressed. The next panel appears in Figure 6. This panel displays the small−signal response of the flyback converter power stage, *H(s)*. The position of the poles and zeros attached to this stage appear in the top of the window. The converter operates in the Continuous Conduction Mode (CCM) and exhibits a duty−ratio of 39%. As you can see, there are several color zones in the panel. These zones highlight the limits brought by the TL431−based compensation circuit. As indicated in Ref. [1], the system features a so−called fast lane that prevents the system from attenuating rather than amplifying. We can show that at high frequencies, when capacitor C_6 of Figure 1 is a short−circuit, the transmission gain becomes:

$$G(s) = \frac{R_{pullup}}{R_{LED,max}} CTR \qquad \text{(eq. 5)}$$

Where CTR is the optocoupler Current Transfer Ratio, $R_{LED,\max}$ is the maximum LED series resistor that can be used without affecting the TL431 bias point (R_8 in Figure 1) and R_{pullup} is the internal pull−up resistor inside the NCP1250. The software computes $R_{LED,\max}$ internally and uses the CTR value supplied in the optocoupler tab. In this case, it is found that the minimum attenuation is ≈−3 dB. Should ask for a 10 dB attenuation, the TL431 could simply not do it as it would require a LED resistor greater than $R_{LED,\max}$. Therefore, any crossover point that requires attenuation beyond 3 dB is rejected as the system cannot do

more than that. For instance, in the gray area at 100 Hz, the type 2 compensator would need to provide an attenuation of 7 dB in order to force a crossover at 0 dB. On the contrary, all points beyond 200 Hz require amplification rather than attenuation and can therefore be selected. Let us pick 1 kHz.

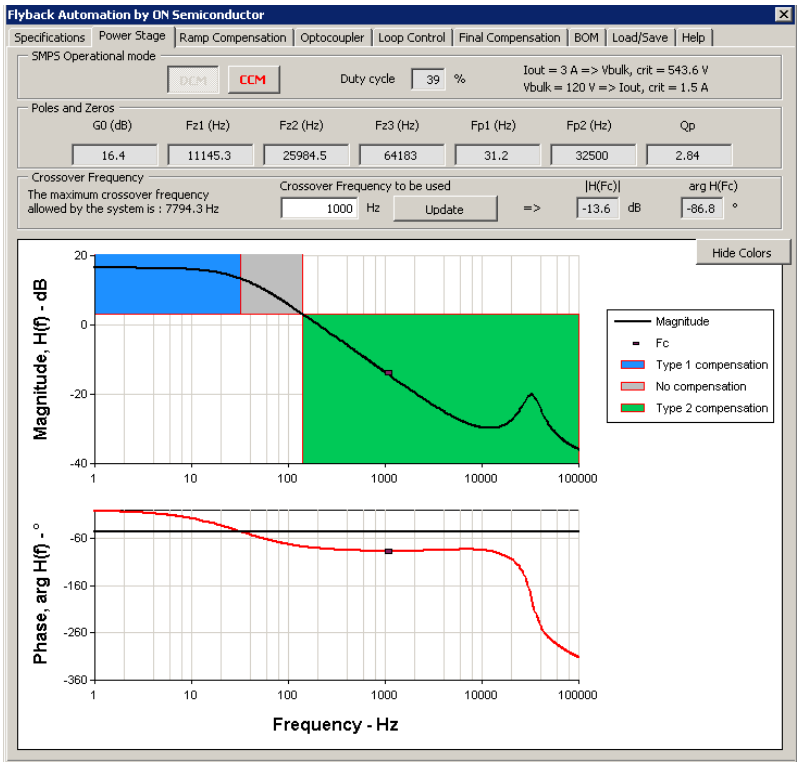

Figure 6. The Power Stage Transfer Function is Now Displayed and Offers Several Crossover Frequency Choices

At 1 kHz, the software indicates a gain deficiency of −13.6 dB together with a phase lag of −86.8°. *G(s)* will thus be tailored to provide a 13.6 dB gain at 1 kHz together with the right boost in phase. Also, the peaking in the curve at half the switching frequency indicates the presence of un−damped sub−harmonic poles and the need for slope compensation.

Compensation Ramp

A compensation ramp is an extra signal which is either subtracted from the feedback signal or superimposed on the current sense signal (the inductor current). Its role is to fight sub−harmonic poles in the current loop located at half the switching frequency. These poles can potentially create oscillations when the duty−ratio approaches 50% in CCM: they must be damped with an external compensation ramp. It can be shown that the power stage transfer function of a current−mode converter operated in CCM obeys a third−order polynomial expression. The equivalent quality coefficient of the double pole depends on the amount of the injected ramp. The software automatically computes the right level to make the quality coefficient Q less than 1 in worst−case conditions. In our application, as shown in Figure 7, the spreadsheet has computed an amount of 33.7% to reduce the quality coefficient below 1. As one can see on the power stage Bode plot, the peaking is well damped. If necessary, you can increase the amount of ramp compensation beyond the suggested 33.7%. However, this is not recommended as more ramp signal (over compensation) will actually push the converter into voltage−mode operation rather than current−mode.

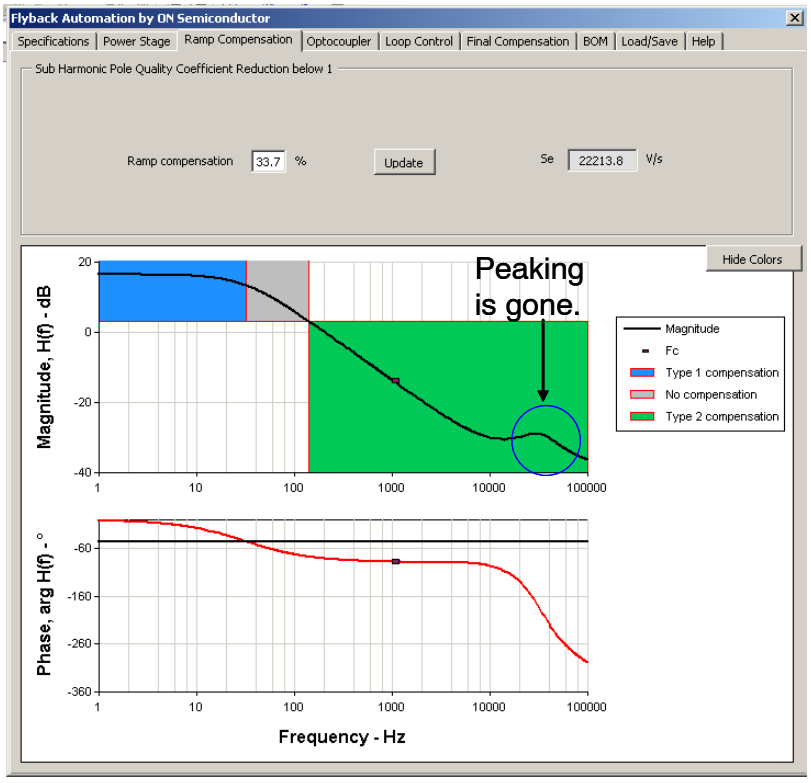

Figure 7. The Software Calculates an Amount of Ramp Compensation of 33.7% to Bring the Double−Pole Quality Coefficient Below 1

The Optocoupler Tab

The figure showing the optocoupler tab appears in Figure 8. In this picture, there are several parameters you need to feed the software with:

- The CTR is the Current Transfer Ratio of the optocoupler. It is simply defined by CTR = I_C/I_d where I_C is the collector current and I_d the LED current. The CTR heavily depends on operating conditions and, in particular, the bias point of the component. These data appears in the optocoupler data−sheet and the minimum value must be entered in the spreadsheet.
- The optocoupler pole illustrates the response speed of the device when operated with a certain pull−up resistor. It has to be characterized (see the PDF file that comes along with the Microsoft Excel spreadsheet) but it also possible to extract it from the data−sheet. The author personally prefers a characterization as it corresponds to the real operating parameters the optocoupler will undergo. If you do not have an idea of the pole position, you can pass the following rough data that will need to be further adjusted. They correspond to measurements carried on a SFH615A device. It all depends on the pull−up resistor actually:

  R_{pullup} = 20 kΩ, $f_p \approx$ 4−6 kHz
  R_{pullup} = 10 kΩ, $f_p \approx$ 6−10 kHz
  R_{pullup} = 4.7 kΩ, $f_p \approx$ 10−15 kHz
  R_{pullup} = 1 kΩ, $f_p \approx$ 20 kHz

- The other dc parameters such as the LED forward drop, the saturation voltage and the V_{DD} are fairly common and play on the dc point calculation, not the ac one.

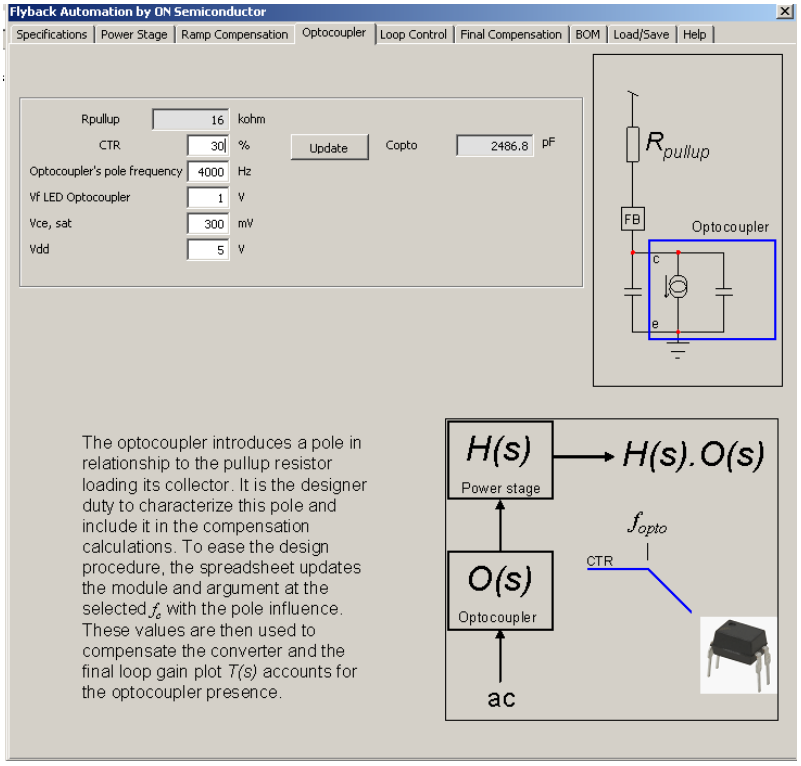

Figure 8. The Optocoupler Needs Some Characterization Data So That Its Presence is Accounted for During the Design Phase

Loop Control

Now that we have a damped power stage, let's see the compensation strategy the software has adopted. Back to Figure 6, the selected 1 kHz crossover frequency requires an upper shift of +13.6 dB. *G(s)* will thus be shaped to provide a 13.6 dB gain at 1 kHz. Regarding the phase, the Bode plot of *H(s)* shows a phase lag of −88° at 1 kHz. Looking for a 60° phase margin (PM), the software will calculate the necessary boost in phase *G(s)* must provide at 1 kHz. It is computed the following way:

$$\arg H(1\text{ kHz}) + \arg G(1\text{ kHz}) + \text{boost} = -360 + PM \quad \text{(eq. 6)}$$

We know that arg *H*(1 kHz) is −88° and the presence of an inversion with an origin pole in *G(s)* gives a permanent −270° phase lag. Asking for a 60° phase margin, we can extract the necessary phase boost the software will need to compute:

$$\text{boost} = -360 + PM - \arg H(1\text{ kHz}) - \arg G(1\text{ kHz})$$
$$= -360 + + 60 + 88 + 270 = 58° \quad \text{(eq. 7)}$$

This the value calculated by the software as illustrated in Figure 9.

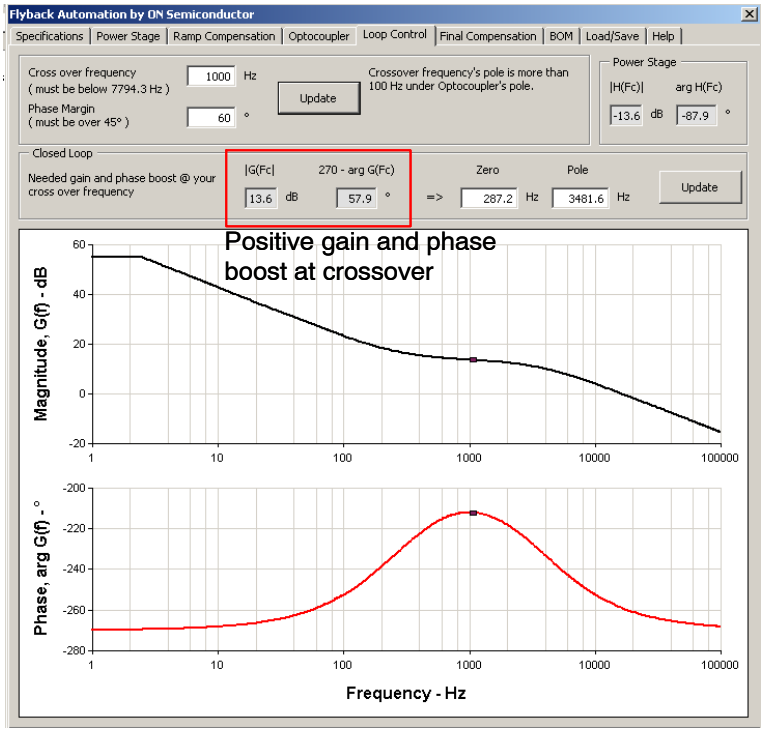

Figure 9. The Software Selects the Pole and Zero Position so that the Maximum Phase Boost Occurs Right at the Geometric Mean Between the Pole and Zero

As you can read, the software decided to place a pole at 3.5 kHz and a zero at nearly 300 Hz. As expected, the phase boost peaks right in the geometric mean of these two values:

$$f_{boost,max} = \sqrt{f_p f_z} = \sqrt{3.48k \times 0.287} \approx 1\ kHz \qquad \text{(eq. 8)}$$

Final Compensation

Having all these elements on hand, the software can now evaluate the needed compensation elements around the TL431. This is the tab “final compensation” that includes the computed values. It appears in Figure 10. This panel now allows you to change, on the fly, the operating conditions (input voltage, output current) but it also lets you vary the parasitic component values, e.g. the capacitor ESR or the optocoupler CTR. Please look in the concerned data−sheet to check the effects of changing these values and make sure the phase margin never goes below 45° roughly. Should you find sections where the phase margin goes too low, you can either select a different crossover frequency or simply shift the zero down the frequency axis. In the above example, lowering the zero to 100 Hz improves the phase margin by 10°.

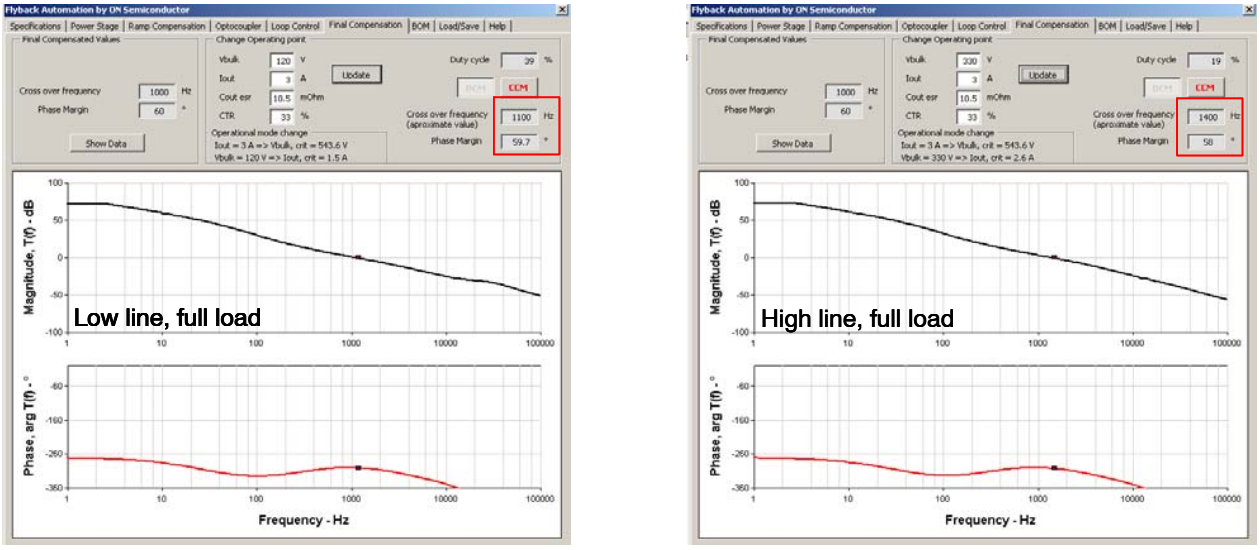

Figure 10. Once Compensated, the Circuit Shows the Expected Phase Margin at Crossover. The Gain Margin is Also Ok

The TL431 Stage

Once everything is calculated by the software, the panel Bill of Material (BOM) can be opened. As shown in Figure 11, the type 2 implementation requires a single capacitor C_{zero} (C_6 on the board) between the divider network and the TL431 cathode.

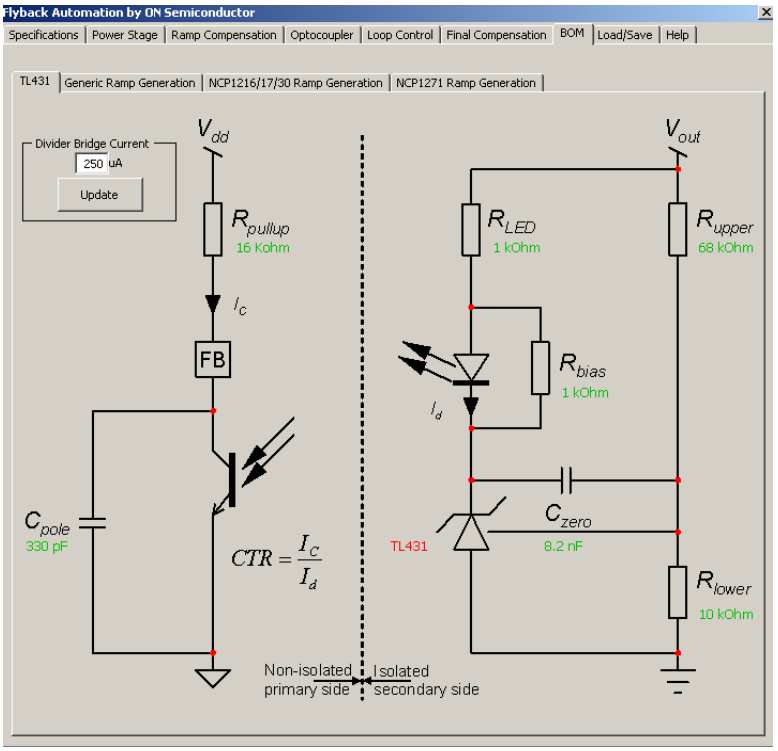

Figure 11. A Type 2 Implementation with a TL431 Requires a Single Capacitor Between the Cathode and the Divider Network

The 1 mA bias current for the TL431 is made by either paralleling a 1 kΩ resistor with the optocoupler LED or by implementing the ON Semiconductor proprietary technique of bias disconnection. As shown in the upper right corner of Figure 1, the technique involves D_4, C_{11} and R_{19}. When the power supply is loaded, the voltage across C_{11} is almost that of the output, fully biasing the TL431 via R_{19}. In light load conditions or in lack of load, C_{11} being weak, the voltage across its terminals simply collapses and the TL431 bias fades away. In this mode, with a 19 V output, you save 20 mW on the secondary, reflected as a power gain around 30 mW − 40 mW on the primary. This method naturally improves the no−load standby power performance as well as the efficiency in other moderate loading conditions.

In this panel also appears the slope compensation circuitry. In the NCP1250, an internal buffered saw tooth ramp drives the current sense pin via a 19 kΩ resistor. The software thus computes the resistor that has to be inserted in series with the current−sense resistor in order to provide the adequate amount of ramp compensation. Figure 11 shows the value computed by the software for the recommended compensation value.

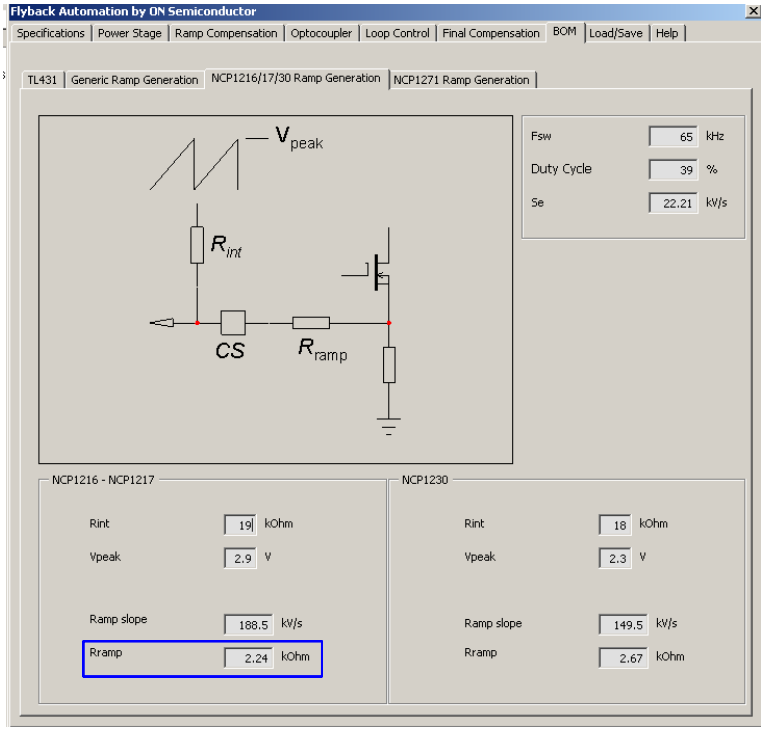

Figure 12. Inserting a Resistor in Series With the Current−Sense Pin Offers a Convenient Way to Compensate the Circuit

Final Tests

If the Microsoft Excel spreadsheet calculates all the elements for us and shows the theoretical compensation results, it is mandatory to test the prototype results to see if the assumptions we made were correct. Once the board is assembled, you should carry a loop gain analysis using a network analyzer. For this purpose, the loop must be opened in order to insert the ac stimulus. This is what Figure 13 shows where the ac source (actually a 20 Ω resistor associated with a transformer) is brought. Please note the short circuit of the series inductance to make sure the fast lane and the slow lane observe a common signal, V_{out}. As the resonance brought by L_2 and C_7 is ten times away from the 1 kHz crossover value, it has little effect on the final phase margin. Further to a warm−up period of 15 minutes, we obtained the curves displayed in Figures 14 and 15. Both graphs show a good agreement with the theoretical calculations brought by the automated software. The small phase difference can come from the ESR values of the capacitors, known to exhibit a fairly large spread. It is now your duty, as a designer, to sweep all possible values of CTR, ESR and input/output conditions to check that the phase margin always remains within the adequate range, usually above 45° at worst case. This exercise could also be automated as a Monte Carlo analysis on a SPICE simulator. Average models such as those found in Ref. [1] lend themselves very well to the exercise.

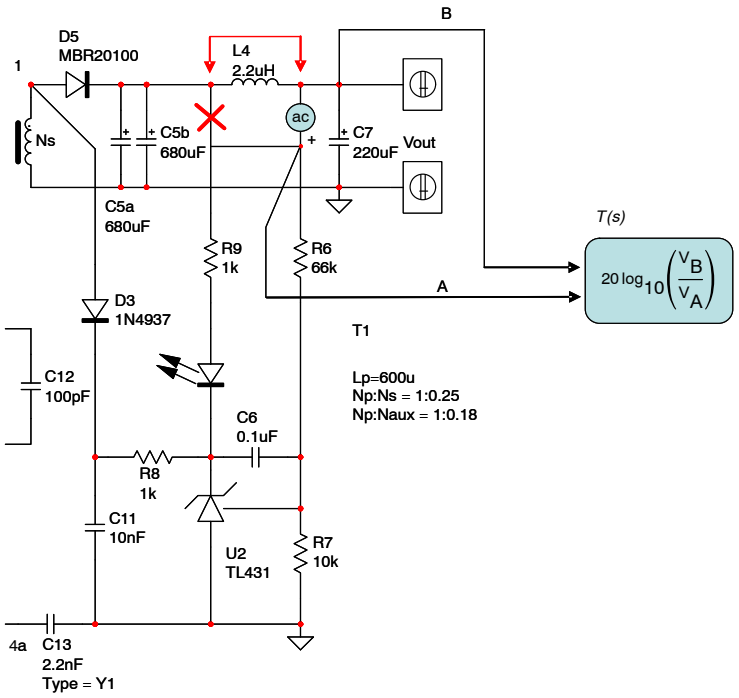

Figure 13. The Loop Opening Requires that You Un−solder One Terminal of R9 and Connect it to V_{out} in Order to Shunt the Fast Lane

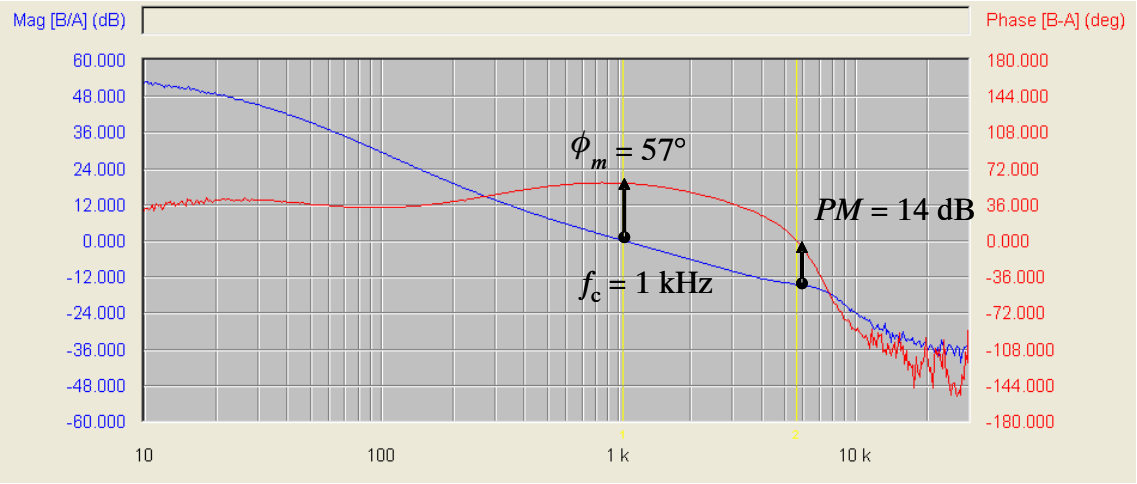

Figure 14. The Low−Line Full−Load Chart Confirms the Good Phase Margin of the Power Supply

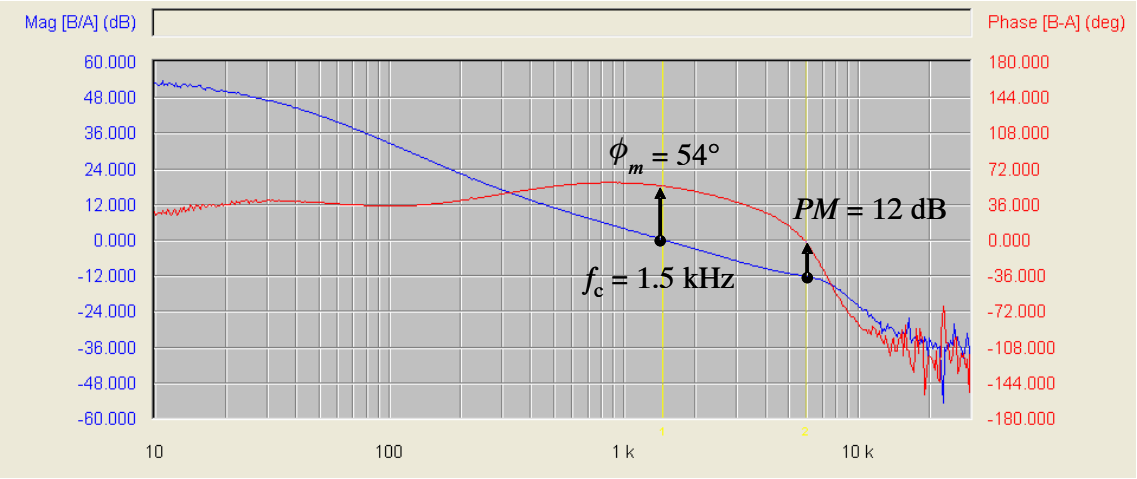

Figure 15. The High−Line Test Also Shows an Adequate Phase Margin at Full Load

Finally, further to these experiments, a transient step confirms the stability of the converter at both input levels as shown in Figure 16. Please note that the oscilloscope shot was taken at the end of a 1.8 m long adapter cable. The load was swept from 0.1 A to 3 A in a slew−rate of 1 A/μs.

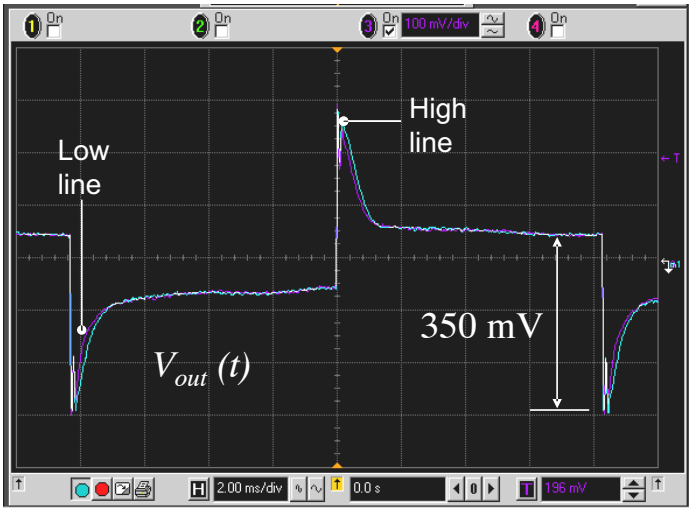

Figure 16. Stability is Ensured Whatever the Input Voltage is, Here at Full Load

Conclusion

This application note together with Ref. [3] shows how an automated sheet could help speeding−up the stabilization process of a switching power supply. Despite the simplicity of the interface, the large equations behind the scene must not make you forget that loop control remains an important design phase of a power supply project inception. A particular attention must be paid to the hidden contributors such as capacitor ESRs and their unavoidable production spreads. Analytical analysis must therefore be accompanied by a thorough investigation on how these elements will impact the converter stability. Finally, despite simulation and analysis tools, it is important to keep bench experiments as a mandatory validation exercise.

References

1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw−Hill, 2008
2. http://www.onsemi.com/pub/Collateral/FLYBACK%20DWS.XLS.ZIP
3. C. Basso, “Loop Control: Hand Calculations or Automation”, How2Power Newsletter December 2009, http://how2power.com/newsletters/0912/index.html

Microsoft Excel is a registered trademark of Microsoft Corporation.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

AND8453/D