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## AMIS-30622 and AMIS-30624 I<sup>2</sup>C Bus Level Shifter

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### APPLICATION NOTE

AMIS-30622 and AMIS-30624 uses a simple bi-directional 2-wire bus for efficient inter-IC control. This bus is called the Inter Integrated Circuit bus or I<sup>2</sup>C bus. The bus voltage of AMIS-30622 and AMIS-30624 is 5 V. Because the I<sup>2</sup>C bus specification does not specify the bus voltage, it's possible that the master controlling AMIS-30622 and/or AMIS-30624 operates at another bus voltage making direct communication impossible.

This application note describes how communication between a master and AMIS-30622 or AMIS-30624 can be done when the master does not use a 5 V I<sup>2</sup>C bus.

#### Introduction

The I<sup>2</sup>C bus consists out of two wires called the serial data (SDA) and serial clock (SCL). Each device connected to the bus is recognized by a unique address and operates as either a transmitter or receiver, depending on the function of the device. AMIS-30622 and AMIS-30624 can both transmit and receive data but will never initiate data transfer. This is why AMIS-30622 and AMIS-30624 are called slave devices.

Figure 1 gives an example of how four stepper motor drivers can be controlled by using the I<sup>2</sup>C bus.

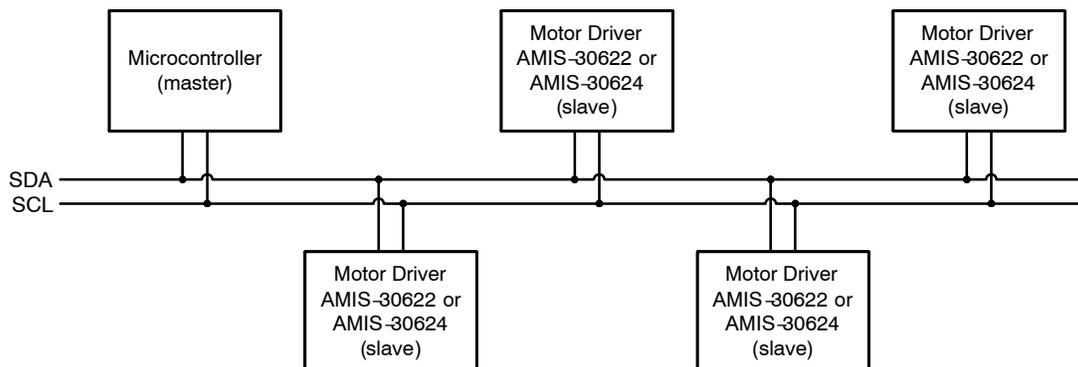


Figure 1. Example of an I<sup>2</sup>C Bus Configuration Using Four Stepper Motor Drivers (Note 1)

The master initiates the data transfer and determines the speed of the communication (master generates clock signal). Although in Figure 1 only one master is displayed, the I<sup>2</sup>C bus specification states that more than one master can be connected to the same I<sup>2</sup>C bus. This means that more than one master could try to initiate data transfer at the same time.

To avoid chaos, an arbitration procedure is used that relies on the wired-AND connection of all I<sup>2</sup>C interfaces to the I<sup>2</sup>C bus. For this the output stages of the devices connected to the I<sup>2</sup>C bus have an open-collector or open-drain output as displayed in Figure 2.

1. Master contains necessary I<sup>2</sup>C bus pull-up resistors

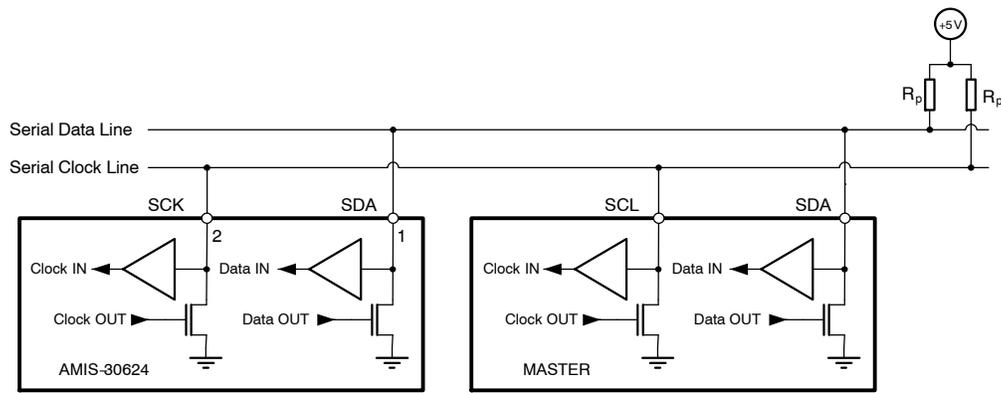


Figure 2. Connection to the I<sup>2</sup>C Bus

More information about the I<sup>2</sup>C bus can be found in the AMIS-30622 and AMIS-30624 datasheet (Ref. 1) or the I<sup>2</sup>C bus specification (Ref. 5).

### Problem Description

As can be read in the AMIS-30622 and AMIS-30624 datasheet, a high level on the I<sup>2</sup>C bus should minimum be  $0.7 \times V_{DD}$ . In worst case scenario,  $V_{DD}$  will be 5.5 V resulting in a minimum high level on the I<sup>2</sup>C bus of 3.85 V.

If the bus-lines are pulled up to 5 V (as displayed in Figure 2), a high level on the I<sup>2</sup>C bus lines will be higher than 3.85 V making communication possible. If a 3.3 V microcontroller is used, the I<sup>2</sup>C bus lines will be pulled up to 3.3 V. This will result in a too low logic '1' signal on the bus making communication with AMIS-30622 or AMIS-30624 impossible.

### Solutions

Several solutions are possible.

#### 5 V Tolerant IO's

The simplest solution is to use a 3.3 V master (microcontroller) with 5 V tolerant IOs. In this way the I<sup>2</sup>C bus lines can be pulled up to 5 V (similar like when a 5 V master is used) making communication between the master and motor driver possible without destroying the master.

Although this is the simplest solution, it will in most cases not be the cheapest solution.

#### Discrete MOSFET Level Shifter

Every bus line has the same level shifter which consists out of a single discrete N-channel enhancement MOSFET. The gate of the MOSFET has to be connected with the lowest supply voltage, the source with the bus line of the lower voltage section and the drain with the bus line of the higher voltage level.

Figure 3 gives an application example by using a Dual N-Channel MOSFET NTMD4840 from ON Semiconductor. A 3.3 V microcontroller is connected with AMIS-30622 or AMIS-30624. For this a 3.3 V and a 5 V voltage regulator (Note 2) are needed ( $U_2$  and  $U_3$ ). The 3.3 V voltage regulator is needed to power the microcontroller and for the pull-up resistors of the 3.3 V I<sup>2</sup>C bus. The 5 V voltage regulator is needed for the 5 V I<sup>2</sup>C bus pull-up resistors (Note 3).

Depending on the required I<sup>2</sup>C speed, pull-ups of 1 k $\Omega$  to 10 k $\Omega$  ( $R_2 \dots R_5$ ) are needed.

Although this is a simple I<sup>2</sup>C bus level shifter, it has no low stand-by power mode or can not be disabled. For high speed applications, low pull-up resistors are required resulting in more power consumption.

2. In this application example a linear voltage regulator is chosen. Another voltage regulator could also be used.  
 3. The VDD pin of AMIS-30622 and AMIS-30624 can deliver maximum 10  $\mu$ A. Because of this the VDD pin may never be used for the 5 V I<sup>2</sup>C bus pull-up resistors. It can however be used as a reference for a voltage follower.

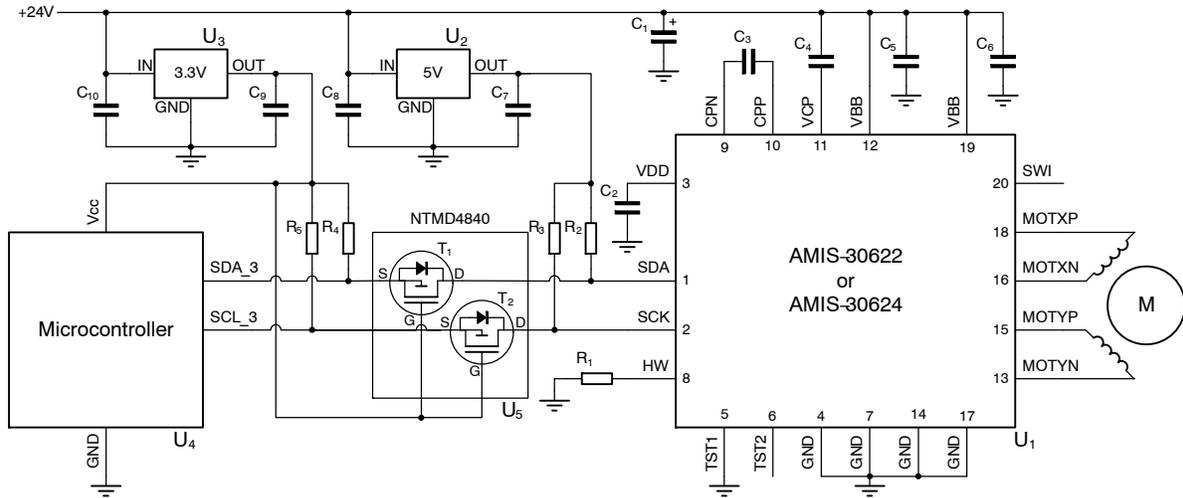


Figure 3. Application Example with Discrete Level Shifter

**Standard I<sup>2</sup>C Bus Level Translator**

Standard I<sup>2</sup>C bus level translator are available that allow bidirectional voltage translation making communication between a 3.3 V master and the motor driver possible. The

ON Semiconductor NLSX4373 2-bit level translator also has integrated 10 kΩ pull-up resistors making it an ideal (1 component) solution for an I<sup>2</sup>C bus level shifter.

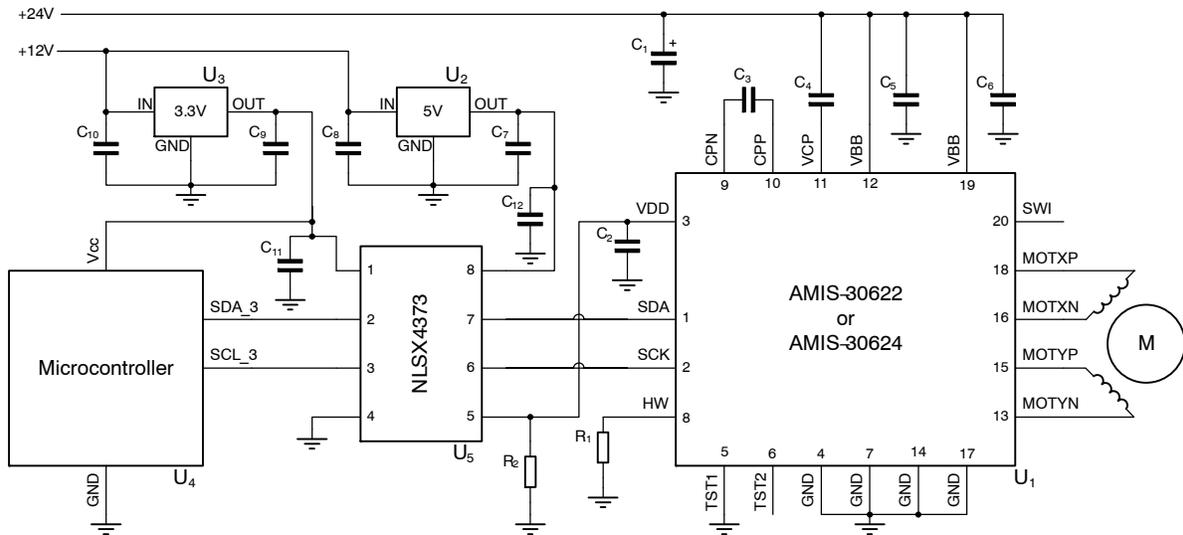


Figure 4. Application Example with 2-bit Level Translator

A high level of 3.3 V placed on the bus by the master will be translated to a high level of 5 V by the I<sup>2</sup>C bus level shifter. In the opposite direction, a high level of 5 V placed on the bus by the motor driver will be translated to a high level of 3.3 V. In this way, communication between two I<sup>2</sup>C busses with different voltage levels is possible.

The VDD pin of stepper motor driver U<sub>1</sub> is connected with the EN pin of the level translator U<sub>5</sub>. When V<sub>BB</sub> (+24 V) gets disconnected the microcontroller is still powered as also the I<sup>2</sup>C bus (in this example). Pin 5 of the level translator U<sub>5</sub> will be pulled low and the IO's of the level translator U<sub>5</sub> are put in high impedance (Note 4).

4. Advised value for R<sub>2</sub> is 1 MΩ.

## AND8449

Figure 5 displays the signals from the application example given in Figure 4. The purple and green curve is the I<sup>2</sup>C communication at the microcontroller side (3.3 V level).

The yellow and blue curve is the I<sup>2</sup>C communication at the motor driver side (5 V level). Notice that the measurement is done at maximum I<sup>2</sup>C speed.

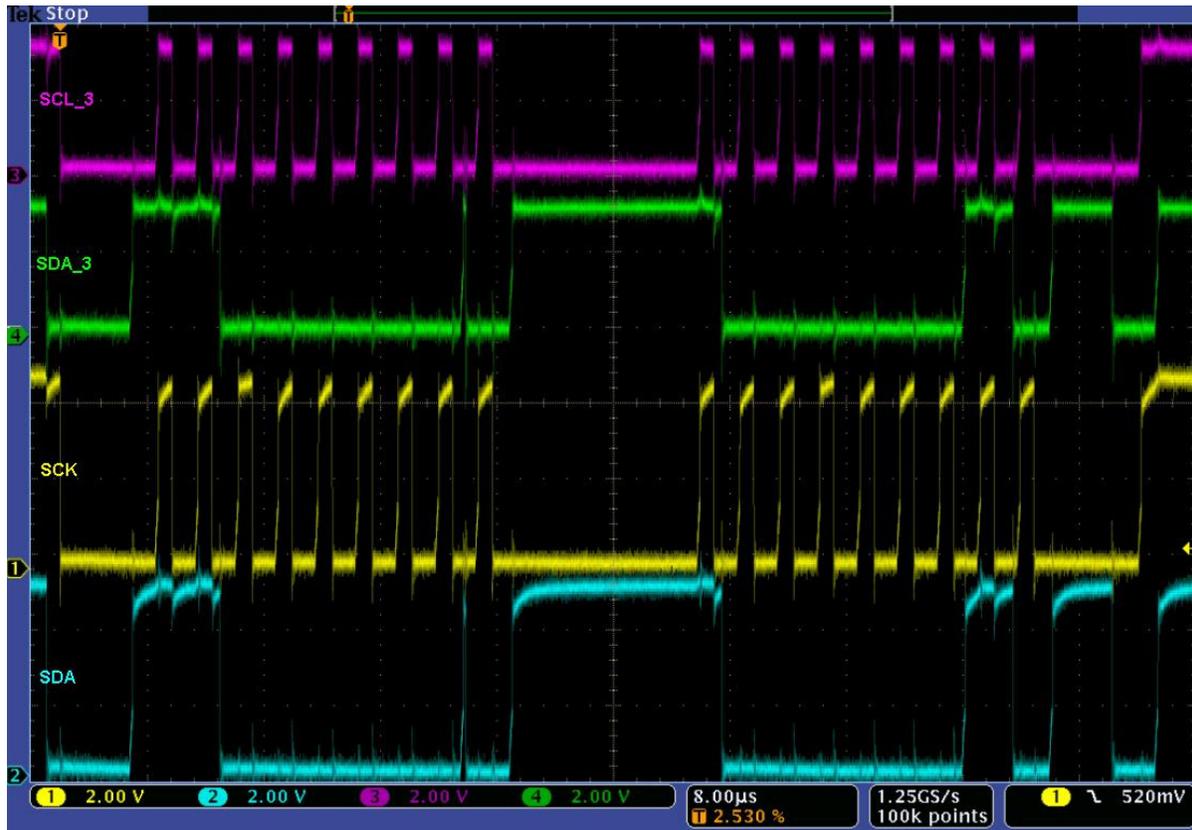


Figure 5. I<sup>2</sup>C Level Shifter Measurement

### IMPORTANT REMARK

Important to know is that the I<sup>2</sup>C level shifter has to be bidirectional for SCK and SDA! SDA is logical because AMIS-30622 and AMIS-30624 needs to acknowledge every data transmission. SCK also needs to be bidirectional because AMIS-30622 and AMIS-30624 can hold the clock line low between two bytes (called clock stretching, see I<sup>2</sup>C specification). Using a simple 5 V buffer with a 3.3 V compliant input as level shifter for the clock line can result in a non-working I<sup>2</sup>C communication.

### References

1. AMIS-30622 and AMIS-30624 Stepper Motor Driver datasheet, [www.onsemi.com](http://www.onsemi.com)
2. NLSX4373, 2-bit 20 Mb/s Dual-Supply Level Translator datasheet, [www.onsemi.com](http://www.onsemi.com)
3. NTMD4840, Dual N-Channel MOSFET datasheet, [www.onsemi.com](http://www.onsemi.com)
4. Application Note AND8336, Design Examples of On Board Dual Supply Voltage Logic Translators, [www.onsemi.com](http://www.onsemi.com)
5. UM10204, I<sup>2</sup>C Bus Specification and User Manual, Rev. 03, 19 June 2007, [www.nxp.com](http://www.nxp.com)
6. Application Note AN10441, Level Shifting Techniques in I<sup>2</sup>C Bus Design, [www.nxp.com](http://www.nxp.com)

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