ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

AND8388/D

Input Dynamic Range Extension of the BelaSigna® 300 Series

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

This application note describes the functioning of the BelaSigna 300 input dynamic range extension (IDRX) feature. The goal of this document is to allow our customers to use this feature in their applications. This document describes the functioning of the IDRX, as well as the configuration parameters related to the IDRX.

In most hearing instruments, the dynamic range of the analog−to−digital (AD) converters is typically 90 dB. For some high precision sound processing, this is not sufficient. This is the reason why ON Semiconductor developed the IDRX concept on the BelaSigna 300 DSP series.

Through the IDRX technology, a pair of 90 dB BelaSigna 300 AD converters can combine to provide an extended 110 dB dynamic range. Combined with a 24−bit DSP architecture, the BelaSigna 300 provides a high precision sound quality.

CONCEPT

High Level Description

The concept of the IDRX is to combine two AD converters to increase the overall input stage dynamic range.

This feature is based on the selection between two ADCs based on variation in the energy of an incoming signal that is provided to both ADCs. The principle is based on switching between both ADCs, depending on the variation of energy of the incoming signal. In parallel, the preamplifiers of both ADCs are also changed based on the energy of this input signal.

For example, when the amplitude of the input signal is above a certain limit, the first AD converter is used to provide the input signal. If its amplitude decreases to a level below that limit, the second AD converter will have its amplification updated to a higher value and the input signal source will be switched to use this converter.

A built−in controller will track the input, and depending on the energy, will set the gain of the unused amplifier. Then, it will switch to the corresponding channel.

Figure 1 shows the high level implementation of this feature:

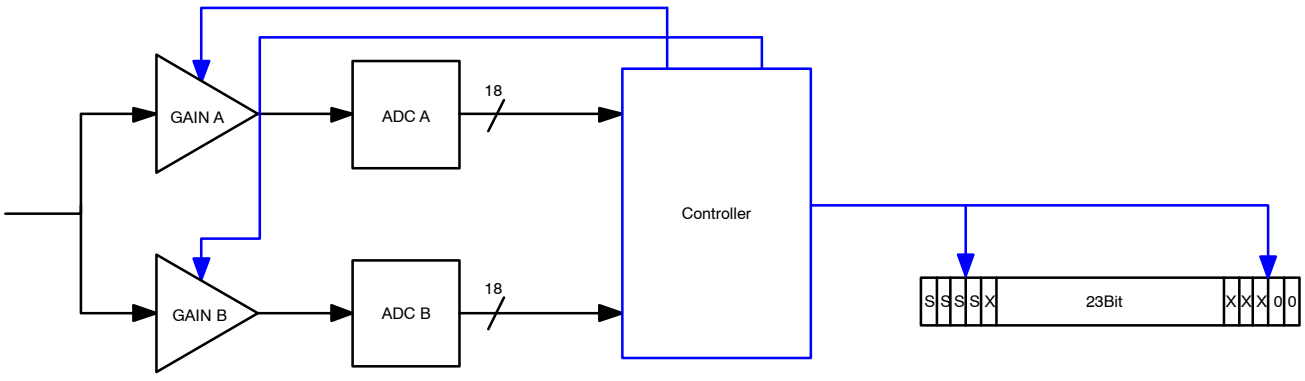

Figure 1. IDRX High Level Block Schematic

Achieved Dynamic Range

Even if the BelaSigna 300 AD converters are 16 bits converters, the output of the decimation and interpolation filters are 18 bit data. Although each ADC is only a 16−bit converter, the output generated by the decimation and anti−aliasing filter when down sampling the provided 16−bit over sampled data is 18−bit output data. As a result, all input data provided by the input stage to the system is handled as 18−bit data.

The maximum 110 dB dynamic range provided by this feature is calculated from the dynamic range that is obtained with the preamplifier configured for 0 dB and 30 dB of preamplifier gain. The dynamic range of the AD converter is approximately 80 dB when using 30 dB of preamplifier gain. By using the switching method between gains from 30 dB to 0 dB, an additional 30 dB of dynamic range will be added, thus the 110 dB range is reached.

Figure 2 shows the behavior of the IDRX controller for an increasing input signal:

The weakest input signal will transition through AD0, preamp gain will be set to PG=30dB

At the 1st amplitude threshold, the signal path is switched through AD1, with preamp gain set to PG=24dB

At the 2nd amplitude threshold, the signal path is switched back to AD0, with preamp gain set to PG=18dB

At the 3rd amplitude threshold, the signal path switched again to AD1, with preamp gain set to PG=12dB

At the highest possible amplitude, the signal will transition through AD0 with preamp gain set to PG=0dB

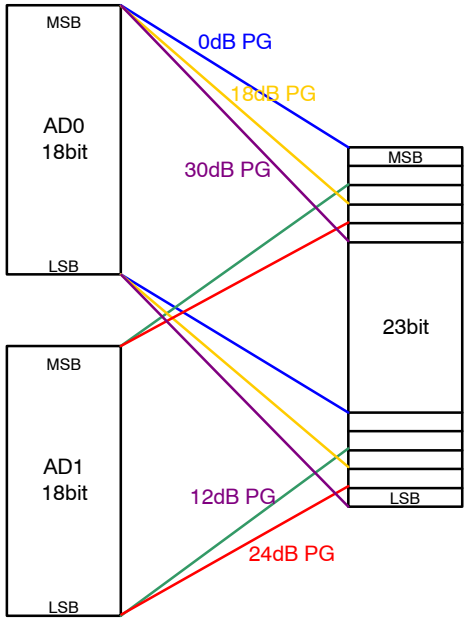

Figure 2. IDRX Behavior for an Increasing Signal

The BelaSigna 300 DSP is a 24−bit architecture, and its FIFOs are built on 24−bit memory. In normal input configurations, the input stage provides 18−bit digitized samples that are stored to input FIFOs aligned to either the upper or lower 18 bits of data. These samples are then converted to 24−bit signed data by sign−extending through the unused MSBs or zero padding unused LSBs. Using the IDRX allows the input stage to provide 23−bit data samples to be stored into the input FIFOs, as shown in Figure 2.

CONTROL AND CONFIGURATION REGISTERS

Enabling and Disabling the IDRX

As mentioned in the preceding section, IDRX groups two ADCs together in order to increase the dynamic range. Channel 0 can be grouped together with channel 1 to provide IDRX channel 0. Channel 2 can be grouped together with channel 3 to provide IDRX channel 1.

The user can enable and disable the IDRX feature in two ways:

- To enable the IDRX using channels 0 and 1, bit 7 of the analog input control register should be set.
- To enable the IDRX using channels 2 and 3, bit 15 of the analog input control register should be set.

Table 1. ANALOG INPUT CONTROL REGISTER

Register Name	Register Description	Address
A_INPUT_CTRL	Analog Input Control	0xE141

Table 2. A_INPUT_CTRL SETTINGS FOR IDRX

Bit Field	Field Name	Field Description
15	INPUT_CTRL_IDRX1_ENABLE	Enable/disable dynamic range extended input using channel 2 and 3
7	INPUT_CTRL_IDRX0_ENABLE	Enable/disable dynamic range extended input using channel 0 and 1

Table 3. INPUT_CTRL_IDRX0_ENABLE AND INPUT_CTRL_IDRX1_ENABLE VALUE SYMBOL

Field Name	Value Symbol	Value Description	Hex Value
INPUT_CTRL_IDRX1_ENABLE	IDRX1_ENABLE IDRX1_DISABLE	IDRX 1 Enable IDRX 1 Disable	0x1 0x0*
INPUT_CTRL_IDRX0_ENABLE	IDRX0_ENABLE IDRX0_DISABLE	IDRX 0 Enable IDRX 0 Disable	0x1 0x0*

*default value.

Important note: When an IDRX input channel is enabled, both of its component input channels need to be connected to the same input signal source. It can be either AI0 connected with AI1 and/or AI2 connected with AI4. See the “External Connections” section for more information.

Minimum and Maximum Preamplifier Settings

The range of the IDRX is controlled by the minimum and the maximum preamplifier values. By default, the minimum preamplifier gain will be 0 dB, and the maximum preamplifier gain will be 30 dB. In this case, the dynamic range will be extended by 30 dB. This default use case was used to show the typical IDRX behavior in Figure 2.

For a reason linked with a specific application use case, the programmer might need to use a smaller overall dynamic range. To do this, the minimum and the maximum preamplifier values can be set. For example, by setting the maximum preamplifier value at 24 dB, and the minimum preamplifier value at 12 dB, the dynamic range would only be extended by 12 dB.

Table 4. IDRX CONFIGURATION REGISTER

Register Name	Register Description	Address
A_IDRX0_CFG	IDRX Channel 0 and 1 Configuration Registers	0xE14C
A_IDRX1_CFG	IDRX Channel 2 and 3 Configuration Registers	0xE14D

Table 5. A_IDRX0_CFG AND A_IDRX1_CFG SETTINGS: MINIMUM AND MAXIMUM PREAMPLIFIER VALUES

Bit Field	Field Name	Field Description
21:20	IDRX_CFG_MAX_PG	Maximum Preamplifier Gain Used by the IDRX
17:16	IDRX_CFG_MIN_PG	Maximum Preamplifier Gain Used by the IDRX

Table 6. IDRX_CFG_MAX_PG AND IDRX_CFG_MIN_PG VALUE SYMBOL

Field Name	Value Symbol	Value Description	Hex Value
IDRX_CFG_MAX_PG	IDRX_MAX_PREAM_GAIN_12 IDRX_MAX_PREAM_GAIN_18 IDRX_MAX_PREAM_GAIN_24 IDRX_MAX_PREAM_GAIN_30	Preamplifier Maximum Gain is 12db Preamplifier Maximum Gain is 18db Preamplifier Maximum Gain is 24db Preamplifier Maximum Gain is 30db	0x0 0x1 0x2 0x3*
IDRX_CFG_MIN_PG	IDRX_MIN_PREAM_GAIN_0 IDRX_MIN_PREAM_GAIN_12 IDRX_MIN_PREAM_GAIN_18 IDRX_MIN_PREAM_GAIN_28	Preamplifier Minimum Gain is 0db Preamplifier Minimum Gain is 12db Preamplifier Minimum Gain is 18db Preamplifier Minimum Gain is 24db	0x0* 0x1 0x2 0x3

*default value

Threshold and Timer Configurations

The channel switching can be configured with two timers and two threshold limits:

- IDRX_CFG_TIMER_1 defines the numbers of samples to be used as delay before the gain of the inactive channel is switched.
- IDRX_CFG_TIMER_2 defines the numbers of samples to be used as delay after the gain of the inactive channel is switched and before the channels are switched. This duration should be longer as the preamplifier stabilization time. If this is not the case, the system switching may cause undesired audio artefacts.
- IDRX_CFG_HIGH_LIMIT defines the high limit threshold that the signal should reach in order to begin the channel switching process.
- IDRX_CFG_LOW_LIMIT defines the low limit threshold that the signal should reach in order to begin the channel switching process.

These settings control the gain setting and switching between channels. The limit values are always relative to the active channel. To prevent endless switching, the difference between the high and low thresholds has to be at least 12 dB if a preamplifier gain of 0 dB is allowed. If the 0 dB preamplifier gain setting is not used the difference between the thresholds must be at least 6 dB.

Switching Algorithm for a Falling Signal

In case of a decreasing input signal, the switching algorithm works as follows. This example illustrates a fall in the observed energy level at the input stage to below the low limit threshold, given by IDRX_CFG_LOW_LIMIT. A slightly different behavior would be seen if the input signal rose above the high limit threshold, given by IDRX_CFG_HIGH_LIMIT.

- When the input amplitude falls below the low threshold limit, the timer T1 is started.
- If the input amplitude rises above the low threshold limit before timer T1 expires, the timer is reset and the selected input channel is not changed. This is shown in Figure 3.

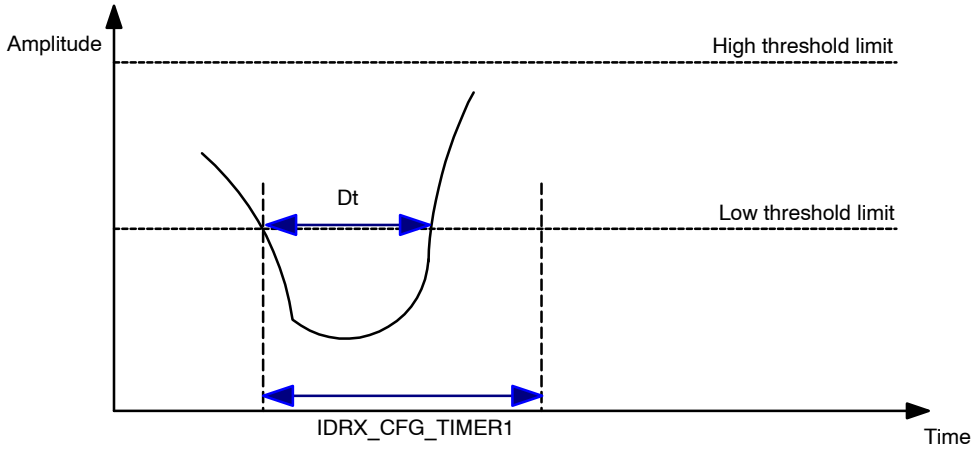

Figure 3. Timer 1 is Reset

- If the timer T1 reaches IDRX_CFG_TIMER_1:
  - The preamplifier gain for the inactive channel is changed, and timer T2 is started.
  - If the input amplitude rises above the low threshold limit before a certain amount of time (IDRX_CFG_TIMER_2), timer 2 expires, timer T2 is reset and the same input channel with the same gain keeps working.
  - If the timer T2 reaches IDRX_CFG_TIMER_2 and the amplitude is still below the low threshold limit, the IDRX block switches to the new channel. This is shown in Figure 4.

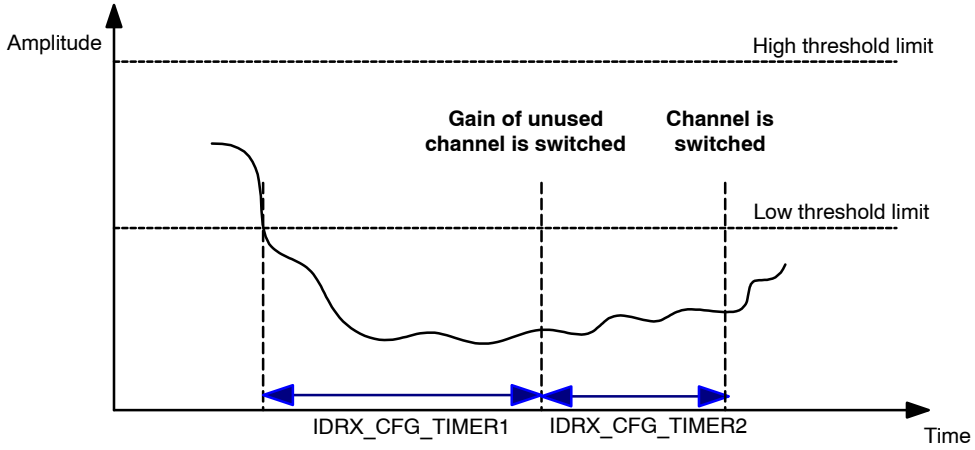

Figure 4. Channel is Switched

The timer T2 can be configured, but the user must make sure that this value is not smaller than the stabilization time of the preamplifier after a change of gain.

Note that if the value preamplifier value does not have to be switched as it has already the desired value, then timer T2 will not be started, and the active channel is switched immediately when timer T1 reaches IDRX_CFG_TIMER1. This situation can be seen for example when the input signal decreases in intensity, producing a gain and channel switch, and directly increasing.

Switching Algorithm for Rising Signal

In case of an increasing input signal, the switching algorithm works as follows. This example illustrates a growth in the observed energy level at the input stage to below the low limit threshold given by IDRX_CFG_HIGH_LIMIT. Here, an extreme saturation should be avoided and timer T1 is never used:

- When the input amplitude rises above the high threshold limit, the preamplifier gain for the inactive channel is changed and timer T2 is started.
- If the input amplitude falls below the high threshold limit before timer T2 expires, the timer is reset and the selected input channel is not changed.
- If the timer T2 reaches IDRX_CFG_TIMER_2 and the amplitude is still above the high threshold limit, the IDRX block switches to the new channel. This is shown in Figure 5.

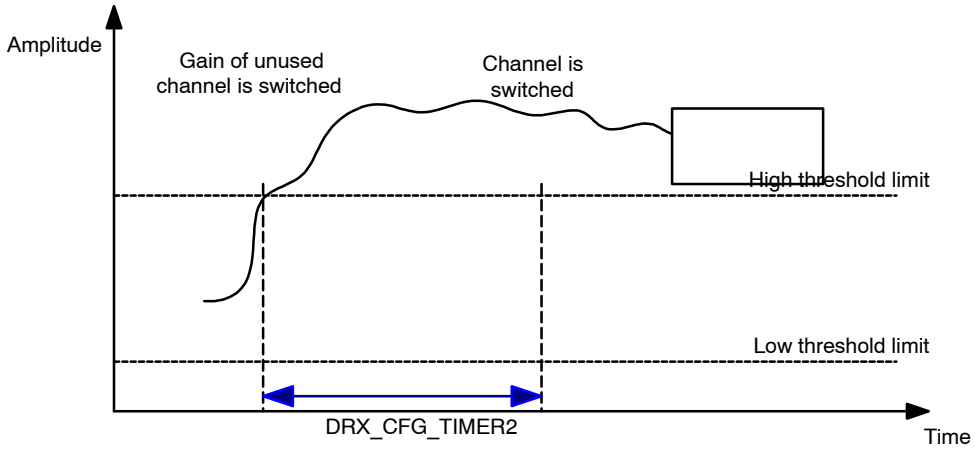

Figure 5. Channel is Switched

Table 7. IDRX CONFIGURATION REGISTER

Register Name	Register Description	Address
A_IDRX0_CFG	IDRX channel 0 and 1 configuration registers	0xE14C
A_IDRX1_CFG	IDRX channel 2 and 3 configuration registers	0xE14D

Table 8. A_IDRX0_CFG AND A_IDRX0_CFG SETTINGS: HIGH AND LOW LIMIT THRESHOLD, TIMER1 AND TIMER2

Bit Field	Field Name	Field Description
15:12	IDRX_CFG_HIGH_LIMIT	High threshold switching limit
11:8	IDRX_CFG_LOW_LIMIT	Low threshold switching limit
7:4	IDRX_CFG_TIMER_2	Timer 2: time delay before the channel is switched. Needs to be longer then the preamplifier stabilization time.
3:0	IDRX_CFG_TIMER_1	Timer 1: time delay before the preamplifier gain of the inactive channel is switched

High Limit Threshold

As mentioned in the "Achieved Dynamic Range" section the amplitude of the incoming signal is digitized to 18 bits. Thus, the range of the input digitalized data is given between -2^{17} and $(2^{17}-1)$.

The high threshold limit is given on 4 bits by the IDRX_CFG_HIGH_LIMIT register with the following relationship:

$$\text{HighThresholdLimit} = (\text{IDRX\_CFG\_HIGH\_LIMIT} \times 4096) + 2048$$

$$\text{HighThresholdLimit(dB)} = 20 \times \log\left(\frac{((\text{IDRX\_CFG\_HIGH\_LIMIT} \times 4096) + 2048)}{2^{17}}\right)$$

For example, if IDRX_CFG_HIGH_LIMIT = 0x0000, the high threshold limit value will be 2048, and this corresponds to –36.1 dB. The default value is IDRX_CFG_HIGH_LIMIT = 0x1001, and this corresponds to 38912 (−10.5 dB).

This limit value is relative to the active channel.

Low Limit Threshold

The low threshold limit is given on 4 bits by the IDRX_CFG_LOW_LIMIT register with the following relationship:

$$\text{LowThresholdLimit} = (\text{IDRX\_CFG\_LOW\_LIMIT} \times 1024)$$

$$\text{LowThresholdLimit(dB)} = 20 \times \log\left(\frac{((\text{IDRX\_CFG\_LOW\_LIMIT} \times 1024))}{2^{17}}\right)$$

For example, if IDRX_CFG_LOW_LIMIT = 0x0001, the low threshold limit value will be 1024, and this corresponds to –42.1 dB. The default value is IDRX_CFG_HIGH_LIMIT = 0x1001, and this corresponds to 9216 (−23.1 dB).

This limit value is relative to the active channel.

Timers

Both time delay settings are given in the number of digitalized samples that the IDRX block gets from the input stage. The two timer values are multiplied by 256 to determine the number of samples to be used as delay.

The timer limits are given on 4 bits by the IDRX_CFG_TIMER_1 and IDRX_CFG_TIMER_2 registers with the following relationship:

$$\text{TimerDelay1} = ((\text{IDRX\_CFG\_TIMER\_1} + 1) \times 256)$$

$$\text{TimerDelay2} = ((\text{IDRX\_CFG\_TIMER\_2} + 1) \times 256)$$

For example, if IDRX_CFG_TIMER_1 = 0x0000, the delay 1 value will be of 256 samples. At 16 kHz, this corresponds to 16ms. For both timers, the default value is 0x0011, and this corresponds to 1024 samples (64 ms at 16 kHz).

Turning off the Inactive Channel

The user of the IDRX has the ability to stop the inactive channel in order to save current consumption. When using this mode, the inactive channel will be switched on as timer T1 reaches IDRX_CFG_TIMER1. In this case, timer T2 should be long enough so that the inactive channel has time to wake−up.

Table 9. IDRX CONFIGURATION REGISTER

Register Name	Register Description	Address
A_IDRX0_CFG	IDRX channel 0 and 1 configuration registers	0xE14C
A_IDRX1_CFG	IDRX channel 2 and 3 configuration registers	0xE14D

Table 10. A_IDRX0_CFG AND A_IDRX1_CFG SETTINGS: ENABLE THE SWITCHING OFF OF THE INACTIVE CHANNEL

Bit Field	Field Name	Field Description
22	IDRX_CFG_ADC_OFF_EN	Switch of the unused channel

Table 11. IDRX_CFG_ADC_OFF_EN VALUE SYMBOL

Field Name	Value Symbol	Value Description	Hex Value
IDRX_CFG_ADC_OFF_EN	IDRX_INACTIVE_ADC_ENABLED IDRX_INACTIVE_ADC_DISABLED	Both channel are always on Inactive channel is switched off	0x0* 0x1

*default value.

EXTERNAL CONNECTIONS

To use the IDRX functionality, the two component input channels that make an IDRX channel have to be connected together on the manufacturer's PCB. It can be either AI0 connected with AI1 and/or AI2 connected with AI4.

Despite the fact that internally in the chip one input can be fed to two or more AD converters, having different pre−amplification factors on the inputs results in differences between the input impedances and DC levels for the two channels. So the channels can not be linked together internally, and this connection must be done at PCB level. Because of this, it is important that the connection between both channels is done before the microphone decoupling capacitance, as shown in Figure 6.

If the DC−remove in the WDF filters is disabled, the output of the IDRX could be erroneous. The decimation filter of channel 3 is slightly different from the decimation filter of channel 2. Due to this asymmetry, the quality of the IDRX channel 0 will be better.

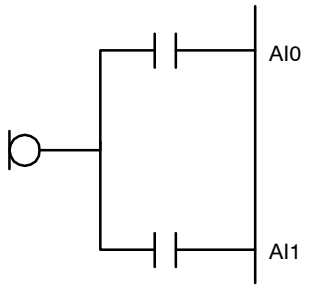

Figure 6. External Connections

BelaSigna is a registered trademark of Semiconductor Components Industries, LLC (SCILLC).

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative