

# ON Semiconductor

## Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

## AMIS-42700 Dual High-Speed CAN Transceiver

### Feedback Suppression

Prepared by:  
ON Semiconductor



ON Semiconductor®

<http://onsemi.com>

### APPLICATION NOTE

#### Introduction and Scope

The AMIS-42700 Dual-CAN transceiver is the interface between up to two high-speed CAN (=HS-CAN) bus lines and the protocol controller and will be used for serial data interchange between different electronic units at more than one bus line. Beside other blocks, it contains two HS-CAN transceivers interconnected with a logic unit.

The logic unit constantly ensures that dominant symbols on one bus line are transmitted to the other bus line without imposing any priority on either of the lines. This feature would lead to an “interlock” state with permanent dominant signal transmitted to both bus lines, if no extra measure is taken.

Therefore feedback suppression is included inside the logic unit of the transceiver. This block masks-out reception on that bus line, on which a dominant is actively transmitted. The reception becomes active again only with certain delay after the dominant transmission on this line is finished.

This application note explains in detail the purpose and characteristics of the feedback suppression. In the second part, it shows measurement results demonstrating the impact of the feedback suppression on the bus signals. Although the

note specifically deals with AMIS42700 – a high-speed CAN repeater – the principles and conclusions can be, to a big extent, used when considering other applications involving repetition of signals between more busses in other network systems.

#### Principle of the Repeater Logic

##### Direct Connection of 2 Transceivers

For the purpose of this application note, a simplified model of a transceiver will be used as depicted in Figure 1. A logical low level on digital pin TxD of the transceiver causes the bus signal going “dominant” while logical high level on TxD pin leaves the bus “recessive”. In the case of the HS-CAN physical layer, “dominant” bus corresponds to a positive differential voltage while “recessive” bus is represented by zero differential voltage. The bus signal is monitored by a receiver signaling the detected level on digital output RxD.

Both the transmission and the reception involve delays as symbolically shown in Figure 1 (the depicted delay values are for illustration only and not to scale).

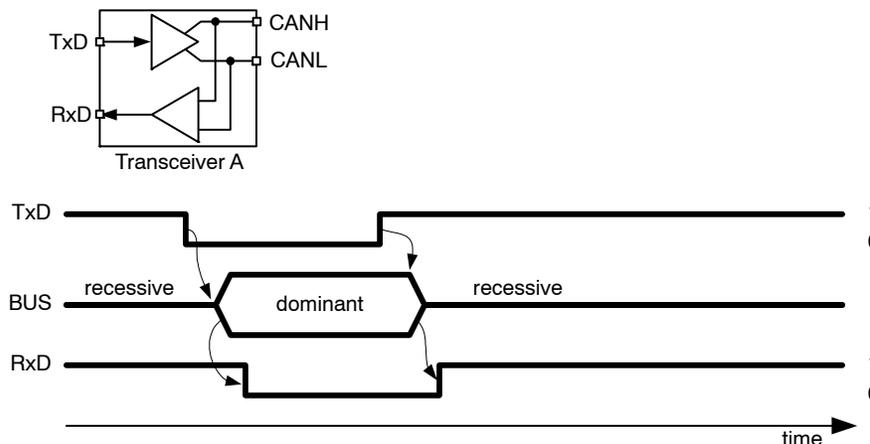


Figure 1. Simplified Model and Timing of a High-speed CAN Transceiver

When two CAN channels should be symmetrically interconnected in order to provide the repetition function, direct connection of two single transceivers via their Tx/D and Rx/D pins presents itself as the easiest solution. According to the example shown in Figure 2, the first dominant signal occurs on BUS1. After the delay needed for correct reception of the dominant symbol, it's signaled on

pin Rx/D1 of the transceiver connected to BUS1. Pin Rx/D1 is directly connected to pin Tx/D2 of the second transceiver which, in turn, re-transmits the dominant signal on BUS2. The delay of the pin interconnection is neglected in this example (in case of an on-chip logic, it's typically negligible compared to the transceiver delays)

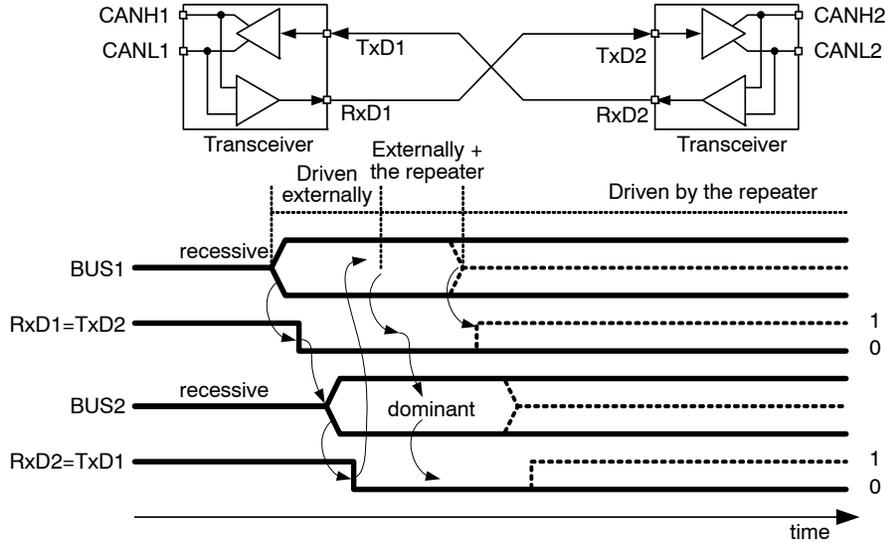


Figure 2. Direct Connection of 2 Transceivers and the Occurrence of a Deadlock on the Bus

However, as the pin interconnection is symmetrical, the dominant symbol on BUS2 will be, with appropriate delays, re-transmitted back on BUS1. The dominant signal on BUS1 is therefore driven both by the external source and the repeater itself. When the external source stops forcing the dominant (the dotted line in Figure 2), BUS1 remains dominant (as so does BUS2) in a self-sustained way, leading to a “deadlock” situation.

locked situation and the communication is blocked. The direct interconnection of Rx/D and Tx/D pins is therefore not sufficient to ensure correct bus signal repetition and extra measures must be taken – they are referred to as “feedback suppression” and will be described in the following paragraph.

The situation described in the above example can be applied also in the opposite direction – i.e. when the first dominant is seen on BUS2 – as the transceivers’ interconnection is fully symmetrical. After the first occurrence of the dominant signal on either bus, the system ends up in a

**Feedback Suppression**

Simplified repeater logic block used in AMIS42700 is shown in Figure 3. Links to the controller pins (Tx0, Text, Rx0, Rint) are not shown but their connection to the repeater logic is, in principle, similar to the internal control of the two on-chip transceivers.

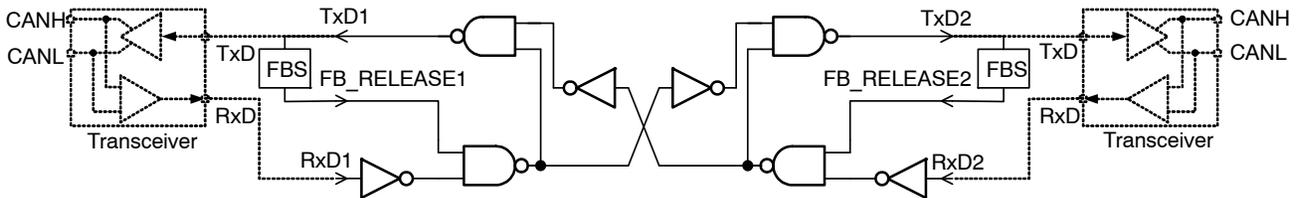
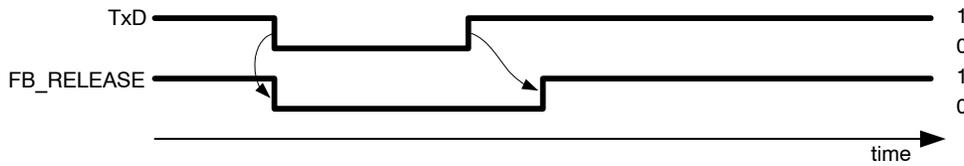


Figure 3. Repeater Logic with Feedback Suppression (FBS) used in AMIS42700 (simplified)

The signals Tx/D1/2 and Rx/D1/2 (which are internal signals inside AMIS42700) have the same meaning as in the direct interconnection of 2 transceivers shown in Figure 2. However, they are not simply cross-connected, but rather mask each other via the block called “FBS” (=feedback suppression). The function of the FBS blocks can be seen from the timing diagram in Figure 4 – as soon as signal Tx/D gets low, thus requesting active transmission of dominant –

the FB\_RELEASE signal gets low as well. Low level of FB\_RELEASE blocks signal Rx/D of the same channel from propagating to Tx/D signal of the other channel. The blocking starts immediately after Tx/D gets low. However, when Tx/D returns to high – i.e. when the transmission of a dominant is not requested any more – the feedback is released only after a certain delay. This allows the bus to return to recessive as well as the receiver to settle in recessive state.

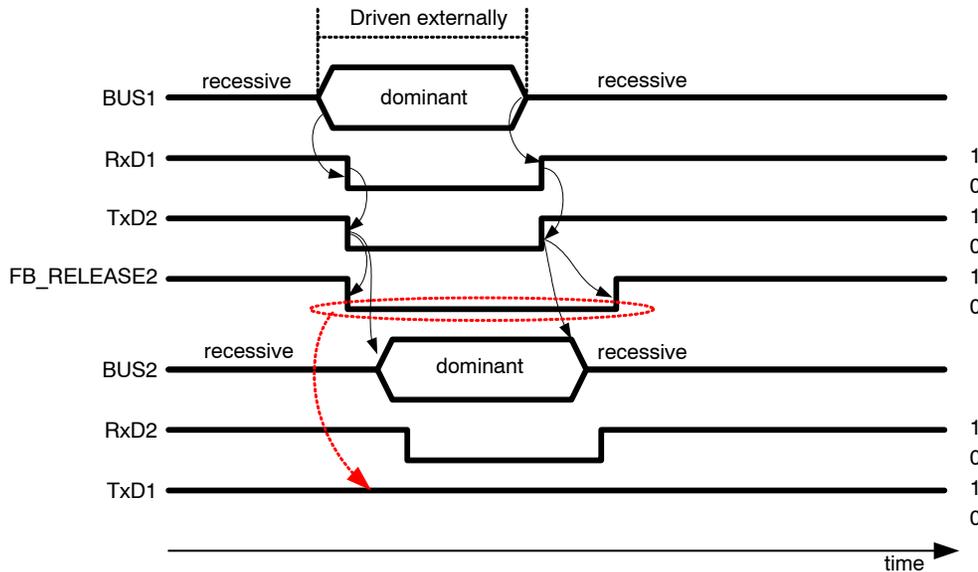
## AND8358



**Figure 4. Function of a Feedback Suppression Block (FBS)**

Figure 5 shows signal repetition with the logic from Figure 3. A dominant signal is again first seen on BUS1. It's received and propagated to internal signal RxD1 directly copied (with negligible delay) to internal signal TxD2. Signal TxD2 ensures re-transmission of the dominant symbol on BUS2. At the same time, signal FB\_RELEASE2 keeps low as long as TxD2 is low and extends slightly beyond the low level of TxD2. Thanks to signal FB\_RELEASE2, the reception of the BUS2 dominant is "suppressed" (i.e. logically masked) as long as BUS2 is

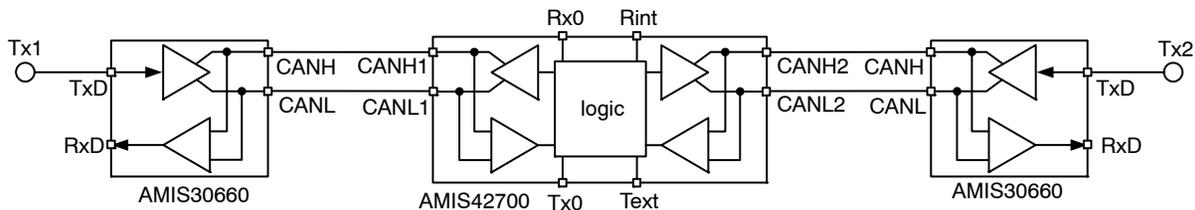
actively driven. When dominant on BUS1 ends, RxD1 and TxD1 return to high and BUS2 settles back to recessive. The BUS2 receiver (signal RxD2) returns to high as well. Thanks to the extension of FB\_RELEASE2 beyond TxD2, the delays of BUS2 transmission and reception don't lead to an interlock – the low-level time extension of FB\_RELEASE signals is designed so, that it covers the sum of transmission and reception delays with sufficient margin. Otherwise, the feedback suppression would become inoperable.



**Figure 5. Signal Repetition Without a Deadlock Thanks to the Feedback Suppression**

### Measurement of the Repeater Function

The function of the AMIS42700 repeater logic was demonstrated with a setup composed of one AMIS42700 HS-CAN repeater and two AMIS30660 standalone HS-CAN transceivers – see Figure 6.

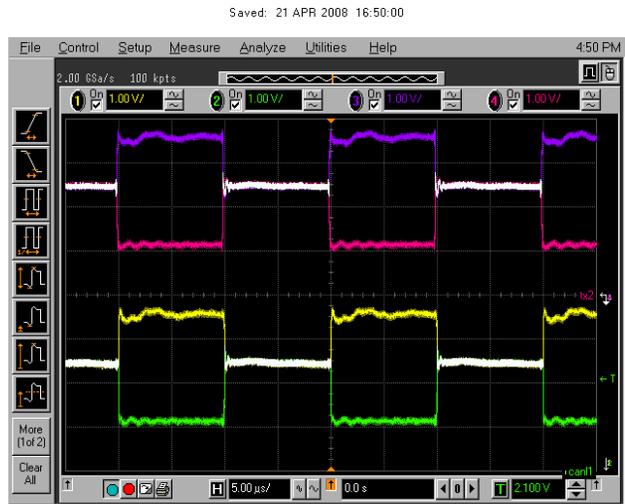


**Figure 6. Measurement setup used to verify the repeater logic of AMIS42700 – bus terminations, common-mode chokes and other components are not depicted.**

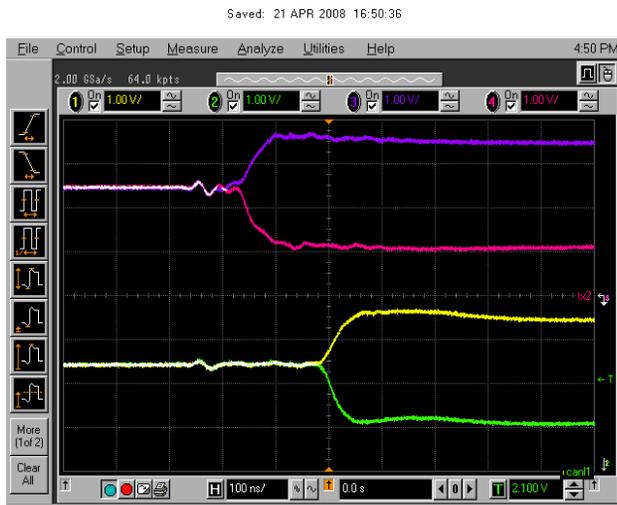
**Measurement of the Repeater Function**

The repeater logic was measured by forcing a rectangular pulse on pin Tx2 in setup of Figure 6 leading to periodic dominants on CANH2 and CANL2. The second transceiver remained passive (Tx1 = High). AMIS42700 was ensuring that the signals on CANH2 and CANL2 were repeated on CANH1 and CANL1. The overall view of the repeater behavior is shown in Figure 7 with zooms to both transitions (recessive->dominant and dominant->recessive) in Figure 8.

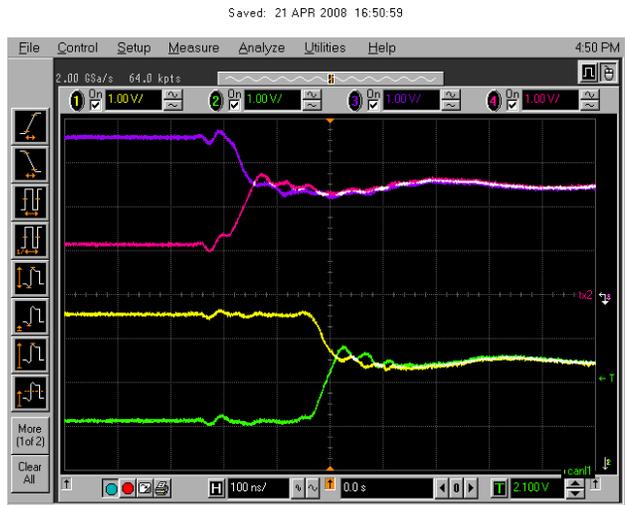
It can be seen that in both directions, the delay from CANH2/CANL2 to CANL1/CANLH1 is ca 150 ns (under typical conditions) – it’s the time needed to receive the signal on one bus plus the time needed to transmit the signal on the other bus – the total delay is equal to the loop delay of one transceiver.



**Figure 7. Signal repetition from CAN bus 2 (blue+ magenta) to CAN bus 1 (yellow + green) in case only one node transmits on bus1.**



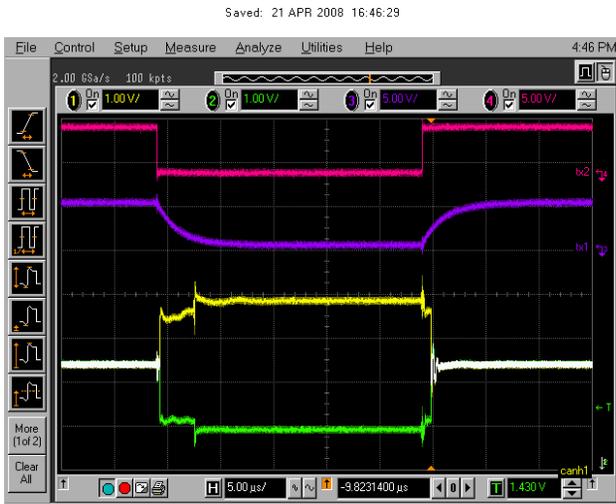
**Figure 8. Signal repetition from CAN bus 2 (blue+ magenta) to CAN bus 1 (yellow + green) in case only one node transmits on bus1. Zooms to both signal transitions**



**Measurement of the Feedback Suppression**

In the “Measurement of the Repeater Function” section, it was shown that dominant signals driven on one bus are correctly re-transmitted on the second bus without any “deadlock” occurring as expected from the feedback suppression feature. In order to visualize the feedback suppression explicitly, overlapping transmission of dominant signals on both branches was measured.

Figure 9 shows the stimuli and the signal on CANH1/CANL1 – pin Tx2 of the setup is again driven by a rectangular signal. The same signal is, via an RC delay, connected to Tx1. Dominant is thus forced by both AMIS30660 transceivers during similar times but mutually shifted.

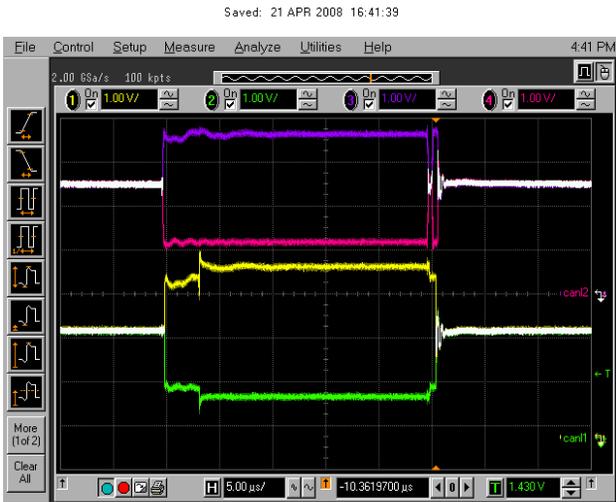


**Figure 9. Signal repetition in case different nodes coincidentally transmit on both branches. Blue – TxD signal of the node on bus1 (delayed with an RC constant); magenta – TxD signal of the node on bus 2; yellow and green – bus voltage on bus1.**

Dominant symbol on CANH1/CANL1 is a combination of both partial dominants – it starts by the dominant repeated from CANH2/CANL2 (which started earlier). When the dominant on CANH2/CANL2 ends, signal on CANH1/CANL1 is still dominant thanks to the standalone transmitter connected to it. When both signals overlap (which represents the majority of the time), the differential voltage is slightly higher because of two transmitters (AMIS30660 and AMIS42700) driving simultaneously the same bus.

The situation on CANH2/CANL2 starts similarly. However, when the dominant forced by the standalone transceiver ends (Tx2 goes high), the bus becomes recessive as the feedback from the other bus is blocked by the feedback suppression. Only when the feedback suppression is released, the still-lasting dominant on CANH1/CANL1 is re-transmitted to CANH2/CANL2 – see Figure 10.

Unlike the situation measured in the “Measurement of the Feedback Suppression” section, signals on both busses are not fully identical – the bus where the transmission ends earlier (CANH2/CANL2 in our case), shows a “dip” in bus voltage directly reflecting the masking effect of the feedback suppression block. This “dip” to recessive is roughly 400 ns long. It’s equal to the FS\_RELEASE signal time extension (see Figure 4) plus the time necessary to transmit the dominant again.



**Figure 10. Signal repetition in case different nodes coincidentally transmit on both branches. Yellow and green – bus voltage on bus1; blue and magenta – bus voltage on bus2. Overall view and zoom on the transition dominant→recessive.**



**Conclusions**

The application note demonstrated the necessity to include the feedback suppression feature into the repeater logic in order to avoid a “deadlock” situation. It has been demonstrated by measurements that the repeater logic with

feedback suppression can successfully pass signals between different bus branches and that the feedback suppression can be directly observed by applying coinciding time-shifted signals to both busses.

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative