AND8350

eFuse Reverse Voltage Protection

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APPLICATION NOTE

Introduction

ON Semiconductor's eFuses offer low cost, low impedance solutions for bus protection and offer much faster protection than many fuse solutions. They are an effective replacement for a polyfuse and TVS clamping diode.

One area in which they differ in performance is reverse polarity protection. While a TVS device and polyfuse will protect against reverse voltages, the nature of an integrated semiconductor device does not inherently allow for this type of protection.

This simple circuit allows the device to protect against reverse voltage situations by simply blocking the reverse voltage. This is equivalent of the action of a poly fuse only with less leakage. In comparison to a mechanical fuse, this is a far superior solution since the mechanical fuse will not reset and this circuit will automatically reset when the correct voltage is applied.

Circuit Description

In order to protect against reverse voltages an external switch is required. There are two basic topologies that can accomplish this function. A p-channel FET can be added in the high side or an n-channel FET can be added in the low side.

N-channel FETs are more cost effective and are normally preferred if it is acceptable to break the ground line. If the load has other connections to circuits that may be energized under a reverse polarity input condition, the ground should remain in tact.

If it is required to break the high side, a p-channel FET should be used. The two circuit configurations are shown in Figures 1 and 2.

The reverse protection circuit includes a zener protection diode to protect against excessive gate to source voltage that could damage the FET. For FETs with 12 V or lower gates, this is recommended. For FETs with 20 V gates, the zener and resistor can be eliminated and the gate tied directly to the other rail as long as the maximum system transient spec is 20 V or less.

A table of suggested FETs is included. The voltage and $R_{DS(on)}$ are only suggestions. The system voltage specifications should be taken into account to determine the maximum FET voltage and the losses due to the $R_{DS(on)}$ of the FET. Please see the ON Semiconductor website (www.onsemi.com) for more options for FET choices.

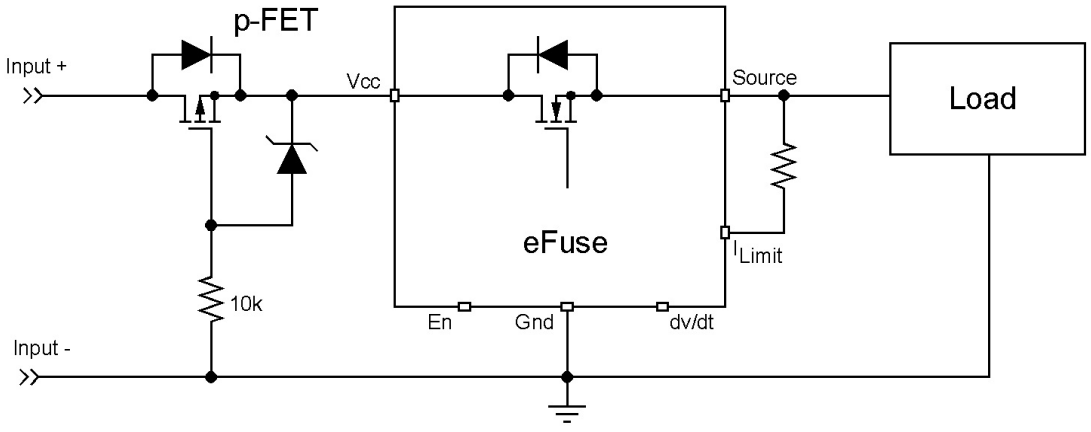

Figure 1. High-side Protection Circuit.

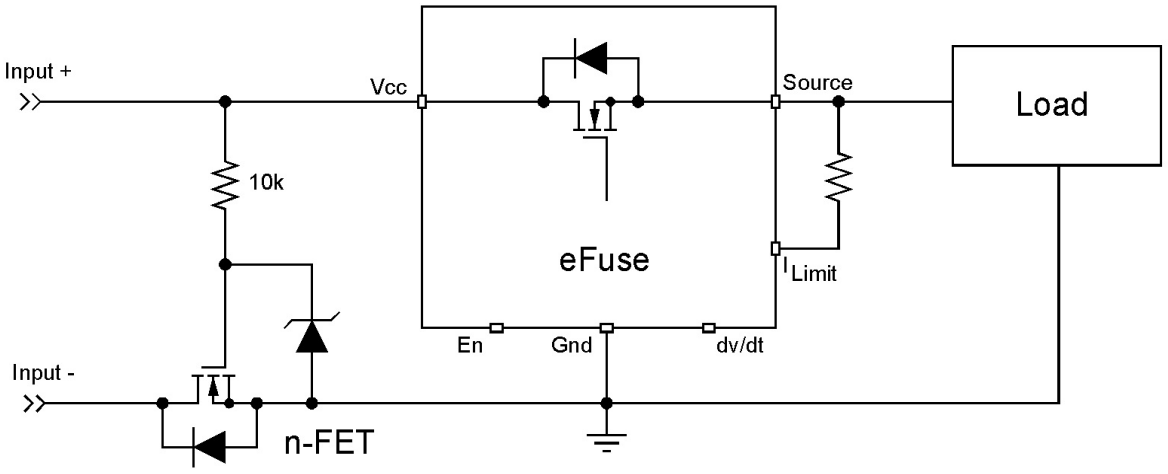

Figure 2. Low-side Protection Circuit.

Table 1. SUGGESTED FETS FOR REVERSE PROTECTION CIRCUITS

N-Channel FETs	Recommended Current	$R_{DS(on)}$	V_{DS}	V_{GS}	Package	Zener
NTD4808N-1G	4 - 12 A	8 mΩ	30 V	±20 V	DPAK	NZ9F20VT5G
NTD4815N-1G	2 – 8 A	13 mΩ	30 V	±20 V	DPAK	NZ9F20VT5G
NTHS4166NT1G	1.5 – 4 A	24 mΩ	30 V	±20 V	TSOP-6	NZ9F20VT5G
NTMS4807N	2 – 10 A	6.1 mΩ	30 V	±20 V	SOIC–8	NZ9F20VT5G
NTMS4816N	2 – 8 A	10 mΩ	30 V	±20 V	SOIC–8	NZ9F20VT5G
NTMS4872N	2 – 6 A	13.5 mΩ	30 V	±20 V	SOIC–8	NZ9F20VT5G
NTGS4141NT1G	1.5 – 4 A	25 mΩ	30 V	±20 V	1.65 x 3.05	NZ9F20VT5G
NTR4170NT1G	1 – 2 A	55 mΩ	30 V	±12 V	SOT-23	NZ9F12VT5G
P-Channel FETs	**Recommended Current**	$R_{DS(on)}$	V_{DS}	V_{GS}	**Package**	**Zener**
NTMS4177PR2G	1.5 – 5 A	19 mΩ	30 V	±20 V	SO-8	NZ9F20VT5G
NTMS4176PR2G	1 – 3 A	30 mΩ	30 V	±25 V	SO-8	NZ9F20VT5G
NTSG4111PT1G	1 – 2 A	60 mΩ	30 V	±20 V	TSOP-6	NZ9F20VT5G
NTLJS4149PTAG	1 – 2 A	62 mΩ	30 V	±12 V	2 x 2	NZ9F12VT5G

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