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AMIS−42700/AMIS−42770 − Redundant Bus Connection

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APPLICATION NOTE

Purpose and Scope

This application note discusses a redundant high−speed CAN bus system created with help of the AMIS−42700/42770 dual−CAN transceivers. In first approximation, the redundant connection could be simply achieved by interconnecting multiple transceivers in parallel with two twisted pairs and keeping both channels constantly enabled in all nodes. Only in case of one of the buses failing would individual control of the transceivers be necessary.

From practical experiments, both in a real application and on a simplified bench, it turns out that such a connection can lead to failures in communication due to logical loops occurring in the architecture. This document introduces the proposed application and analyzes the reason for its failure. It then briefly shows how the application should be modified in order to work correctly. The note concludes with a report of bench measurements illustrating the problem.

The statements and measurements presented in this application note are equally valid for AMIS−42700 and AMIS−42770 devices.

Introduction and Analysis

AMIS−42700/42770 is a dual high−speed CAN transceiver featuring two individual transceivers and a logic block ensuring the repeating function between both buses. The difference between both marketing codes is the allowed length of transmitter dominant symbol. While AMIS−42700 features a transmission time−out fostering communication speed above ca 48 kbps, AMIS−42770 allows bus speeds below 1 kbps. For the problem discussed in this document, both devices behave identically.

Figure 1 shows the considered application where two high−speed CAN nodes are connected with two differential lines. Both buses are supposed to transfer identical data under normal conditions (when both differential lines are correctly working). The CAN controllers inside the nodes are related to the dual transceivers with only two pins: Rx0 and Tx0 – similar to the case with single transceivers. At the same time, the internal logic of AMIS−42700/42770 ensures that data from Tx0 are passed to both buses and the Rx0 will reflect data received on both buses. The application diagram can be therefore evaluated as correct.

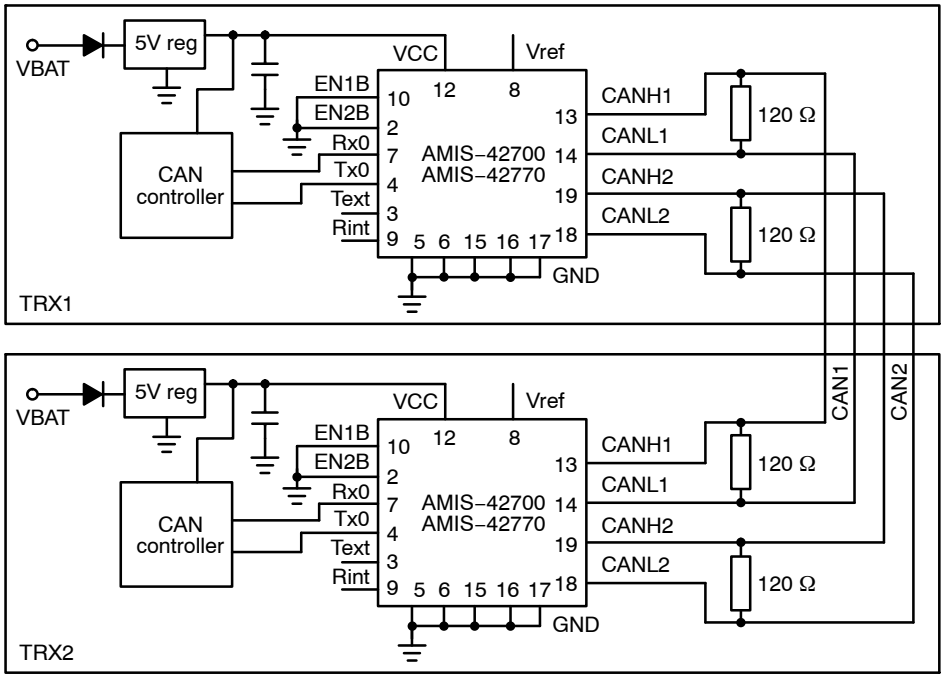

Figure 1. AMIS−42700/42770: Principle Schematic of the Targeted Application

The goal is to have two buses permanently enabled under normal conditions (all ENxB pins grounded) and controlled by single CAN controllers in the individual nodes. In case of one of the buses failing, it would be necessary to drive the enable signals individually – a measure not reflected in the picture.

However, practical experiments with a real network have shown that the communication in such a configuration can fail, as both buses will (sometimes) become dominant without external data being transmitted. This behavior is strongly setup−dependent as other topologies (different bus lengths, loads etc.) could lead to successful results.

After bench measurements, summarized in the next chapters, and after analyzing the logical structure of the application, the problem has been identified as depicted in Figure 2. The connection of multiple (i.e. two or more) dual CAN transceivers creates several logical loops. The internal loops inside individual transceivers, created by the repetition logic, are treated with the “feedback suppression” function, avoiding a dead−lock through the logic. One example of such a loop is shown in Figure 2 and marked with crosses indicating that this type of loop does not intervene.

However, other logical loops occur through different transceivers as also shown in Figure 2. There is no feature in the system blocking this type of loop, which is created by any couple of dual transceivers with both buses enabled. The exact effect depends on the dynamics of the full system – the delays, the delay symmetry etc. These aspects define whether the external loop does or does not intervene, in what direction and with what exact effect (ringing, oscillations, self−sustained dominant etc.)

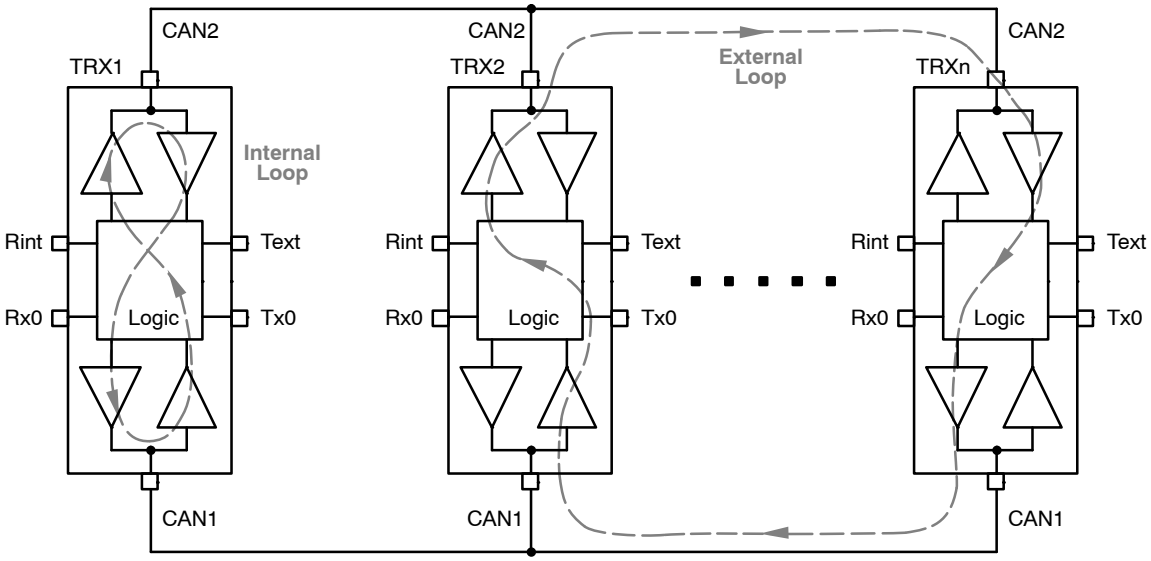

Figure 2. AMIS−42700/42770: Example of Logical Loops Existing in the Redundant CAN Bus Connection with Simplified Models of the AMIS−42700/42770 Devices.

The internal loop is created through the repetition logic and is “solved” by the feedback suppression feature of the dual transceivers. The external loop is not treated however, and can intervene into the signal propagation in an un−predictable way as it depends on many dynamic parameters of the application. The shown logical loops are not exhaustive – the internal loop exists in every dual transceiver and the external loop can be drawn through any two dual transceivers with both buses enabled.

In order to keep using the connection of two CAN buses through all nodes, the application must be extended as principally shown in Figure 3. The host MCU firmware must ensure that at most one dual transceiver is fully enabled at any time. It can be achieved by keeping only one of the buses enabled as long as it is working, toggling the enable based on a pre−defined schedule etc. The exact algorithm is out of this document’s scope.

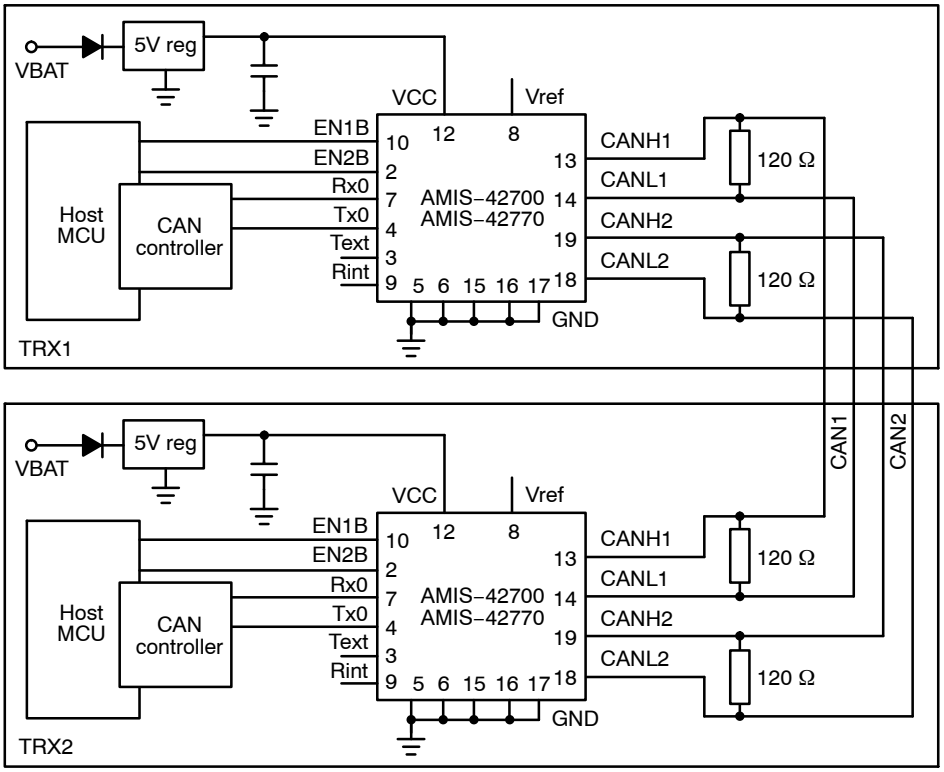

Figure 3. AMIS−42700/42770: Principle Schematic of the Solution

The host MCUs in individual nodes must ensure at any moment, that no two nodes have both transceivers enabled at the same time.

Bench Measurements

Setup Description

To emulate a redundant CAN bus, the PCB shown in was used in the following way:

- Both transceivers (TRX1 and TRX2, AGA mask set) were supplied with independent power supplies decoupled with 150 nF + 33 μF on the PCB. Unless otherwise specified, these supplies are set to 5 V.
- Whenever possible, the grounds of both transceivers were separated (which was not possible, e.g., when the same oscilloscope was used to probe simultaneously on both transceivers)
- CAN1 and CAN2 connectors, respectively, were connected with industrial−grade CAN cables 120 cm long. Only CANL and CANH nodes were inter−connected, the shield of the cables was left floating.
- All 4 terminal points of the two CAN buses were terminated with 120 Ω resistors.
- All 4 transceivers were enabled (all corresponding ENxB signals were set Low).
- The transmission was controlled by Tx0 signals on either TRX1 or TRX2 from a function generator.
- Whenever possible, the scope probes were connected on the side of TRX1 with their grounds connected to the ground of TRX1.

An example of the full setup connection is shown in Figure 5.

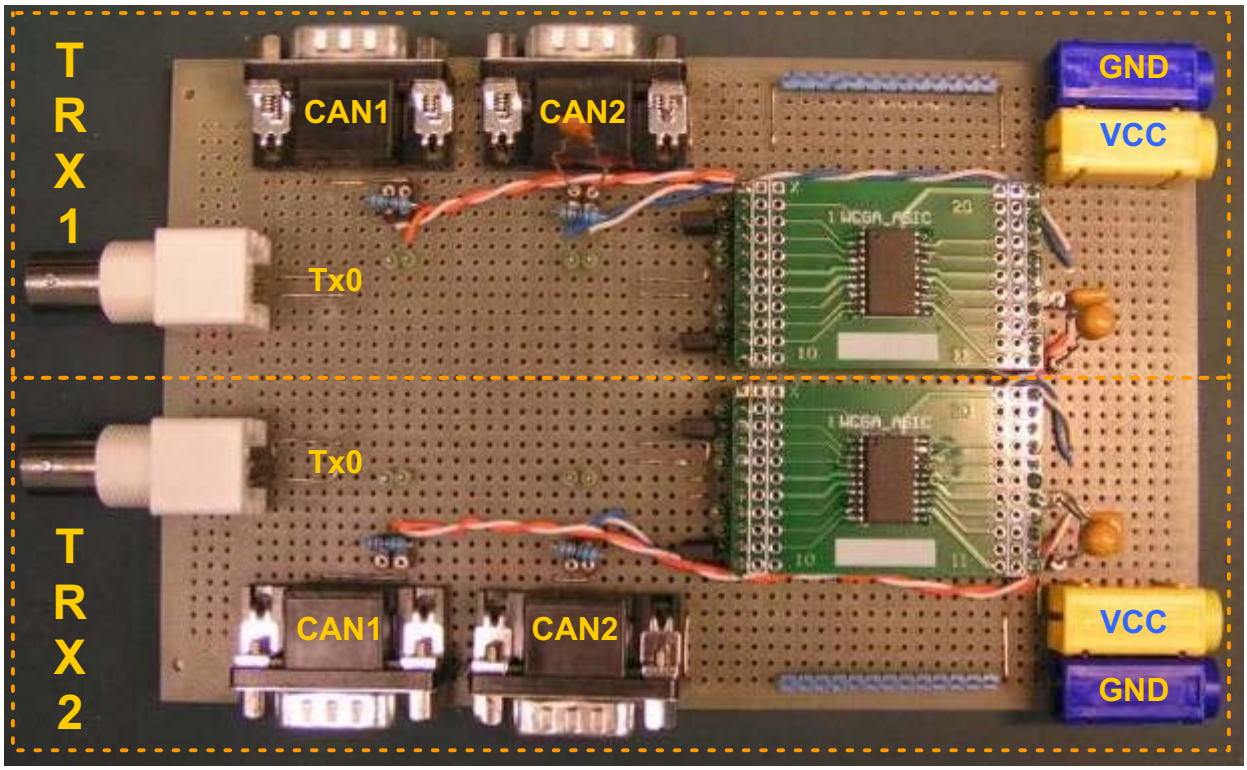

Figure 4. AMIS−42770: Photograph of the Setup without External Connections – the Board Contains Two AMIS−42770 CAN Repeaters with Separated VCC and GND Connections.

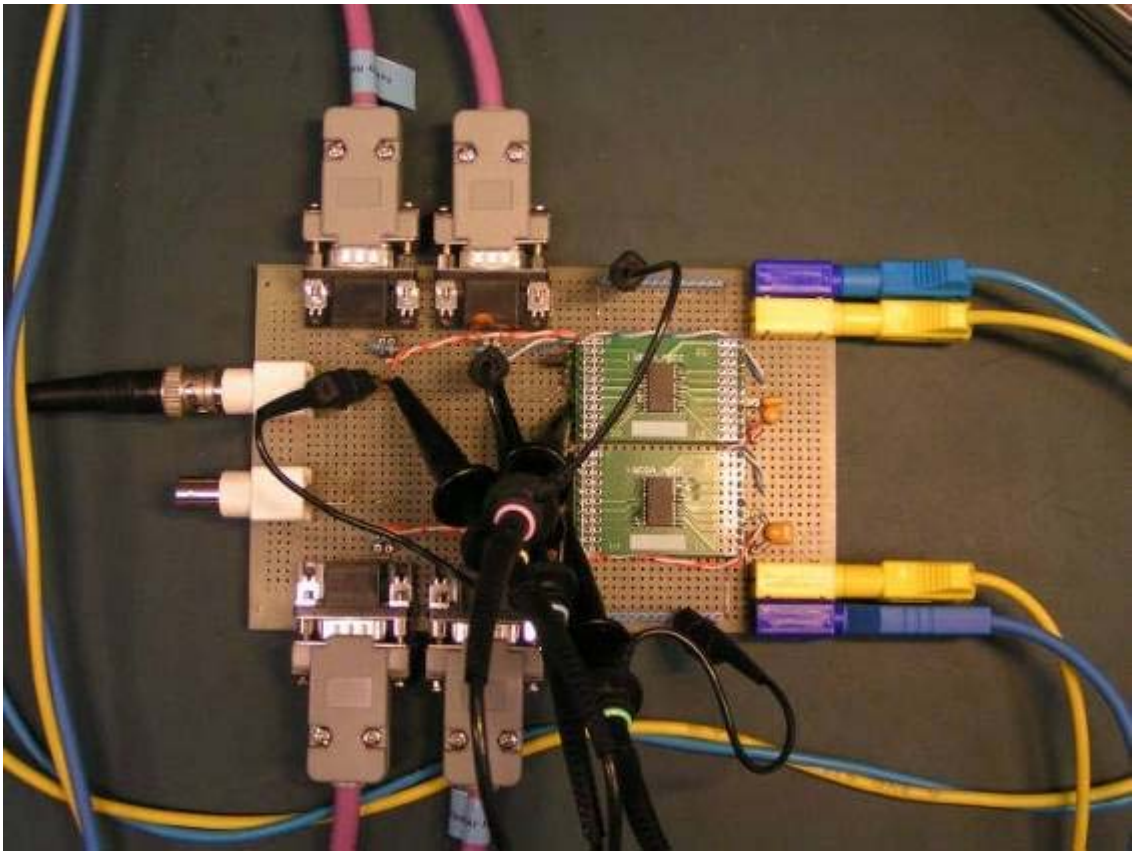

Figure 5. AMIS−42770: Photograph of the Setup with External Connections

The depicted situation corresponds to probing of: CANH1 and CANH2 of TRX1 (the respective CANLx signals being grounded) and Rx0 of both transceivers. Because of the Rx0 probing, the ground of both transceivers is connected through the oscilloscope in this case.

The following variations of the behavior have been observed:

- Identical buses vs. buses with forced delay asymmetry (achieved by capacitive loading of one of the buses)
- In function of which transceiver initiated the communi−cation (might be a result of not fully identical samples)
- Depending on how the scope probes were connected (causing, again, different capacitive loading)
- Depending on the exact VCC voltage supplied to the transceivers, which directly influences the delays inside the logical loops

Measurements of Bus Voltages

The below waveforms were probed on TRX1 − all four bus signals were captured by individual scope probes grounded to the ground of TRX1.

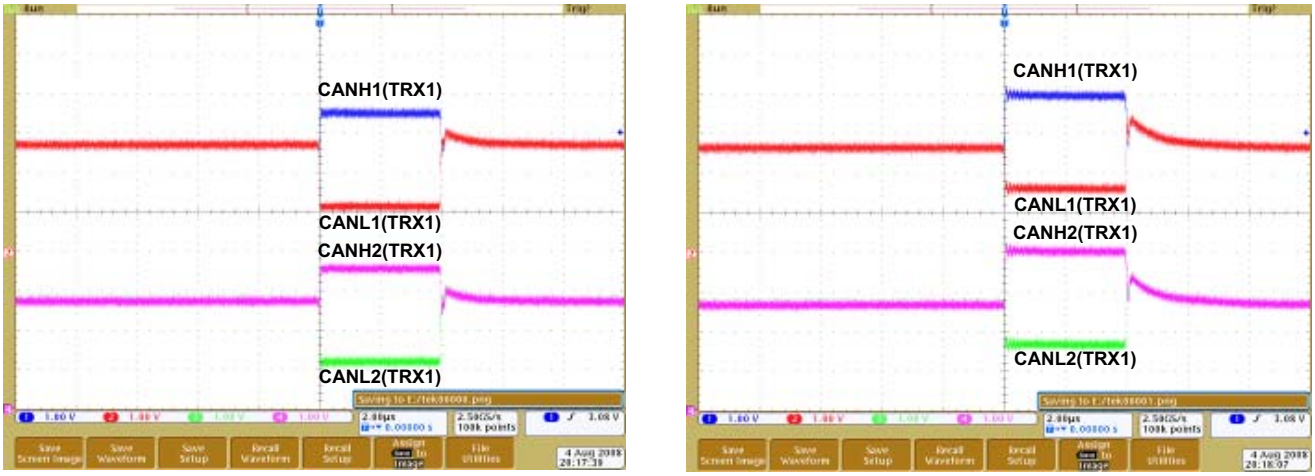

Figure 6. AMIS−42770: Bus Voltages in Case of Normal Termination
(120 Ω resistor on both extremities of both buses)

Low pulse of 4 μs is applied on Tx0 pin of transceiver 1 (left picture) or transceiver 2 (right picture). In both situations, virtually identical shapes are seen on both buses with differential levels corresponding to a single transmitter.

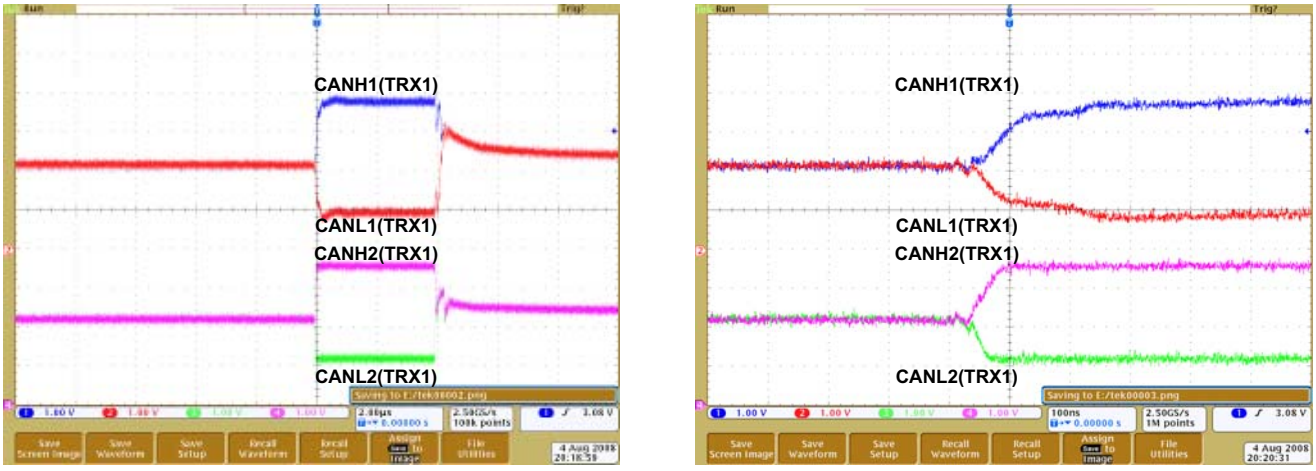

Figure 7. AMIS−42770: Bus Voltages in Case of Normal Termination
(120 Ω resistor on both extremities of both buses) + 1 nF capacitor connected between bus lines on CAN1 of TRX1.

Low pulse of 4 μs is applied on Tx0 pin of TRX 1. Right picture is a zoom−in of the left one. The dominant voltage on CAN1 is higher than the signal on CAN2, indicating that both transmitters on the bus are active. Because of the delay on CAN1 (caused by the capacitor), the second transceiver starts to “repeat” the signal on CAN2 before it receives the signal on CAN1 − it is seen as a step on the zoomed snapshot.

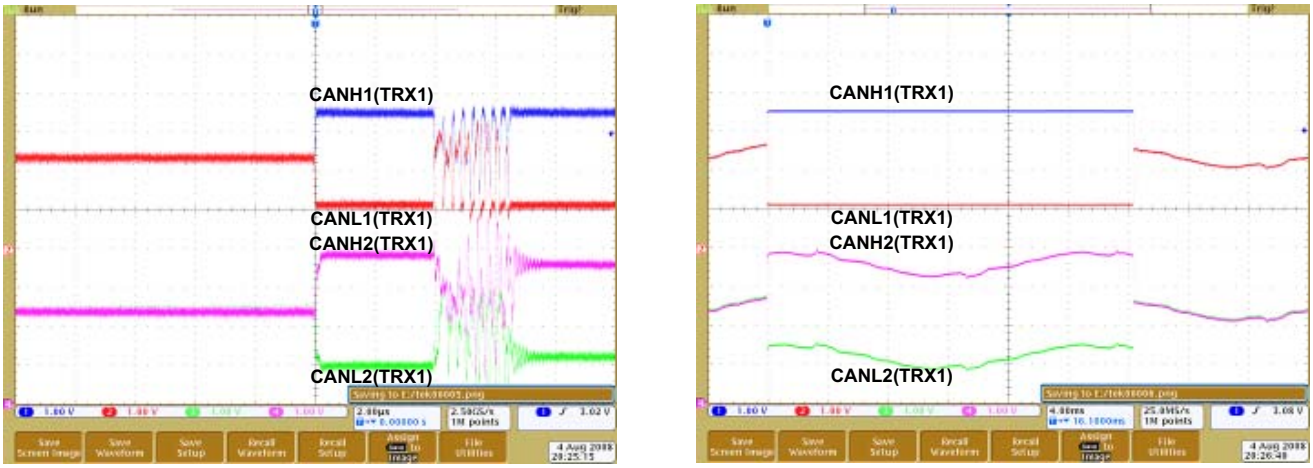

Figure 8. AMIS−42770: Bus Voltages in Case of Normal Termination
(120 Ω resistor on both extremities of both buses) + 1 nF capacitor connected between bus lines on CAN2 of TRX1.

Low pulse of 4 μs is applied on Tx0 pin of transceiver 1. Right picture is a zoom−out of the left one. This time, the dominant signal on bus 2 is higher because of the delay introduced by the additional capacitor. Additionally, this situation leads to a dead−lock – after the active transmission is supposed to finish (Tx0 gets High), a complex transient occurs stabilizing in a permanent dominant. Only after the built−in time−out (see the right zoom−out), the dominant is cut.

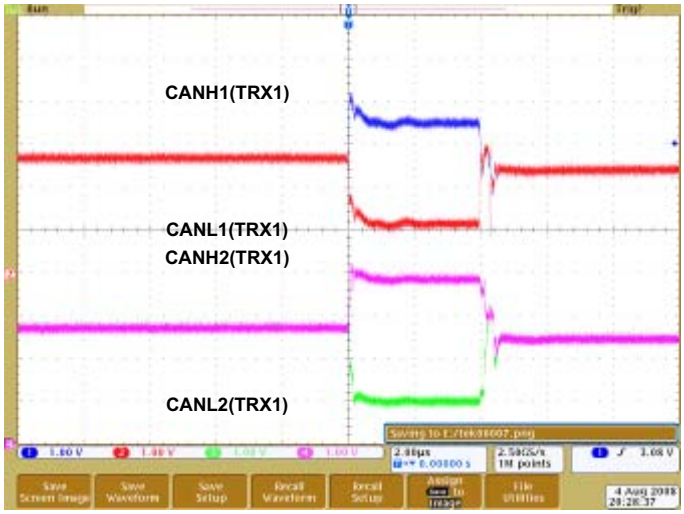

Figure 9. AMIS−42770: Bus Voltages in Case of Normal Termination
(120 Ω resistor on both extremities of both buses) + 1 nF capacitor connected between bus lines on CAN2 of TRX1.

Low pulse of 4 μs is applied on Tx0 pin of TRX2. Compared to Figure 8, the only difference is the signal Tx0. When Tx0 Low was applied to TRX1, a dead−lock resulted. When Tx0 Low is applied on TRX2 in the same bus configuration, only increased voltage on bus 2 occurs, but the transmission is ended as expected.

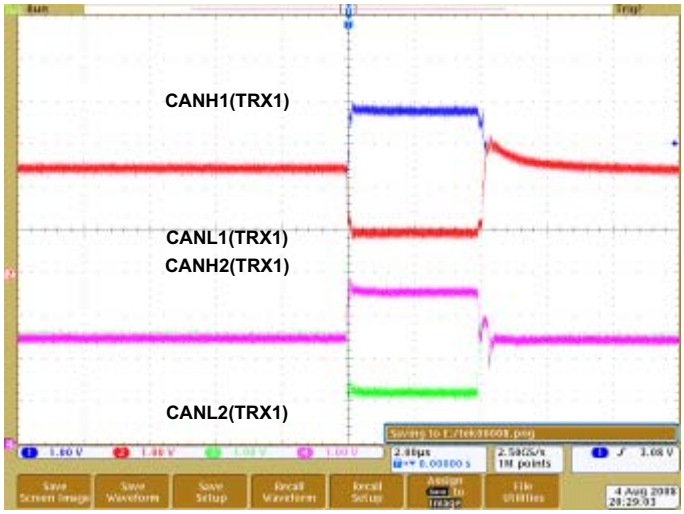

Figure 10. AMIS−42770: Bus Voltages in Case of Normal Termination
(120 Ω resistor on both extremities of both buses) + 1 nF capacitor connected between bus lines on CAN1 of TRX1.

Low pulse of 4 μs is applied on Tx0 pin of TRX2.

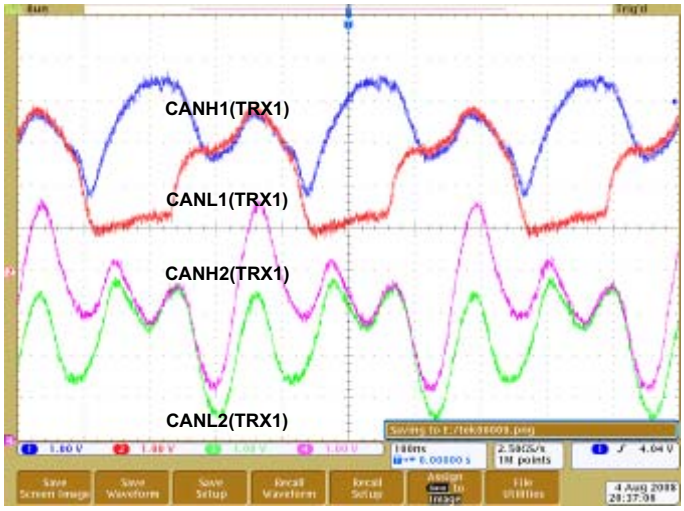

Figure 11. AMIS−42770. Bus Voltages in Case of Normal Termination
(120 Ω resistor on both extremities of both buses) + 1 nF capacitor connected between bus lines on CAN2 of TRX1.

VCC of TRX1 is 6 V, VCC of TRX2 is 5 V. Application of Tx0 Low results in self−sustained oscillations on the buses.

Measurement of Logical Signals

In the following pictures, the bus voltages were measured by single probes on the side of TRX1 – the probe was connected to the corresponding CANH signal, while CANL was grounded. The behavior of the bus was partly changed compared to the previous paragraphs (with two probes per channel).

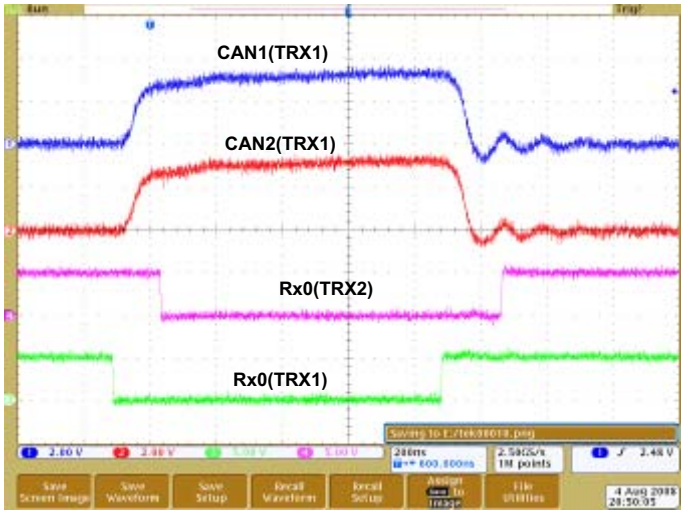

Figure 12. AMIS−42770: signals on buses and Rx0 pins in case of normal termination. Tx0 applied to TRX1.

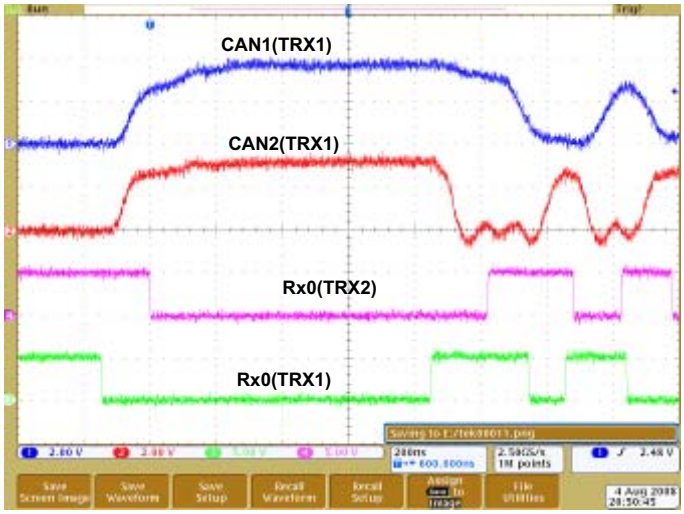

Figure 13. AMIS−42770: Signals on Buses and Rx0 Pins in Case of Normal Termination + 1 nF on bus 1 of TRX1. Tx0 applied to TRX1.

Together with a higher voltage on bus1, a dominant deadlock occurs – this is different from the case when the CAN signals are probed individually (see Figure 7).The different probe connection probably changes impedance/reflection properties of the bus.

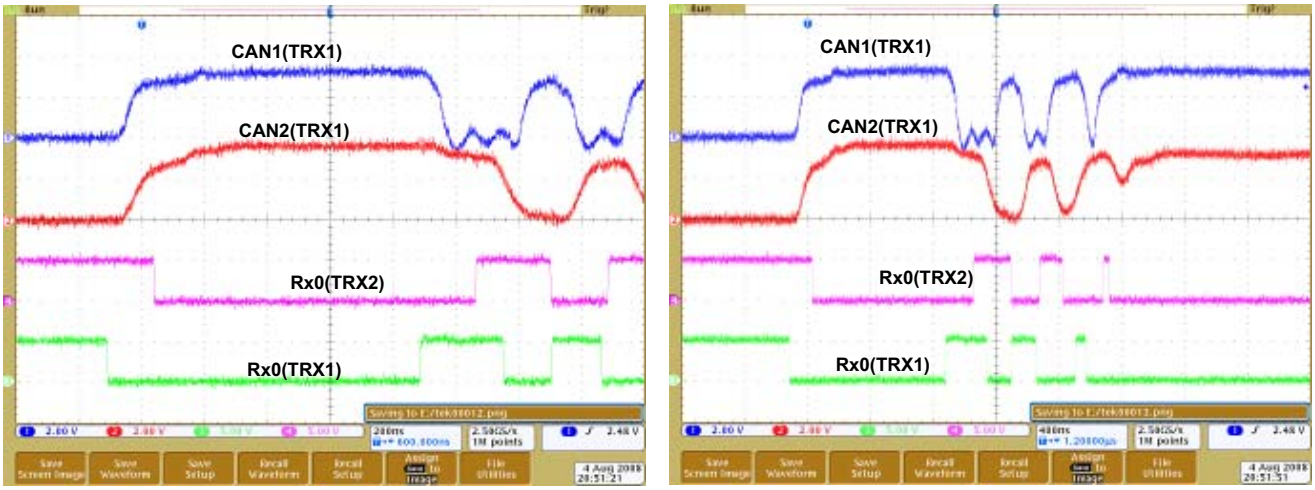

Figure 14. Figure 15 AMIS−42770: Signals on Buses and Rx0 Pins in Case of Normal Termination + 1 nF on bus2 of TRX1.

Tx0 applied to TRX1. Together with a higher voltage on bus2, a dominant deadlock occurs. The right picture is a zoom−out of the left one.

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