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PCB Design Guidelines for Dual Power Supply Voltage Translators

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Introduction

The design of the PCB is an important factor in maximizing the performance of a dual power supply voltage translator. The PCB design guidelines presented in this document offer the following benefits:

- Effective power supply decoupling is provided by placing ceramic capacitors next to the IC with minimum length connection traces
- Short PCB traces and ground planes reduce RF susceptibility and radiated emissions
- Robust ESD and EMI protection is achieved by placing Transient Voltage Suppressors (TVS) diodes next to the I/O connector

Decoupling Capacitors

Decoupling capacitors increase the noise immunity level of a translator by reducing the supply voltage droop. The capacitors filter and bypass noise signals on the power supply voltage lines to ground. These transients are due to the high peak, but short duration switching transients that can cause problems such as glitches on the output voltage signals.

Figure 1 provides an example of the recommended locations of the V_L and V_{CC} decoupling capacitors. Ceramic capacitors with a magnitude of 0.01 μF to 0.1 μF are a good choice because they are inexpensive, small and have excellent high frequency attenuation specifications. Ground and power planes are one option commonly used to provide short, low impedance trace connections.

Minimizing the Loop Area

Figure 2 shows that the translator's I/O_1 and I/O_2 traces form a loop with the ground trace. The loop area functions as an antenna that allows high frequency noise to enter (susceptibility) and leave (emissions) the PCB. Furthermore, RF susceptibility and emissions are proportional to the size of the loop and the frequency or bandwidth of the signals. The bandwidth of a digital signal is produced by the fast rise and fall times and can be approximated as $f_{BW} \cong 1 / (\pi t_{Rise}) \cong 1/ (\pi t_{Fall})$.

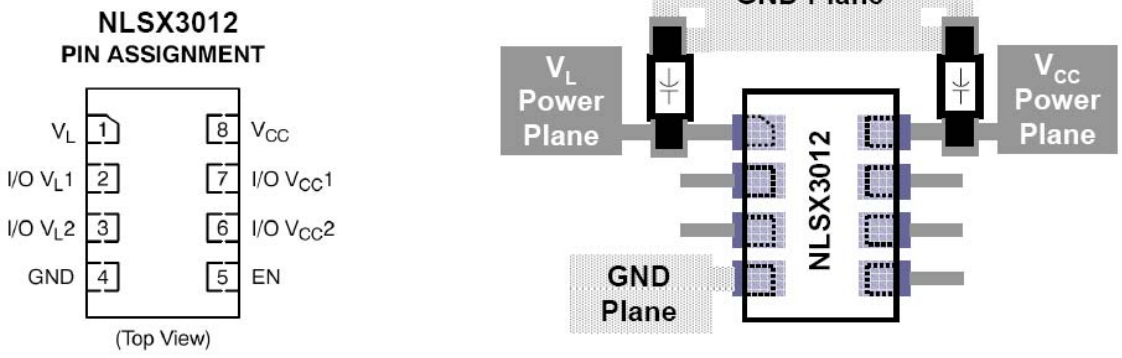

Figure 1. Effective Power Supply Decoupling is Provided by Locating the Capacitors as Close as Possible to the V_L and V_{CC} Power Pins while Providing a Low Impedance Ground Connection

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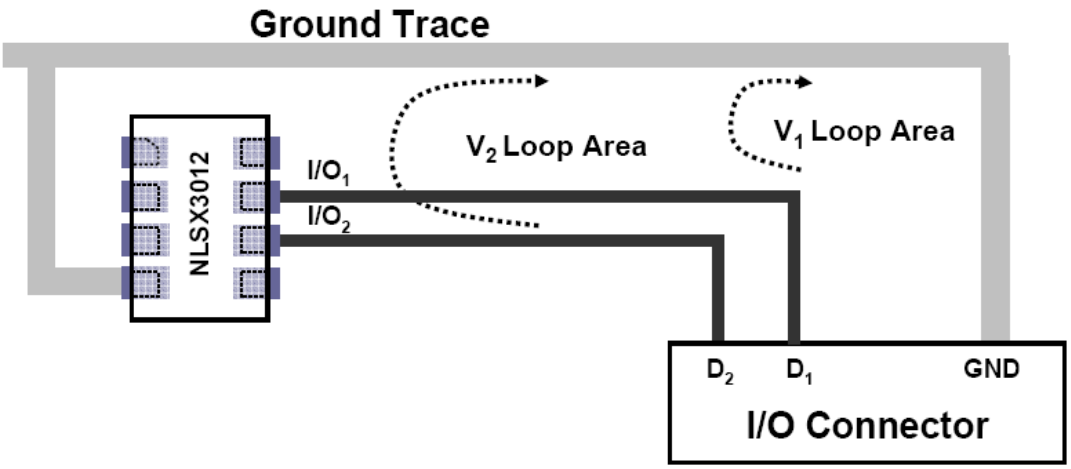


Figure 2. Long PCB Traces Increase RF Susceptibility and Emissions

RF susceptibility and radiated emissions can be reduced by minimizing the loop area formed by high speed data and ground lines. The first step is to shorten the translator's I/O−to−connector trace lengths. Next, incorporating a ground plane in the PCB design will reduce the loop area. Loop problems can also be minimized by slowing the edge rate of the signals; however, this approach typically is not an option because translator's have a relatively modest output current specification. Figure 3 shows a layout that can be used to reduce the translator's RF susceptibility and emissions.

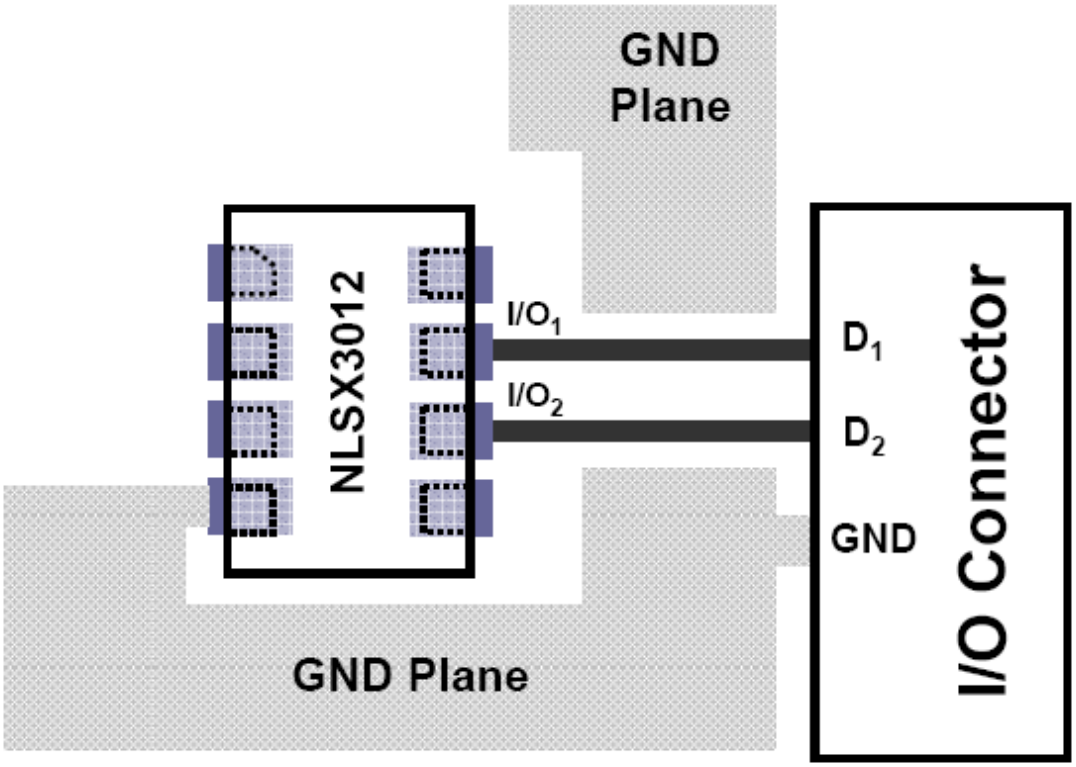


Figure 3. Short PCB Traces and Ground Planes Decrease RF Susceptibility and Emissions.

TVS Diode Protection Devices

Why are TVS devices required?

TVS devices typically are not required for internal PCB translations; however, they should be used for external module−to−module applications. Translators that are connected to I/O connectors are exposed to potential harmful ESD and EMI surge voltages. The power supply and data cables plugged into the I/O connector are common entry points for conducted and coupled transient surge voltages. Also, the parasitic cable capacitances and inductances provide a path for the power line surge voltages to be coupled into the data lines.

Voltage translators typically have a much higher ESD rating then a conventional logic IC; however, their immunity level for other surge pulses is not specified. In contrast, TVS diodes have a higher ESD rating and are specified for longer duration, higher energy surge pulses. The surge ability of a TVS device is proportional to die size and it is not practical to incorporate large protection devices inside an IC. The translator's small protection devices can reliably withstand only a limited number of low energy, short duration surge events such as ESD. In contrast, external TVS devices have a relatively large die size and are designed to withstand very high ESD levels and repetitive long duration transient surge voltages.

TVS PCB Layout Guidelines

Only a few design layout rules are needed to for TVS diodes to increase the translator's ability to suppress surge voltages. Figure 4 provides a graphical representation of the layout recommendations. The PCB design guidelines include:

- Locate the TVS devices close to the I/O connector
- Connect the surge protection circuits to chassis or power ground
- Select surface mount TVS devices

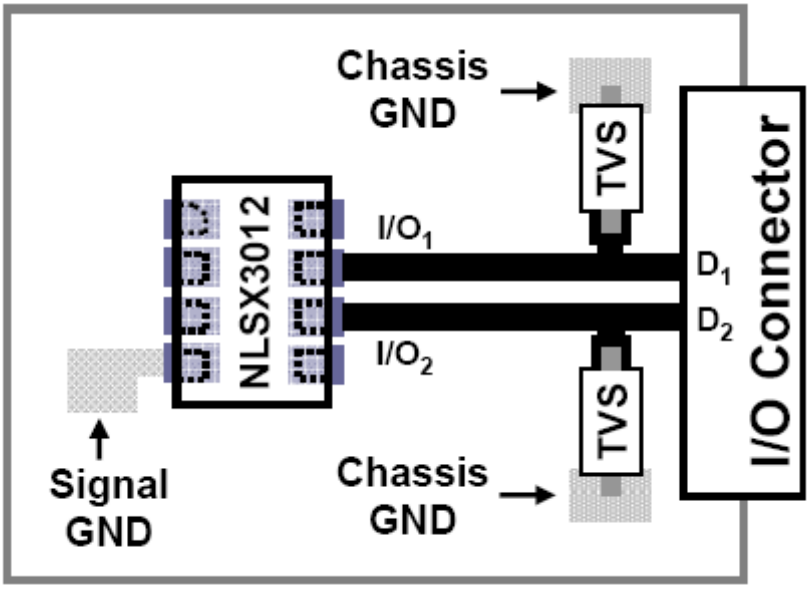


Figure 4. Locating the TVS Devices Close to the I/O Connector Ensures that a Surge Voltage Entering the PCB will be Clamped by the Protection Circuit Before the Pulse can be Coupled into Adjacent Traces

Location

TVS devices should be located close to the connector with short, low impedance connection traces. If the TVS diode and internal IC protection circuits have a similar turn−on voltage, the impedance of their PCB traces will be the key factor that determines where the surge energy will be dissipated. The close proximity of the TVS devices to the connector results in a trace impedance that is less than the translator−to−I/O connector trace. This ensures that the surge current will be dissipated by the external TVS devices rather than by the translator's internal protection circuit.

Ground Options

The TVS devices should shunt the surge voltage to chassis ground rather than signal ground. Shunting the surge voltage directly to the translator's signal ground can cause ground bounce. PCBs that have a single ground can minimize the TVS device's ground connection impedance by using "stub" traces that are relatively short and wide.

Package Selection

A small TVS device usually has better EMI characteristics than a device housed in a larger leaded package. The inductance of a TVS diode is proportional to its size; thus, a small SMT package reduces the magnitude of the voltage spike that is produced by the $V = L \Delta I/\Delta t$ inductance term. In addition, inductance degrades the high frequency attenuation characteristics of the TVS device.

TVS Diode Selection Guidelines

Diode arrays and Avalanche TVS diodes provide a simple, low cost solution to protect the translator's I/O pins. A TVS device can also be used on the power line associated with the I/O connector; however, the decoupling capacitor typically is adequate. Additional details on TVS diodes are provided in references [1] and [2].

Diode Array Protection Circuit

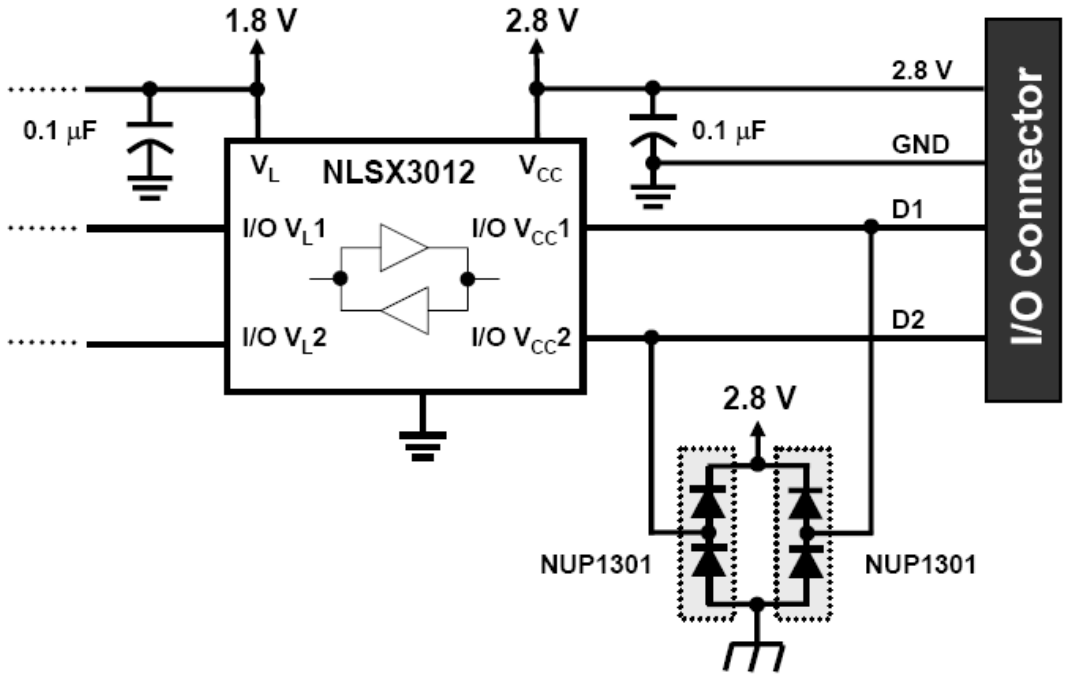


Figure 5. A Diode Array Protection Circuit Clamps a Negative and Positive Surge Pulse to −0.7 and V_{CC} + 0.7 V, Respectively

Figure 5 provides an example of a diode array protection circuit. Diodes arrays steer the surge current into the ground and power supply planes to dissipate the energy of the transient voltage pulse. The main advantage of the array is that the capacitance of a switching diode is low and will not distort a high speed digital signal. Diode arrays, such as the NUP1301, with a capacitance of less than 1 pF are readily available.

The main disadvantage of the diode array circuit is that a potential for back drive can exist. Backdrive occurs when a path exists for current to flow through the diode array via a data line. The data line connecting the two modules can unintentionally provide power to ICs that are connected to the power rail if the voltage at the I/O connector is greater than V_{CC}. This condition can cause power−up problems and anomalies such as the illumination of indicator lights on an unpowered PCB.

Avalanche TVS Diode Protection Circuits

Avalanche TVS diodes do not have a backdrive problem because they clamp the surge voltage to ground and do not have a path to V_{CC}. Figure 6 provides an example of a uni−directional avalanche circuit, while Figure 7 shows a bi−directional circuit. In most applications, either uni− or bi−directional TVS devices can be used to protect the translator. In general, a bi−directional Avalanche diode will have a lower capacitance than a uni−directional device, but a larger capacitance than a diode array.

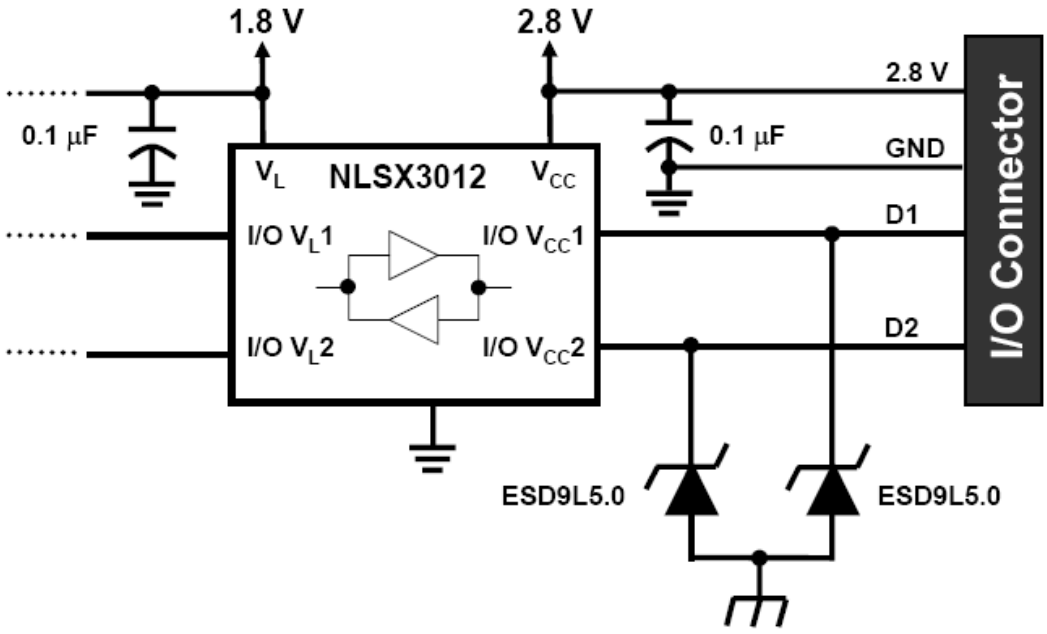


Figure 6. A Uni−Directional Avalanche TVS Protection Circuit Clamps a Negative and Positive Surge Voltage to −0.7 V and + V_{BR}, Respectively, where V_{BR} is Equal to the Diode's Breakdown Voltage

Designers often incorrectly believe that the negative symmetrical clamping voltage of a bi−directional TVS device violates the "Maximum Rating" Table of a translator. Most translators have a specified minimum value equal to −0.5 V. The datasheet rating is not violated because the voltage at the power and I/O pins is specified for DC steady−state value and is not applicable for a transient pulse with a duration that is usually less than 1 μs.

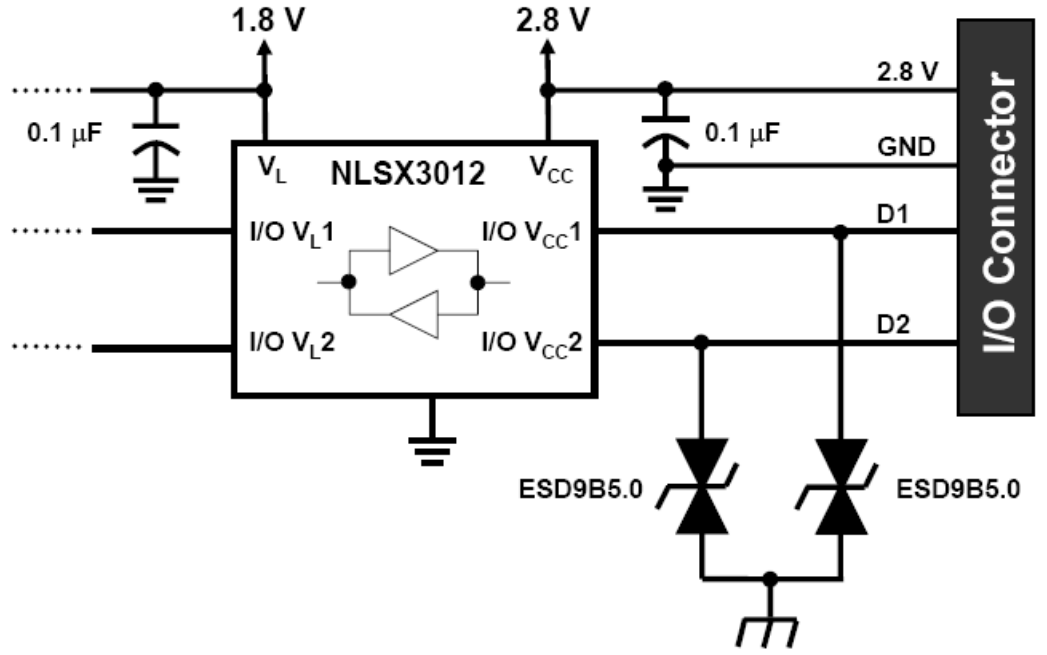


Figure 7. A Bi−Directional Avalanche TVS Protection Circuit Clamps a Negative and Positive Surge Voltage to −V_{BR} and +V_{BR}, Respectively

Summary

Figure 8 provides a graphical representation of the recommended PCB layout guidelines for a dual supply voltage translator. A multi−layer PCB provides a simple method to incorporate power and ground planes into the layout design. Typically, signal traces are located on the top and bottom layers, while the power and ground planes are located on separate internal layers.

The key PCB design guidelines include:

- Locate the decoupling capacitors as close as possible to the power pins
- Provide ground and power planes to minimize the PCB trace lengths
- Use short I/O traces and ground planes decrease RF susceptibility and radiated emissions
- Locate Avalanche TVS diodes next to the I/O connector to enhance the translator's ESD and EMI immunity

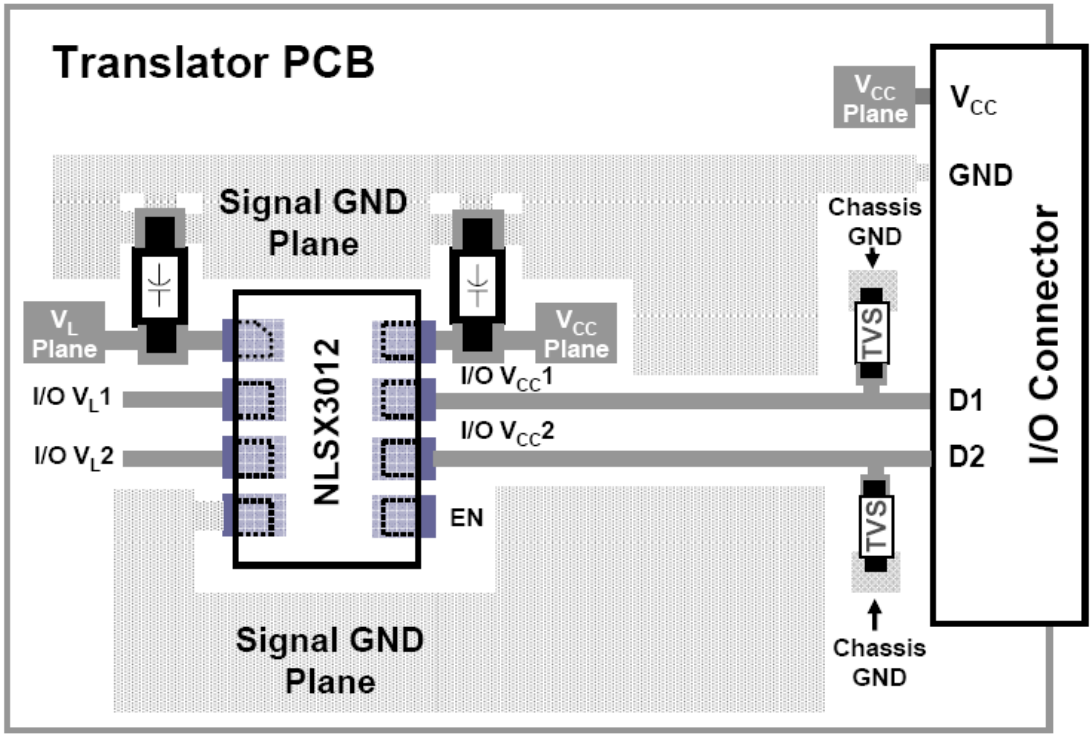
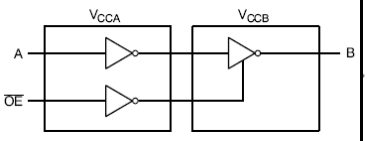
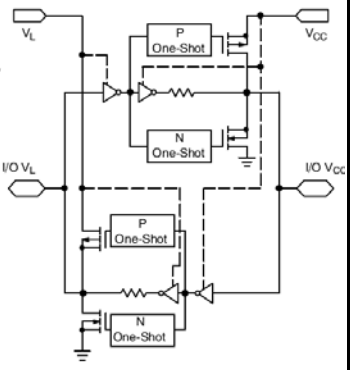
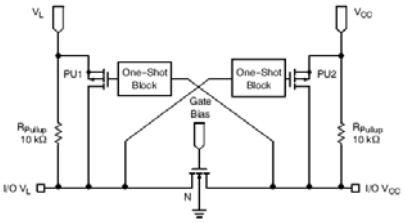


Figure 8. The PCB Layout of the I/O Traces, Decoupling Capacitors and TVS Diodes are Important Factors that Maximize the Performance of a Voltage Translator

Bibliography

1. Lepkowski, J., "AND8231 − Circuit Configuration Options for TVS Diodes", ON Semiconductor, 2005.
2. − , "AND8232 − PCB Design Guidelines that Maximize the Performance of TVS Diodes", ON Semiconductor, 2005.

Appendix I: ON Dual Power Supply Voltage Translators

	Uni−Directional Translator	Autosense Bi−Directional Translator (Push−Pull Output)	Autosense Bi−Directional Translator (Open Drain Output)
Block Diagram			
Attributes	• High Data Rate • Low Power Consumption	• High Data Rate • Low Power Consumption • Flexible PCB Design	• High Output Drive • Low Power Consumption • Flexible PCB Design
Trade−Offs	• Fixed Input & Output Pins	• Modest Output Current	• Modest Bandwidth
Applications	• SPI • GPIO	• SPI • GPIO	• I²C™, SMBus, PMBus • GPIO • SDIO Cards • 1−Wire Bus®
ON Semiconductor Products (I/O Channels / Package)	• NLSV1T34 (1−bit, ULLGA6) • NLSV1T240 / 244 (1−bit, UDFN6) • NLSV2T240 / 244 (2−bit, UDFN8) • NLSV4T240 / 244 (4−bit, UQFN12) • NLSV4T3234 (4−bit, CSP11) • NLSV8T240 / 244 (8−bit, UDFN20)	• NLSX3012 (2−bit, UDFN8) • NLSX3014 (4−bit, UQFN12) • NLSX3013 (8−bit, CSP20) • NLSX3018 (8−bit, UDFN20)	• NLSX3373 (2−bit, UDFN8) • NLSX3378 (4−bit, CSP12)

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