AND8211/D

Board Level Application Notes for DFN and QFN Packages

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APPLICATION NOTE

INTRODUCTION

Various ON Semiconductor components are packaged in an advanced Dual or Quad Flat−Pack No−Lead package (DFN/QFN). The DFN/QFN platform represents the latest in surface mount packaging technology. It is important to follow the suggested board mounting guidelines outlined in this document. These guidelines include printed circuit board mounting pads, solder mask and stencil pattern and assembly process parameters.

DFN/QFN Package Overview

The DFN/QFN platform offers a versatility which allows either a single or multiple semiconductor devices to be connected together within a leadless package. This packaging flexibility is illustrated in Figure 1 where three devices are packaged together with a custom pad configuration in a QFN.

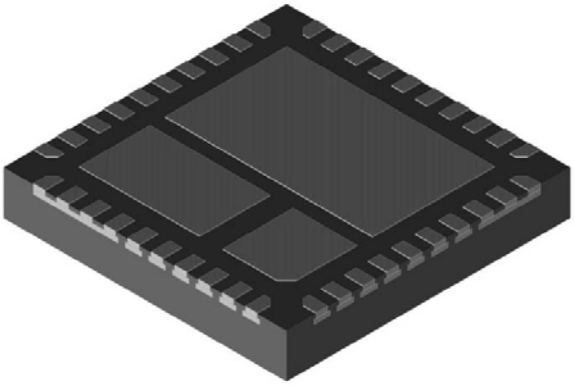

Figure 1. Underside of a Three−Chip 40 Pin QFN Package

Figure 2 illustrates a DFN semiconductor device package which allows for a single device.

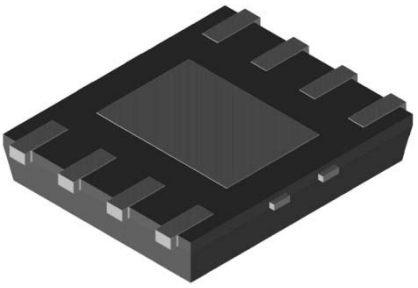

Figure 2. Underside of a Single−Chip 8 Pin DFN Package

Figure 3 illustrates how the package height is reduced to a minimum by having both the die and wirebond pads on the same plane. When mounted, the leads are directly attached to the board without a space−consuming standoff, which is inherent in a leaded package.

Figure 3 also illustrates how the ends of the leads are flush with the edge of the package. This configuration allows for maximizing the board space efficiency.

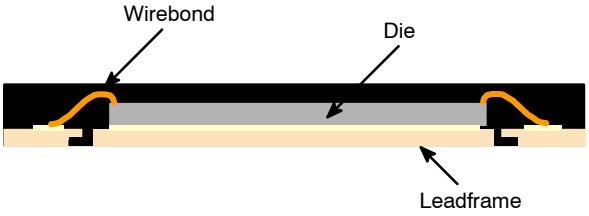

Figure 3. Cross−Section of a Single−Chip DFN Package

In addition to these features, the DFN/QFN package has excellent thermal dissipation and reduced electrical parasitics due to its efficient and compact design.

DFN/QFN Board Mounting Process

The DFN/QFN board mounting process can be optimized by first defining and controlling the following:

1. PCB solder pad design.
2. PCB solder mask design.
3. Solderable metallization on PCB pads.
4. Solder screening onto PCB pads.
5. Choice of solder paste.
6. Package placement.
7. Reflow of the solder paste.
8. Final inspection of the solder joints.

Recommendations for each of these items are included in this application note.

Printed Circuit Board Solder Pad Design Guidelines

Refer to the case outline (specification sheet) drawing for the specific DFN/QFN package to be mounted. Based on the case outline's "nominal" package footprint dimensions, the PCB mounting pads need to be larger than the nominal package footprint (See Figure 4).

Note: On the occasion that there is not enough board space to grow the PCB mounting pads per these guidelines, the recommendation would be to come as close to these guidelines as possible.

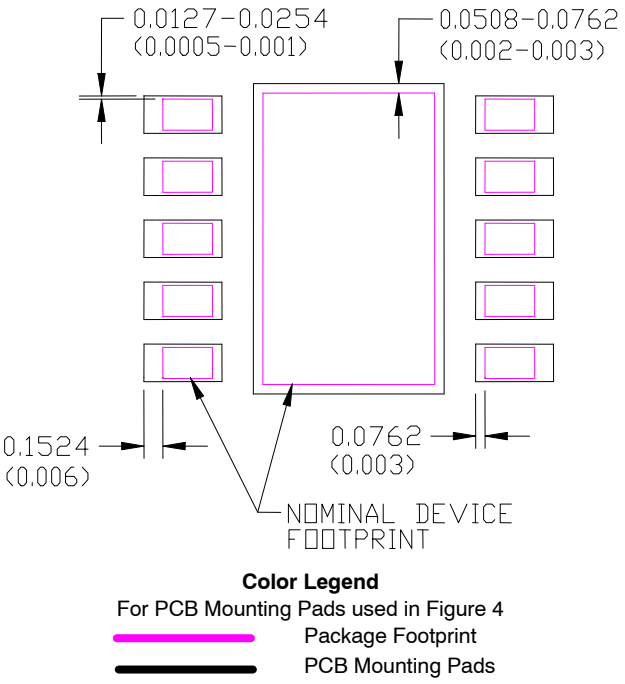

Figure 4. 10 Pin DFN Package Footprint Shown with PCB Mounting Pads

Printed Circuit Board Solder Mask Design Guidelines

SMD and NSMD Pad Configurations

Two types of PCB solder mask openings commonly used for surface mount leadless style packages are:

1. Non Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD)

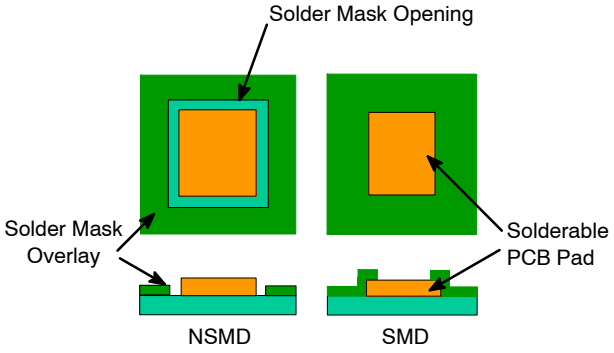

Figure 5. Comparison of NSMD vs. SMD Pads

As their titles describe, the NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in Figure 5. With the SMD Pads, the solder mask restricts the flow of solder paste on the top of the metallization which prevents the solder from flowing along the side of the metal pad. This is different from the NSMD configuration where the solder will flow around both the top and the sides of the metallization.

Typically, the NSMD pads are preferred over the SMD configuration since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of a tighter tolerance than the solder masking process. This also allows for visual inspection of solder fillet.

In addition, the SMD pads will inherently create a stress concentration point where the solder wets to the pad on top of the lead. This stress concentration point is reduced when the solder is allowed to flow down the sides of the leads in the NSMD configuration.

When dimensionally possible, the solder mask should be located within a range of 0.0762–0.1270 mm (0.003–0.005 in) away from the edge of the PCB mounting pad (See Figure 6). This spacing is used to compensate for the registration tolerances of the solder mask process, as well as to insure that the solder is not inhibited by the mask as it reflows along the sides of the metal pad.

The solder mask web (between openings) is the controlling factor in the pattern, and needs to be held to a minimum of 0.1016 mm (0.004 in). This minimum is the current PCB suppliers standard minimum web for manufacturability. Because of this web restriction, solder mask openings around PCB pads may need to be less than the recommended shown. Whenever possible, keeping to the range given will provide for the best results.

Due to ever shrinking packages with finer pitches between mounting pads, a solder mask web may not be possible. It may be necessary to have a single solder mask window opening around the package without solder mask web between mounting pads. When this occurs, care must be taken to control the solder during reflow. Where the web aided in controlling the solder, in its absence, solder may bridge between mounting pads causing shorts.

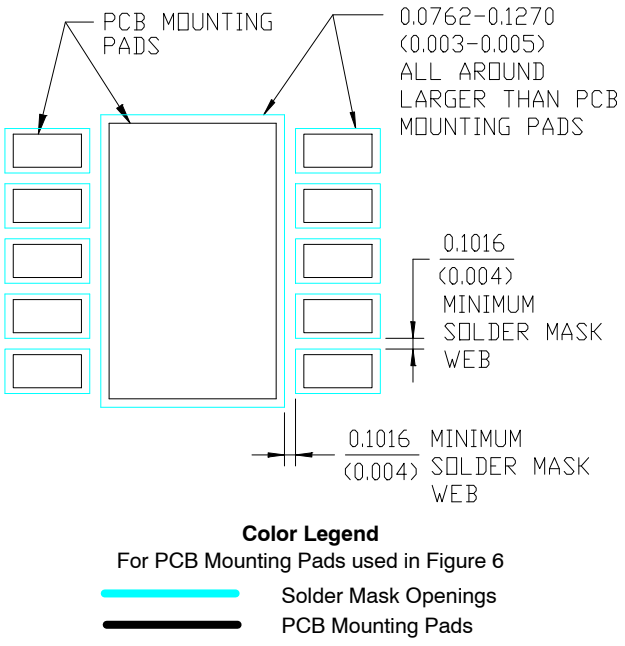

Figure 6. Typical DFN Package − PCB Mounting Pads Shown with Solder Mask Openings (NSMD)

PCB Solderable Metallization

There are currently three common solderable coatings which are used for PCB surface mount devices − OSP, ENiAu and HASL. In any case, it is imperative that the coating is uniform, conforming, and free of impurities to insure a consistant solderable system.

The first coating consists of an Organic Solderability Protectant (OSP) applied over the bare copper feature. OSP coating assists in reducing oxidation in order to preserve the copper metallization for soldering. It allows for multiple passes through reflow ovens without degradation of the solderability. The OSP coating is dissolved by the flux when the solder paste is applied to the metal features. Coating thickness recommended by OSP manufacturers is between 0.25 and 0.35 microns.

The second coating is plated electroless nickel/immersion gold over the copper pad. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. Even though the gold metallization is typically a self−limiting process, the thickness should be at least 0.05 microns thick, but not consist of more than 5% of the overall solder volume. Excessive gold in the solder joint can create gold embrittlement. This may affect the reliability of the joint.

The third PCB pad protective coating option is Hot Air Solder Level (HASL); SnPb. Since the HASL process is not capable of producing solder joints with consistent height, this pad finish is not recommended for DFN/QFN type packages. Inconsistent solder deposition results in dome-shaped pads of varying height. As the industry moves to finer and finer pitch, solder bridging between mounting pads becomes a common problem with this coating.

Solder Screening onto the PCB

Stencil screening the solder paste onto the PCB is commonly used in the industry. The recommended stencil thickness used is 0.075 mm to 0.127 mm (0.003 in to 0.005 in). The sidewalls of the stencil openings should be tapered approximately 5° along with an electro−polish finish to aid in the release of the paste when the stencil is removed from the PCB.

On a typical 0.5 mm pitch or larger DFN/QFN the stencil opening for the perimeter pattern should be the same size as the PCB mounting Pad. The center stencil opening for the center mounting pad(s) should allow for 70-80% coverage of the center mounting pad(s). (See Figure 7.) Dividing the larger die pads into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones.

On less than a 0.5 mm pitch DFN/QFN the stencil opening for the perimeter pattern should be the same size as the device nominal footprint. The center stencil opening for the center mounting pad(s) should allow for 60-70% coverage of the center mounting pad(s). (See Figure 8.) Dividing the larger die pads into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones.

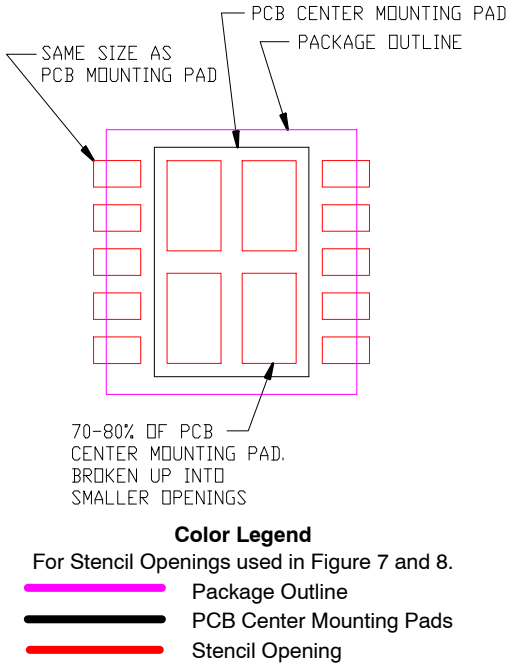

Figure 7. Typical for 0.5 mm Pitch or Greater DFN/QFN Package with Stencil Openings Shown Over PCB Mounting Pads

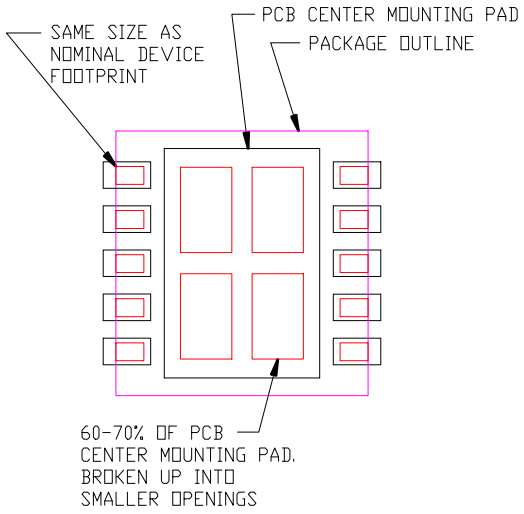

Figure 8. Typical Less than 0.5 mm Pitch DFN/QFN Package with Stencil Openings Shown Over PCB Mounting Pads

Solder Paste

Solder paste such as Cookson Electronics' WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water−soluble flux for cleaning. Cookson Electronics' PNC0106A can be used if a no−clean flux is preferred.

Package Placement onto the PCB

An automated pick and place procedure with magnification is recommended for component placement since the pads are on the underside of these packages. A duel image optical system enables alignment of the underside of the package to the PCB and should be used. Pick and place equipment with the standard tolerance of ±0.05 mm (0.002 in) or better is recommended. Once placed onto the board, the package self−aligns during the reflow process due to surface tension of the solder.

Solder Reflow

Once the component is placed on the PCB, a standard surface mount reflow process can be used to mount the part. Figures 9 and 10 are examples of typical reflow profiles for lead free and standard eutectic tin lead solder alloys, respectively.

The preferred profile is provided by the solder paste manufacturer and is dictated by variations in chemistry and viscosity of the flux matrix in the solder paste. These variations may require small adjustments to the profile for process optimization.

In general, the temperature of the part should increase by less than 2°C/sec during the initial stages of reflow. The soak zone occurs at approximately 150°C and should last for 60 to 180 seconds for lead free profiles (30−120 sec for eutectic tin lead profiles). Typically, extending the length of time in the soak zone reduces the risk of voiding within the solder. The temperature is then increased. Time above the liquidus of the solder is limited to 60 to 150 seconds for lead free profiles (30−100 sec for eutectic tin lead profiles) depending on the mass of the board. The peak temperature of the profile should be between 245°C and 260°C for lead free solder alloys (205°C and 225°C for eutectic tin lead solders).

If required, removal of the residual solder flux can be done using the recommended procedures set forth by the flux manufacturer.

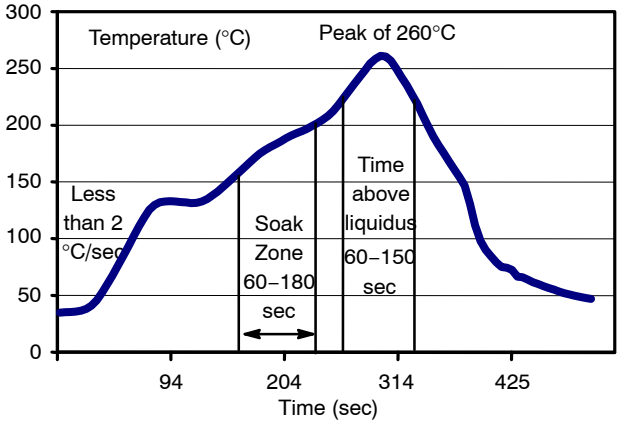

Figure 9. Typical Reflow Profile for Lead Free Solder

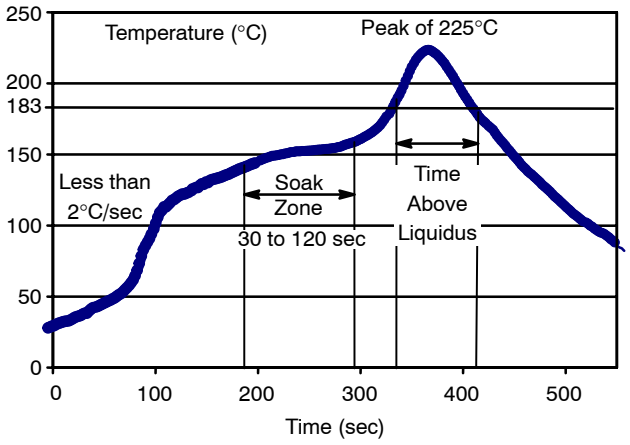

Figure 10. Typical Reflow Profile for Eutectic Tin / Lead Solder

Final Solder Inspection

Solder joint integrity is determined by using an X-ray inspection system. With this tool, defects such as shorts between pads, open contacts, and voids within the solder and extraneous solder can be identified. In addition, the mounted device should be rotated on its side to inspect the side of the solder joints for acceptable solder joint shape and stand-off height. The solder joints should have enough solder volume and stand−off height so that an “Hour Glass” shaped connection is not formed as shown in Figure 11. “Hour Glass” solder joints are a reliability concern and should be avoided.

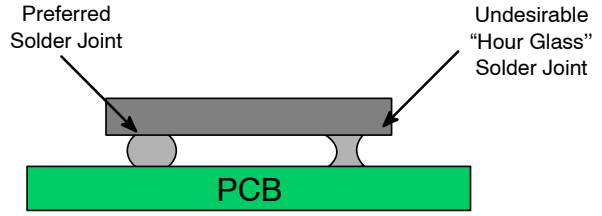

Figure 11. Illustration of Preferred and Undesirable Solder Joints

Rework Procedure

Since the DFN/QFN’s are leadless devices, the package must be removed from the PCB if there is an issue with the solder joints.

Standard SMT rework systems are recommended for this procedure since airflow and temperature gradients can be carefully controlled. It is also recommended that the PCB be placed in an oven at 125°C for 4 to 8 hours prior to package removal to remove excess moisture from the packages. In order to control the region which will be exposed to reflow temperatures, the PCB should be heated to 100°C by conduction through the backside of the board in the location of the device. Typically, heating nozzles are then used to increase the temperature locally and minimize any chance of overheating neighboring devices in close proximity.

Once the device’s solder joints are heated above their liquidus temperature, the package is quickly removed and the pads on the PCB are cleaned. The cleaning of the pads is typically performed with a blade−style conductive tool with a de−soldering braid. A no clean flux is used during this process in order to simplify the procedure.

Solder paste is then deposited or screened onto the site in preparation of mounting a new device. Due to the close proximity of the neighboring packages in most PCB configurations, a miniature stencil for the individual component is typically required. The same stencil design that was originally used to mount the package can be applied to this new stencil for redressing the pads.

Due to the small pad configurations of the DFN/QFN, and since the pads are on the underside of the package, a manual pick and place procedure with the aid of magnification is recommended. A system with the same capabilities as described in the **Package Placement** section should be used.

Remounting the component onto the PCB can be accomplished by either passing it through the original reflow profile, or by selectively heating the specific region on the PCB using the same process used to remove the defective package. The benefit of subjecting the entire PCB to a second reflow is that the new part will be mounted consistently using a previously defined profile. The disadvantage is that all of the other soldered device will be reflowed a second time. If subjecting all of the parts to a second reflow is either a concern or unacceptable for a specific application, then the localized reflow option is the recommended procedure.

Optimal board mounting results can be achieved by following these suggested guidelines.

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