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AND8206/D

NCP30x Series Reference Designs for Supply-Voltage Sequencing Control Applications

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APPLICATION NOTE

Supply−Voltage Sequencing Requirements

As we know, highly integrated system chips that combine multiple digital and analog functions into a single package often require multiple power supplies. Usually the microprocessor's input/output (I/O) and core voltages are two separate and independent power requirements. A typical contemporary microprocessor's I/O section usually operates at 3.3 V or 2.5 V, but the core sections work at 1.8 V, 1.5 V, 1.3 V or lower. Improper supply sequencing can result in device latch−up, incorrect device initiation, or degradation of long−term reliability. And considering of different outputs sequence results from different power solutions, it's important to add a part of circuit to control the supply−voltage up and down sequencing to guarantee the microprocessor operating normally. For example, DSPs and some other multi−voltage needed processors require their I/O voltage to be present before applying the core voltage. On the contrary, some systems based on FPGAs needs the core voltage to be fully created before the I/O supplying. So it could be happen that different processors, FPGAs and ASICs on the same board may have different outputs sequencing requirements. For robust system operation it can prove important to add a circuit block to control the supply−voltage up and down sequencing to guarantee the microprocessor operating normally.

Depending on the different power supply solutions we can use particular method to realize the sequencing control. We will describe the implementations of using discrete components and devices of NCP30x families to control the sequencing.

Use of Discrete Components

A simply approach for sequencing the supply voltage of two power requirements is to add a delay between them. The way is to monitor the primary supply and allow the second supply coming up with a small delay after ensuring that primary supply reaches a certain level. Figure 1 illustrates this method for a system in which the power voltage supply is provided by a remote power converter module without individual output on/off control. One comparator, NCS2200 properly is used to drive the switch short or open. The reference voltage on the negative input of the comparator sets the level to be reached by the V_{cc1} before V_{cc2} turning on.

An RC combination on the other input adds a delay to the trigger. A P−channel MOSFET on the V_{cc2} operating as a high−side switch model controlled by the comparator guarantees no power flows to the output before Vcc1 rising above the preset V_{ref}. A small N−channel MOSFET controls the P−channel MOSFET switch.

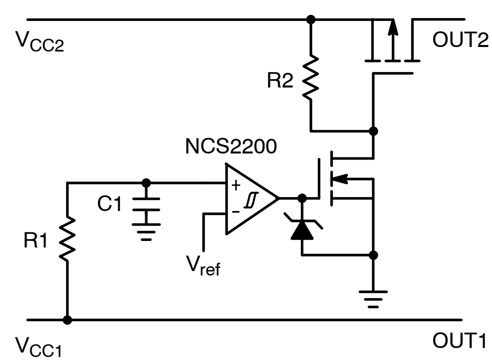

Figure 1. RC Approach with Comparator and MOSFET

This approach can guarantee that the V_{cc2} will not be present to out2 before V_{cc1} reaching the preset V_{ref}. The timing delay after V_{cc1} rises above the V_{ref} depends upon V_{cc1}. It's not a fixed and reliable constant and will be affected by the slew rate of V_{cc1} input. For example, assuming the V_{cc1} is applied below the V_{ref} through the duration of C1 charging. At this time if V_{cc1} rises above the V_{ref}, the delay time will be shorter and hence it may cause the error. Or, when the V_{cc1} goes down below the V_{ref}, because of the RC combination the output of the comparator will turn over after a little delay due to the C1 discharge. All these above cannot be accepted by the system designers. Another drawback is that at least six components are needed to realize this approach.

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Use of NCP302 Supervisors

The circuit in the Figure 1 is not very difficult to upgrade through the use of the NCP302 series of voltage supervisory products, the result is fewer components, higher timing precision and more flexible timing control. Figure 2 illustrates the arrangement for using of the NCP302 and P−channel MOSFET−NTR2101.

The NCP302 includes voltage reference, comparator, fixed reset threshold and programmable delay time. The delay time can be programmable by connecting an external capacitor C1. We can save some components through use of NCP302 family's product. C1 is connected between the C_D pin and GND. The delay time after V_{cc1} rises above the preset threshold to the reset output turning over is programmable by adjusting the value of the capacitor C1.

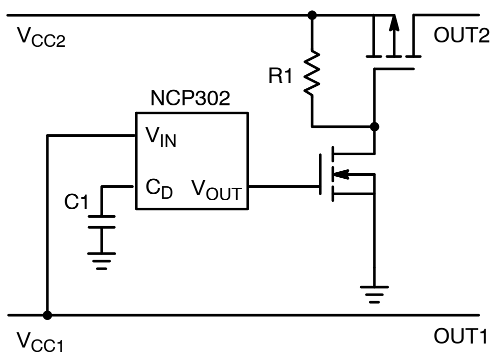

Figure 2. NCP302 Approach with NTR2101 MOSFET

From the simple internal circuit and the timing sequencing diagram of NCP302 family we can have a better understanding of the behavior.

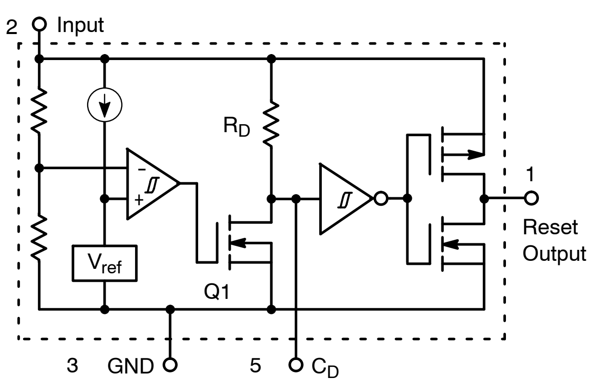

Figure 3. Internal Logical Diagram of NCP302 Family

The internal reference circuit provides a fixed and accurate V_{ref} voltage. This reference voltage, connected to the positive input of the comparator, sets the level of the comparator's detection threshold. This level, by the mean of the bridge resistor ratio, gives the input voltage detection threshold V_{DET+}. When V_{IN} rises to its nominal level and become greater than V_{DET+}, the schematic of voltage will turn off the Q1−N−channel MOSFET and allow the pullup resistor R_D to charge the external capacitor C1. This gives the delay time t_{D2} before releasing the reset signal. When the voltage at Pin 5 exceeds the inverter/buffer threshold, typically 0.675 V_{IN}, the reset output will revert back to the high state. The voltage detector and inverter/buffer have built−in hysteresis to prevent erratic reset operation. If there is a power loss and V_{IN} begins to decay, it will fall below the lower detector threshold ($V_{DET−}$) and the external time delay capacitor C_D will be immediately discharged by an internal N−channel MOSFET (Q1) that connects to Pin 5. This sequence of events causes the Reset output to enter the low state. The Timing Diagram is shown below.

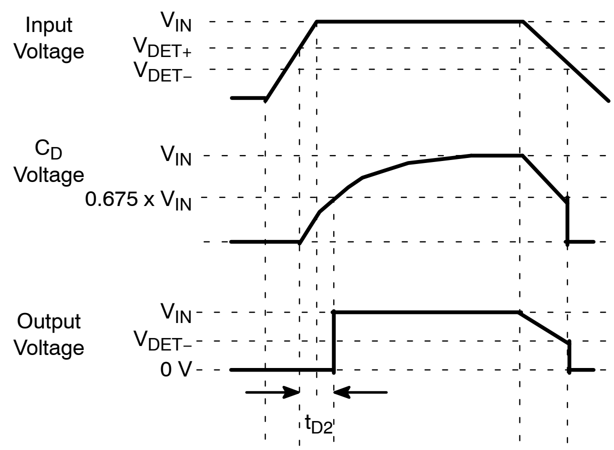

Figure 4. Timing Diagram of NCP302

As mentioned before, delay time t_{D2} at rise of V_{IN} can be established and programmable by the capacitor connected to the C_D Pin. The equation below shows the relation between the capacity of the external capacitor and delay time.

$t_{D2} = 1.124 \times C1 \times R_D$ ($T_A = 25°C$)

C1: External Delay Capacitor

R_D: Internal Resistor

Normally the value of internal resistor R_D is 1.0 MΩ. So we can simplify the equation as:

$$t_{D2} = 1.124 \times 1.0\ M\Omega \times C1\ (T_A = 25°C) \qquad \text{(eq. 1)}$$

For example, if a 100 nF capacitor is connected to the C_D pin, based on the above equation we can see the nominal delay time t_{D2} is approximately 112 ms. The designer could obtain the required timeout delay by using different capacitor values.

From the internal circuit analysis, we could find another benefit of NCP302. We previously described a way to control power supply setting up. On the other hand, the NCP30x can be used as power supply turn off control: once the output of NCP30x has been released, allowing OUT2 voltage to turn on, for any reason (power down sequence, low power requirements…) the user software may want to turn it off again. It can be easily achieved by shorting the C_D pin to ground by the mean of an external NMOS or an open drain logic gate (according to Figure 5). Grounding the C_D pin, will force the NCP30x output to low level and turn the PMOS off, isolating OUT2 from V_{cc2}. Releasing the short to ground will turn on again the PMOS, allowing OUT2 to be connected again to V_{cc2} (of course after the t_{D2} delay time).

This feature is also useful for the power and reset design to guarantee the entire system operating normally and stably.

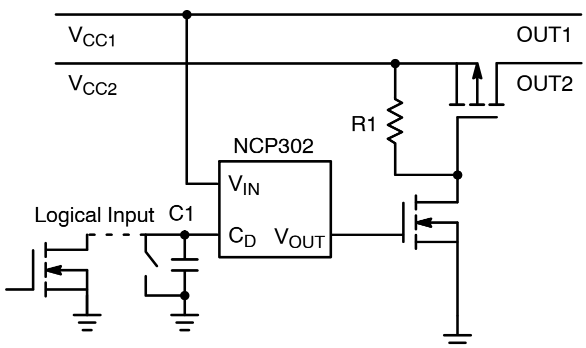

Figure 5. NCP302 Approach with NTR2101 MOSFET

Furthermore, we can choose a co−packaged device such as NTJD1155L integrating a P and N−Channel together. This device is particularly suited to be driven from low voltages. The internal N−Channel MOSFET, with an external resistor (R1) functions as a level−shifter to drive the main P−MOSFET. The NTJD1155L operates on supply lines from 1.8 V to 8.0 V and can drive loads up to 1.3 A. The modified schematic looks like below.

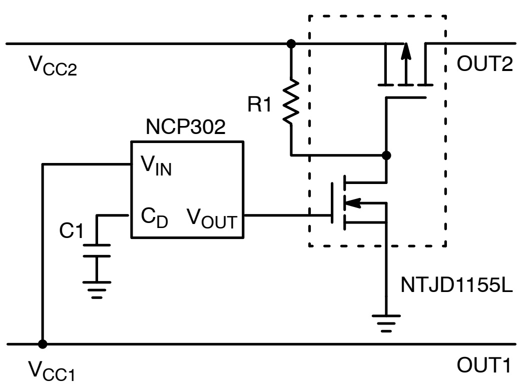

Figure 6. Voltage Sequencing by NCP302 and NTJD1155L

For example a typical microprocessor V_{cc1} powers the I/O section operating at 3.3 V and the V_{cc2} supports the core section operating at 1.8 V. Commonly the I/O supply should be present before the core. We can use the NCP302LSN29T1 and NTJD1155L with a pullup resistor of 10 KΩ and delay produced capacitor of 100 nF to design an application circuit for power−up sequencing control. The NCP302LSN29T1 is a voltage detector circuit with programmable timeout delay. The suffix “L” after the main part number means the output of this circuit is Active−Low. And the suffix ”29” means the detect voltage is 2.9 V. As mentioned before, the capacitor of 100 nF connected between the C_D pin of the NCP302 and GND can produce about 110 ms delay after the input voltage increasing above the threshold and before the output deasserted. The particular schematic is similar to the Figure 6.

Usually, the OUT2 output is connected to the load and to decoupling capacitors. At turn on, the inrush current required to charge the decoupling capacitors can be very high. The Figure 7 gives a way to control this inrush current.

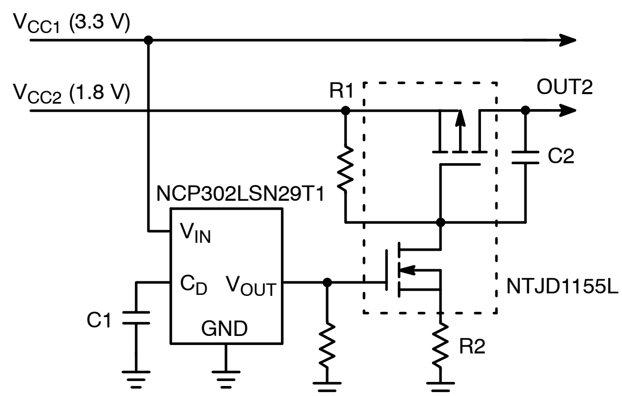

Figure 7. Dual Voltage−Supply Sequencing

The simple RC network, R2 and C2, is used to substantially slow the slew rate of P−channel MOSFET gate, thereby get the control to the inrush current through the P−channel MOSFET turn on duration. The typical value of the C1 is less than 1000 pF. And the ratio of the R1 and R2 should be at least 10 to ensure the adequate N−channel MOSFET turn−on.

To examine actual circuit operation we can input a square−wave operating at 2.0 Hz between 0 V to 3.3 V to V_{CC1} and a DC voltage at 1.8 V to V_{CC2} for testing the circuit above. If the C_D pin is unconnected, there is only about 120 μs propagation delay between the V_{CC1} and Out2. The waveform looks like below.

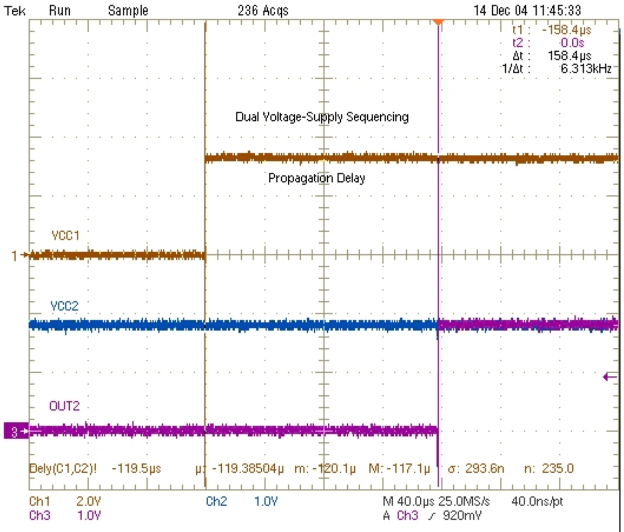

Figure 8. Propagation Delay of Dual Voltage

If the C_D pin is connected to the GND by a capacitor of 100 nF. The results looks similar to the above, but obviously the delay between the V_{CC1} and Out1 is different. The delay is increased to approximately 120 ms. This result is consistent with the value calculated by using the Equation 1. Since the delay time is programmable by the capacitor connected to the C_D pin, the user can adjust the basic schematic which is needed for their specific system requirements.

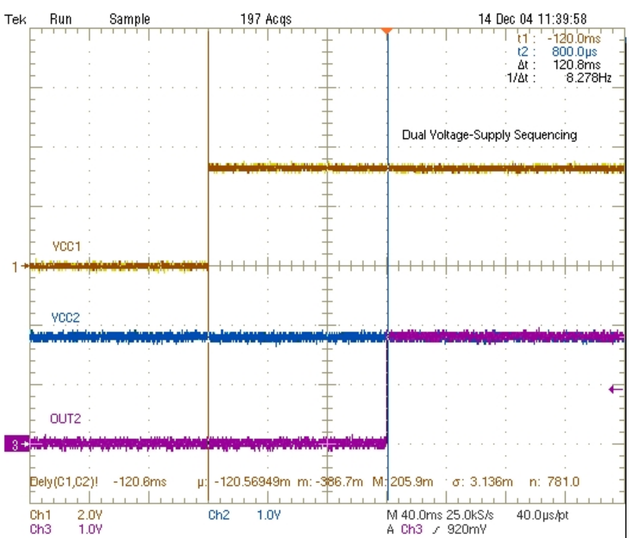

Figure 9. Programmable Timeout between Dual Voltages

The waveform below illustrates the C_D pin operation as the delay is producing. The purple wave in the below picture is the voltage rising of the C_D pin. When the voltage at this pin reaches around 0.675 x V_{CC1}, the output will be deasserted.

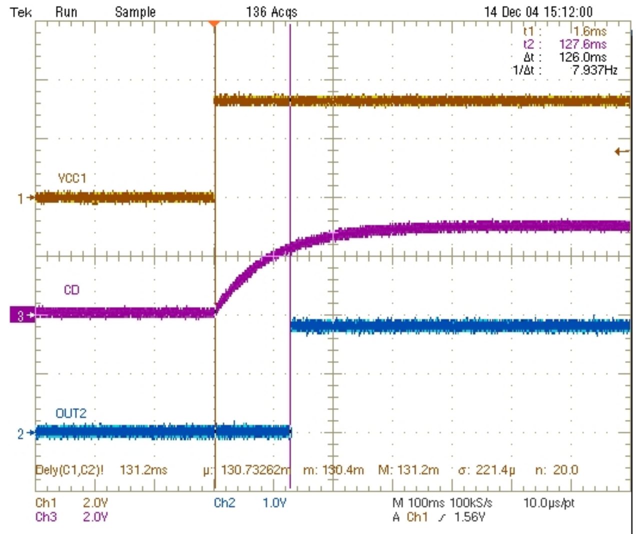

Figure 10. Waveform on the C_D Pin

The above solution is based on the dual power supplies provided by one power converter module or two converters without remote output enable control. Furthermore, the I/O voltage supply and core voltage supply may come from two different power converters with the individual enable pin control. We also can use the supervisor from NCP30x family to realize the sequencing control. The below diagram indicates the implementation of using the NCP30x in this case. This example makes sure that the V_{cc2}, generated by Converter2.

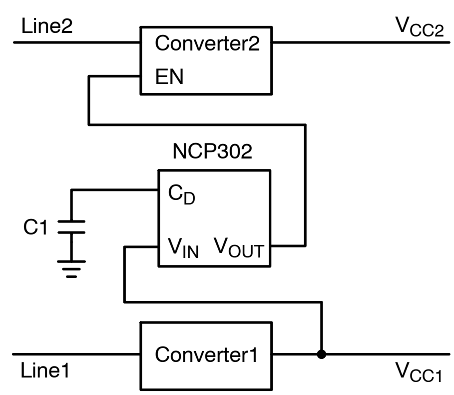

Figure 11. Based on the Two Converter Supply

The schematic circuit below shows an application example of a power supply solution for a Microprocessor using two NCP1529 high efficiency step−down converters which provide the I/O power requirement of the processor and the power to processor’s core. The supervisor, U3 is the sequencing control to guarantee the I/O voltage present before core voltage. And the supervisor, U4 having different threshold version to the U3 is the detector of the core voltage. It also can be used to generate the reset signal to the processor.

We can find in Figure 11 that C7 and C8 are used for delay generation. The C7 capacitor makes V_Core rising about 1.0 ms after V_I/O, while C8 produces the time delay between V_Core present and RESET output deasserted. This reset time delay, necessary for the clock stabilization and for the processor initialization could be adjusted according to the requirement of the processor.

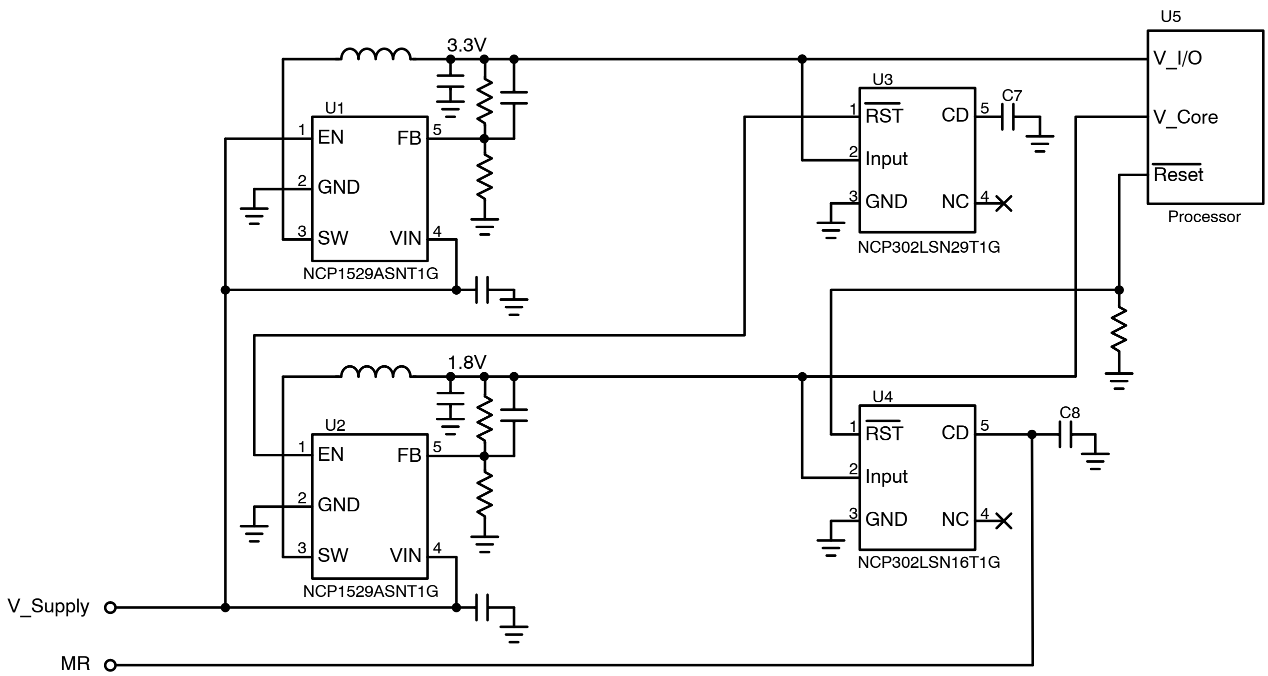

Figure 12. Application Using an ON DC−DC Device

Summary

With a few components, the NCP30x offers a simple way to control the power−up cycle of various power lines on a board. While monitoring a primary supply voltage, these devices enable or disable a secondary voltage via an external MOSFET or the individual enable pin off the voltage converter.

By adding a simple low cost NMOS transistor or an open collector logic gate, we also showed that the user can control power down of the power supply in a very simple and safe manner.

Regarding the different voltage supply sequencing requirements by the special digital system, the NCP302 series provide the function of programmable timeout delay. Only one external capacitor is required.

At last, we gave a concrete example of a power on sequencing, using an NCP30x for controlling the enable pin of a DC/DC converter, another NCP30x providing the microcontroller reset signal.

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