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## A 30 W Power Supply Operating in Quasi-Square Wave Resonant Mode

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### APPLICATION NOTE

#### INTRODUCTION

Quasi-Square Wave Resonant converters, often noted QR converters, offer an elegant means to make Flyback supplies look more friendly on the Electro-Magnetic Interference (EMI) point of view. By delaying the ON switching event until the drain-source voltage has decayed to a minimum, switching losses are reduced and rising slopes lose their stiffness. Designers get an immediate benefit from this configuration since the MOSFET runs cooler and the EMI input filter becomes easier to implement. Designing QR Switch-Mode Power Supplies (SMPS) requires some attention but is not an area dedicated to experts only. You will discover through the following lines how new ON Semiconductor solutions can help you to quickly turn your quasi-resonant project into a working device.

#### What is Quasi-Resonance?

The term quasi-resonance is normally related to the association of a real hard-switching converter and a resonant tank. While the operation in terms of control is similar to that of a standard PWM controller, an additional network is added to shape the variables around the MOSFET: current or voltage. Depending on the operating mode, it becomes possible to either switch at zero current (ZCS) or zero voltage (ZVS). Compared to a conventional PWM converter, a QR operation offers less switching losses but the RMS current circulating through the MOSFET increases and forces higher conduction losses. However, one of the main advantage in favor of the quasi-resonance is the reduced spectrum content either conducted or radiated.

True ZVS quasi-resonance means that the voltage present on the switch looks like a sinusoidal arch. Figure 1 shows how such a signal could look.

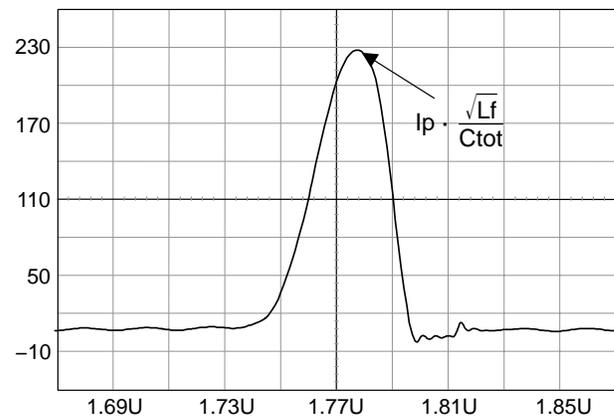


Figure 1. A Truly Resonating Vds Signal on a Quasi-Resonant Flyback Converter

The main problem with this technique lies in the very high voltage generated at the switch opening. Most of the time, these resonant offline designs require around 1.0 kV BV<sub>DSS</sub> MOSFETs whose price is clearly incompatible with high volume markets. As a result, designers orientate their choice toward another compromise called quasi-square wave resonant power supplies.

#### Quasi-Square Wave Resonant Converters

As we saw, true resonant operation hampers the MOSFET selection by imposing a high voltage at the switch opening. If we closely look at the standard hard-switching waveform (Figure 2), we can see that there exists a time where the drain voltage gets minimum. This occurs just after the core reset.

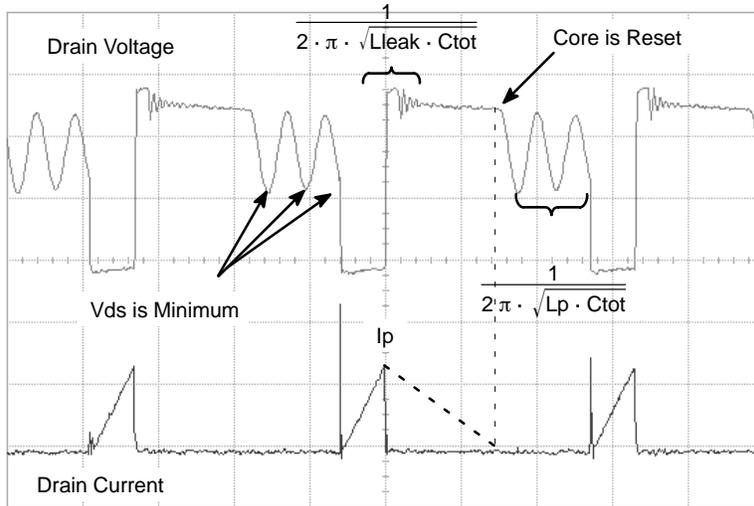


Figure 2. Hard-Switching Waveforms in Discontinuous Conduction Mode (DCM)

From Figure 2, it is possible to imagine a controller that turns a MOSFET ON until its current grows-up to the setpoint to turn it off and then waits until the core reset is detected (usually via an auxiliary winding) to reactivate this transistor. As a result, the controller does not include any standalone clock but only detects the presence of events conditioned by load/line conditions: this is a so-called free-running operation. Converters based on this technique are often designated as Self-Oscillating Power Supplies (SOPS), valley switching converters, etc.

Oscillations origins can be seen from Figure 3 arrangement where L-C networks appear. Depending on the event, two different configurations are in play:

- At the switch closing, the primary current crosses the primary inductance but also the leakage inductance,  $L_{leak}$ . When the turn-on time expires, the energy stored in  $L_p$  is transferred to the secondary side of the

transformer via the coupling flux. However, the leakage inductance, which models the coupling between both transformer sides, reverses its voltage and imposes a quickly rising drain voltage. The slope of this current is  $\frac{I_p}{C_{tot}}$  (eq. 1) where  $C_{tot}$  lumps all capacitances surrounding the drain node: MOSFET capacitors, primary transformer parasitics but also those reflected from the secondary side etc. As a result,  $L_{leak}$  and  $C_{tot}$  form a resonating network of natural frequency  $\frac{1}{2 \cdot \pi \cdot \sqrt{L_{leak} \cdot C_{tot}}}$  (eq. 2). The maximum drain voltage can then be computed using the characteristic impedance of this LC network.

$$V_{ds \max} = V_{in} + \frac{1}{N} \cdot (V_{out} + V_f) + I_p \cdot \sqrt{\frac{L_{leak}}{C_{tot}}} \quad (\text{eq. 3})$$

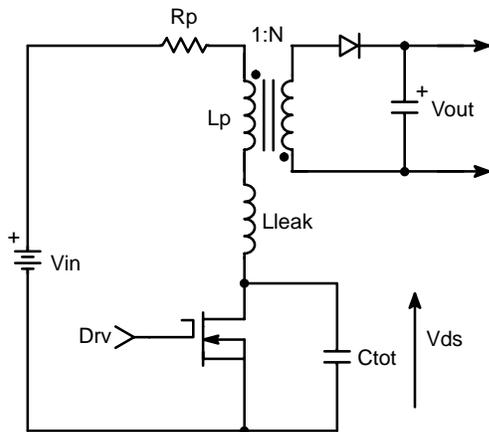


Figure 3. A Typical Flyback Arrangement Unveils Two Different Resonating Networks

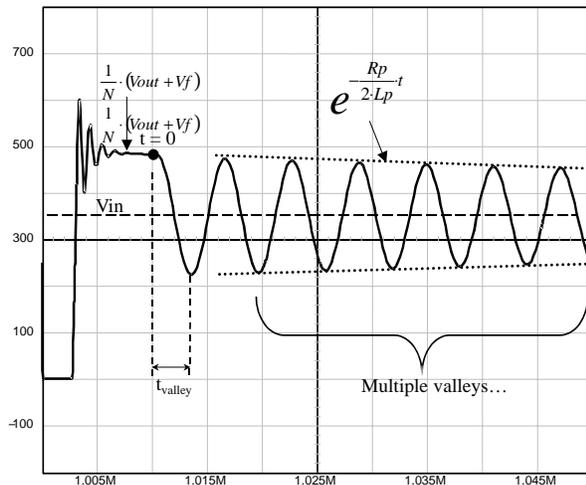


Figure 4. A Typical Flyback Ringing Waveform Occurring at the Switch Opening

- When the transformer core resets, primary and secondary currents drop to zero: the secondary diode stops its conduction and the reflected voltage on the primary naturally dies out. From eq. 3, this implies that the terms after  $V_{in}$  all collapse to zero and  $V_{ds}$  tends toward  $V_{in}$ . However, the transition would be brutal in the lack of a resonating network, this time made by  $L_p$ , the primary inductance, and nearly the same  $C_{tot}$  as before. As you can imagine, a sinusoidal ringing takes place, damped by the presence of ohmic losses (DC + AC resistance of the primary winding modeled by  $R_p$ ). The drain–source shape rings as the below formula details:

$$V_{ds}(t) = V_{in} + \frac{1}{N} \cdot (V_{out} + V_f) \cdot e^{-\alpha \cdot t} \cdot \cos(2 \cdot \pi \cdot f_{prim} \cdot t) \quad (\text{eq. 4})$$

with:  $\alpha = \frac{R_p}{2 \cdot L_p}$  (eq. 5) (the damping factor),  $f_{prim} =$

$$\frac{1}{2 \cdot \pi \cdot \sqrt{L_p \cdot C_{tot}}} \quad (\text{eq. 6}) \quad (\text{natural ringing frequency}),$$

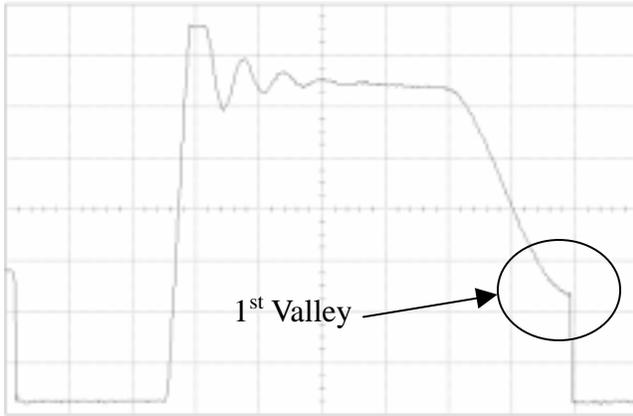


Figure 5. A Typical Drain–Source Shot of a Quasi–Square Wave Converter

As one can see, the total period is made of different events, where the core is first magnetized ( $T_{on}$ ), then fully reset ( $T_{off}$ ) and finally a time ( $T_w$ ) delay is inserted to reach the lowest value on the drain. Let us look at how the frequency moves by respect to the input/output conditions.

**Evaluating the Free–Running Switching Frequency**

The free–running frequency can be evaluated by looking at Figure 6, where the primary current (circulating in the primary inductance) is depicted. From the definition of the various slopes, we can express the first two events,  $T_{on}$  and  $T_{off}$  quite easily:

$$t_{on} = \frac{L_p}{V_{inDC}} \cdot I_p \quad (\text{eq. 8})$$

$$t_{off} = \frac{L_p}{\left[ \frac{N_p}{N_s} \cdot (V_{out} + V_f) \right]} \cdot I_p \quad (\text{eq. 9})$$

$V_{in}$  is the input voltage,  $V_f$  the diode’s forward drop and  $N$ , the  $N_s:N_p$  turn ratio.

We can see from Figure 4 that the drain is the seat of various voltage drops when going down the ringing wave. These drops are called “valleys”. If we manage to switch the MOSFET right in the middle of these valleys, we ensure minimum turn–on losses, particularly those related to capacitive dissipation:

$P_{avgcap} = \frac{1}{2} \cdot C_{tot} \cdot V_{ds}^2 \cdot F_{sw}$  (eq. 7)  $\rightarrow 0$ . Thus, quasi–square wave operation or valley switching, will imply a reactivation of the switch when  $V_{ds}$  is minimum. As various figures portray, this occurs some time further to the transformer core reset. By implementing this method, we build a converter which naturally exhibits a variable frequency operation since the reset time depends upon the input/output operating conditions. Figure 5 shows a typical shot of a quasi–square wave converter.

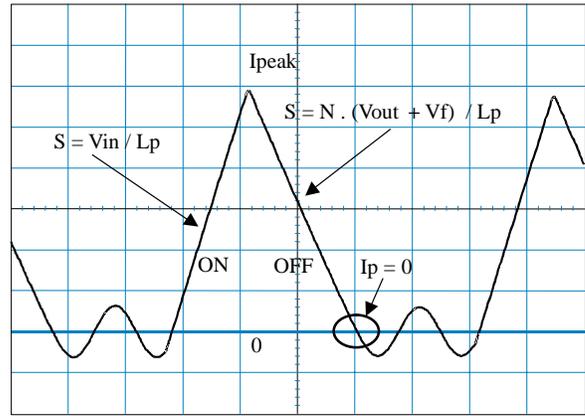


Figure 6. The Primary Inductance Current is Made of Two Different Slopes (here a restart occurs on the second one)

For the  $T_w$  event, which is one fourth of the natural ringing frequency given by equation 4, we will compute the derivative of equation 4 and null it to find its minimum:

$$\frac{d(V_{in} + e^{(-\alpha \cdot t)} \cdot \cos(2 \cdot \pi \cdot f_{prim} \cdot t))}{dt} = 0 \quad (\text{eq. 10})$$

Which gives a result of:

$$T_w = \frac{1}{2 \cdot f_t} - \frac{1}{2} \cdot \frac{\alpha \tan\left[\frac{\alpha}{2 \cdot \pi \cdot f_{prim}}\right]}{\pi \cdot f_{prim}} \quad (\text{eq. 11})$$

However, this result is not very practical because of its inherent complexity. If we observe equation 10, we can see that the minimum is reached when the term  $\cos(2 \cdot \pi \cdot f_{prim} \cdot t)$  equals  $-1$ . Otherwise stated, we can solve  $t$  for which the cosine is null or the full product equals  $\pi$ . This gives:  $T_w = \frac{1}{2 \cdot f_{prim}} = \pi \cdot \sqrt{L_p \cdot C_p}$  (eq. 12)

However, this result is valid only for low damping coefficient, that is to say,  $e^{-\alpha \cdot t} \approx 1$ . Experience shows that it is good enough for the vast majority of cases.

As a result, the final switching period is computed by summing up all these sequences and introducing the input power expression:

$$T_{sw} = T_{on} + T_{off} + T_w \quad (\text{eq. 13})$$

$$T_{on} + T_{off} + T_w = I_p \cdot L_p \cdot \left[ \frac{1}{V_{inDC}} + \frac{1}{\left[ \frac{N_p}{N_s} \cdot (V_{out} + V_f) \right]} \right] + \pi \cdot \sqrt{L_p \cdot C_p} = \frac{1}{F_{sw}} \quad (\text{eq. 14})$$

$$P_{in} = \frac{P_{out}}{\eta} = \frac{1}{2} \cdot L_p \cdot I_p^2 \cdot F_{sw} \quad (\text{eq. 15})$$

$$\text{from eq. 15, } I_p = \sqrt{\frac{2 \cdot P_{out}}{\eta \cdot L_p \cdot F_{sw}}} \quad (\text{eq. 16})$$

Now, plugging  $F_{sw}$  (eq. 14) in eq. 16, gives:

$$I_p \cdot L_p \cdot \left( \frac{1}{V_{inDC}} + \frac{1}{V_{reflect}} \right) + T_w = \frac{L_p \cdot I_p^2 \cdot \eta}{P_{out} \cdot 2} \quad (\text{eq. 16a})$$

with:

$$V_{reflect} = \frac{N_p}{N_s} \cdot [V_{out} + V_f]$$

$$I_p = \frac{\left[ A \cdot V_{reflect} + A \cdot V_{in} + \left[ \sqrt{A \cdot (A \cdot V_{reflect}^2 + 2 \cdot A \cdot V_{reflect} \cdot V_{in} + A \cdot V_{in}^2 + 2 \cdot \eta \cdot V_{in}^2 \cdot V_{reflect}^2 \cdot T_w)} \right] \right]}{(\eta \cdot L_p \cdot V_{in} \cdot V_{reflect})} \quad (\text{eq. 17})$$

From equation 16, one can then compute the switching frequency using the calculated peak current:

$$F_{sw} = \frac{2 \cdot P_{out}}{L_p \cdot I_p^2} \quad (\text{eq. 18})$$

However, equation 17 is not very practical since it involves  $L_p$ , what we are actually looking for. It can certainly be used to discover the operating peak current from known inductance and capacitor values but neglecting  $T_w$ , offers a simpler formula that can be used as first frequency iteration (e.g. to feed a Spice simulator for instance):

$$F_{sw} = \frac{1}{L_p \cdot 2 \cdot P_{out} \left( \frac{N \cdot (V_{out} + V_f) + V_{in}}{\eta \cdot (V_{in} \cdot (N \cdot (V_{out} + V_f)))} \right)^2} \quad (\text{eq. 19})$$

Entering equation 18 into a spreadsheet and plotting  $F_{sw}$  versus various parameters ( $V_{out}$ ,  $I_{out}$  etc.), it gives an idea about the high frequency variability of the system. Figure 7 and Figure 8 respectively plot  $F_{sw}$  in function of the input voltage and the output current for a given application.

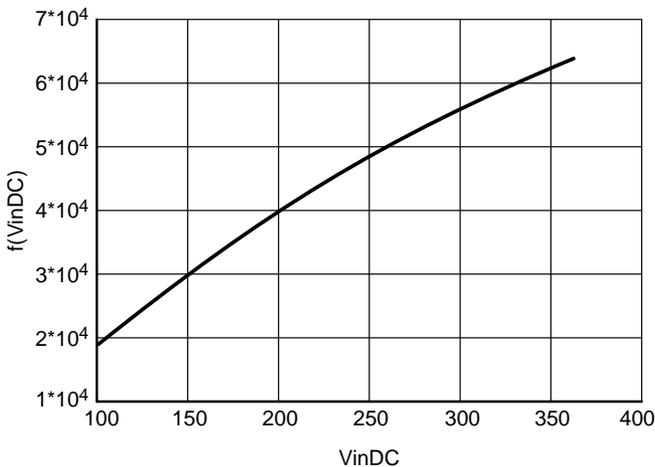


Figure 7. Frequency Variations for a 100 W SMPS Operated from Universal Mains

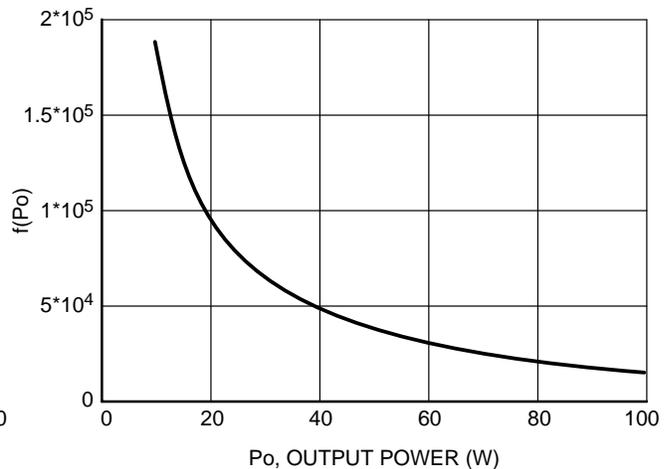


Figure 8. Frequency Dependency with Load at a Given Input Voltage (100 V)

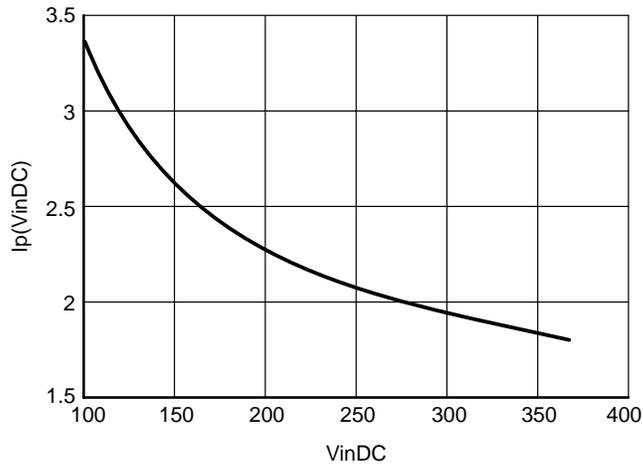


Figure 9. Peak Current Variations for a 100 W Output Power with Different Line Voltages

**A Quiet EMI Signature**

Manipulating sinusoidal (or close-to) variables always offer a narrower spectrum content compared to hard-switching systems. Figures 10 and 11 depict the

conducted EMI signature of two systems operated at the same point but implementing different switching techniques.

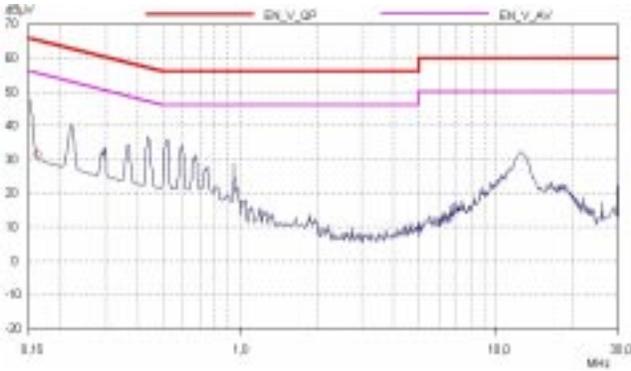


Figure 10. A soft-switching approach reduces the energy content above 1.0 MHz . . .

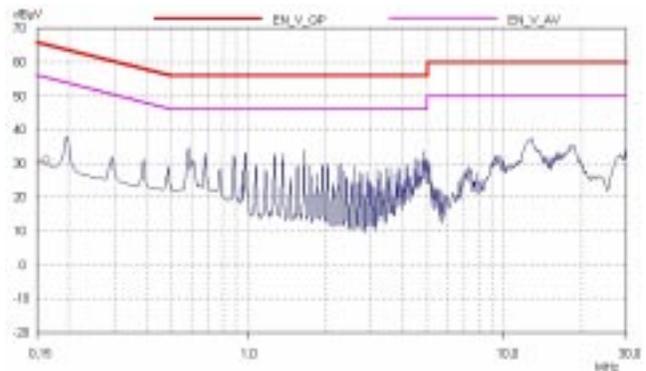


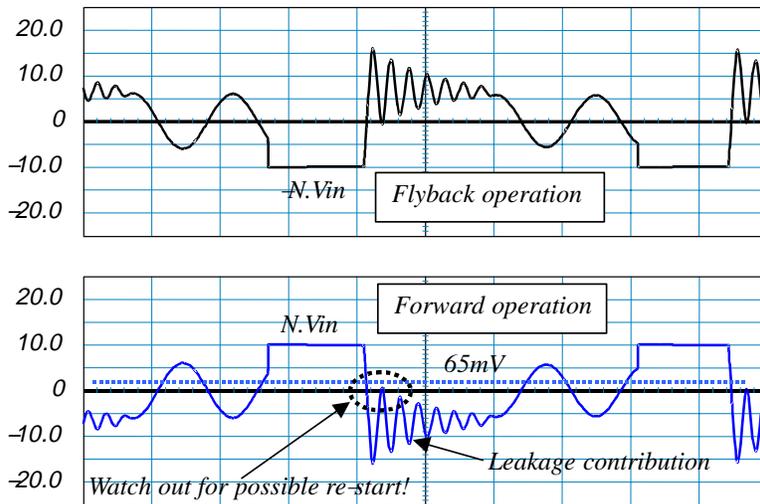
Figure 11. . . while a hard-switching system generates a lot of noise in this portion

Since the MOSFET is reactivated at the lowest drain level, the classical Coss capacitor discharge at the switch closing is non-existing and the very narrow peak current has gone (also this peak is often confusing the current-sense comparator when it is really energetic, even sometimes despite the presence of the LEB circuitry). As a result, Quasi-square wave converters are recommended where the Switch-Mode Power Supply (SMPS) needs to operate close to Radio-Frequency section, e.g. Set Top Boxes, TV sets, etc.

**Detecting the Core Reset Event**

Core reset detection is usually done via a dedicated auxiliary winding whose voltage image is directly linked to the transformer flux by  $V_{aux} = N \cdot \frac{d\phi}{dt}$  (eq. 20) . Depending on the controller device, the polarity of the observed signal must fit its detection circuitry. In ON Semiconductor NCP1205, this polarity should be of Forward type, that is to say, when the MOSFET opens, the auxiliary voltage (actually the Flyback level) dips below ground and stays there, safely clamped at  $-0.7$  V, until the core reset occurs. Figure 12 gives an example of a demagnetization signal given by an auxiliary winding wired in both types.

## AND8129/D



**Figure 12. Core Reset Detection Signal Coming From Either a Forward or Flyback Winding**

Operating the auxiliary winding in Forward offers various advantages as the use of the variable  $V_{cc}$  level to introduce overpower compensation. Also the controller is always operating (supplied) whatever the secondary output conditions. Figure 14 shows a possible way to do that. Please note the presence of a small RC filter necessary to a) introduce a time delay after the core resets (and thus activate the MOSFET right in the minimum of the valley wave) b) to filter out any leakage contribution that could adversely restart the controller at a higher switching frequency (see Figure 12 evidence).

Overpower compensation is there to avoid a larger overcurrent trip point at high-line compared to low-line conditions. For instance, suppose that the maximum peak current at low line (100 V) would be 3.3 A to pass 100 W and that your maximum peak current (given by the sensing element and the internal clamping setpoint, usually 1.0 V) is

fixed to 4.0 A. It means that the overcurrent condition exists as soon as the output load slightly increases, perhaps to 120 W, which is what was defined with a maximum peak of 4.0 A. Now, if you run the converter at high line, e.g. 350 VDC, the peak current will decrease, as shown by Figures 9 thru 14, down to 1.8 A. As a result, you still have a dynamic of 2.2 A to go before hitting the 4.0 A maximum current trip point. The SMPS can thus theoretically deliver up to 220 W before it actually trips. To overcome this problem, you can wire a resistor between the  $V_{cc}$  and the current sense pin since, in forward polarity,  $V_{cc} = \frac{N_{aux}}{N_p} \cdot V_{inDC}$  (eq. 21) which is a direct image of the mains. As a result,  $V_{cc}$  moves with the high-voltage rail and offsets the current sense reading, offering a natural, low power, input feedforward.



- **Low Standby Power:** If SMPS naturally exhibits a good efficiency at nominal load, they begin to be less efficient when the output power demand vanishes. By smoothly reducing the number of switching cycles per second, the NCP1205 drastically reduces the power wasted during light load conditions. In no-load conditions, the NCP1205 allows the total standby power to easily reach and exceed the next International Energy Agency (IEA) recommendations.
- **Short-Circuit Protection:** By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short-circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation. For given applications, you can easily disconnect this protective feature. This short-circuit detection is independent from the auxiliary level, hence a loose coupling between auxiliary and power windings is not a problem.
- **Overvoltage Protection:** By continuously checking its own Vcc rail, the NCP1205 can safely go into latch-off phase when the operating voltage exceeds 36 V. In Forward winding applications, this options lets you also protect the design against transient mains over voltages. For application where an adjustment is necessary, the DIP14 versions pins out the dedicated comparator input to let you select the protection level of your choice.
- **Large Supply Range:** Battery charger applications require that the controller can still control the output current when the output voltage is close to zero (e.g. a discharged battery). This is called Constant-Current/Constant-Voltage (CC-CV) operation. To allow the controller self-supply when the output voltage disappears, one needs to wire the auxiliary winding in the Forward mode. However, most of today's primary side controllers have difficulty to cope with a Forward auxiliary winding operated on a universal mains because of the large voltage dynamics it implies. Fortunately, by authorizing 7.0 V through 36 V operation, the NCP1205 eases the designer task on the self-supply side.
- **Low Output Ripple in Standby:** Some loads are sensitive to the ripple present on the output. This is the case for Li-Ion batteries where a clean voltage is required to ensure the longest service. Standard hysteretic controllers produce un-acceptable output ripple. By smoothly reducing the operating frequency, the NCP1205 generates a lower ripple when entering the standby mode.
- **No Acoustic Noise While Operating:** Instead of reducing the switching frequency at high peak currents, the NCP1205 waits until the peak current demand falls below a fixed 1/3<sup>rd</sup> of the peak maximum limit. As a result, frequency reduction takes place without having a singing transformer. You can thus select cheap magnetic components free of noise problems.

- **External MOSFET Connection:** By leaving the external MOSFET external to the IC, you can select avalanche proof devices which, in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).
- **SPICE Model:** A dedicated model that lets you run transient cycle-by-cycle simulations is available to verify your theoretical design. Ready-to-use templates can be downloaded in OrCAD's PSpice and INTUSOFT's from ON Semiconductor web site, NCP1205 related section.

Complete details regarding the implementation of the NCP1205 are given in the application note AND8043.

### A 30 W Power Supply Design Using the Quasi-Resonant Approach

$P_{out\ nominal} = 30\ W$

$V_{out} = 16.8\ V$

Universal input voltage = 90–265 VAC

$V_{dc\ min} \approx 100\ VDC$  (including losses and ripple)

$V_{dc\ max} \approx 370\ VDC$

Short-circuit protection

Standby power less than 300 mW at no-load

The design of a quasi-resonant converter featuring low standby power requires the understanding of several parameters before calculating anything:

1. Do we need to ensure true Zero Voltage Switching (ZVS) operation over a large operating input range?
2. If we ensure high switching frequency at maximum power and low mains, while it minimizes the magnetics, the frequency foldback will eventually take place at higher input voltages.
3. At what peak current level do we authorize the frequency foldback to avoid acoustical noise in the transformer?

#### Answer 1:

Yes, because we will shape the drain-source voltage (especially at the switch opening) to be as smooth as possible to a) soften the EMI signature b) wire a large resonating capacitor whose losses should be minimized (see eq. 7) c) due to b, we will save a costly RCD clamping network. As a result, we will reflect as much as we can, taking into account a 800 V BV<sub>dss</sub> MOSFET and higher secondary rectifier losses (peak and RMS secondary currents go up). We have selected a turn ratio of 16.6 who gives a reflected voltage of 288 V. The drain stress at high line without leakage, is thus:  $(265 \times 1.414) + 288 = 662\ V$ , which gives room for the leakage effects. Please remember that the best is to reflect the maximum voltage from the secondary side, best case being  $V_{reflect} = N \times (V_{out} + V_f) = V_{in}$ . But in that

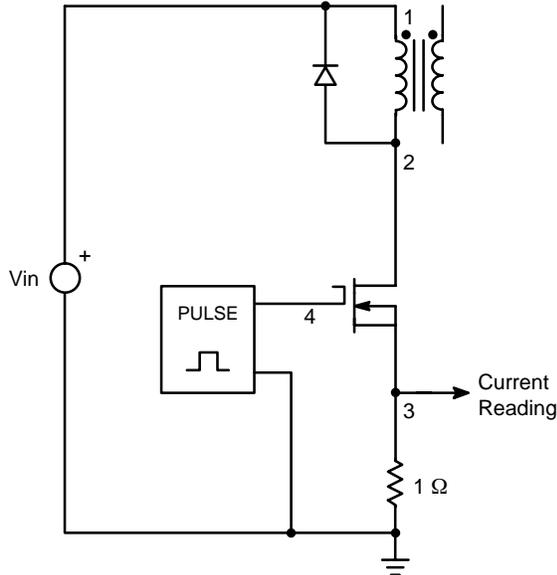
latest case, you would probably need to pick up a 900 V or 1.0 kV BV<sub>dss</sub> MOSFET.

**Answer 2:**

In our case, we prefer to avoid any foldback at nominal load over the whole input voltage. Frequency foldback starts by discrete jumps between valleys and can create some noise. If we accept to increase the frequency at high line before folding the frequency back (with a 1.0 nF connected to pin 4, we clamp at F<sub>min</sub> = 90 kHz), then we can accept to lower the switching frequency at low lines, but not too low to avoid entering audible frequencies.

**Answer 3:**

The answer really depends upon the transformer structure you have used, e.g. the type of core, bobbin, etc. The best is to setup a test structure where you impose a peak current in your transformer prototype at low, audible, frequency (e.g. around 5.0 kHz). Figure 16 offers a possibility to do that via a power MOSFET.



**Figure 16. A power MOSFET and an adjustable duty-cycle generator lets you select the right peak current.**

By adjusting the PULSE source duty-cycle, it becomes possible to impose a given peak current, directly sensed across the 1.0 Ω resistor via an oscilloscope. The freewheel diode could be a 1N4937/MUR160 or equivalent whereas the source Vin can be around 30 VDC with a 100 V BV<sub>dss</sub> 6.0 A MOSFET. Start by low peak currents and slowly increase the duty-cycle until noise can be heard. This corresponds to the very maximum peak current you can pass while skipping cycles or when entering frequency foldback without having a singing transformer. The best is actually to

generate burst of pulses to drive the MOSFET. The discontinuity associated with the burst sequence is more favorable to trigger mechanical resonances compared to evenly spaced pulses. Suppose that a 550 mA peak current is offering the best value with your transformer. Since the 1205 folds back at 30% of the maximum primary current, you will select a maximum peak current of 1.0 V/1.65 A or an R<sub>sense</sub> of 0.6 Ω. Iterations using the dedicated Excel spreadsheet will therefore help to select the right primary inductance and turns-ratio to reach good performance in standby without making noise.

Let's now follow the below design steps to build our 30 W QR Switch-Mode Power Supply:

1. In our opinion, the very first element to dimension is the primary to secondary turn ratio. In effect, it will condition, among other parameters, a) the drain-source stress of the MOSFET at its opening b) the Peak Inverse Voltage (PIV) of the secondary rectifier at the switch closing c) the area where the supply operates in Zero Voltage Switching (ZVS). As we have seen before, if we select an 800 V MOSFET, we can select the turn ratio by (including a 10% safety margin):

$$\max \text{Vin}_{\text{DC}} + \frac{N_p}{N_s} \cdot (\text{Vout} + \text{Vf}) \leq 800 \text{ V} - 10\% \quad (\text{eq. 22})$$

→ N<sub>p</sub>/N<sub>s</sub> < 19.5. We selected a 16.6 turn-ratio which will ensure ZVS up to Vin = 16.6 x (16.8 + 1) = 295 VDC.

2. Having the right turn ratio, we can calculate the primary peak current needed to pass the 30 W of power. If we neglect the delay to reach the valley of V<sub>ds</sub>(t) (see eq. 12), then we end up with a simplified current definition:

$$I_{p \text{ max}} = 2 \cdot P_{\text{out}} \cdot \frac{\frac{N_p}{N_s} \cdot (\text{Vout} + \text{Vf}) + \min \text{Vin}_{\text{DC}}}{\eta \cdot \min \text{Vin}_{\text{DC}} \cdot \frac{N_p}{N_s} \cdot (\text{Vout} + \text{Vf})}$$

plugging values into it gives us a maximum peak current of: 0.94 A. This value will slightly change as soon as you consider other parasitic elements (see AND8089, “Determining the Free-Running Frequency for QR Systems”), but is a good starting point.

3. From that value, we know that the NCP1205 will start folding back the frequency into the audible range at a peak current equal to 30% of the maximum value (this is the way the NCP1205 is designed). We know by experience (see Figure 16), that we shall not go over 550 mA to avoid having a singing transformer. In our case, 30% of 0.94 A is well within our specs. We even have place for improvement if we feel a need to increase I<sub>p max</sub> for parameter variation reasons.

4. The inductor is defined knowing what frequency range we want to cover. As exemplified by Figure 16, the switching frequency increases at high input voltage (whereas  $I_p$  goes low) and decreases at low input voltages (whereas  $I_p$  goes up). In some cases, it is desirable to keep the magnetics small and thus operate at high frequency at low line. On the other way, some designers find that is desirable to compensate the higher RMS losses at low line, by reducing the switching losses via a lower switching rate. We will stick for this latest option and calculate  $L_p$  to be above the audible range at low line and maximum output power. Rearranging equation 19, leads to solve:

$$L_p \geq \frac{1}{F_{sw \min} \cdot 2 \cdot P_{out} \left[ \frac{\frac{N_p}{N_s} \cdot (V_{out} + V_f) + V_{in \min}}{\left( \eta \cdot \left( V_{in \min} \cdot \left( \frac{N_p}{N_s} \cdot (V_{out} + V_f) \right) \right) \right)} \right]^2} \quad (\text{eq. 23})$$

or  $L_p$  greater than 1.9 mH. This number is a first result and we will see that further iterations are needed to freeze this number.

5. Since we implement true ZVS up to 295 V, we can connect a large capacitor between drain and ground to clamp the maximum voltage generated by the leakage inductance. The  $V^2$  capacitor losses will be null in ZVS (see eq. 7) but will start to increase at high line when ZVS is lost. We believe that even if it is a bit detrimental to efficiency, the cost improvement brought by the absence of a RCD clamping network and smoother waveforms (good for EMI), really justifies the addition of this drain-ground capacitor. By tweaking equation 3, we can calculate the amount of necessary capacitance we need between drain and ground:

$$C_{reso} \geq \frac{L_{leak}}{\left( V_{ds \max} - V_{in} - \frac{N_p}{N_s} \cdot (V_{out} + V_f) \right)^2} \cdot I_p^2 \quad (\text{eq. 24})$$

If we consider a leakage inductance of around 30  $\mu\text{H}$  (first estimation) and we plug our values into equation 24, then  $C_{reso}$  needs to be greater than 1.6 nF.

By losing ZVS at 295 V, we can imagine that the switch restart will occur on a drain wave at  $330 \text{ V} - 295 = 35 \text{ V}$ . These nominal conditions imply a *theoretical* switching frequency of 131 kHz (eq. 19) and capacitive losses of (eq. 7):  $P_{loss} = 0.5 \times 35^2 \times 1.6 \text{ n} \times 131 \text{ k} = 130 \text{ mW}$  which is acceptable.

6. You can see through the lines we wrote that many parameters can be changed to obtain different converters at the end. The reflected voltage is

obviously one of the most sensitive parameters which influences others. Increasing the reflected voltages to keep a wider ZVS operating range has a price on other numbers:

The switching frequency increases (reset voltage on  $L_p$  is stronger)

The primary peak current and conduction losses are improved (if  $F_{sw}$  goes up, the peak demand goes low)

The secondary peak current and conduction losses increase

The MOSFET undergoes a bigger stress at the switch opening

MOSFET turn-on losses can be really null (if ZVS is achieved)

7. Final values will be obtained due to the design spreadsheet available to download from ON Semiconductor web site which includes parasitic elements (such as the leakage inductance and the  $C_{ds}$  capacitor) and whose formulae are described in AND8089. After we entered our desired operating conditions, the below numbers were extracted from the spreadsheet:

$L_p = 1.2 \text{ mH}$

$L_{leak} (\text{measured}) = 15 \mu\text{H}$

$N_p/N_s = 16.6$

$I_p \text{ max} = 1.5 \text{ A}$ , to include various tolerances

$R_{shunt} = 2 \times 1.2 \Omega$  in parallel

$C_{reso} = 1.5 \text{ nF}/1.0 \text{ kV}$

Calculated frequency at nominal load and minimum input voltage = 50 kHz (120 VDC and 30 W)

Calculated frequency at nominal load and maximum input voltage = 87 kHz (370 VDC and 30 W)

### Using SPICE to Check for the Validity of the Assumptions

Despite the existence of a dedicated NCP1205 SPICE model, it is faster and easier to use a simplified free-run approach to have an idea of the final results. Figure 17 offers a possible way to represent a free-running controller: the demagnetization path includes a standard flip-flop which latches the transition while the feedback signal fixes the current setpoint. Due to a simple arrangement, the system simulates really quickly and allows an immediate assessment of what has been suggested by the Excel spreadsheet. The feedback loop is purposely simplified with a Zener diode arrangement, but you can upgrade it with a TL431 circuitry. It will simply take longer simulation time to settle. As Figures 18 and 19 show, it is difficult to make the distinction between the simulation and the real measurement on the demoboard.

# AND8129/D

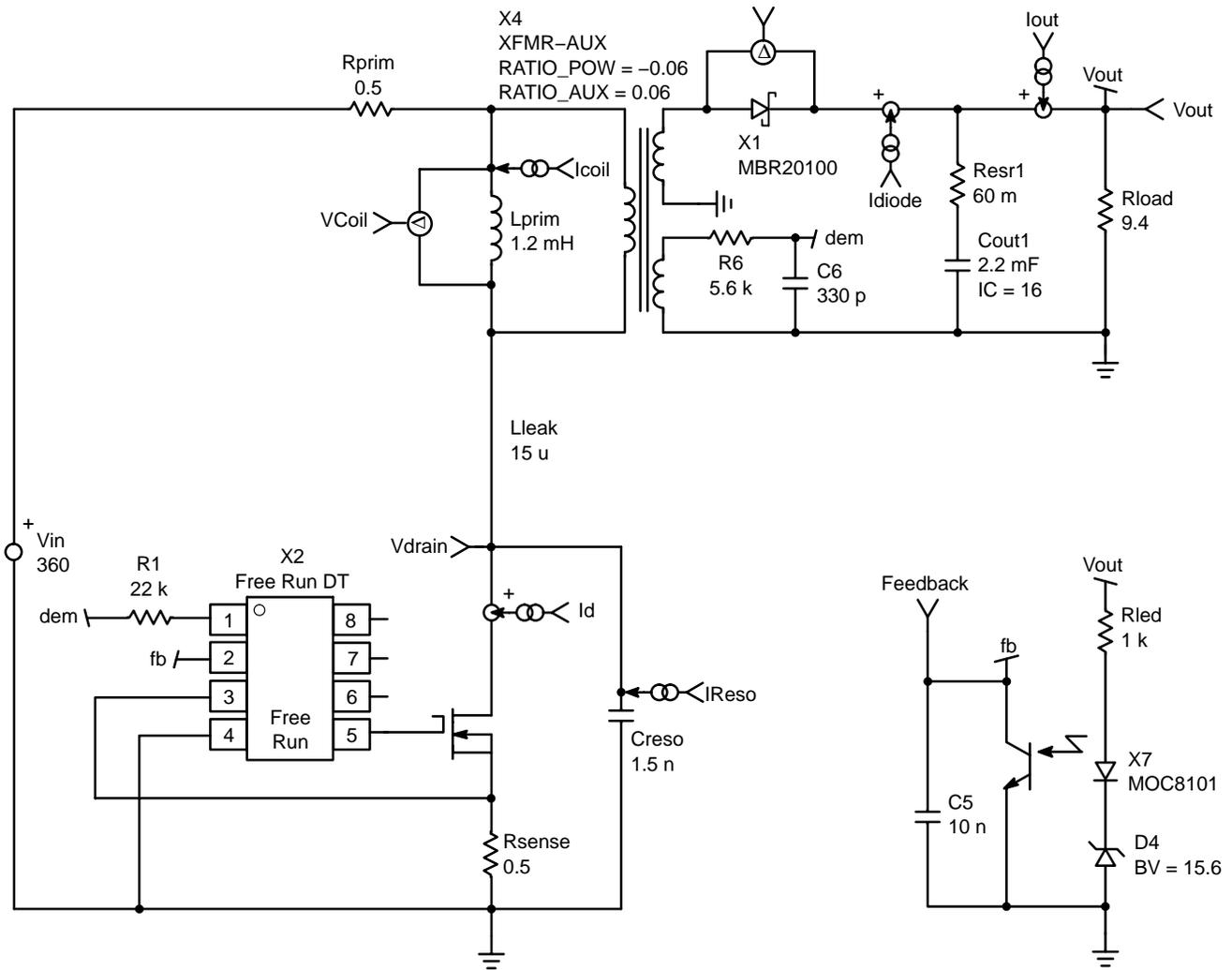


Figure 17. A Simplified Free-Running Controller Eases the Simulation Setup and Increases Speed

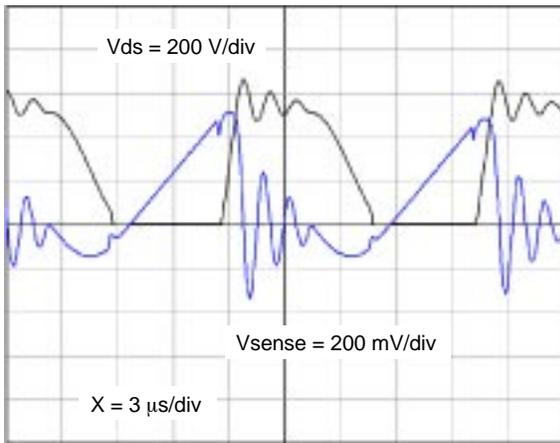


Figure 18.



Figure 19.

It becomes difficult to differentiate the simulation from the real world . . . Figure 18 is simulation, Figure 19 is measured.

The Spice simulation offers another advantage which is the evaluation of the component stresses. Due to good models, you can immediately measure the MOSFET conduction losses worse case, the RMS current in the rectifiers, in the resonating capacitor, etc. Figure 20 portrays these typical waveforms. In light of this data, we can now select components and peripherals accordingly:

**MOSFET:** Depending on the type, you compute the power using:  $P_{conduction} = RDS(ON) @ T_j = 100^{\circ}C \times Id_{RMS}^2 = 3 \times 0.465^2 = 650 \text{ mW}$  at low line. In our case, switching losses are close to zero due to ZVS and ZCS. When the main grows up to 370 VDC on the bulk capacitor, the ZVS effect goes away and capacitive losses appear due to Creso. Simulation shows that conduction losses stay below 1.0 W. We selected an 800 V MOSFET from ST.

> A small note about MOSFET Spice models: They do not reflect  $T_j$  temperature effects on the  $RDS(ON)$  and other parameters (e.g.  $V_{th}$ ). As a result, calculating the total power (including switching losses) by multiplying and averaging  $V_{ds}(t) \times I_d(t)$  over one period does only make sense for junction temperatures of  $27^{\circ}C$ .

**Resonating Capacitor:** This device shall sustain the voltage peak but also a large RMS current. Simulations show that worse case occurs at high line with a RMS current of 370 mA. We have used a WIMA FPK1 series with good results.

**Primary Inductance:** Low line imposes the highest stress on the transformer. The following specs to be passed to the transformer manufacturer:

$L_p = 1.2 \text{ mH}$

$I_{pmax} = 2.0 \text{ A}$

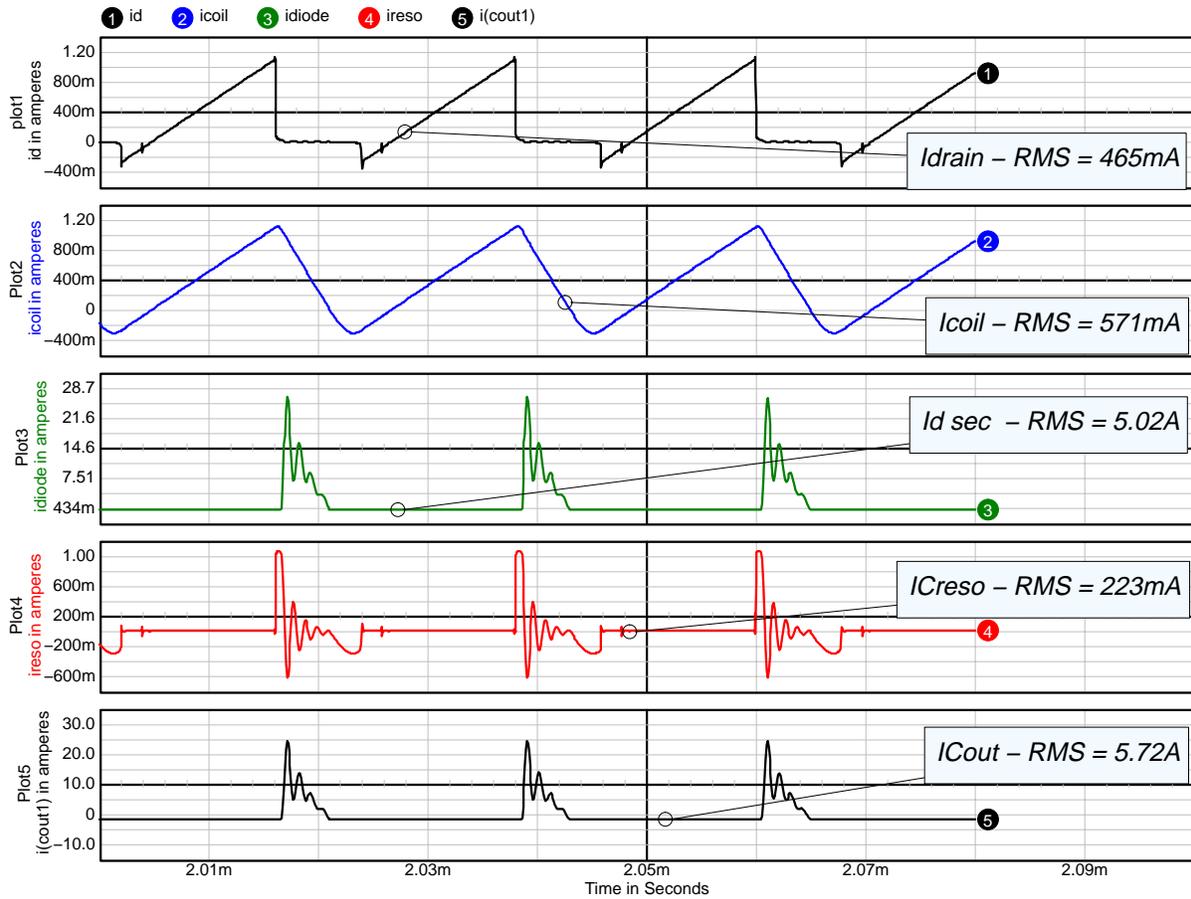
$I_{pRMS} = 571 \text{ mA}$

$N_p:N_s = 1:0.06$

$N_p:N_{aux} = 1:0.06$

**Secondary Rectifier:** The conduction losses of a diode are given by:  $P = Id_{RMS}^2 \times R_d + V_f @ I_d \times Id_{AVG}$ . In our case, we obtain theoretical total losses of 1.21 W. An MBR10100 can be a good choice.

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**Figure 20. Typical Waveforms Obtained by a Spice Simulation of the Quasi-Resonant Converter**

**Output Capacitor:** This component will be selected based on the required output ripple but also on its ability to sustain the total RMS current. The dissipation of the capacitor is dictated by its Equivalent Series Resistor (ESR) and follows the following formula:  $P_{cap} = R_{ESR} \times I_{ripple}^2$ . A 5.7 A RMS current will thus be the primary criterion when selecting the right device. It is also possible to wire capacitors in parallel to split the total current between devices.

### Final Schematic

Figure 21 shows the final schematic implemented in the NCP1205 demoboard. As you can see, the large capacitor placed on the drain allows us to avoid a costly and noisy RCD clamping network. However, the PCB layout offers the necessary place to include one if experiments are needed. The auxiliary winding is wired to offer a stable Flyback

voltage but a diode (D5) is placed in series with ground to generate the right Forward polarity (see Figure 15). Because of the resonating capacitor placed between drain and ground, a spike can occur at high line as soon as the ZVS effect is lost. To help the LEB circuitry inside the NCP1205, an additional cleaning network is added through R2-C2. Please note that the resonating capacitor C14 is wired between drain and ground and *not* between drain and source. This is to avoid any negative current flowing inside the current sense pin at turn-off (during the natural drain-source ringing). The feedback loop is standard and uses a TLV431 to further lower the secondary side standby power. Since its minimum operating current is 100  $\mu$ A, there is no need to waste 1.0 mA in it as with traditional TL431 series.



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The use of a TLV431 really reduces the output power wasted in no-load. But sometimes, the repetition rate of the switching pulses in standby is so low, that the auxiliary goes down and reaches the NCP1205 UVLOlow, restarting the high-voltage current source. To avoid this situation, you either need to increase a bit the auxiliary turn ratio (this is not a problem because the extended Vcc range offers that flexibility) or slightly load the output by a resistor. Experience has shown that when the auxiliary Vcc was close to 8.2 V, a simple 10 mW bleeding element connected to Vout was enough to bring Vauxiliary to around 9.0 V, giving the necessary headroom.

### Demoboard Performance and Typical Waveforms

The 30 W demoboard is available from ON Semiconductor. It corresponds to Figure 21 sketch. Below are some shots and measurements captured on the board, testifying for its good characteristics:

Efficiency @ 230 VAC = 86.6%

Standby power (Pout = 0) = 174 mW

Efficiency @ 110 VAC = 84.4%

Standby power (Pout = 0) = 65 mW



Figure 22. Drain-source signals at different powers: P1 < P2 < P3 < P4, you can note the multiple valley jumping.

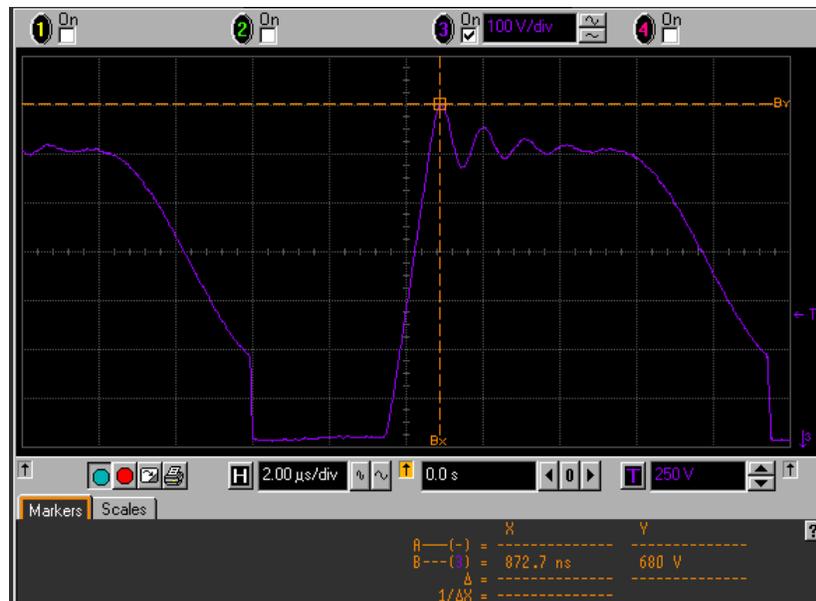


Figure 23. At high line and nominal power, the drain level is kept below the MOSFET breakdown.

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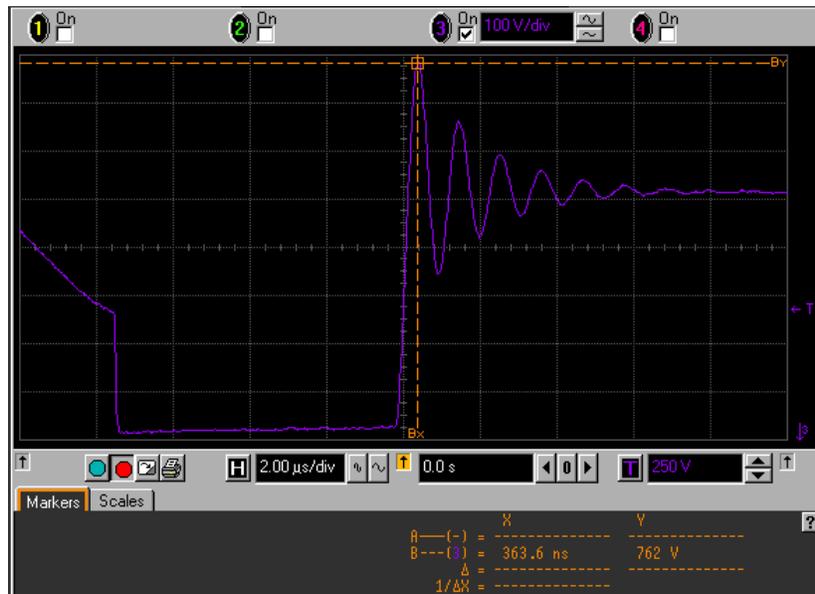


Figure 24. At high line, an output short circuit does not jeopardize the MOSFET's life.

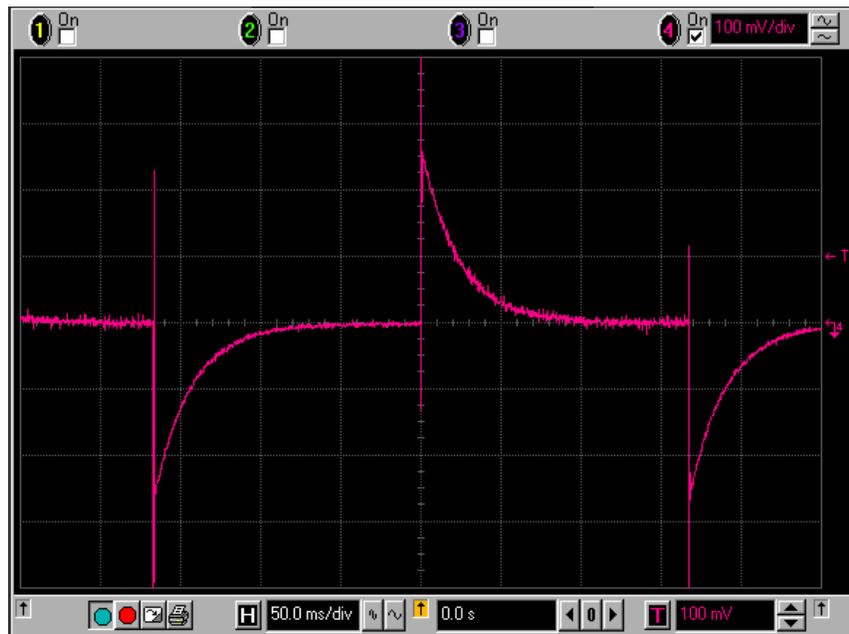


Figure 25. An output bang-bang test (1 to 2.5 A) does not reveal any instability. The spikes are related to the LC filter installed on the output.

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### Bill of Materials

All resistors are 1/4 W 5% SMD unless otherwise noted.

Part Value	Designator	Type	Manufacturer	Reference	Comments
00	R1				
1.0 k	R2				
10	R14				
2.2 k	R15				
18 k	R17				
100 k	R19				
33	R20	Through Holes			
18 k	R23				
1.2	R26				1.0 W
1.2	R25				1.0 W
3.3 k	R21				
1.0 k	R22				
39 k	R24				
3.9 k	R30				
6.8 k	R31	Through Holes			
6.8 k	R32	Through Holes			
220 nF	C1				
220 pF	C2				
47 $\mu$ F/400 V	C12	Snap-in	BC Comp.	2222-057-56479	
82 pF	C13				
1.5 nF/1.0 kV	C14		Wima	1500-FKP1	
1000 $\mu$ F/25 V	C15	Vertical			
1000 $\mu$ F/25 V	C16	Vertical			
1000 $\mu$ F/25 V	C17	Vertical			
6.8 nF	C18				
220 $\mu$ F/25 V	C19				
1.0 nF	C20				
47 $\mu$ F/25 V	C22				
2.2 nF	C23		Roederstein	WY Series Y1	
10 $\mu$ H	L3		Coilcraft	PCV-2-103-05	
2 x 27 mH	L4		Schaffner	RN114-08/0.2	
BRIDGE D8			KBU-8J		
MBR20100	D7		ON Semiconductor		
STP5NB80	M2		ST		
NCP1205P	IC4		ON Semiconductor		
SFH6156-2	IC5		Infineon		
TLV431	IC6		ON Semiconductor		TO-92
30 W Transformer	T1		Coilcraft	Z9508-A	
			Pulse-Engineering	PF0137	

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