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A Quasi−Resonant SPICE Model Eases Feedback Loop Designs

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Within the wide family of Switch Mode Power Supplies (SMPS), the Flyback converters represent the structure of choice for use in small and medium power applications. For compact designs and radio−frequency sensitive applications, e.g. TV sets or set−top boxes, Quasi− Resonant power supplies start to take a significant market share over the traditional fixed frequency topology. However, if the feedback loop control is well understood with this latter, for instance via a comprehensive literature and SPICE models, the situation differs for self−oscillating variable switching frequency structures where no model still exists. This article will show how a simple large−signal averaged SPICE model can be derived and used to ease the design work during stability analysis.

Quasi−Resonant Operation

It is difficult to abruptly dig into the analytical analysis without giving a basic idea of the operation of a converter working in Quasi−Resonance (QR). Figure 1 depicts a typical FLYBACK converter drain−source waveform as you probably have already observed. When the switch is closed, the drain−source voltage V_{DS} is near 0 V and the input voltage V_g appears across the primary inductance L_P: the current inside L_P ramps up with a slope of

$$S_{ON} = \frac{V_g}{L_P} \qquad \text{(eq. 1)}$$

When the controller instructs the switch opening, the drain−source quickly rises and the energy transfer between primary and secondary takes place: the secondary diode conducts and the output voltage flies back on the primary side, over L_P. This “Flyback” plateau is equal to $V_g + (V + V_f) / N$, where N is the secondary to primary turn ratio, V the output voltage and V_f the diode forward voltage drop. During this time, the primary current decreases with a slope now imposed by the reflected voltage

$$S_{OFF} = \frac{(V + V_f)}{N \times L_P} \qquad \text{(eq. 2)}$$

Figure 2 zooms on the simulated primary current (actually circulating in the magnetizing inductor), showing how it moves over one switching cycle.

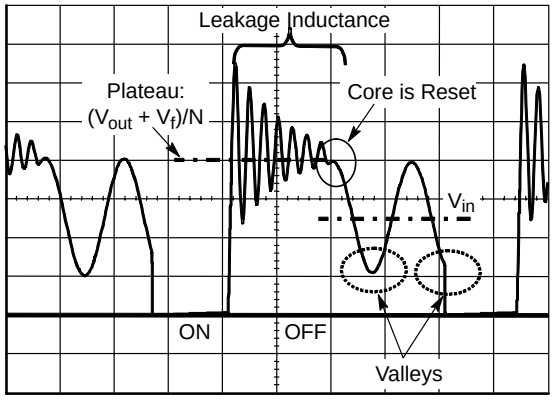

Figure 1. A Typical FLYBACK Drain−Source Waveform

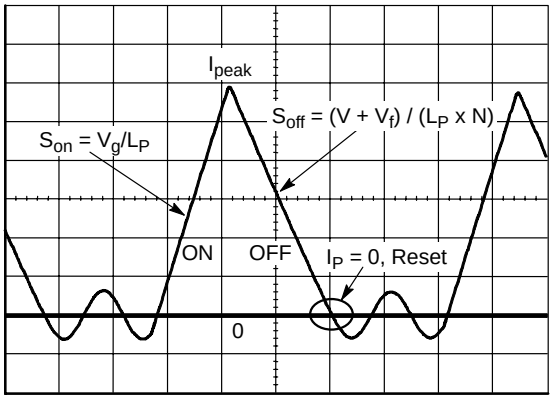

Figure 2. The Primary Current Ramps Up and Down to Zero in DCM

When the primary current reaches zero, the transformer core is fully demagnetized: we are in Discontinuous Conduction Mode (DCM). The primary inductance L_P together with all the surrounding capacitive elements C_{tot} create a LC filter. When the secondary diode stops conducting at $I_P = 0$, the drain branch is left floating since the MOSFET is already open. As a result, a natural oscillation occurs, exhibiting the following frequency value:

$$F_{ring} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_P \cdot C_{tot}}} \qquad \text{(eq. 3)}$$

As in any sinusoidal signal, there are peaks and valleys. When you re−start the switch in one valley, where the voltage is minimum, the MOSFET is no longer the seat of heavy turn−on losses engendered by capacitive effects: this is the so−called Quasi−Resonance operation where the switching frequency depends on the peak current, the various slopes ON and OFF and the number of valleys you choose after the core reset. In our study, we will first concentrate on a simplified SPICE version where the power switch is actuated right after the reset detection point (parasitic ringings are neglected) and later on, a more sophisticated declination will incorporate parasitic delays.

Modeling the Switch Network

Figure 3 depicts a Flyback topology where the switching elements generating the above waveforms have been highlighted: the power switch (usually a MOSFET transistor) and a diode, performing a rectification job. During the converter operation, the Pulse Width Modulator controller (PWM) instructs the transistor to turn ON, in order to store energy in the primary side. The primary current builds up until the setpoint imposed by the feedback loop is reached. At this time, the controller toggles the transistor to the OFF state and energy transfers to the secondary side. If the ON and OFF states can be described by a set of linear equations, there exists a discontinuity linking these two events. Despite the presence of linear elements in the converter (capacitors, inductors and resistors), the presence of the commuting switch clearly introduces the non−linearity that prevents us from directly writing the small−signal equations…

When learning electronic circuits at school, there were some exercises in which we were asked to reveal the transfer function of bipolar amplifiers. At that time, we learned to replace the transistor symbol by its equivalent small−signal model: the schematic turned into the simple association of current and voltage sources that greatly simplified the analysis. In the average circuit modeling technique, we also follow the same philosophy: the exercise lies in isolating and replacing the switch network with a set of current and voltage sources whose electrical architecture do not vary with time. Therefore, plugging the equivalent model back into the converter of interest allows us to resolve its transfer characteristics.

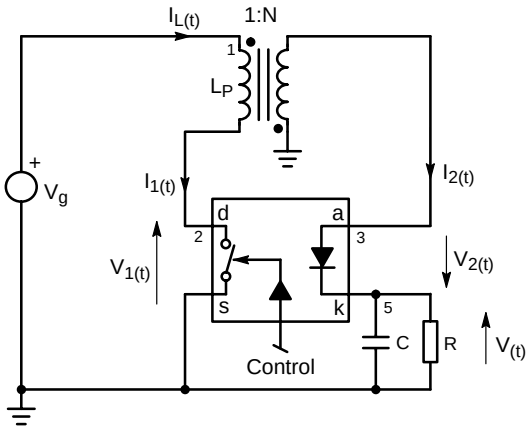

Figure 3. A Flyback Power Supply where Switches have been Isolated…

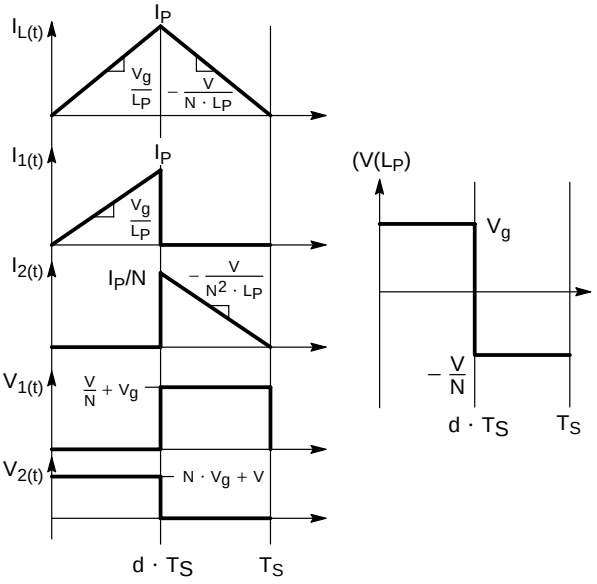

Figure 4. …**and Individual Signals Separately Plotted.**

Deriving Equations

The object of deriving a model consists in writing the equations that describe the switch network averaged input and output quantities that a) depend from each other b) obey to the control input. Let us draw the various waveforms before starting any line of algebra (Figure 4). From this picture, we can develop equations that will finally describe the *averaged* evolution of the values of interest, the input / output voltage and current of our switch network:

$$< I_{1(t)} > = \frac{I_P}{2} \times d \qquad \text{(eq. 4)}$$

$$< I_{2(t)} > = \frac{I_P}{2 \times N} \times d' \qquad \text{(eq. 5)}$$

$$< V_{1(t)} > = \frac{V + N \times V_g}{N} \times d' \qquad \text{(eq. 6)}$$

$$< V_{2(t)} > = [V + N \times V_g] \times d \qquad \text{(eq. 7)}$$

where: V is the output voltage, V_g the input voltage, I_P the primary peak current, N the N_S / N_P turn ratio and d the duty−cycle ($d' = 1 - d$).

Please note that in this first approach, we do not consider any delay occurring at the switch opening or induced by equation 3. These events will considered later on, in a more complex model.

Averaging Input / Output Voltages

From the inductor volt−second balance approximation, we know that the average voltage across an inductor operated in a steady−state converter is null. By looking at the $V(L_P)$ sketch, we obtain the following equation:

$$< V(L_P) > = d_{(t)} \times < V_{g(t)} > - \frac{d'_{(t)} \times < V_{(t)} >}{N} = d_{(t)} \times < V_{g(t)} > - \frac{(1 - d_{(t)}) \times < V_{(t)} >}{N} = 0 \quad \text{(eq. 8)}$$

which lets us extract the classical output / input voltage ratio

$$\frac{< V_{(t)} >}{< V_{g(t)} >} = N \times \frac{d_{(t)}}{(1 - d_{(t)})} \quad \text{(eq. 9)}$$

and as a result, the duty−cycle expression:

$$d_{(t)} = \frac{< V_{(t)} >}{< V_{(t)} > + N \times < V_{g(t)} >} \quad \text{(eq. 10)}$$

Now, by plugging equation 10 in equation 6, we obtain the average voltage across the primary switch terminal: $<V_{1(t)}>$ =

$$\frac{< V_{(t)} > + N \times < V_{g(t)} >}{N} \times (1 - d_{(t)}) = \frac{< V_{(t)} > + N \times < V_{g(t)} >}{N} \times \left(1 - \frac{< V_{(t)} >}{< V_{(t)} > + N \times < V_{g(t)} >}\right) = < V_{g(t)} > \quad \text{(eq. 11)}$$

which agrees with the inductor volt−second balance approximation (from Figure 1 since, by definition, $<V(L_P)> = 0$, then V_g appears across the switch terminals).

To reveal $<V_{2(t)}>$, let us plug equation 10 into 7: $<V_{2(t)}>$ =

$$[< V_{(t)} > + N \times < V_{g(t)} >] \times d_{(t)} = [< V_{(t)} > + N \times < V_{g(t)} >] \times \frac{< V_{(t)} >}{< V_{(t)} > + N \times < V_{g(t)} >} = < V_{(t)} > \quad \text{(eq. 12)}$$

which again could be deduced from Figure 3 since the average voltage across the secondary inductance is zero…

Averaging Input / Output Currents

The peak inductor current depends on the time during which V_g is applied over L_P. If we recall that this time (actually t_{on}) is d x T_S, then:

$$I_P = \frac{V_g}{L_P} \times d \times T_S \quad \text{(eq. 13)}$$

From Figure 4, the average current $<I_{1(t)}>$ can be obtained by evaluating the triangular area (charge in $Coul_{omb}$) and dividing by the switching period. This is expressed by equation 4. Now plugging equation 13 in 4, we obtain:

$$< I_{1(t)} > = \frac{1}{2} \times \frac{< V_{g(t)} >}{L_P} \times d_{(t)} \times T_S \times d_{(t)} = \frac{< V_{g(t)} > \times d_{(t)}^2 \times T_S}{2 \times L_P} \quad \text{(eq. 14)}$$

however, from equation 11, we know that $<V_{1(t)}> = <V_{g(t)}>$ thus equation 14 turns into:

$$< I_{1(t)} > = \frac{< V_{1(t)} > \times d_{(t)}^2 \times T_S}{2 \times L_P} \quad \text{(eq. 15)}$$

Applying the same technique to the secondary current $I_{2(t)}$, leads to:

$$< I_{2(t)} > = \frac{1}{T_S} \int_{d.T_S}^{T_S} I_{2(t)} \cdot dt = \frac{1}{2} \times \frac{I_P}{N} \times d'_{(t)} \quad \text{(eq. 16)}$$

plugging equation 13 in 16 leads to:

$$< I_{2(t)} > = \frac{< V_{g(t)} > \times d_{(t)} \times (1 - d_{(t)}) \times T_S}{2 \times N \times L_P} = \frac{< V_{1(t)} > \times d_{(t)} \times (1 - d_{(t)}) \times T_S}{2 \times N \times L_P} \quad \text{(eq. 17)}$$

A 100% Efficiency Power Transfer…

Assuming that 100% of the primary stored energy is released to the secondary side, then we can use equations 11 and 12 to write:

$$<P_{(t)}> = <V_{1(t)}> X <I_{1(t)}> = <V_{2(t)}> X <I_{2(t)}> \quad \text{(eq. 18)}$$

From equation 15, we can see that a current is generated by a voltage multiplied by a term. This term is obviously homogenous to the inverse of an impedance. By re−arranging equation 15, we obtain:

$$Re_{(d)} = \frac{< V_{1(t)} >}{< I_{1(t)} >} = \frac{2 \times L_P}{d_{(t)}^2 \times T_S} \qquad \text{(eq. 19)}$$

where the input impedance depends on the duty−cycle $d_{(t)}$. However, in quasi−resonant converters, the power transfer adjusts by varying the peak current I_P which finally imposes the operating frequency. Since by definition $t_{on} = d \times T_S$, we can re−arrange equation 9 to reveal

$$T_S = t_{on} \times \frac{(N \times V_g) + V}{V} \qquad \text{(eq. 20)}$$

By finally plugging equation 10 and 20 into 19, we obtain a t_{on}−dependent input effective resistance definition:

$$Re(t_{on}) = \frac{2 \times L_P \times (V + N \times V_g)}{t_{on} \times V} \qquad \text{(eq. 21)}$$

that Figure 5 portrays:

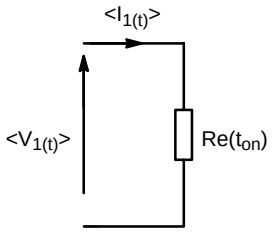

Figure 5.

The average input waveforms of the switch can be modeled via the above equivalent network.

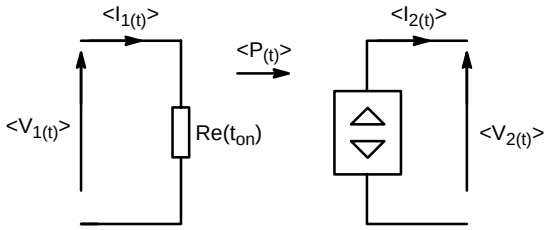

Figure 6.

The two−port loss−free network where all the input power transforms into output power.

As reference [1] details, the apparent power consumed by R_e, P_{in}, is entirely transmitted to the output since we assume a 100% efficiency. Therefore, equation 19 can be re−written by:

$$< P_{(t)} > = < V_{1(t)} > \times < I_{1(t)} > = \qquad \text{(eq. 22)}$$
$$< V_{2(t)} > \times < I_{2(t)} > = \frac{< V_{1(t)} >^2}{Re(t_{on})}$$

Our switch network can thus modeled according to the so−called loss−free network where all the power developed across an input resistance transfers to the output without any loss (Figure 6) [1].

A More Complex Model Including Parasitic Effects

The above simplified model assumes that there are no transient times between the conduction and demagnetization phases. A more precise modelling approach requires that the two following delays Δ_{t1} and Δ_{t2} are taken into account, as highlighted by Figure 7 and 8:

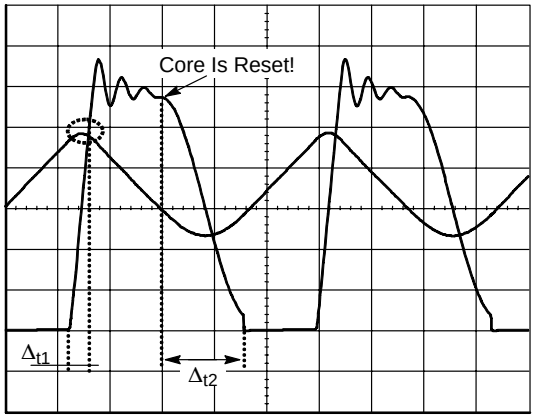

Figure 7.

The presence of a capacitive node slows−down the V_{DS} rising and makes the drain sinusoidally ring at the core reset…

1. At the end of the ON−time, the power switch opens but the energy transfer to the secondary side does not start immediately. The primary inductor current (I_P) that cannot flow through the power switch, charges the surrounding capacitive elements (C_{tot}) until C_{tot} voltage exceeds

$$V_g + \frac{V}{N} \qquad \text{(eq. 23)}$$

At that moment, the secondary diode starts to conduct and current feeds the output capacitor. One can assume that the C_{tot} charging time (Δ_{t1}) is short enough to consider that the primary inductor current stays equal to I_P during this interval. Then, Δ_{t1} is the time necessary to charge the capacitor C_{tot} with a current I_P from zero to

$$V_g + \frac{V}{N} \quad \text{, i.e.:} \quad \Delta t1 = C_{tot} \times \frac{V_g + \frac{V}{N}}{I_P} \qquad \text{(eq. 24)}$$

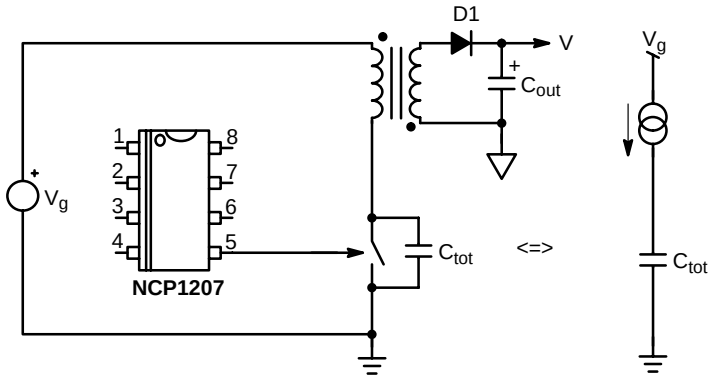

Figure 8.

When the power switch turns off, the primary inductor behaves like a current source that charges the C_{tot} capacitor. This sequence ends when voltage developed across C_{tot} exceeds $[V_g+(V+V_f)/N]$, that is when the secondary diode D1 starts to conduct.

2. At the end of the core reset, both switches (power switch and secondary diode) are off. The primary inductor L_P together with C_{tot} form a LC network. C_{tot} voltage (and thus the drain source voltage of the power switch) oscillates around the input voltage V_g between a peak value (the initial level: $V_g + \frac{V}{N}$) and a valley value $V_g - \frac{V}{N}$, the damping effects being neglected. To benefit from the quasi−resonant mode, it is recommended to turn the power switch on in the valley, where the drain−source voltage is minimized. This naturally reduces the dV/dt and switching losses to a minimum (in practice, an appropriate delay inserted after the core reset detection provides an effective method to synchronize the power switch turn on with the valley event). A simple look at Figure 7 shows that the valley occurs at half the oscillation period. Therefore, the delay Δ_{t2} between the core reset completion and the optimal turn on time is given by the following equation:

$$\Delta t2 = \pi \times \sqrt{L_P \times C_{tot}} \qquad \text{(eq. 25)}$$

Once these delays are defined, it is about time to revise the previous equations in order to include Δ_{t1} and Δ_{t2} effects. The main parameters of interest are the average input and output currents, the equivalent resistance and the switching period. If we combine equations 24 and 13 that express I_P as a function of the input voltage, the inductor value and the ON−time leads to:

$$\Delta t1 = L_P \times C_{tot} \times \frac{V_g + \frac{V}{N}}{V_g \times t_{on}} \qquad \text{(eq. 26)}$$

If (d′ x T_S) depicts the core reset time, Δ_{t1} and Δ_{t2} times require to change (d′=1−d) into:

$$d' = 1 - d - \frac{\Delta t1 + \Delta t2}{T_S} \qquad \text{(eq. 27)}$$

The inductor volt−second balance approximation of equation 8 still holds. However, it must be revised by replacing d′(t) by its novel value as expressed by equation (27):

$$< V(L_P) > = d \times V_g - \frac{\left(1 - d - \frac{\Delta t1 + \Delta t2}{T_S}\right) \times V}{N} = 0 \qquad \text{(eq. 28)}$$

Re−arranging equation (28), one can unveil the duty cycle expression:

$$d = \frac{\left(1 - \frac{\Delta t1 + \Delta t2}{T_S} \times V\right)}{(N \times V_g) + V} \qquad \text{(eq. 29)}$$

The switching period is the sum of the on−time, the core reset time (t_{demag}), Δ_{t1} and Δ_{t2}:

$$T_S = t_{on} + t_{demag} + \Delta t1 + \Delta t2 \qquad \text{(eq. 30)}$$

The time t_{demag} can be easily deducted from the Figure 4 sketch. Since the core reset is the time necessary to discharge the primary inductor from I_P to zero with a $(V+V_f)/N$ slope, it comes:

$$t_{demag} = \frac{L_P \times I_P}{V/N} = t_{on}\frac{N \times V_g}{V} \qquad \text{(eq. 31)}$$

Substitution of equation (31) into (eq. 30), leads to the following expression where T_S is a function of t_{on}:

$$T_S = \Delta t1 + \Delta t2 + \frac{[(N \times V_g) + V] \times t_{on}}{N} \qquad \text{(eq. 32)}$$

Equation (15) that defines the average input current as a function of the input voltage, the duty cycle, the inductor value and the switching period, still holds. Substitution of equation (29) into equation (15) leads to:

$$< I_{1(t)} > = \frac{V_g \times \left(1 - \frac{\Delta t1 + \Delta t2}{T_S}\right) \times V \times t_{on}}{2 \times L_P \times [(N \times V_g) + V]} \qquad \text{(eq. 33)}$$

Replacing T_S by its equation 32 expression, it comes:

$$< I_{1(t)} > = \frac{V_g \times \left(1 - \frac{\Delta t1 + \Delta t2}{\Delta t1 + \Delta t2 + \frac{[(N \times V_g) + V] \times t_{on}}{V}}\right) \times V \times t_{on}}{2 \times L_P \times [(N \times V_g) + V]} \qquad \text{(eq. 34)}$$

Re−arranging this equation, one can obtain:

$$< I_{1(t)} > = V_g \times \frac{t_{on}^2}{2 \times L_P \times \left\{ \Delta t1 + \Delta t2 + \frac{[(N \times V_g) + V] \times t_{on}}{V} \right\}} \quad \text{(eq. 35)}$$

Similarly to the simplified model analysis, one can note that the average input current is proportional to the input voltage. The effective resistance Re is thus: $Re(t_{on})$ =

$$\frac{2 \times L_P}{t_{on}^2} \times \left\{ \Delta t1 + \Delta t2 + \frac{[(N \times V_g) + V] \times t_{on}}{V} \right\} \quad \text{(eq. 36)}$$

It is pleasant to confirm that if $\Delta_{t1}=\Delta_{t2}=0$, the $Re(t_{on})$ expression reduces to equation 21…

Then, the equivalent circuit depicted in Figure 6 and based on the loss−free resistor $Re(t_{on})$ can be applied. To complete the model, let's calculate $<I_{2(t)}>$ by combining equations (17) where d′ is taken equal to (t_{demag}/T_S), (13) and (31):

$$< I_{2(t)} > = \frac{1}{N} \times \frac{V_g \times t_{on}}{2 \times L_P} \times \frac{t_{on}}{T_S} \times \frac{N \times V_g}{V} \quad \text{(eq. 37)}$$

Substitution of equation (32) giving T_S into equation (37), leads to: $<I_{2(t)}>$ =

$$\frac{V_g \times t_{on}}{2 \times L_P} \times \frac{t_{on}}{\Delta t1 + \Delta t2 + \frac{[(N \times V_g) + V] \times t_{on}}{V}} \times \frac{V_g}{V} \quad \text{(eq. 38)}$$

This expression can be simplified as follows: $<I_{2(t)}>$ =

$$\frac{V_g}{Re(t_{on})} \times \frac{V_g}{V + V_f} = < I_{1(t)} > \times \frac{V_g}{V + V_f} \quad \text{(eq. 39)}$$

The model assumes a 100% efficiency power transfer. To better stick to reality, the above expression should be multiplied by the estimated efficiency to obtain the final $<I_{2(t)}>$ equation:

$$< I_{2(t)} > = < I_{1(t)} > \times \frac{V_g}{V + V_f} \times \mathit{eff} \quad \text{(eq. 40)}$$

where *eff* is the efficiency.

The following table summarizes the main equations upon which our model is based:

Delay between the power switch opening and the start of the energy transfer to secondary side:	$\Delta t1 = L_P \times C_{tot} \times \frac{V_g + \frac{V}{N}}{V_g \cdot t_{on}}$
Delay between the core reset completion and the next turn on of the power switch (Note 1):	$\Delta t2 = \pi \times \sqrt{L_P \times C_{tot}}$
Equivalent input resistance:	$Re(t_{on}) = \frac{2 \times L_P}{t_{on}^2} \times \left\{ \Delta t1 + \Delta t2 + \frac{[(N \times V_g) + V] \times t_{on}}{V} \right\}$
Switching Frequency:	$f_{SW} = \frac{1}{\Delta t1 + \Delta t2 + \frac{[(N \times V_g) + V] \times t_{on}}{V}}$
Average input current:	$< I_{1(t)} > = V_g / Re(t_{on})$
Average output current:	$< I_{2(t)} > = \frac{V_g}{V} \times < I_{1(t)} > \times \mathit{eff}$

NOTE: *: even if the proposed value appears to us as the optimal one, SMPS designers might make a different choice for Δ_{t2}. That is why, if the model proposes $\Delta t2 = \pi \times \sqrt{L_P \times C_{tot}}$ as default value, you can modify this simulation parameter to stick to your application in case valley switching is not considered.*

Implementing the SPICE Model with the Loss−Free Network

As exemplified by Figure 6, the model shall emulate an input resistor being t_{on} dependent and then transmit a power following equation 23. Different ways exist to implement this topology in Spice. INTUSOFT's IsSpice authorizes behavioral resistors, e.g. following any particular ohmic evolution with time, voltage, current etc. For instance, the following code would be accepted by the simulator:

R1 1 2 R = 2.0 * v(1)^0.5 + 3.0*v(2)*time + v(2)*sqrt(temp)

Unfortunately, despite its obvious interest, this code is not very portable and would constrain the model usage to IsSpice only. Figure 9 offers a more practical association using behavioral voltage and current sources [2]:

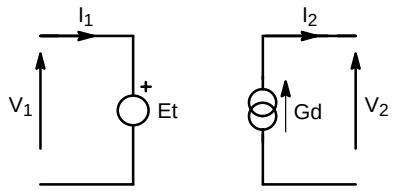

Figure 9. Implementing the DCM Model via Two Controlled Elements

The input voltage source being supposed to emulate a resistance, its expression shall be in the form of:

Et = I_1 x Re where Re is simply equation 22, thus:

$$Et = I_1 \times \frac{2 \times L_P \times (V + N \times V_g)}{t_{on} \times V} \qquad \text{(eq. 41)}$$

where t_{on} is an input port of the model, imposed by the control loop. In the final model, this value will be derived from L_P and the peak current given by the error voltage divided by R_{sense}, where V, V_g and N are to be passed or sensed by the model.

The output current source together with V_2 shall deliver the output power as imposed by equation 22. Thus, i_2 generation shall follow:

$$I_2 = \frac{R_{in(eq)} \times i_1^2}{v2} = \frac{2 \times L_P \times (V + N \times V_g)}{t_{on} \times V} \times \frac{i_1^2}{v2} \qquad \text{(eq. 42)}$$

Also, one can introduce the efficiency by simply multiplying the I_2 current source by {eff}, where *eff* is a parameter entered by the user in the model. Hence, I_2 can be written as:

$$I_2 = \frac{2 \times L_P \times (V + N \times V_g)}{t_{on} \times V} \times \frac{i_1^2}{v2} \times \mathit{eff} \qquad \text{(eq. 43)}$$

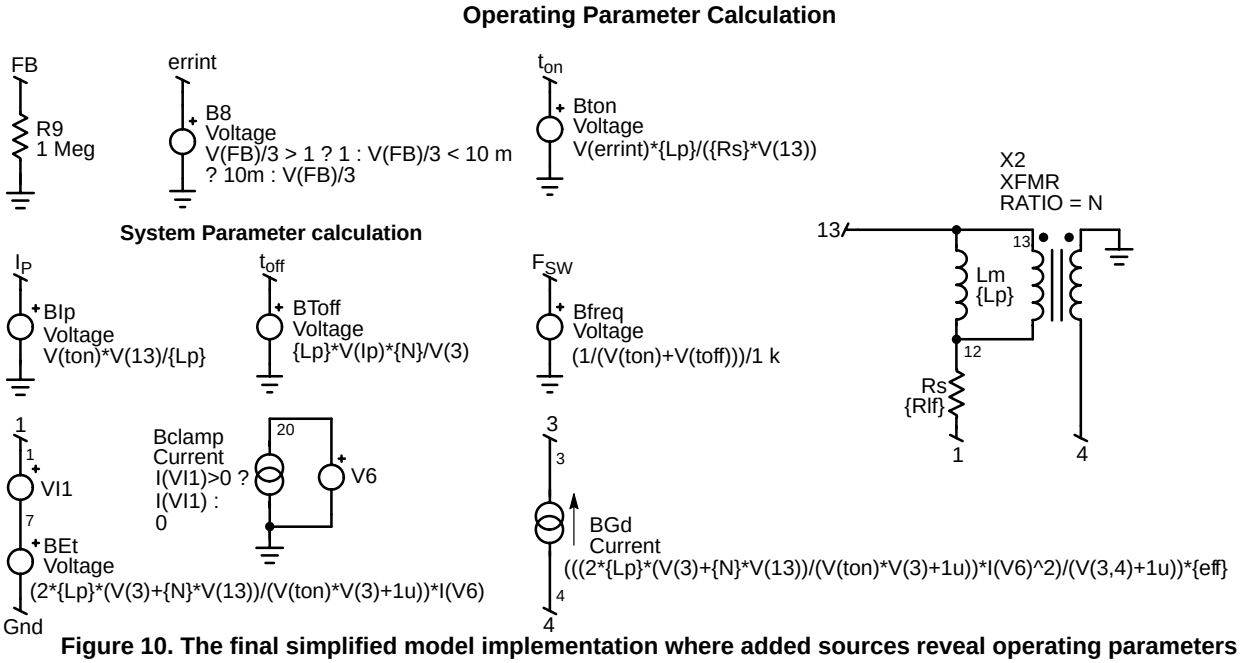

Figure 10. The final simplified model implementation where added sources reveal operating parameters such as T_{on}, F_{SW} and the peak current I_P

Figure 10 portrays the final simplified model subcircuit where all relevant sources appear, among them, the switching frequency, peak current and T_{on} calculations. For the extended model, only BGd and BEt sources need to be changed. As you can see, there are plenty denominator expressions where a variable such as T_{on} appears. If during the bias point calculation SPICE T_{on} starts or goes close to zero, the simulator can fail to converge (or find a wrong bias point which is worse). To avoid this potential problem, a trick consists in inserting a fixed value, small enough like 1 μ or less, to clamp the maximum value the source can take if T_{on} becomes null. To the opposite, the frequency expression modeled by a voltage source can deliver kV to express kilo Hz. The simulator dynamic being bounded, mixing values of a few mV with sources delivering kV can puzzle the bias point calculation. Again, a division by 1000 will limit the range. The FB pin undergoes a division by 3 to be further clamp by a 1 V limiter, a classical circuitry found in most PWM controllers (I_P max = 1 V / R_{sense}).

DC−bias calculation always represents a difficult task for SPICE simulators running averaged models. In order to enhance the extended model robustness (the one including parasitic effects), we have constrained the BGd source to be positive only by using a simple in−line equation that differs depending on the simulator syntax:

IsSpice

```
BGd 4 3 I= ((2*{Lp}/V(ton)) * ( ({N}*V(13)+V(3))/(V(3)+1u) + {DEL}/V(ton) +
+({Lp}*{Ctot}/V(ton))*(1+(V(3)/{N})/V(13)) ) * I(V6)^2)/(V(3,4)+1u)*{EFF} < 10m ? 10m :
+((2*{Lp}/V(ton)) * ( ({N}*V(13)+V(3))/(V(3)+1u) + {DEL}/V(ton) +
+({Lp}*{Ctot}/V(ton))*(1+(V(3)/{N})/V(13)) ) * I(V6)^2)/(V(3,4)+1u)*{EFF}
```

PSpice

```
Gd 4 3 TABLE { ((2*{Lp}/(V(ton)+10n)) * ( ({N}*V(13)+V(3))/(V(3)+1u) + {DEL}/(V(ton)+10n) +
+({Lp}*{Ctot}/(V(ton)+10 n))*(1+(V(3)/{N})/V(13)) )
+ * I(V6)^2)/(V(3,4) + 1u)*{EFF} } ( (10m,10m) (1000,1000) )
```

Finally, the model comes with two different names:

.SUBCKT QuasiFly 13 FB GND 3 I_P T_{on} F_{SW} params: L_P = 3.22 m R_S = 0.5 N = 0.06 eff = 0.86
the simplified model version

QuasiFlyDel 13 FB GND 3 I_P T_{on} F_{SW} params: L_P = 3.22 m R_S = 0.8 N = 0.06 eff = 0.86 C_{tot} = 100 p
the complete model including parasitic effects

Passed parameters are:

C_{tot}, the lump parasitic component present on the drain.
L_P, the primary inductance
R_{lf}, the ohmic losses of the primary winding
N, the N_P : N_S ratio with N_P=1
Eff, the circuit estimated efficiency

Please note that for the sake of simplicity, both models do not account for the secondary rectifier forward drop V_f whose effect is nevertheless negligible in our approach.

Putting the Model to Work

Different ways exist to test the validity of a model. The first one is by using SPICE only, where one can compare the transient response of the averaged model versus that of the equivalent cycle−by−cycle. The other one implies the comparison of the averaged model results versus a real board measurement. In this paper, we will depict both approaches, using our simplified cycle−by−cycle transient model.

The averaged template is depicted by Figure 11 where Figure 10 sources have been pushed into a single graphic symbol. The symbol must be fed by Lp, Efficiency, R_{sense}, transformer turn ratio and the primary inductance ohmic loss. The FB pin goes to a component arrangement particular to the NCP1207 series from ON Semiconductor where the optocoupler collector is internally pulled−up to a reference voltage.

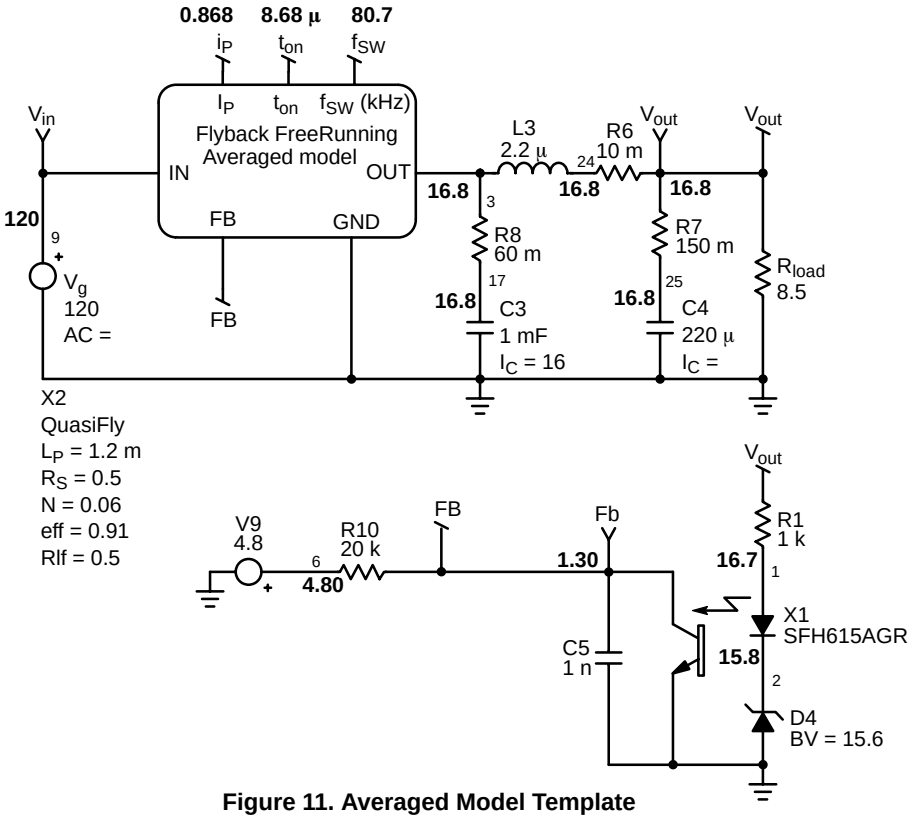

Figure 11. Averaged Model Template

The averaged model template featuring DC bias points which confirms the correct bias point calculation

In Figure 11, once the simulation has been done, DC points are reflected to the schematic and confirm the validity of the original calculation. The feedback loop is made of a simple Zener diode to avoid any long feedback time constants as with a standard TL431. The cycle−by−cycle circuitry uses our simplified QR transient model which emulates a free−running controller such as ON Semiconductor NCP1207 or NCP1205 [3] (Figure 12). The output stage and feedback configuration conforms to Figure 11 in order to compare similar topologies. The first test consists in testing the input audio susceptibility by stepping the input voltage from 200 V to 350 VDC. Figure 13 reveals the good agreement between the averaged response and the cycle−by−cycle one. The next experience will step load the converter output from light to heavy load in a few µs. Figure 14 testifies for the right behavior on both configuration, average or cycle−by−cycle.

On the static point of view, the following data compare numbers given by the averaged model and the cycle−by−cycle one:

I_P AVG = 868 mA / I_P TRAN = 858 mA

T_{on} AVG = 8.68 µs / T_{on} TRAN = 8.78 µs

F_{SW} AVG = 80.7 kHz / F_{SW} AVG = 77.8 kHz

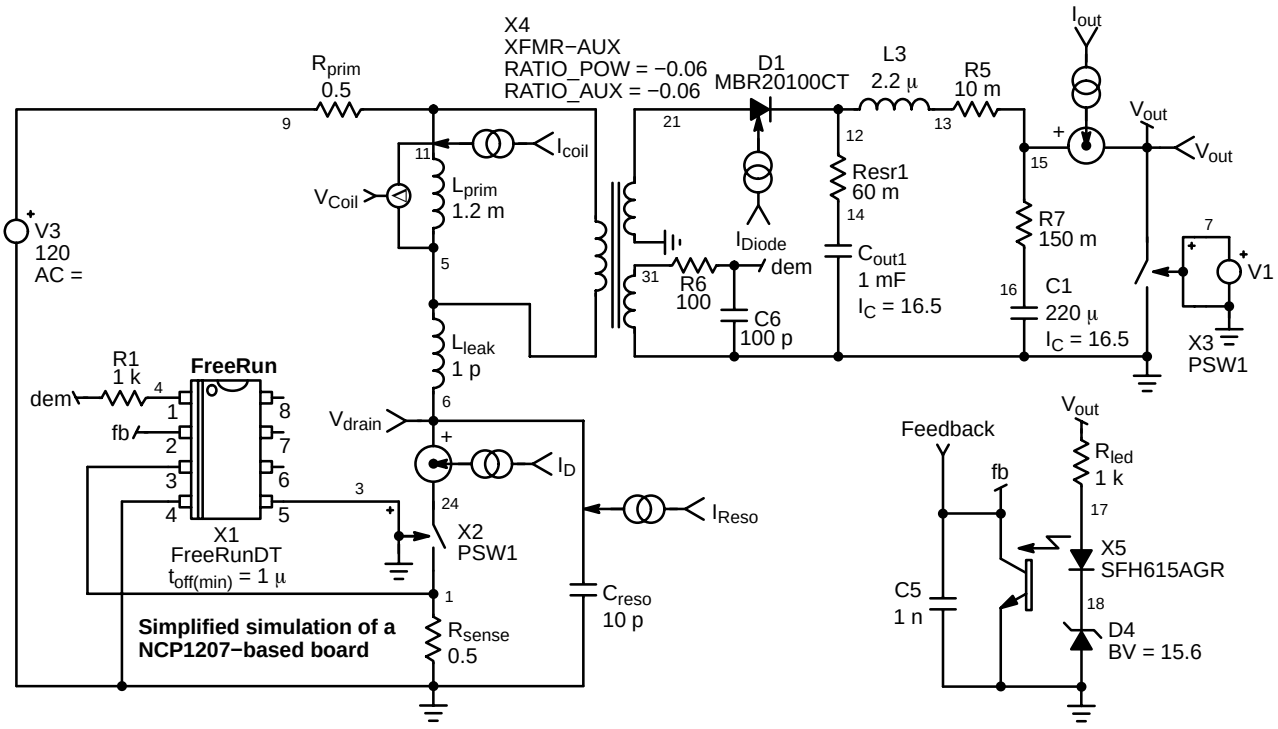

Figure 12. This Simplified Transient Model Will Help to Check the Averaged Results

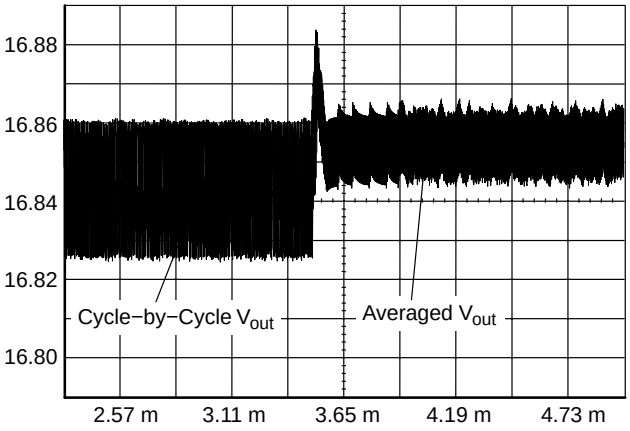

Figure 13. Audio Susceptibility with a Line Step (200 to 350 V)…

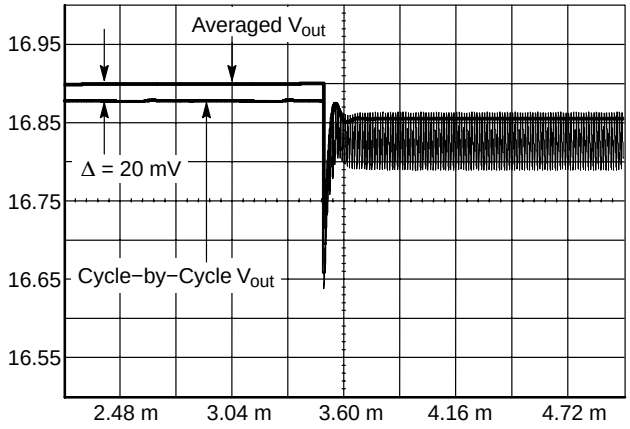

Figure 14. … and Load Step Response Comparison Between Models (50 Ω to 0.5 Ω)

Real World Confrontation

Even if the above paragraph gives us the assumption that our model sticks to reality quite well, nothing replaces a real board measurement with a network analyzer. However, on the NCP1207, the collector of the optocoupler is directly internally pulled−up to a reference via a resistor, it thus becomes difficult to open the loop via the series transformer method. We thus went back to a simple open−loop configuration where a DC source fixes the expected operating point. It does not cause any problem in our case since the overall gain $V_{control}$ to V_{out} is low. The AC injection is then made via a 1000 µF capacitor. Figure 15 depicts the adopted configuration on the bench, but also replicated on the averaged model.

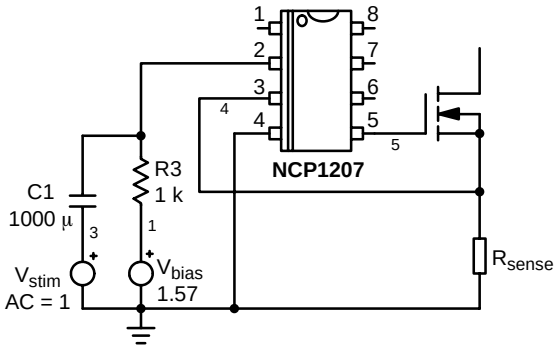

Figure 15.

The AC measurement is obtained once the proper operating point is reached by adjusting V_{bias}. The gain being low, there is no problem of output runaway as long as V_{bias} is slowly increased.

The bandwidth measurement has been carried on a board further to a 15 mn warm−up. This board does not use any clamping network but a 800 V MOSFET instead and a large capacitor connected between drain and ground Figure 16 and 17 compare the obtained results with the averaged model including valley and turn−off delays:

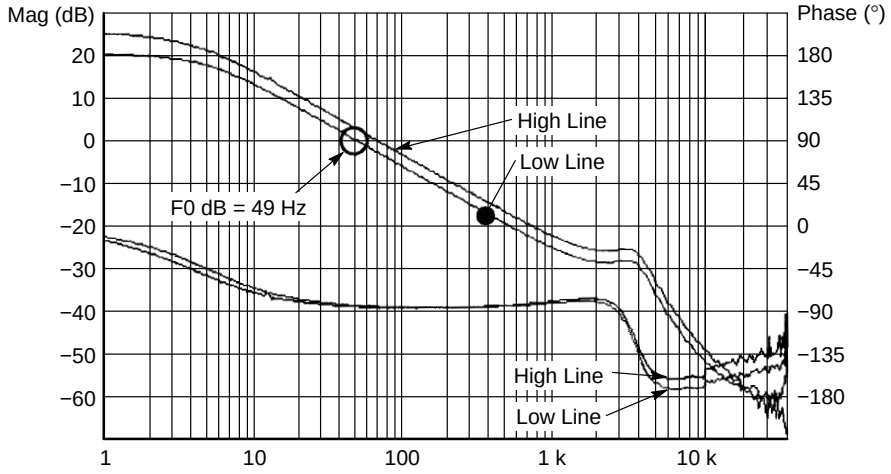

Figure 16. Bode Plot Captured with a Network Analyzer

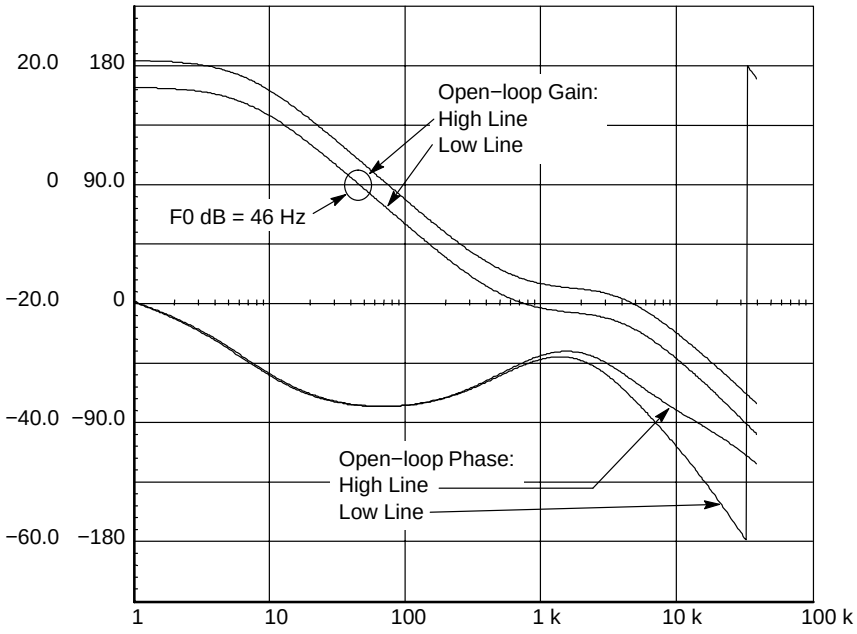

Figure 17. Bode Plot Obtained with the Averaged Model

One can detect a slight gain difference (around 3.5 dB) in DC but the overall simulated shape stays in good agreement with the real measurement. The phase dips are imputed to the presence of the LC network whose cut−off frequency obviously affects the results. The small−signal analysis details are available in [5].

Finally, a step−load response was performed on a real board fed back by a TL−431 network and compared to our SPICE model, also implementing the same control loop structure. Results prove that the proposed model accuracy is acceptable to predict board stability and final transient response:

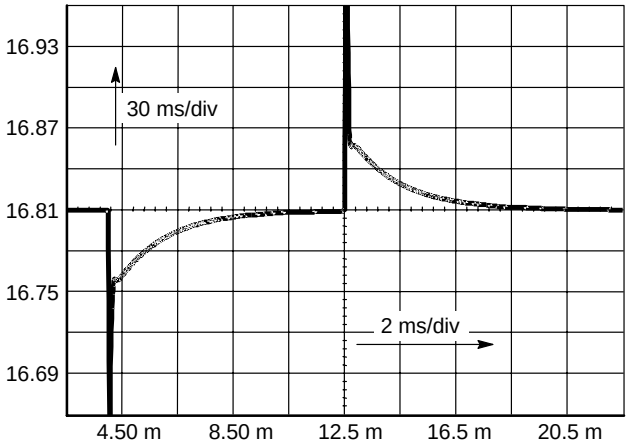

Figure 18. The Simulated Step−Load Response On a TL431−based Feedback Loop…

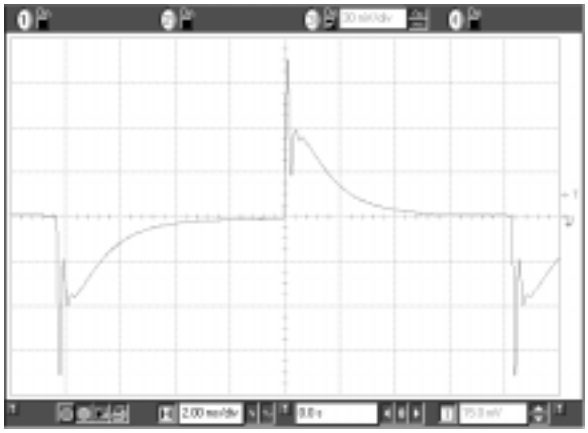

Figure 19. …**versus Real Board Oscilloscope Shot**

Conclusion

A SPICE model dedicated to the AC analysis of free−running topologies was missing. The simple model presented in this article shows that loop stabilization of QR converters becomes easy thanks to the simulation. Furthermore, the good agreement between simulated results and hardware measurements will surely diminish the prototype development time. As usual, the application templates of the paper examples are available to download from the author's website [5] in both Intusoft's IsSpice and OrCAD's PSpice.

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