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AND8104/D

MicroIntegration Technology Solutions for Protection in High Speed I/O Data Lines

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

Static electricity conditions (ESD) can cause catastrophic damage to I/O ports, IC malfunction, and worst of all, ghost data bits in electronic systems. When product damage or product malfunction results in a “Hard failure” or destroyed component, it is easy to isolate and replace the failed component and put the system back in service, however, if a “soft failure” occurs (CMOS component degraded), the system anomaly is not detected in retesting, and hours are wasted in troubleshooting because the system continues to produce irregular data bits. Such failures have a very negative impact in the final product because they increase the cost of warranty repairs and diminish the perception of the product’s quality.

These days, our modern society has rapidly come to fully depend on electronics. And modern computers are based increasingly on low power logic chips, all with ESD sensitivity due to MOS dielectric breakdowns and bipolar reverse junction current limits. The ICs that control I/O ports (USB, Ethernet, etc.) are not an exception since the majority of them are designed and manufactured based on CMOS processes which make them extremely sensitive to damage from ESD conditions. Because the majority of I/O ports are hot insertion and removal systems, they are extremely vulnerable to receive ESD conditions possibly generated by the users or by air discharges. Users can induce ESD conditions while plugging or unplugging any cables, and air discharges can happen a few inches away from the conducting surface.

In addition to all the previous problems caused by static discharge conditions in unprotected ICs, ESD protection now is becoming a strong requirement mainly in the European market, which causes the manufacturers to be barred from selling in this market unless their product/equipment meets the minimum levels of ESD performance. *For all these reasons, engineers and designers must fully understand ESD, which means to be aware of industry standards, testing methods, voltage and current waveforms, application circuits, and selection of the right devices for the protection required in each particular application.*

Electrostatic Discharge Generation

When two insulating materials are rubbed together, an electric charge builds up between them (as electrons are stripped off one surface and deposited on the other surface). The surface with the excess of electrons becomes negatively charged, and the surface with the shortage of electrons becomes positively charged. This effect is known as the “triboelectric” effect (the action of rubbing). Electrostatic voltage is then a function of the separation of the materials in the series, the intimacy of contact, and the rate of separation. Therefore, any time there are two nonconductive materials flowing in opposition to each other, an electrostatic voltage will be generated. The level of electrostatic potential generated depends on the relative charge affinity between materials, the humidity, and other factors.

Test Methods for ESD

Two test methods are the most common standards used to test the ESD susceptibility of integrated circuits. These two methods are the “Human Body Model (HBM)” and the “Machine Model (MM)”.

JEDEC developed standards of ESD testing for both the Human Body Model and Machine Model. These standards were reviewed and approved by the EIA general counsel.

JEDEC Standard JESD22−A114−B,
Electrostatic Discharge (ESD) Sensitivity Testing
Human Body Model (HBM)

This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed.

The Human Body Model test method simulates the typical capacitance and source impedance of a human body. The resulting current waveform represents the ESD that occurs when a person touches objects, such as ICs.

The equivalent circuit for the HBM ESD is shown in Figure 1, it is basically composed by a high voltage supply, and an RC network.

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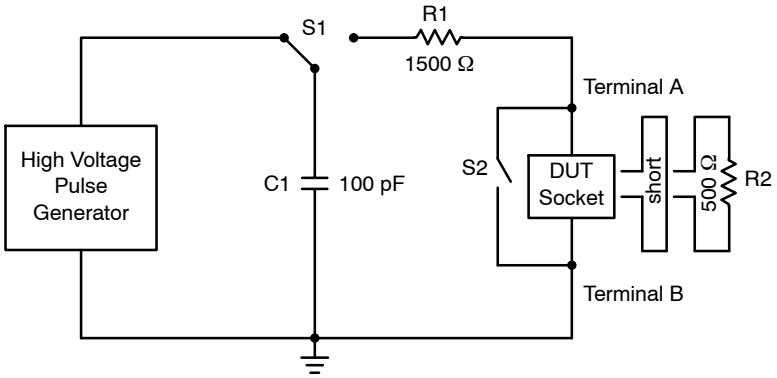


Figure 1. Simplified Test Circuit of HBM

The current waveforms generated by this circuit are shown in Figures 2, 3, 4 and 5:

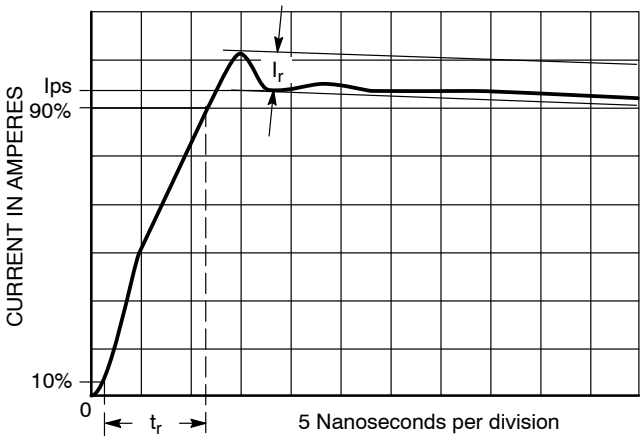


Figure 2. Pulse Rise Time (t_r)

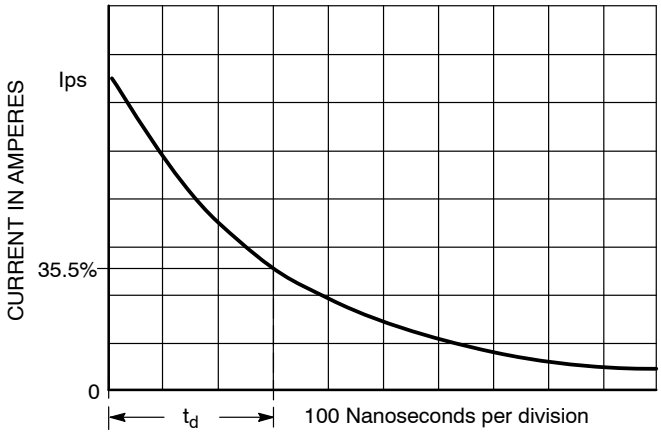


Figure 3. Pulse Decay Time (t_d)

NOTE: Current waveforms generated through a shorting wire.

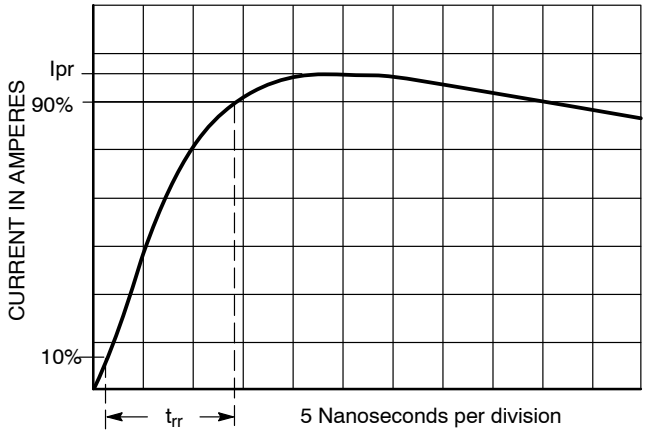


Figure 4. Rise Time (t_{rr})

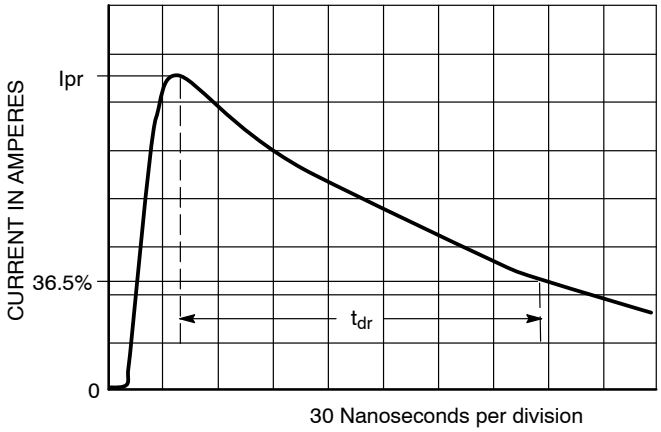


Figure 5. Decay Time (t_{dr})

NOTE: Current waveforms generated through a 500 Ω resistor.

The classification criteria is based on the failure point of the parts tested. Table 1 shows the criteria of the JEDEC standard for HBM:

Table 1. HBM ESD Ratings

JEDEC Ratings

HBM Rating	Conditions
Class 0	Failure < 250 V
Class 1A	250 V < = Failure < 500 V
Class 1B	500 V < = Failure < 1000 V
Class 1C	1000 V < = Failure < 2000 V
Class 2	2000 V < = Failure < 4000 V
Class 3A	4000 V < = Failure < 8000 V
Class 3B	Failure = > 8000 V

JEDEC Standard EIA/JESD22−A115−A, Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate classifications can be performed. The machine model test method generates a current waveform similar to the one produced when an IC makes contact with its handling machinery. This waveform simulates static discharges seen during machine assembly.

The equivalent circuit for the MM ESD is shown in Figure 6:

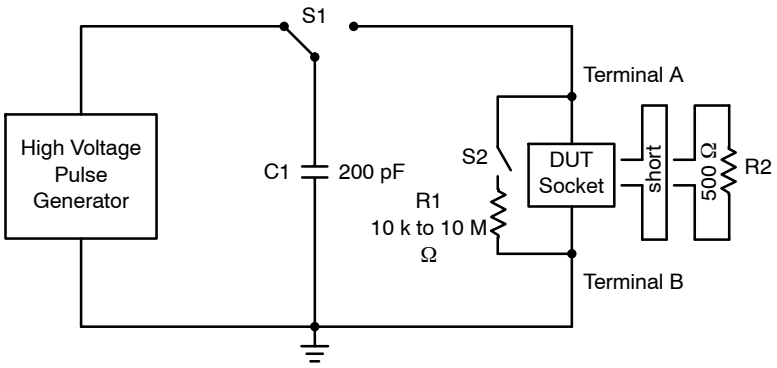


Figure 6.

The current waveforms generated by this circuit are shown in Figures 7 and 8:

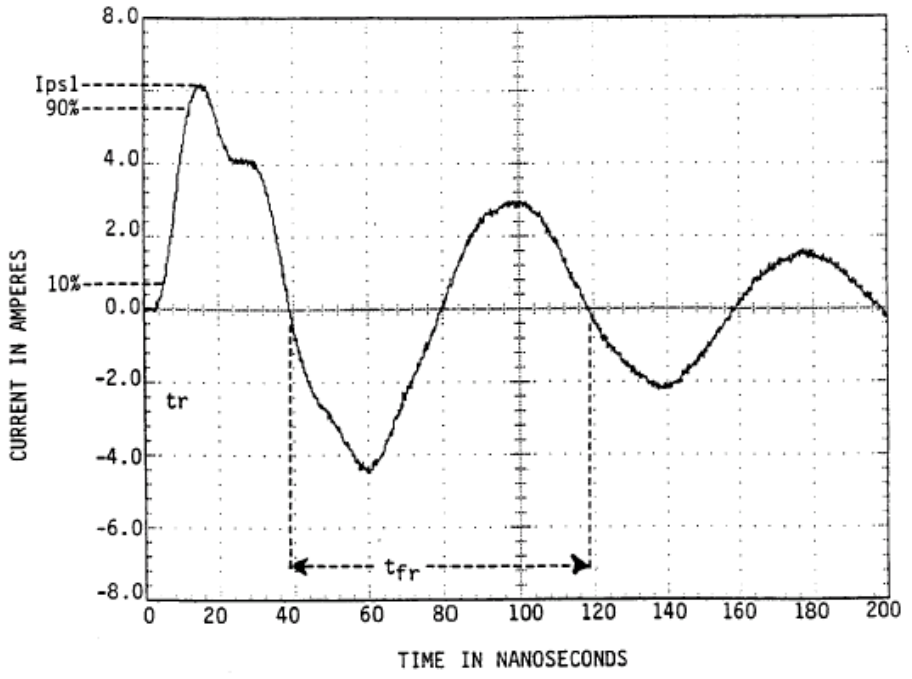


Figure 7. Current Waveform Through a Shorting Wire (400 V Discharge)

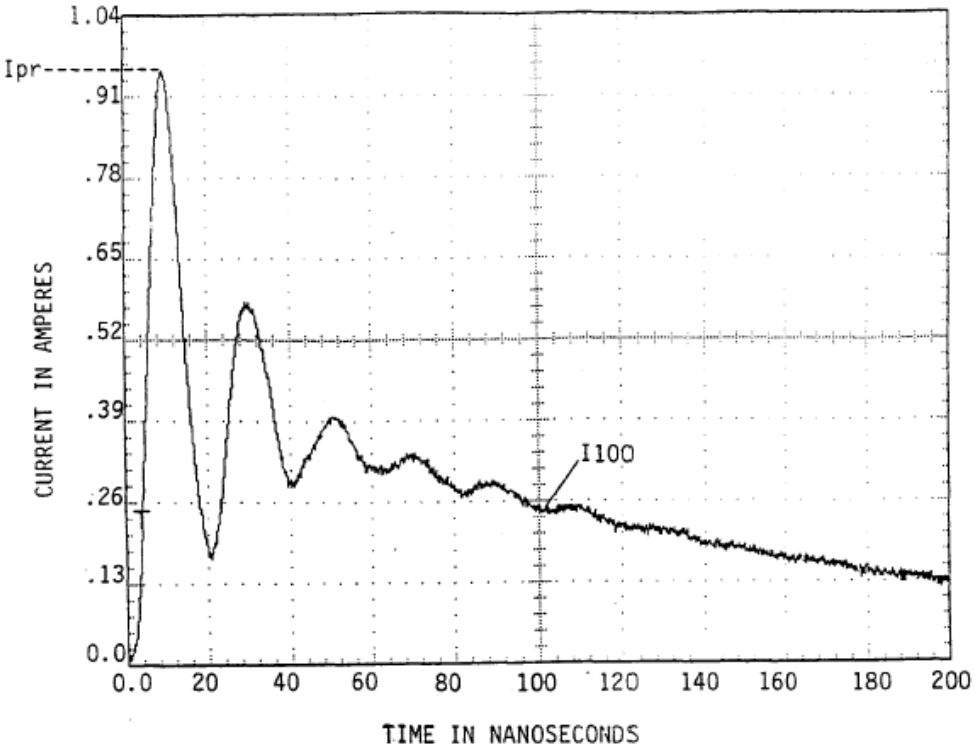


Figure 8. Current Waveform Through a 500 Ω Resistor (400 V Discharge)

The classification criteria is based on the failure point of the parts tested. Table 2 shows the criteria of the JEDEC standard for MM:

Table 2. MM ESD Ratings

JEDEC Ratings

MM Rating	Conditions
Class A	Failure < 200 V
Class B	200 V < = Failure < 400 V
Class C	Failure = > 400 V

Both the HBM and MM methods are complementary tests, therefore designers and engineers should not choose one over the other. Because electrostatic discharge can damage ICs during manufacturing, assembly, and after the end product is put in operation, a test based on either the human body model and the machine model together provides adequate assurance on the IC's tolerance for the processes of manufacturing and insertion.

IEC 61000−4−2, ESD International Standard

The IEC 61000−4−2 International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to static electricity discharges, from operators directly, and to adjacent objects. It additionally defines ranges of test levels which relate to different environmental and installation conditions and establishes test procedures. The object of this standard is to establish a common and reproducible basis for evaluating the performance of electrical and electronic equipment when subjected to electrostatic discharges. In addition, it includes electrostatic discharges which may occur from personnel to objects near vital equipment.

This method is recommended for testing ICs that include I/O pins. It was originally intended as an acceptance condition for end products to be sold in the European market, however it is now gaining acceptance in USA and Japan markets as well.

The IEC 61000−4−2 model is similar to the HBM circuit, but with different component values. It includes a resistance of 330 Ω that represents a human holding a certain metallic object such as screwdriver, and a capacitor of 150 pf that represents another estimation of human body capacitance.

The equivalent circuit for the IEC 61000−4−2 ESD is shown in Figure 9 and the current waveform generated is shown in Figure 10:

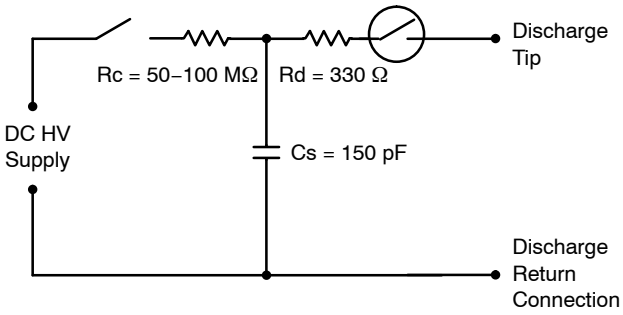


Figure 9. Simplified Test Circuit of IEC 61000−4−2

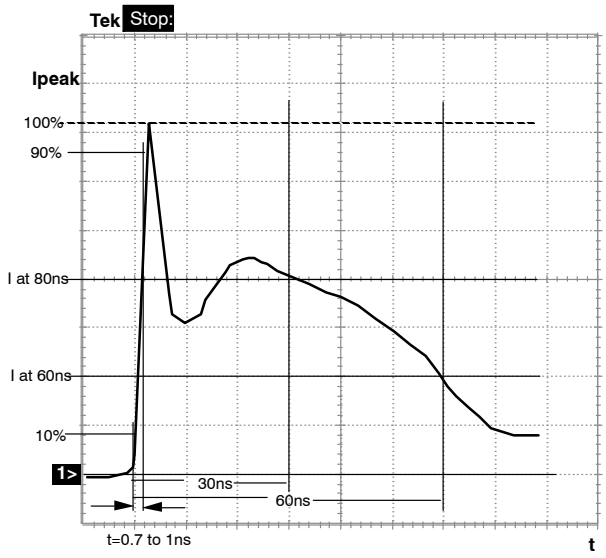


Figure 10. IEC 61000−4−2 Current Waveform

The IEC 61000−4−2 specification defines four test levels of compliance based in the maximum voltage supported by the ICs. These test levels are described in Table 3:

Table 3. IEC 61000−4−2 ESD Levels

Level Ratings

Level	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)	First Peak Current (Amp)	Peak Current at 30 ns (Amp)	Peak Current at 60 ns (Amp)
1	2	2	7.5	4	8
2	4	4	15	8	4
3	6	8	22.5	12	6
4	8	15	30	16	8

ESD Protection for High Speed I/O Data Lines

Protection for ESD requires engineers and designers to add external protection devices or select robust ICs with a certain level of protection built in. Having ICs with some sort of protection built in sometimes is not entirely convenient since the ICs must absorb the power created by the ESD conditions which may cause problems in the IC's functionality or reduce its efficiency. Therefore, external protection devices are the ideal case to keep the ESD conditions and their secondary effects away from the ICs.

ESD protection for high speed I/O data lines not only implicates compliance with the ESD industrial standards previously explained, but it also implicates the usage of very sophisticated devices capable to operate under conditions of high speed data transmission and the high technology of the IC controllers, so conventional methods using discrete devices would be obsolete and non−efficient to protect high speed I/O data lines. Some of the key characteristics that ESD protection devices intended for high speed I/O data lines must have are listed below:

- Low capacitance (< 5.0 pf) to minimize the signal attenuation at high speed data rate (such as 480 Mbs for USB 2.0)
- Fast time operation response (nanosecond) to protect the ICs against the fast rise time of the ESD pulses
- Low leakage current to minimize the power consumption under normal operation conditions
- Robustness to drive and absorb repetitive ESD conditions without damage
- Integrated and reduced package

Non−Semiconductor Protection Devices

There are some protection circuits that include non−semiconductor devices such as metal−oxide varistors or pulse guard suppressors (polymer composite materials), those type of devices sometimes do not offer a very reliable protection and have some disadvantages. Varistors usually are degraded each time they are activated, which makes it very difficult to identify the total damage. On the other hand, pulse guard suppressors normally specify high clamping voltage (100 V or more), and high triggering voltage (1.0 kV or more), which reduces tremendously their effectiveness for suppressing ESD conditions. Figure 11 shows the response of a pulse guard suppressor device when it is zapped with 8.0 kV of HBM ESD pulse:

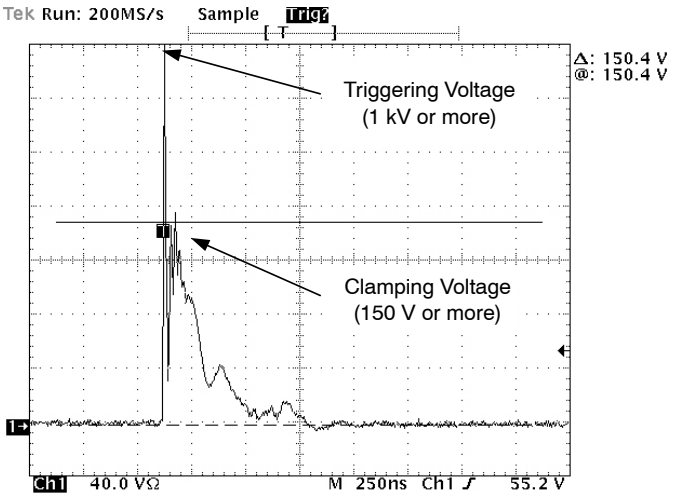


Figure 11. Typical Clamping Voltage of Non−Semiconductor Devices (Pulse Guard Suppressor)

As shown in Figure 11, the resulting clamping voltage of the pulse guard suppressor non−semiconductor device is around 150 V, which may be too high for the IC that is controlling the protected I/O line, therefore the risk of damaging the IC is still there.

ON Semiconductor's MicroIntegration Protection Devices

ON Semiconductor offers different solutions for ESD and surge protection in high speed I/O data lines. These solutions are based on two main semiconductor technologies: steering diodes and transient voltage suppressor devices (TVS). These two technologies can be combined to achieve reliable protection for different configurations, and for different applications needs.

As previously mentioned, ESD protection in high speed I/O data lines requires special device's characteristics to achieve proper and effective protection. Although both technologies can be used to protect high speed I/O data lines, there are certain things that have to be considered before selecting the protection devices.

The NUP4201DR2 device for example is an integrated TVS−Diode array intended to protect four high speed I/O data lines and the power line. It can be used for protection in USB 2.0 applications or any other high speed I/O data line applications. The typical schematic diagram for USB 2.0 applications is shown in Figure 12:

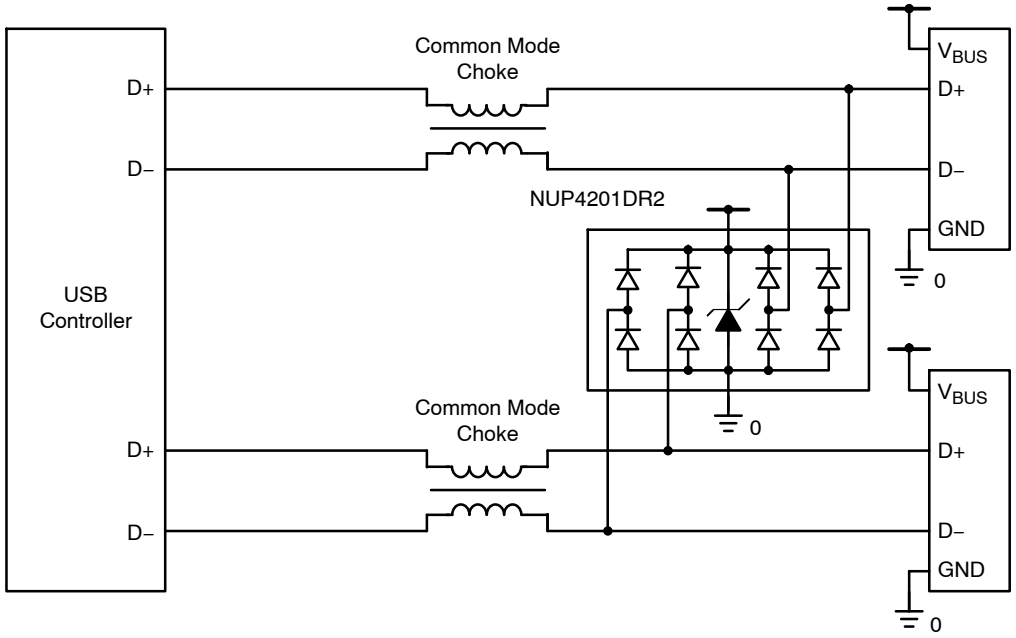


Figure 12. Typical Application Scheme for USB 2.0 Port Protection

As shown in the schematic, the steering diodes protect the four I/O data lines of the two USB ports while the TVS protects the general VBUS power line. If ESD occurs in any of the four data lines, the steering diodes are forward biased driving those conditions away from the protected IC. The integrated TVS will drive the resulting voltage spike to ground. If ESD occurs in the power line, the TVS device will also suppress that condition to ground.

Figure 13 shows the response of the integrated steering diodes when they are zapped with 8.0 kV of HBM ESD positive pulse, and Figure 14 shows the response of the integrated TVS when it is zapped with the same condition:

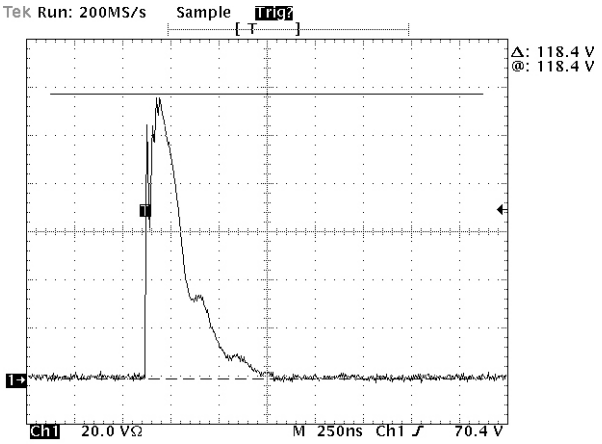


Figure 13. Typical Vf Behavior of Steering Diodes When Applied HBM ESD Pulse

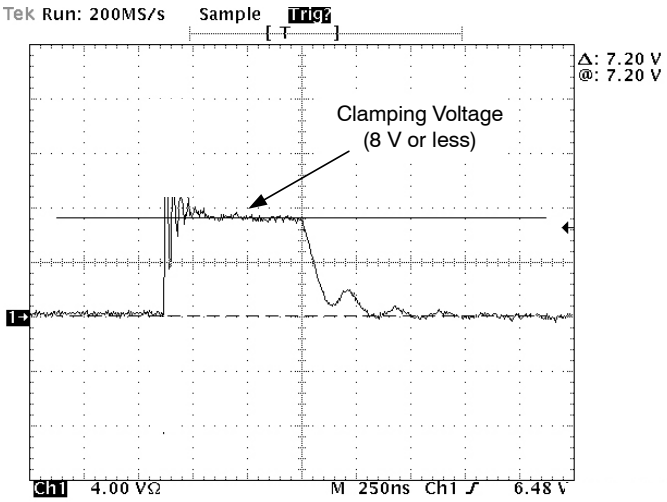


Figure 14. Typical Clamping Voltage of TVS Technology When Applied HBM ESD Pulse

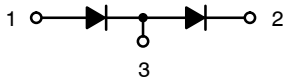
As shown in Figure 13, the steering diodes reduce the voltage amplitude of the ESD condition from 8.0 kV to 120 V approximately, and then they drive this reduced voltage to the integrated TVS device keeping away the ESD conditions from the I/O lines of the ICs. The integrated TVS will drive this reduced voltage condition to ground. If only integrated steering diodes are used, then the reduced voltage is driven to the positive polarity of the power line. The power line normally has big capacitors connected to ground which will absorb this reduced voltage condition until total elimination.

On the other hand, Figure 14 shows the clamping voltage of the integrated TVS when a 8.0 kV HBM ESD pulse occurs in the power line. As shown in this figure, the TVS suppresses the ESD condition from 8.0 kV to 7.0 V approximately, which demonstrates by itself the superiority of the semiconductor technology over the non–semiconductor devices.

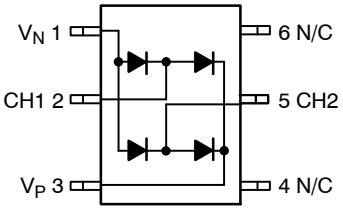
The two previous plots basically show the typical performance of the two more traditional semiconductor technologies used for ESD protection. Although different combinations of TVS devices and steering diodes can be made, the performance expected for ESD suppression should be similar.

ON Semiconductor MicroIntegration technology offers several protection solutions for different application circuits and needs. The most common configurations are described as follows:

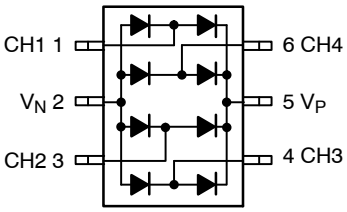
– Low capacitance diode arrays for ESD protection in high speed I/O data lines only:



NUP1301
- One I/O Line
- SOT−23 Package
- ***Available Q1/2003***

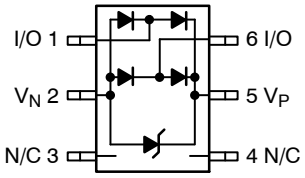


NUP2301MR6T1
- Two I/O Lines
- SC−88 Package
- ***Available Q1/2003***

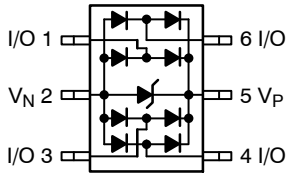


NUP4301MR6T1
- Four I/O Lines
- TSOP−6 Package
- ***Available Q1/2003***

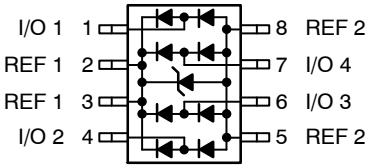
– Low capacitance TVS − Diode arrays for ESD protection in high speed I/O data lines, and power line:



NUP2201MR6T1
- Two I/O Lines and Power Line
- TSOP−6 Package
- ***Available Q1/2003***

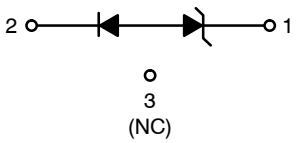


NUP4201MR6T1
- Four I/O Lines and Power Line
- TSOP−6 Package
- ***Available Q1/2003***



NUP4201DR2
- Four I/O Lines and Power Line
- SO−8 Package
- ***Available Now***

– Low capacitance TVS for ESD protection in I/O data lines:



SL05T1
- One I/O Line
- SOT−23 Package
- ***Available Now***

All the previous ON Semiconductor devices are low capacitance solutions that provide very effective ESD protection in high speed I/O data lines. They all are designed and manufactured under the same MicroIntegration technology base, which guarantees their effectiveness and reliability of operation.

But effective ESD protection not only depends on the type of devices used, it also depends on the quality of the board layout. Inadequate layout increases the parasitic impedances which results in the creation of significant negative effects from the L(di/dt) phenomena. ESD waveforms are characterized by their fast rise times, so circuit board traces must not add additional inductance because they are also part of the protection loop.

Some techniques can be used to optimize the ESD protection:

- Locate the protection devices as close to the I/O connector as possible
- Minimize the PCB trace lengths to the protection devices
- Minimize the PCB trace lengths for the ground return
- Minimize the inductance and capacitance of the traces

Typical Applications Schemes for ESD Protection in High Speed I/O Lines

Video Interface Protection

Video interfaces are hot plugging/unplugging systems that are susceptible to receive electrostatic discharges (ESD) from users or air. These conditions can damage or even destroy the IC of the video interface if it is not protected. Because video interfaces are high speed data rate applications, it is necessary to use protection devices with extremely low capacitance and low leakage current so that the integrity of the video signal is not affected. In addition, protection devices must also offer the proper ESD ratings to cover the most common ESD industry standards (IEC 61000−4−2, HBM class 3B and MM class C). The NUP4301MR6T1 device is designed to provide ESD protection in this type of applications. Figure 15 shows the typical applications scheme.

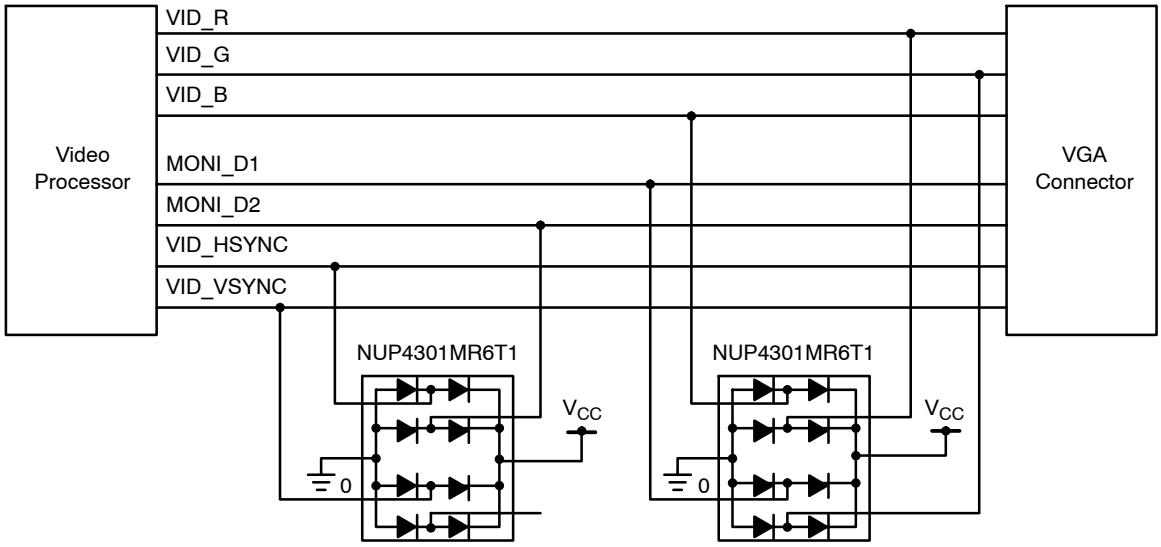


Figure 15.

I/O Port Protection in Microcontroller Applications

ESD protection in I/O ports of microcontrollers is extremely important to avoid damage or malfunction in the total control system. ESD conditions can cause hard or soft failures in microcontrollers, resulting in hours wasted in troubleshooting because the system continues to produce irregular data bits, therefore protection devices is a MUST. Protection devices must offer the proper ESD ratings to cover the most common ESD industry standards (IEC 61000−4−2, HBM class 3B and MM class C). The NUP2301MR6T1 device is designed to provide ESD protection for two I/O ports. Figure 16 shows a typical applications scheme for I/O port protection in Microcontrollers circuits.

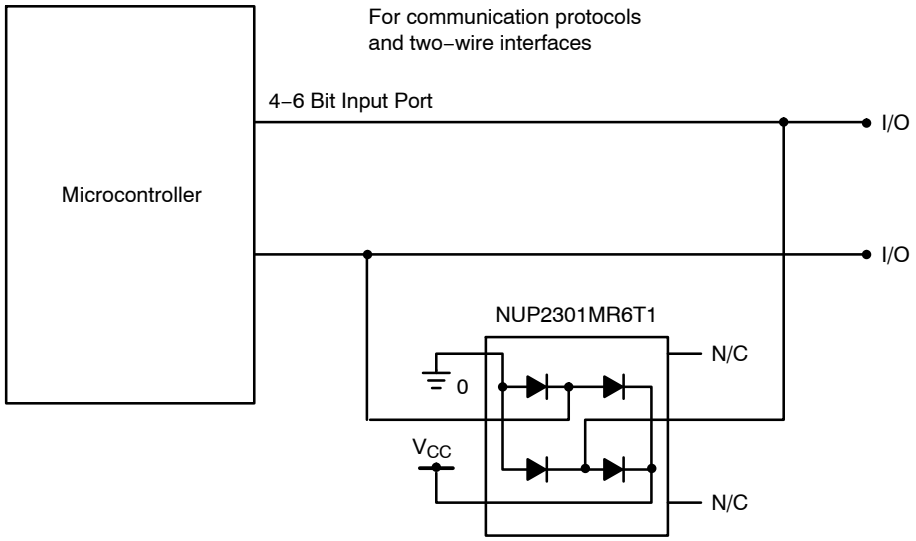


Figure 16. I/O Port Protection in Microcontrollers Applications

10 / 100 Ethernet Protection

Ethernet IC's are also susceptible to electrostatic discharges that can cause damage to them. Although the Ethernet chip may have some sort of integrated protection, it is unlikely that it can cover the ESD ratings specified by the international standard IEC 61000−4−2. Depending on the magnitude of the electrostatic discharge, it can cause hard or soft failures in the IC which will result in the malfunction of the system.

Ethernet is a local area network technology that transmits information between computers at speeds of 10 and 100 Mbps. Currently the most widely used version of Ethernet technology is the 10−Mbps twisted−pair variety.

The 10−Mbps Ethernet media varieties include the original thick coaxial system, as well as thin coaxial, twisted−pair, and fiber optic systems. The most recent Ethernet standard defines the new 100−Mbps Fast Ethernet system which operates over twisted−pair and fiber optic media.

For the most typical Ethernet system, a twisted−pair consists of two differential signal pairs, one pair is for the transmitter and the other for the receiver. Electrostatic discharges can appear across the line pairs of the transmitter or receiver, which are induced to the Ethernet chip through the coupling of the transformer. Figure 17 shows a typical application scheme for protection in Ethernet applications, the protection is provided in differential mode.

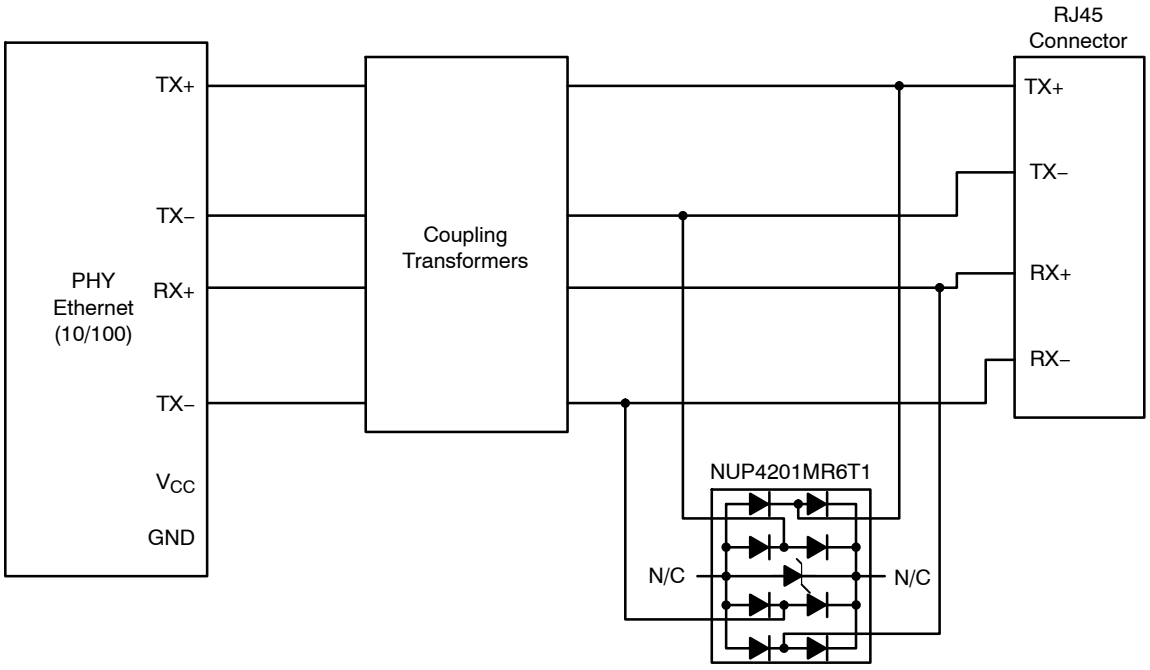


Figure 17. Protection for Ethernet 10/100 (Differential Mode)

Protection for USB Ports

ESD Protection in USB applications requires the usage of very sophisticated semiconductor devices capable to operate under conditions of high speed data transmission and the high technology of the USB controller, so conventional discrete methods to protect serial ports would be obsolete and non–efficient for USB applications. The NUP4201MR6T1 and NUP2201MR6T1 devices provide unique integrated Low Capacitance TVS Diode Arrays designed to protect multiple four or two I/O lines, and also the power supply line against damage due to ESD conditions or transient voltage conditions. Figure 18 shows a typical applications scheme for USB protection.

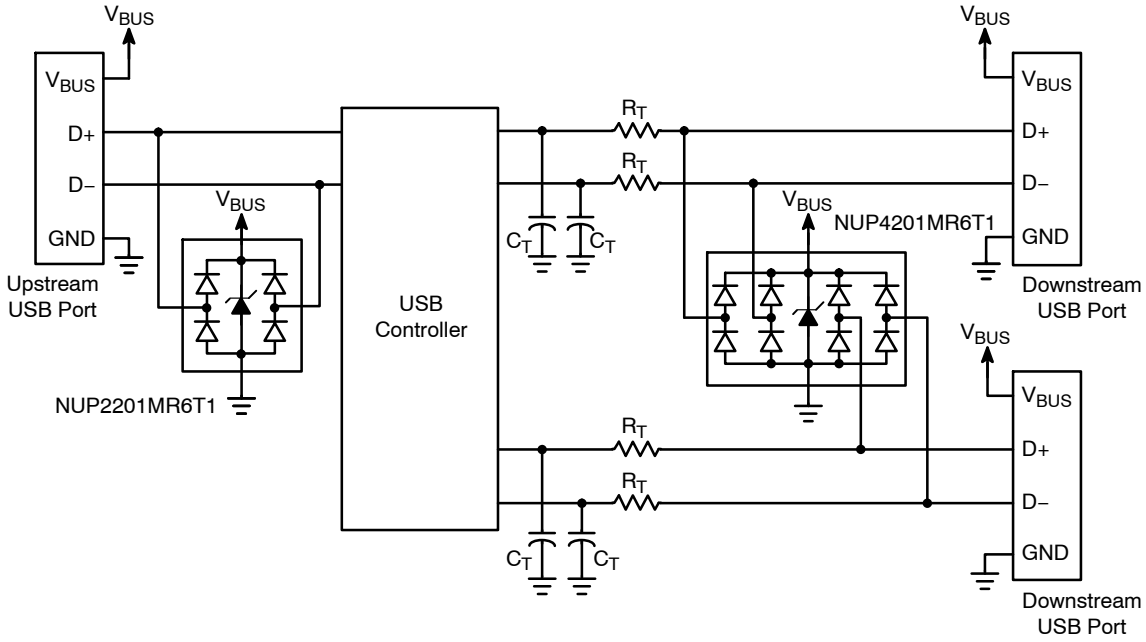


Figure 18. Protection for USB Ports

Bibliography

1. International Standards IEC 61000−4−2.
2. JEDEC standards JESD22−A114−B and JESD22−A115−A.
3. Article about ESD Considerations for Electronic Manufacturing by Donald E. Frank, 1996.
4. ON Semiconductor Application Note number AND8026/D.
5. Radio Electronics Article about Electrostatic discharge by David Hollander, 1990.

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