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AND8026/D

Solving EMI and ESD Problems with Integrated Passive Device Low Pass Pi Filters

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Background

The demand of cost sensitive portable products such as cellular telephones has resulted in the development of the ON Semiconductor NZMM7V0T4 Integrated Passive Device (IPD) EMI filter with ESD protection. This integrated filter array is used to replace low pass filters that have been implemented with discrete resistors, capacitors, and zener diodes. The filters, as shown in Figures 1, 2 and 3, use the capacitance of a zener diode to form a resistor/capacitor (RC) low pass Pi filter. An IPD IC will reduce the component count and the required printed circuit board space. Also, this filter solution offers the advantage that it is manufactured using standard integrated circuit manufacturing processes to achieve a low cost solution in a small IC package.

The NZMM7V0T4 multiple channel filter array, as shown in Figure 5, is the first member of a new family of IPD EMI filters that will include single, dual, and multiple filter arrays with various cut–off frequencies (f_{-3dB}). The NZMM7V0T4 was developed to protect cellular telephone I/O connectors; however, this IC can provide a low cost EMI and ESD filter solution for a wide range of applications. The ON Semiconductor family of IPD EMI filters also consists of a single and a dual channel filter. The NZF220TT1 is the single channel device and is available in a three pin SC–75 package. The NZF220DFT1 is the dual channel device and is available in a five pin SC–88A package. Both the single and the dual channel devices are functionally identical to the nine channel NZMM7V0T4 filter array.

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APPLICATION NOTE

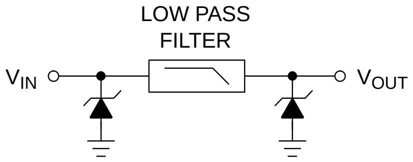

Figure 1. Functional Schematic Representation of the NZMM7V0T4

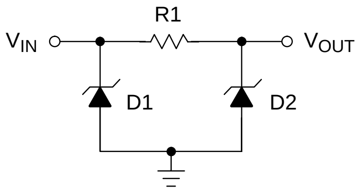

Figure 2. NZMM7V0T4 Filter Channel

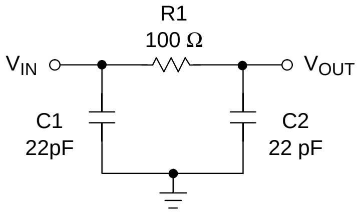

Figure 3. NZMM7V0T4 Filter Channel – Equivalent Circuit

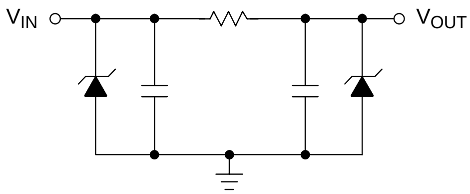

Figure 4. Equivalent Discrete Pi Filter

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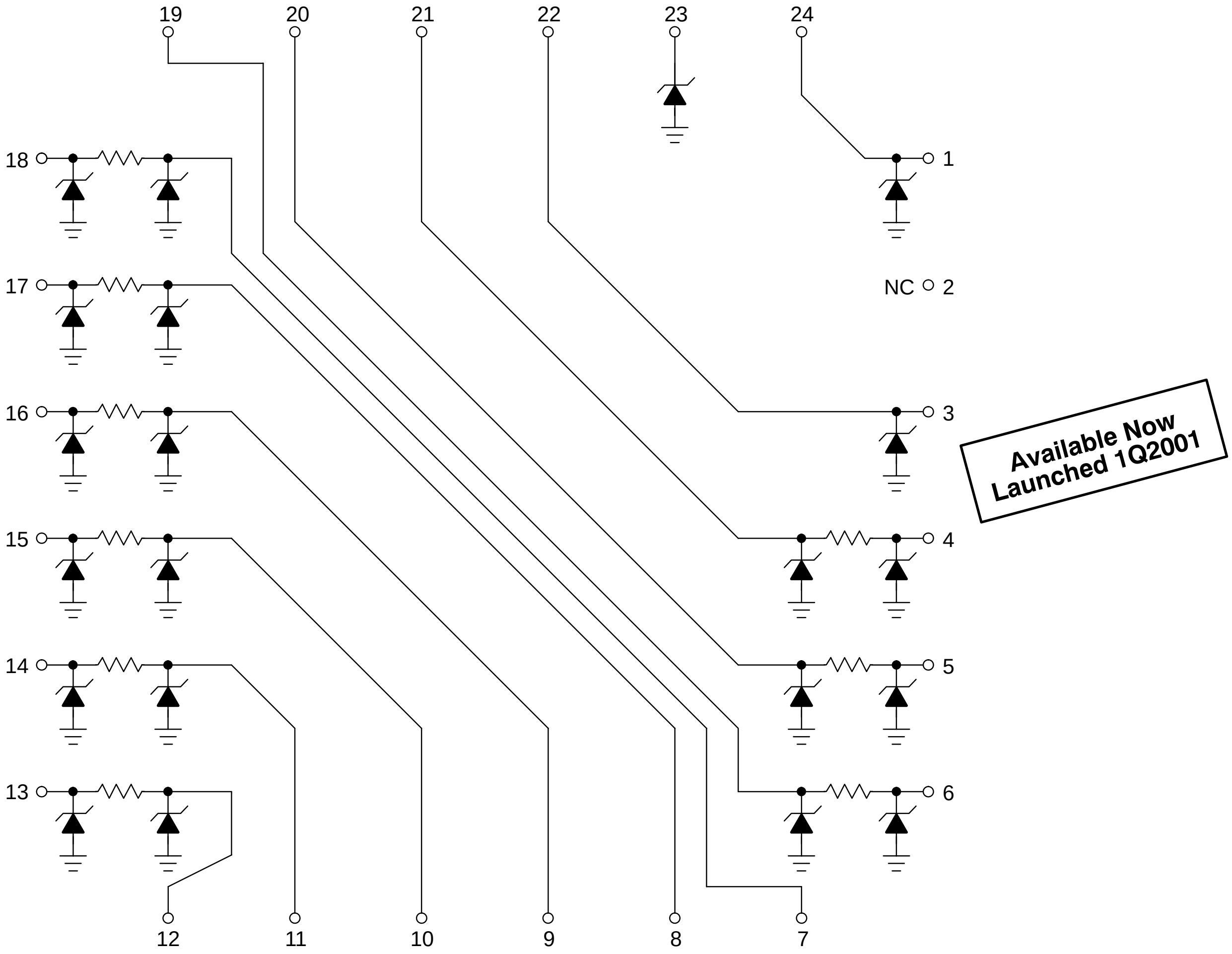

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Figure 5. NZMM7V0T4 Device Schematic

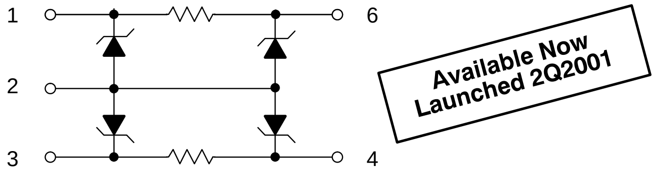

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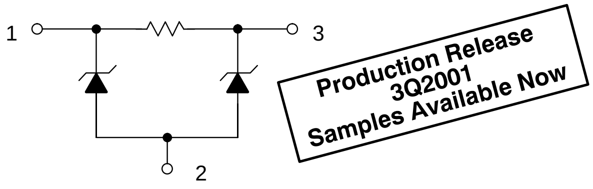
Figure 6. NZF220DFT1 Device Schematic



Production Release
3Q2001
Samples Available Now

Figure 7. NZF220TT1 Device Schematic

Functional Description

The NZMM7V0T4 contains nine low pass filter channels and three separate zener diodes. The low pass filters are formed by a 100 ohm resistor and two zener diodes that function as 22 pF capacitors. The resulting Pi filter configuration attenuates noise signals that are both entering and exiting the filter network. Components R1 and C2 form a filter that attenuates the high frequency signals entering the network via the I/O cable, while R1 and C1 attenuates the high frequency noise that is exiting the network. The RC Pi filters are first order filters with a frequency attenuation roll–off of –20 dB/decade.

The NZMM7V0T4 also provides ESD protection by clamping any high input voltage to a non–destructive voltage level that is equal to the zener voltage of the diode. In contrast, a RC filter will limit the slew rate of the transient voltage waveform, but will not clamp the ESD voltage to a safe voltage level unless external zener diodes are added to the filter configuration. The NZMM7V0T4's Pi filters are an ideal configuration to provide ESD protection because two zener diodes are used in the circuit. This configuration results in a clamping voltage that is equal to the zener breakdown voltage.

The NZMM7V0T4's three separate zener diodes have a capacitance of 8 pF and a zener breakdown voltage of 7 V. These diodes can be used for a variety of applications, including the protection of USB or RS232 serial ports.

The NZMM7V0T4 IPD is an ideal EMI/ESD solution for portable cost sensitive applications. Each filter channel in the IPD can replace the equivalent discrete component filter shown in Figure 4 that requires one resistor, two capacitors and two zener diodes. Note the discrete filter requires the two zener diodes to provide the ESD protection and to protect the capacitor on the input side of the filter from an over–voltage condition. Therefore, the nine filter channels in the NZMM7V0T4 can replace 9 resistors, 18 capacitors, and 18 diodes, in addition to the three separate zener diodes. Thus the NZMM7V0T4 can replace 48 discrete components, which reduces both the system cost and the required PCB space. In addition, the integration of the filtering network in the small chip scale package provides for a better attenuation characteristic than a discrete filter by minimizing the parasitic impedances that result from the multiple contacts between the components.

The schematics for the NZF220TT1 single channel and the NZF220DFT1 dual channel filters are shown in Figures 6 and 7. The single and dual filter channel devices are identical to the NZMM7V0T4 nine channel device. Each filter channel consists of a Pi filter that is formed by a 100 Ω resistor and two zeners that have a junction capacitance of 22 pF.

Manufacturing Details

The 24 pin NZMM7V0T4 is manufactured using conventional planar processing on a silicon substrate. The IPD is housed in a 24 pin Lead Frame Chip Scale Package (LFCSP). The LFCSP package is only 16 mm^2 square in size with a package height of less than 1 mm. Figure 8 shows a cross section of the silicon wafer.

The zener diodes housed in the NZMM7V0T4 are small in size compared to standard zener diodes; therefore, it is possible to package multiple filter channels in the small LFCSP IC package. The transient voltage pulse resulting from an ESD event is relatively low in energy because of the short pulse duration; therefore, a very small PN junction can absorb the energy without damage. Furthermore, the capacitance of a PN junction is proportional to the size of the diode; thus the zener capacitance will be small in magnitude. The value of the capacitance (C_o) is a function of

1. The material resistively (ρ) where the doping level determines the nominal zener breakdown voltage
2. The diameter (D) of the junction which determines the power dissipation
3. The voltage across the junction (V_c)
4. A constant K

This relationship is expressed as:

$$C_o = \sqrt{\frac{K\,D^4}{\rho V_c}}$$

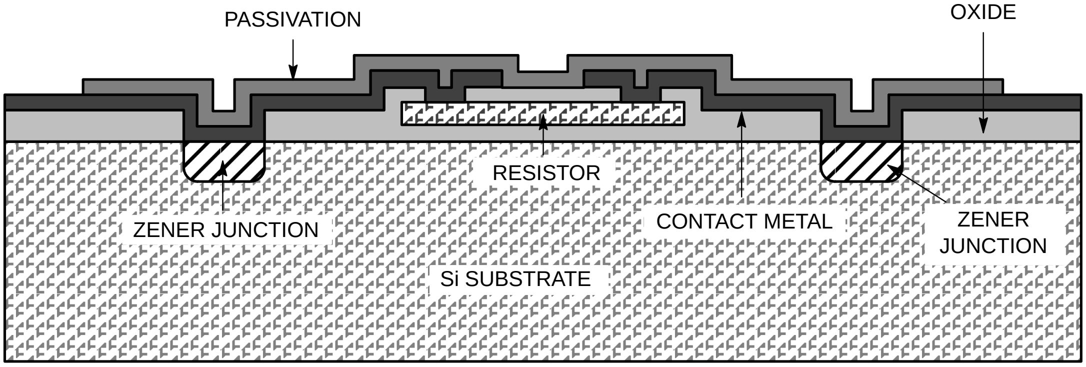
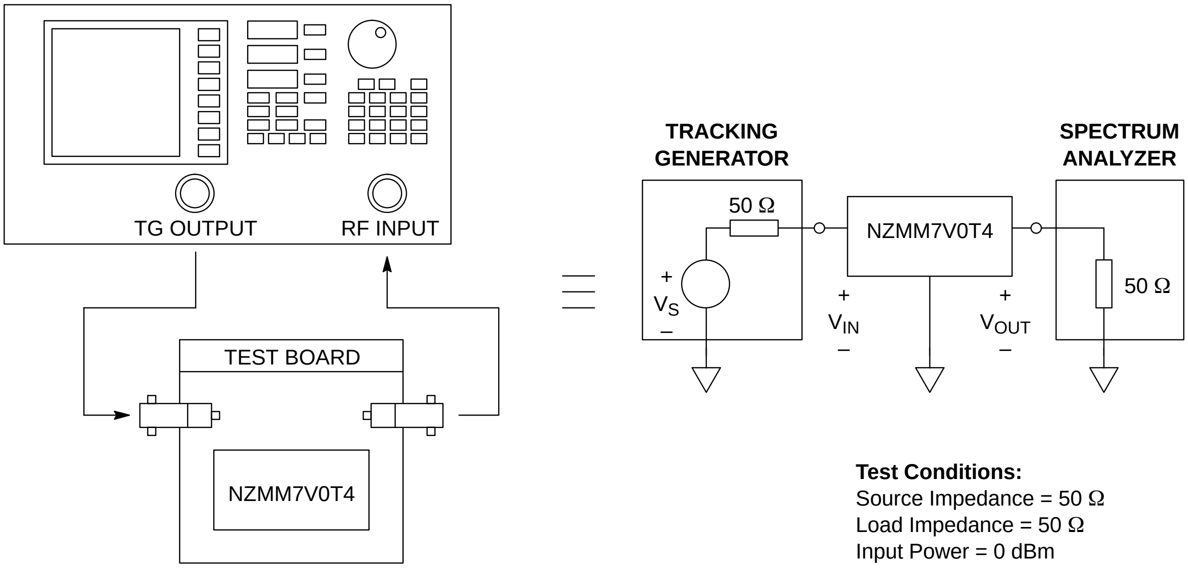


Figure 8. Cross Section View of Filter Channel

Interpreting the Data Sheet Specifications

The IPD’s frequency and insertion loss characteristics can be measured using a spectrum analyzer with a tracking generator as shown in Figure 9. Figure 10 shows the frequency response of the NZMM7V0T4 using the evaluation PCB shown in Appendix I. The four main characteristics of the NZMM7V0T4 that need to be analyzed are listed below:

1. Cut–off (f_{-3dB}) frequency
2. Insertion loss
3. High frequency rejection specification
4. ESD clamping voltage



Test Conditions:
Source Impedance = 50 Ω
Load Impedance = 50 Ω
Input Power = 0 dBm

Figure 9. Measurement Conditions

Cut–off (f_{-3dB}) Frequency

The cut–off frequency, or f_{-3dB} frequency, is defined as the corner frequency where the gain (attenuation) of the filter decreases (increases) by 3 dB from the low frequency gain (attenuation). Also, the f_{-3dB} frequency is the point where the gain of the filter is equal to 0.707 $(1/\sqrt{2})$. The frequency response of a discrete filter is dependent on the impedance of the source (transmitter) and load (receiver) circuits. The IPD’s frequency response in the customer circuit will be different than the data sheet characteristics because it is unlikely that the actual source and load impedances are equal to 50 ohms. This issue is discussed in the *Filter Design Equations* section of this paper.

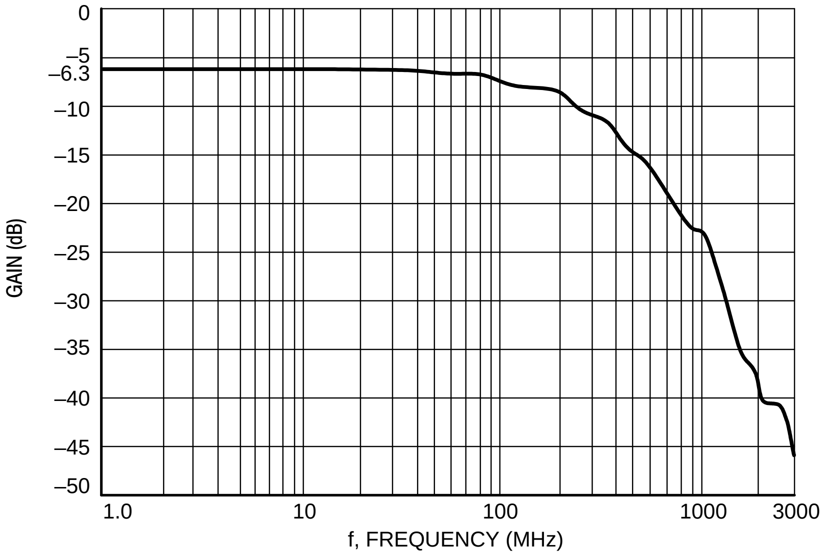


Figure 10. Typical EMI Filter Response
(50 Ω Source and 50 Ω Load Termination,
Insertion Loss = –6.3 dB,
f_{-3dB} = 220 MHz)

Insertion Loss

The insertion loss is defined as the ratio of the power delivered to the load with and without the filter network in the circuit. This characteristic is dependent on the impedance of the source (transmitter) and load (receiver) circuits, and is proportional to the magnitude of the filter resistance. The insertion loss equation is listed below.

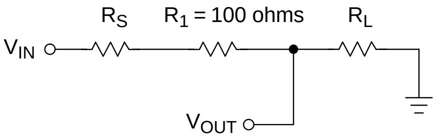
$$\text{Insertion Loss(dB)} = 20\log_{10}\left(\frac{R_S + R_1 + R_L}{R_S + R_L}\right)$$

$$\text{for } R_S = R_L = 50\ \Omega \text{ and } R_1 = 100\ \Omega$$

$$\text{Insertion Loss} = 6.02\text{ dB}$$

If the transmitter and receiver circuits are digital circuits, the insertion loss can be neglected and V_{OUT} will be equal to V_{IN} . The output impedance of a digital circuit (R_S) is typically very small, while the input impedance (R_L) is usually equal to a small capacitor, and is essentially an open circuit load at DC. The insertion loss is usually not a concern for digital circuits; instead, the filter's effect on the rise and fall times of the digital pulse waveform must be evaluated. This issue is discussed in Application Note AND8027 (2).

If the transmitter and receiver are analog circuits, the insertion loss must be analyzed. The RC Pi filter will function as a voltage divider because of the resistive element. The DC voltage divider effect of the filter can be analyzed by using the simplified schematic shown in Figure 11, with the equations listed below.



R_S = Transmitter output impedance
R_L = Receiver input impedance

$$V_{OUT} = \left(\frac{R_L}{R_S + R_1 + R_L}\right) V_{IN}$$

Figure 11. Insertion loss analysis

In addition, the voltage divider equation can usually be simplified. For example, if the transmitter is an operational amplifier, R_S will be equal to the output impedance of the amplifier, which is typically equal to less then an ohm. Thus, the R_S term can be neglected.

High Frequency Rejection Specification

The attenuation or rejection level of a specific high frequency is application specific and is used to verify the attenuation of a particular frequency. For example, it is critical in a cellular phone that the EMI filter attenuates the system's operating frequency. Thus, the NZMM7V0T4 has a minimum attenuation level specified at 900 MHz. For non–cellular applications, the designer should verify the filter's attenuation for noise sources such as the microprocessor's clock frequency.

ESD Clamping Voltage

In addition to its noise filtering function, the NZMM7V0T4 also provides ESD protection. The NZMM7V0T4 is rated to meet the IEC61000–4–2 specification that simulates the case when a person carrying a metallic object touches an interface contact. The NZMM7V0T4's circuit configuration of two zeners results in an ESD clamping voltage that will be within a few millivolts of the zener breakdown voltage. The nominal clamping voltage of 7 V should be safe for most designs; however, the designer should verify that the clamping voltage is less than the maximum input voltage rating of the filter's interface circuitry.

Filter Design Equations

Frequency Response

The two port analysis method can be used to obtain the filter's transfer equation and an equation for the $f_{–3dB}$ frequency. Additional details on the derivation of the two port equations and the equations defining the input impedance (Z_{in}), output impedance (Z_{OUT}), and current gain (A_I) are provided in reference (3).

Table 2 lists the transfer equations that define the voltage gain and filter characteristics of the Pi filter. Included in the table are equations that show that the Pi filter's $f_{–3dB}$ is influenced by the source (transmitter) and load (receiver) circuits that are connected to the filter. In addition, equations are given that show the bi–directional filter feature of the Pi network.

The $f_{–3dB}$ frequency is found by determining the location of the poles of the transfer equation. Then the $f_{–3dB}$ frequency is obtained by substituting s = jω into the equation, where $\omega = 2\ \pi f$.

The transfer equation A_{V1} is the transfer equation that is representative of the Pi filter when the effects of the source impedance (Z_S) and the load impedance (Z_L) are neglected. A_{V1} can be used to obtain an estimate of the $f_{–3dB}$ frequency; however, the transfer equation $A_V\oplus$ should be used to obtain a more accurate calculation. The voltage gain A_{V1} is defined as the ratio of the output voltage (V_{OUT}) to the input voltage (V_{IN}) when the load impedance is an open circuit ($Z_L = \infty$ and $I_{OUT} = 0$). A_{V1} can also be interpreted as the equation defining the circuit that filters the noise signals that "enter" the Pi network.

In contrast, A_{V2} reverses the input and output assignments of the circuit to show the bi–directional filter characteristic of a Pi network. A_{V2} is defined as the ratio of the input voltage (V_{IN}) to the output voltage (V_{OUT}); therefore, A_{V2} can be interpreted as the equation defining the circuit that filters the noise signals that "exit" the Pi network.

The transfer equation $A_V\oplus$ is the transfer equation that is representative of the spectrum analyzer / tracking signal generator frequency measurement system. $A_V\oplus$ is calculated by comparing the output voltage (V_{OUT}) to the voltage at the input of the filter (V_{IN}). $A_V\oplus$ can be derived by substituting $Z_S = 0$ into the A_{V*} equation. In contrast to the second order A_{V*} equation, the $A_{V\oplus}$ equation is a first order equation. Thus the $A_{V\oplus}$ equation provides for a simple expression that can be solved to determine the f_{-3dB} frequency.

The $A_{V\oplus}$ equation is often a very good approximation of the system transfer equation A_{V*} for analog circuits. For example, assume that the transmitter circuit is an operational amplifier. The output impedance of an ideal analog amplifier is zero; therefore, the Z_S in the A_{V*} equation can be neglected because $Z_S << R_1$ and $Z_S << R_L$.

In addition, the $A_{V\oplus}$ equation is also a very good approximation of A_{V*} for digital logic circuits. Now assume that the transmitter circuit is a CMOS digital logic IC that has an output stage consisting of a PMOS and a NMOS transistor. For both the logic output “high” and “low” cases, the output impedance of the logic chip will be equal to the channel resistance (r_{ds_ON}) of the transistor that is turned “ON”. The output impedance of the CMOS IC can be neglected because the output impedance of the “ON” transistor ($r_{ds\_ON} \approx$ milli–ohms) is in parallel with the output impedance of the “OFF” transistor ($r_{ds\_OFF} \approx$ mega–ohms).

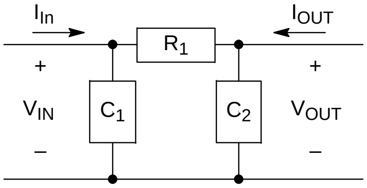
The major factor effecting the f_{-3dB} frequency of a passive filter is the magnitude of the source and load impedances. To a smaller degree, the frequency response is also a function of the initial tolerances of the resistors and capacitors, the component changes over temperature, and the bias voltage of the signal. These errors can be neglected for most applications; however, a detailed analysis of the component error terms is shown in Application Note AND8027 reference (2).

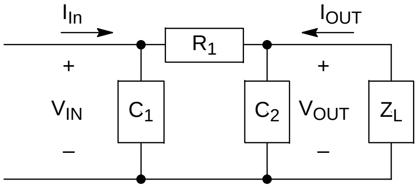
The transfer equation A_{V*} is defined as the system voltage gain and is the transfer equation that is representative of the ESD characteristics of the Pi filter. A_{V*} is calculated by dividing the output voltage (V_{OUT}) by the input voltage of the source (V_S). A_{V*} shows that the frequency response of the Pi filter is dependent on the impedance of the driver and receiver circuits that are connected to the filter. Because the transfer equation includes the source and load impedances, A_{V*} will be a second order equation that is relatively complex with a frequency roll–off of –40 dB. Thus, a simple expression to determine the poles of the equation (i.e. the f_{-3dB} frequency) is not readily apparent. However, A_{V*} can be evaluated by using a mathematical software program such as Microsoft’s Excel to obtain a Bode plot of the frequency response. Then the –3 db frequency can be determined directly from the Bode plot. Also, the –3 db frequency can be determined by performing a SPICE circuit simulation.

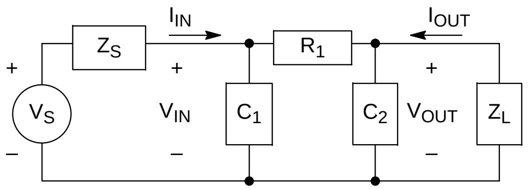
Table 1. Definition of Y Parameters

Admittance matrix (Y)	Short circuit input admittance	Short circuit forward transfer admittance	Short circuit reverse transfer admittance	Short circuit output admittance
$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$	$Y_{11} = \frac{I_1}{V_1} \bigg\vert V_2 = 0$	$Y_{21} = \frac{I_2}{V_1} \bigg\vert V_2 = 0$	$Y_{12} = \frac{I_1}{V_2} \bigg\vert V_1 = 0$	$Y_{22} = \frac{I_2}{V_2} \bigg\vert V_1 = 0$
Pi filter Y parameters	$Y_{11} = sC_1 + G_1$	$Y_{21} = -G_1$	$Y_{12} = -G_1$	$Y_{22} = G_1 + sC_2$

Table 2. Pi Filter Frequency Characteristics

Pi Filter Circuit	
Voltage Gain	$A_{V1} = \frac{V_{OUT}}{V_{IN}} = \frac{-Y_{21}}{Y_{22}}$ $A_{V2} = \frac{V_{IN}}{V_{OUT}} = \frac{-Y_{21}}{Y_{11}}$
	$A_{V1} = \frac{V_{OUT}}{V_{IN}} = \frac{G_1}{G_1 + sC_2} = \frac{\frac{1}{R_1C_2}}{s + \frac{1}{R_1C_2}}$ $A_{V2} = \frac{V_{IN}}{V_{OUT}} = \frac{G_1}{G_1 + sC_1} = \frac{\frac{1}{R_1C_1}}{s + \frac{1}{R_1C_1}}$
f_{-3dB}	$f_{-3dB\_A_{V1}} = \frac{1}{2\pi R_1C_2}$ $f_{-3dB\_A_{V2}} = \frac{1}{2\pi R_1C_1}$
	$f_{-3dB\_A_{V1}} = f_{-3dB\_A_{V2}} = 72$ MHz with $C_1 = C_2 = 22$ pF and $R_1 = 100\ \Omega$
Application	*Useful to approximate f_{-3dB} *$Z_S = 0$ & $Z_L = \infty$

Pi Filter Circuit	
Voltage Gain	$A_V \oplus = \frac{V_{OUT}}{V_{IN}} = \frac{-Y_{21}}{Y_{22} + Y_L}$
	$A_V \oplus = \frac{V_{OUT}}{V_{IN}} = \frac{G_1}{sC_2 + Y_L + G_1} = \frac{\frac{G_1}{C_2}}{s + \frac{Y_L + G_1}{C_2}}$
f_{-3dB}	$f_{-3dB} = \frac{Y_L + G_1}{2\pi C_2}$
	$f_{-3dB} = 217$ MHz with $R_L = 50\ \Omega$, $C_1 = C_2 = 22$ pF and $R_1 = 100\ \Omega$
Application	*Representative of most analog and digital circuits *Representative of Spectrum Analyzer/Tracking Generator System *$Z_S = 0$ & $Z_L \neq \infty$

Pi Filter Circuit	
Voltage Gain	$A_V{}^* = \frac{V_{OUT}}{V_S} = \frac{-Y_{21}}{Y_{22} + Y_L + Z_S\,(\Delta Y + Y_{11}Y_L)}$
	$A_V{}^* = \frac{V_{OUT}}{V_S} = \frac{G_1}{as^2 + bs + c}$ where $a = Z_S C_1 C_2$ $b = Z_S C_1 G_1 + Z_S C_2 G_1 + Z_S Y_L C_1 + C_2$ $c = Z_S G_1 Y_L + Y_L + G_1$
f_{-3dB}	***Note 4** $s = \frac{-\,b \pm \sqrt{b^2 - 4ac}}{2a}$ $s = j\omega = 2\,\pi f$ $f_{-3dB} = \frac{\omega}{2\,\pi}$
	$f_{-3dB} = 121$ MHz with $R_S = R_L = 50\ \Omega$, $C_1 = C_2 = 22$ pF and $R_1 = 100\ \Omega$
Application	*Representative of ESD analysis circuit $^*Z_S \neq 0$ & $Z_L \neq \infty$

1. Admittance (Y) is equal to the reciprocal of the impedance (i.e. Y = 1/Z)
2. Conductance (G) is equal to the reciprocal of the resistance (i.e. G = 1/R)
3. $\Delta Y = Y_{11}\,Y_{22} - Y_{12}\,Y_{21}$
4. Typically solved using Excel or SPICE

ESD Equations

The protection characteristics of the Pi filter can be analyzed by considering the Pi circuit as two separate stages, as shown in Figure 12. The voltage at the first stage (V_{IN}) will have a peak or overshoot voltage that is significantly above the clamping voltage of because of the dynamic resistance of the zener as shown below. In contrast, the voltage at the second stage (V_{OUT}) will be very close to the zener's clamping voltage because the R_D*I_P term is small in comparison to the magnitude of the R_D*I_P term of the first stage.

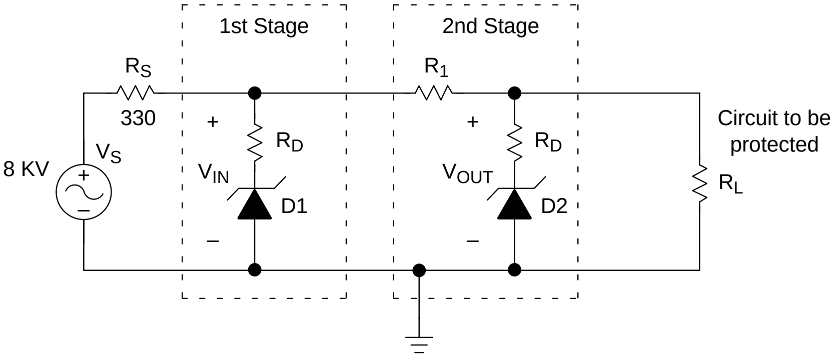


Figure 12. ESD Analysis of Pi Filter

The equations describing the ESD characteristics are listed below.

$$V_{Clamping\_voltage} = V_{br} + R_D * I_P$$

$$V_{IN} = V_{br} + \left(\frac{R_D}{R_S + R_D}\right)V_S \cong V_{br} + \left(\frac{R_D}{R_S}\right)V_S$$

$$V_{OUT} = V_{br} + \left(\frac{R_D}{R_1 + R_D}\right)V_{IN} \cong V_{br} + \left(\frac{R_D}{R_1}\right)V_{IN}$$

Where

V_S = IEC 61000–4–2 Voltage waveform = ± 8 kV
R_S = IEC 61000–4–2 source impedance = 330 Ω
V_{br} = breakdown voltage = 7 V
R_D = dynamic resistance of the zener ≤ 1 Ω
I_P = Peak ESD Current
R_1 = 100 Ω
$C_1 = C_2$ = 22 pF
$R_D << R_S$
$R_D << R_1$

The results for the ESD calculation gives the results listed below, assuming R_D is equal to one ohm:

V_{IN} = 31.2 V
V_{OUT} = 7.3 V

The voltage at V_{OUT} confirms that the NZMM7V0T4 will clamp the ESD voltage to a safe value. Note that these equations do not include any parasitic inductances that cause the clamping voltage to have an overshoot peak voltage. It is necessary to locate the NZMM7V0T4 close to the connector (ESD source) and to minimize the PCB inductances in order to optimize the ESD performance.

PCB Design Issues

The design of the NZMM7V0T4's PCB is critical to the ESD and filter performance of the device. Standard high frequency PCB design rules should be used in the layout to minimize any parasitic inductance and capacitance that will degrade the filter's performance. The most important PCB layout issue is to locate the NZMM7V0T4 as close to the connector as possible.

The Pi filter is a bi–directional filter. By convention, the NZMM7V0T4's input pins (V_{IN}) are normally connected to the I/O connector, while the output (V_{OUT}) pins are connected to the circuitry on the PCB. The labeling of the filter pins as either inputs or outputs is arbitrary; therefore, the user has the flexibility to re–assign the inputs and outputs in order to simplify the PCB routing.

Listed below are design guidelines to follow to optimize the NZMM7V0T4's EMI/ESD performance. This list was derived from experience and the references (1), (4) and (5).

PCB Recommendations

Optimizing EMI Filter Performance

- Filter all I/O signals entering / leaving the noisy environment
- Locate the NZMM7V0T4 as close to the I/O connector as possible
- Minimize the loop area for all high speed signals entering the filter array
- Use ground planes to minimize the PCB's ground inductance

Optimizing ESD Protection

- Locate the NZMM7V0T4 as close to the I/O connector as possible
- Minimize the PCB trace lengths to the NZMM7V0T4
- Minimize the PCB trace lengths for the ground return connections

Appendix I shows the PCB artwork that was used to evaluate the NZMM7V0T4.

Application Information

The NZMM7V0T4 can be used as a low cost EMI and ESD filter solution for a wide range of applications including cellular phones, PCs, and input circuits such as analog switches and multiplexers / demultiplexers. Listed below are a list of application examples. Figures 13 through 17 show example circuits using the NZMM7V0T4.

Cellular Telephones

- Remote speaker
- Microphone
- Earphone
- SIM connector
- RS232 / USB serial port
- Keypad

Personal Computers

- Keyboard
- Game port
- Parallel port
- Mouse
- USB / RS232 serial port
- Flat panel display I/O port

General Purpose Applications

- ESD/EMI protection of analog switches, multiplexers, and demultiplexers
- ESD protection for industrial motherboards

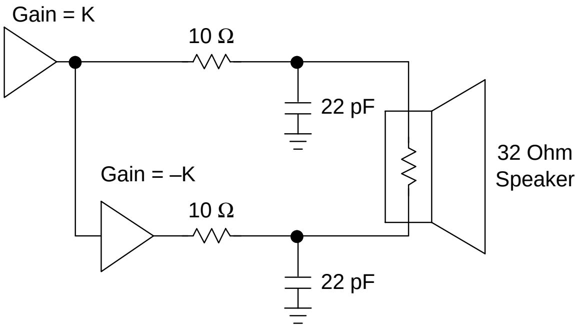


Figure 13a

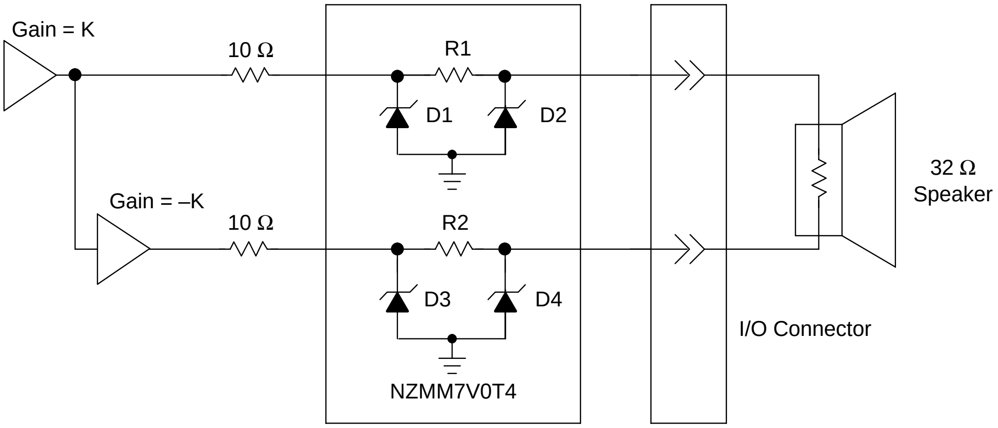


Figure 13b

Figure 13. Bridge Tied Load (BTL) Audio Power Amlifier (13a) with Remote Speaker (13b)

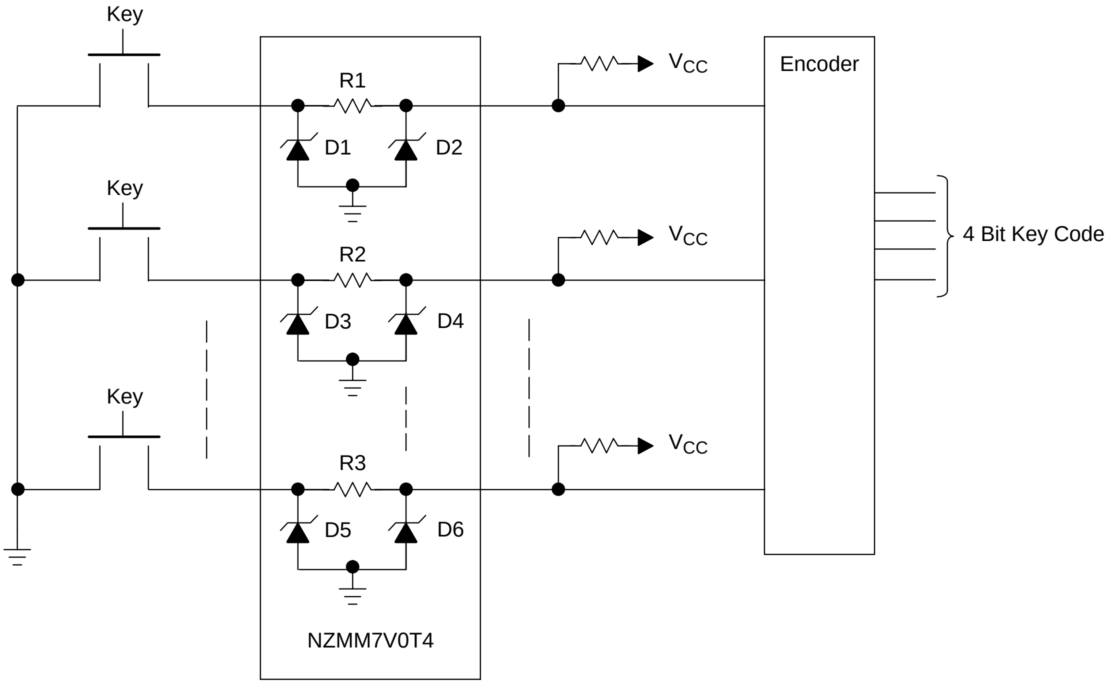


Figure 14. Keypad Application

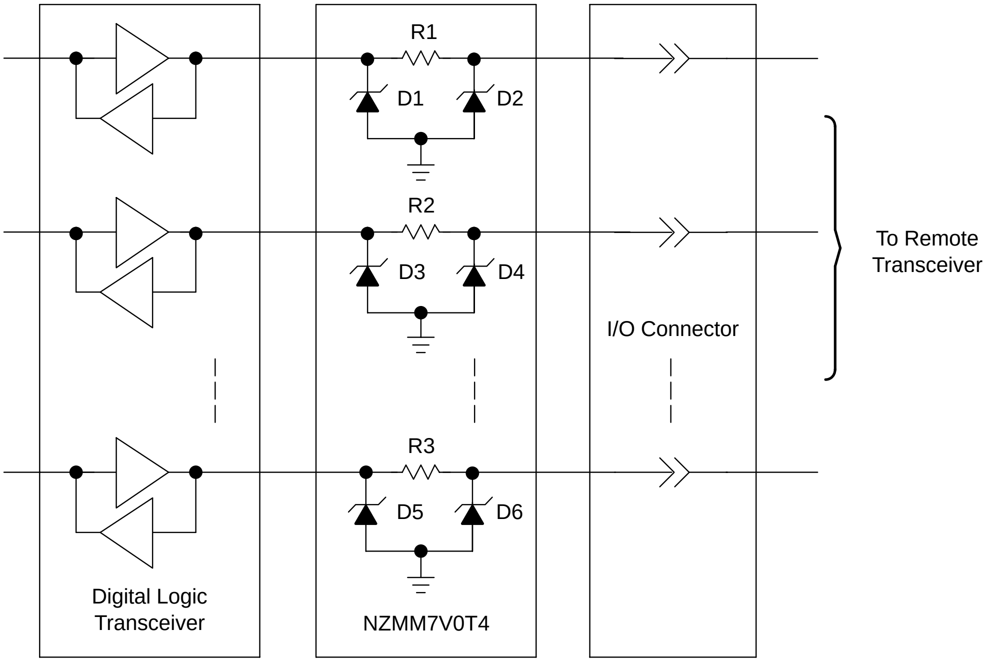


Figure 15. Digital Application where the NZMM7V0T4 Protects a Logic Transceiver

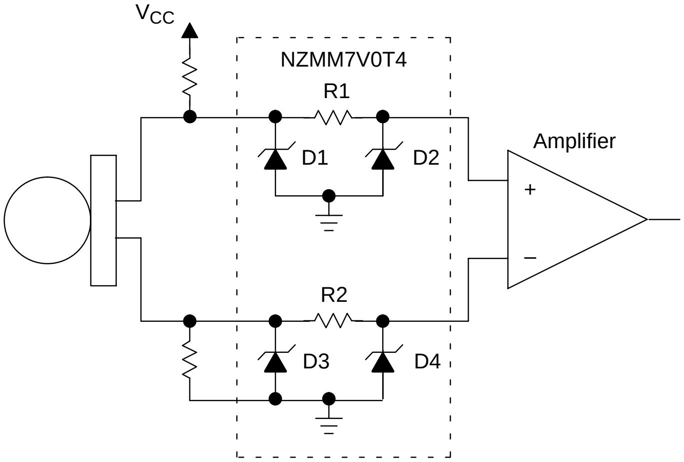


Figure 16. Microphone Amplifier Application

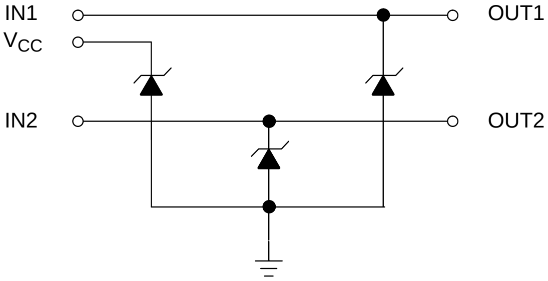


Figure 17. NTZMM7V0T4’s Zener Diodes Protect a USB or RS232 Serial Port

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Appendix I

Listed below is the documentation on the test PCB that was used to evaluate the NZMM7V0T4.

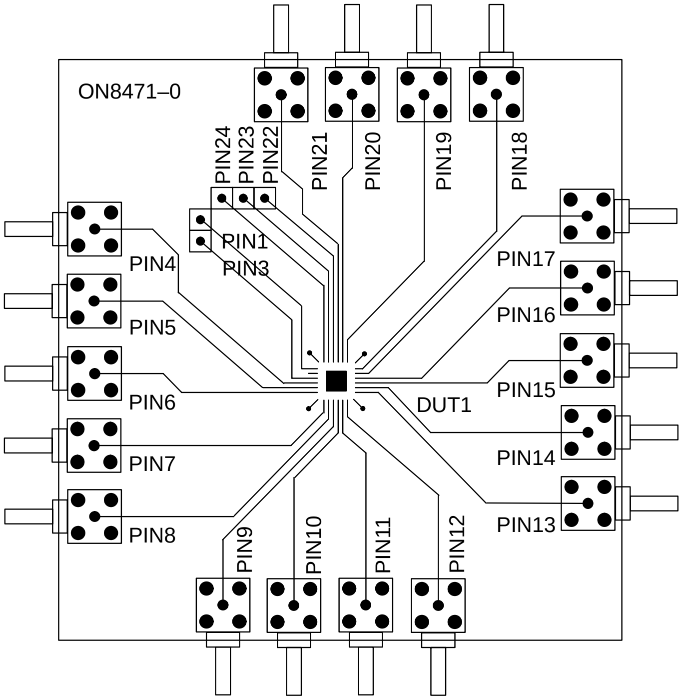


Figure A1: PCB Component Side

Note: Connector Part Number: AMP414026–3

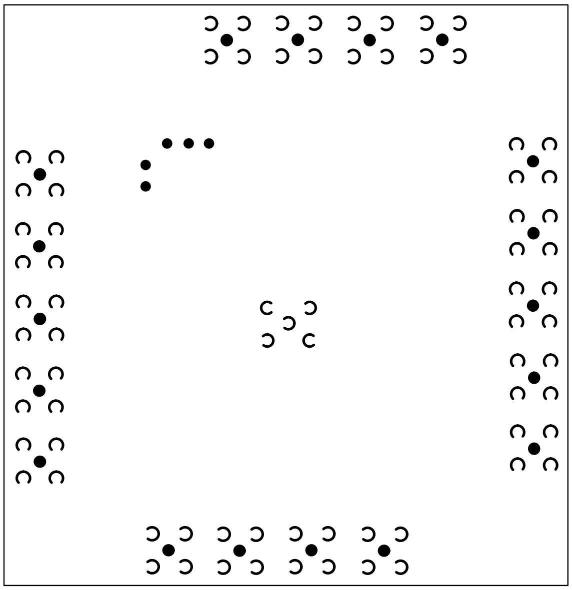
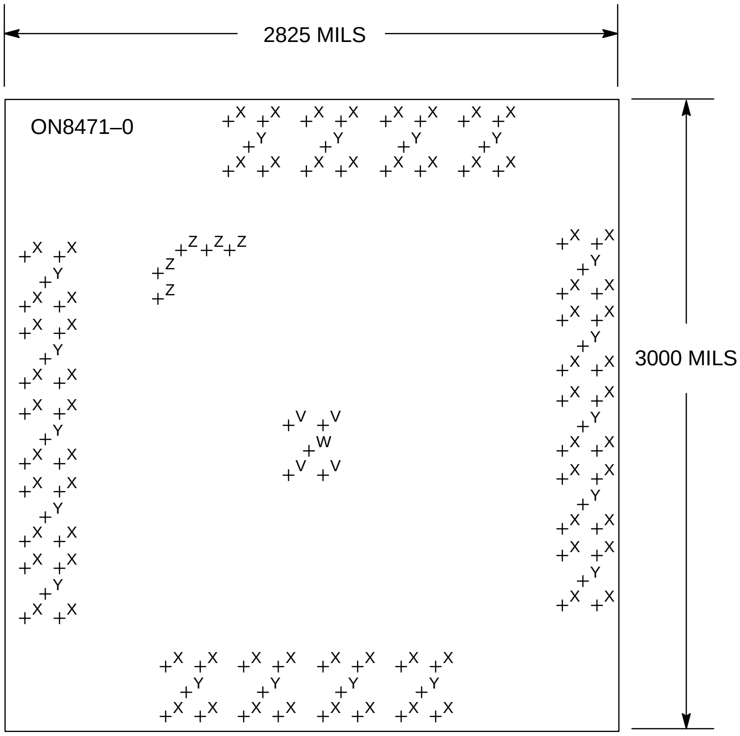


Figure A2: PCB Solder Side

Note: Dashed circles are ground connections and solid circles are signal connections



1. MATERIAL FR–4 0.062 FINISHED
2. DISTANCE BETWEEN LAYER CRITICAL
3. SOLDERMASK LPI GREEN
4. DISTANCE BETWEEN LAYERS SHALL MEET IPC 600 D

SIZE	QTY	SYM	PLTD
15	4	V	PLTD
14.96	1	W	PLTD
60	72	X	PLTD
50	18	Y	PLTD
37	5	Z	PLTD

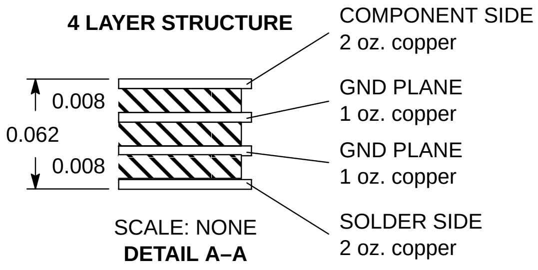


Figure A3: PCB Drill Plot

Notes

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