

H124, 125, 350-352 Translator I/O SPICE Modelling Kit

Prepared by: Debbie Beckwith
Andrea Diermeier
ECL Applications Engineering



ON Semiconductor®

<http://onsemi.com>

APPLICATION NOTE

This application note provides the SPICE information necessary to accurately model system interconnect situations for designs which utilize the translator circuits of the MECL 10KH family. Also included is information on the H124, H125, H350, H351, and H352 translators.

INTRODUCTION

With the difficulty in designing high-speed controlled impedance PC boards and the expense of reworking those boards, the ability to model circuit behavior prior to committing to a board layout is essential for high speed logic designers. The purpose of this document is to provide the user with enough information to perform basic SPICE model analysis on the interconnect traces being driven or driving the H124, H125, H350, H351, and H352 translator chips. The packet includes schematics of the input and output structures as well as ESD protection structures and package models which may affect the waveshape of the input and output waveforms. Internal bias regulators and logic circuitry are not included as they have little impact on the I/O characteristics of the device and add a significant amount of time to the standard simulation analysis. In addition, a SPICE parameter set for the devices referenced in the schematics is provided. The remainder of this document will introduce the various input and output stages for the above translators as well as the other structures which affect the I/O characteristics of these devices.

Schematic Overview

There are five basic schematics which can represent the I/O for the MECL10KH family of translator chips. The rest of the schematics provided represent subcircuit schematics for the above mentioned I/O buffers and package models. The devices shown in shaded boxes on the I/O buffer schematics are modelled by the subcircuits illustrated on the

appropriate subcircuit schematic sheet. This hierarchical method of schematic representation is used to help simplify and clarify the buffer schematics.

The H124 I/O buffer is represented by the H124 I/O Gate schematic of Figure 1. This device is a dual supply device which means it requires +5 V, -5.2 V, and ground supplies. The AIN and CSTROBE inputs are single-ended TTL level inputs and should be driven with the minimum HIGH level at 2.4 V and the maximum LOW level at 0.5 V.

Package Models

Due to different dimensions of the packages and the different lead lengths of center and corner pins, different package models are asserted.

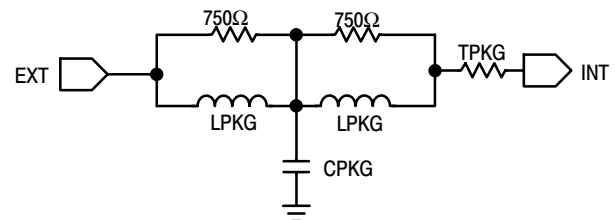


Figure 1. Package Model

The H125 is also a dual supply device represented by one structure as shown in the H125 I/O schematic of Figure 2. The H125 requires a differential input, IN and INN, which should be driven from 0.9 to 1.75 V.

AN1598/D

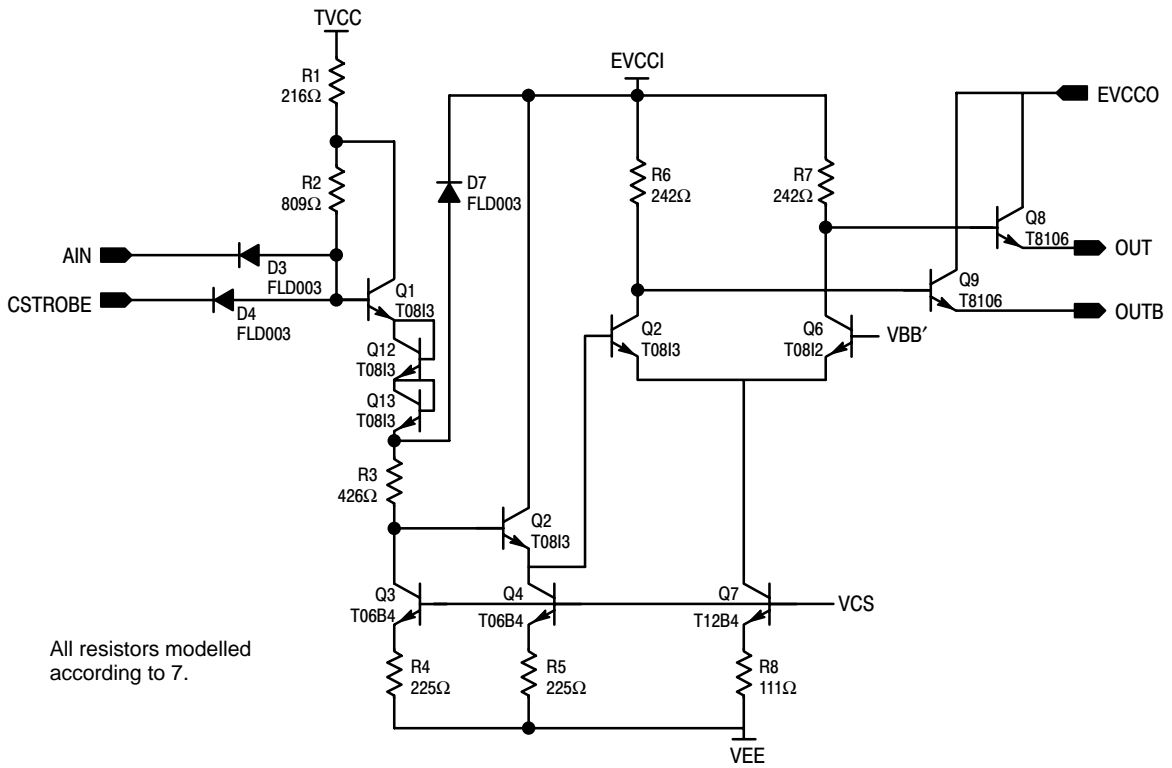


Figure 2. H124 I/O Gate

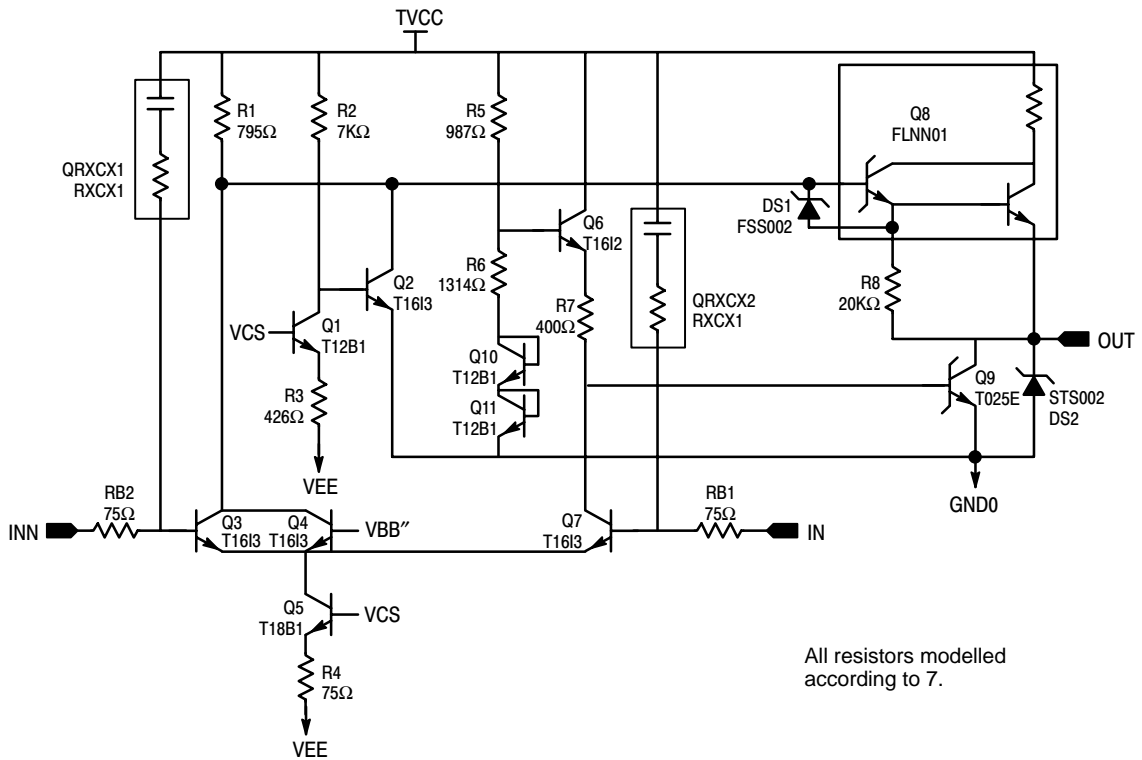


Figure 3. H125 I/O Gate

AN1598/D

The H350 I/O gate is represented by the schematic of Figure 4. The H350 I/O gate is designed to operate from a single supply of $V_{CC} = 5.0$ V. The IN and INN inputs should

be driven differentially with standard PECL input swings of $V_{CC} - .9$ to $V_{CC} - 1.75$ V.

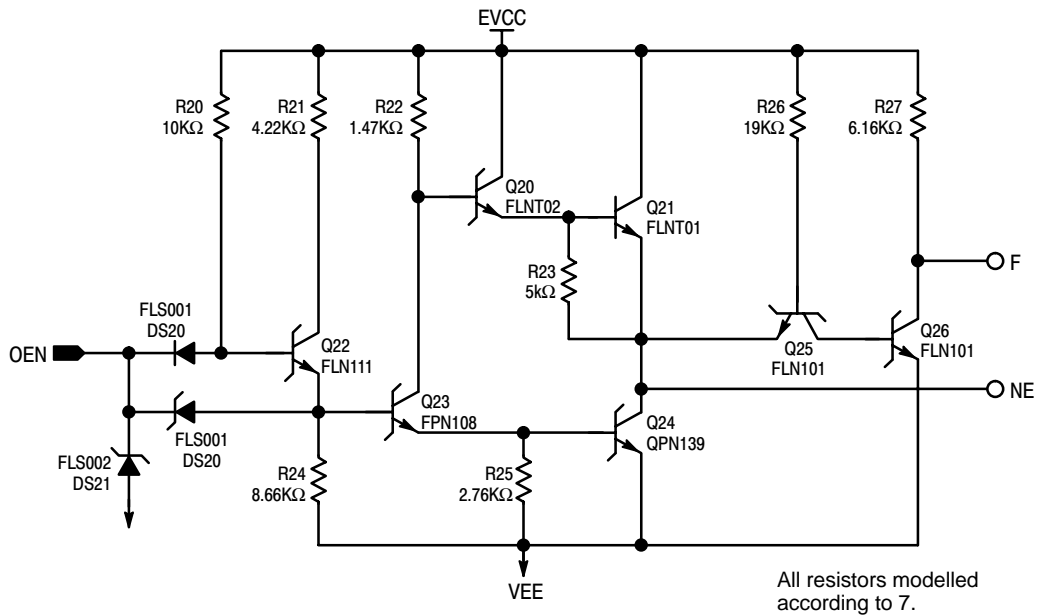
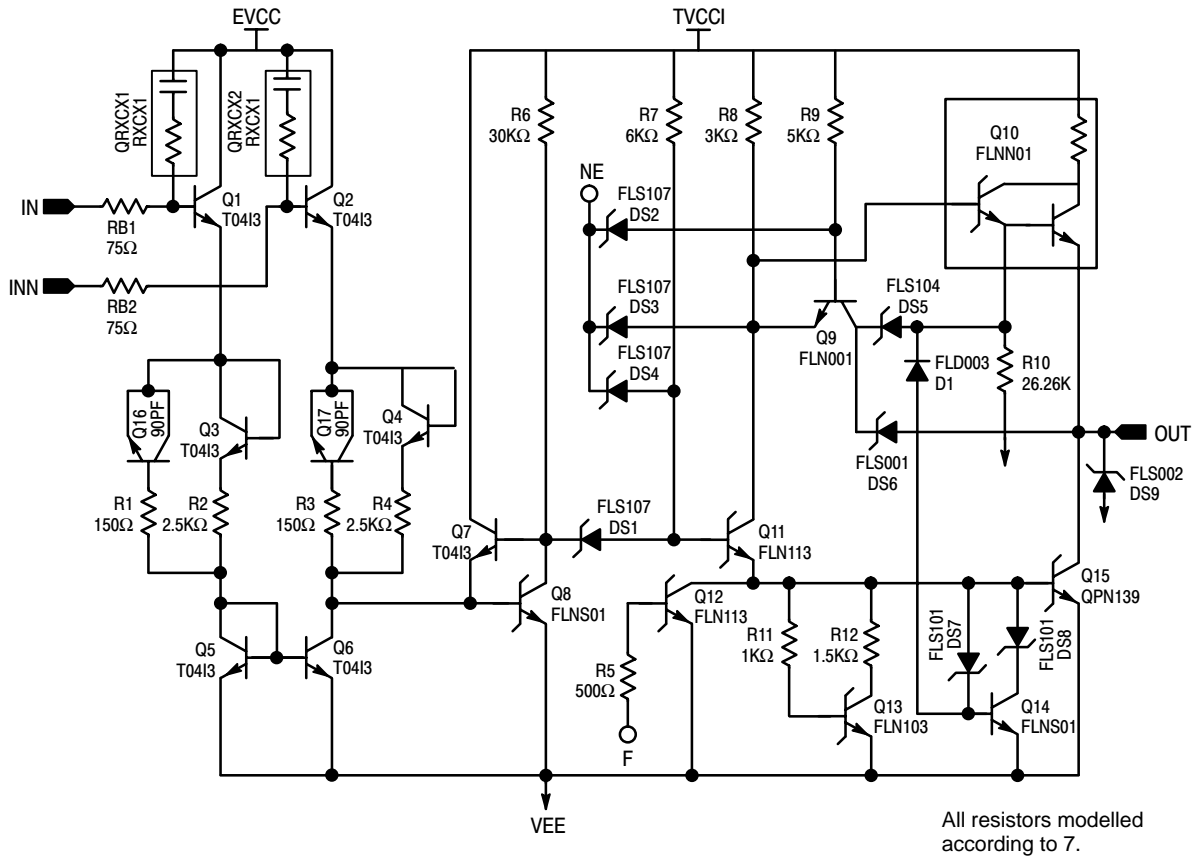


Figure 4. H350 I/O Gate

AN1598/D

The H351 and H352 utilize similar I/O buffers. These buffers are represented by the “H351 I/O Gate Schematic” and the “H352 I/O Gate Schematic” of Figures 5 and 6, respectively. For the H351, the IN input should be driven with single ended TTL level voltage swings with the minimum HIGH level at 2.4 V and the maximum LOW level

at 0.5 V. The single ended input, STROBE, enables the output when driven with a “high” TTL level input. For the H352, the IN input should be driven with single ended CMOS level voltage swings from 0 to 5 V. The single ended input, STROBE, enables the output when driven with a “high” CMOS level input.

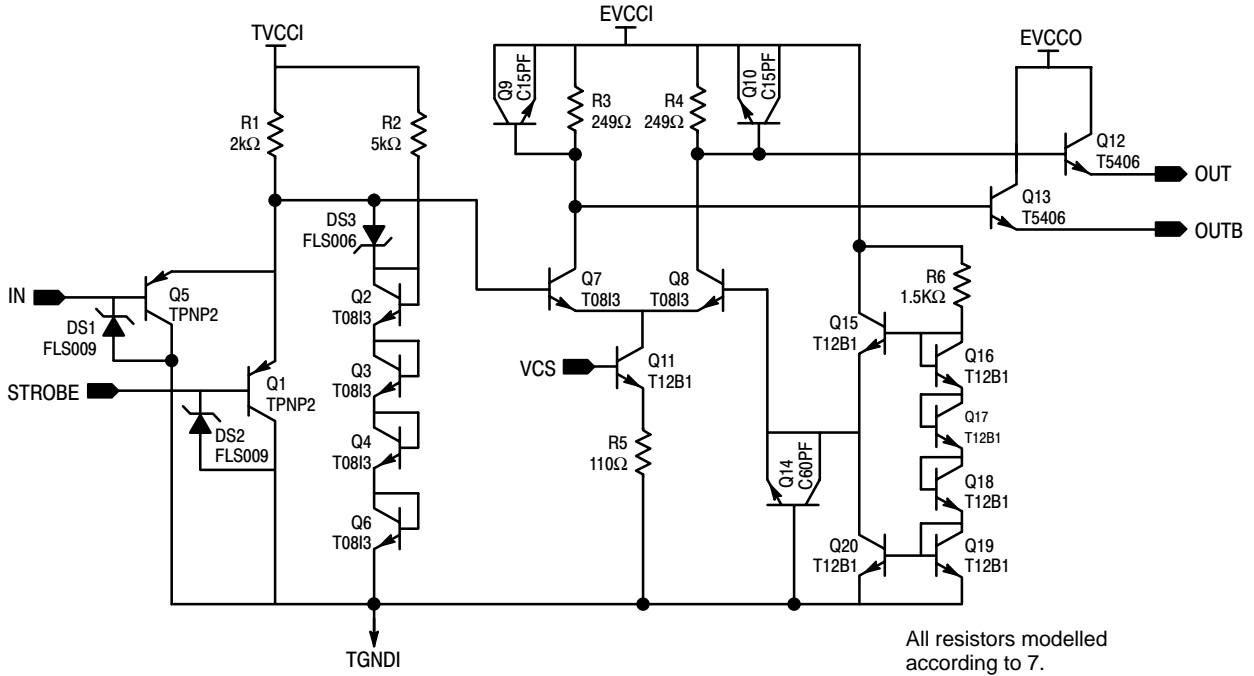


Figure 5. H351 I/O Gate

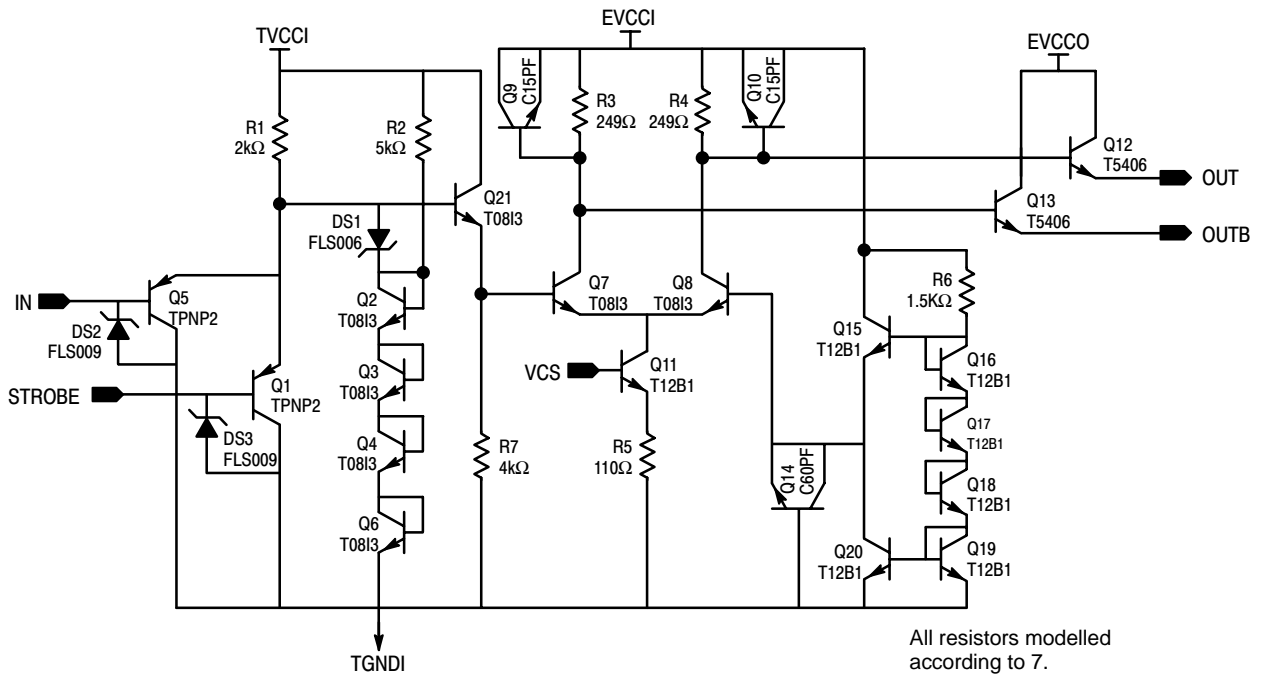


Figure 6. H352 I/O Gate

Table 1 is provided to summarize the various internal voltage swings and bias levels required to run the appropriate SPICE simulations.

Table 1. Input and Bias Levels

Schematic	Input	Levels
H124 I/O	AIN/BIN V_{BB}' V_{CS}	0.5 to 3.5V -2.1V $V_{EE} + 1.3V$
H125 I/O	IN/INN V_{BB}'' V_{CS}	-0.9 to -1.75V $V_{CC} - 2.9V$ $V_{EE} + 1.3V$
H350 I/O	IN OEN	($V_{CC} - 0.9$ to $V_{CC} - 1.75$) 0.5 to 3.5V
H351 I/O	IN Strobe V_{CS}	0.5 to 3.5V 0.5 to 3.5V $V_{EE} + 1.3V$
H352 I/O	IN Strobe V_{CS}	0 to 5.0V 0 to 5.0V $V_{EE} + 1.3V$

For the dual supply devices with ECL inputs, the V_{CC} and the V_{EE} on the typical ECL input gates should be tied to ground and -5.2 V respectively. All input pins should have a package model connected to them. The "Package Model" of Figure 1 is self explanatory, the parasitic values provided in Table 2 are worst case numbers. The package capacitance combines with the parasitic transistor, capacitance of the input device and the ESD circuitry to comprise the load capacitance of the input. The typical ECL input schematic represents a single ended ECL input, the V_{BB} reference should be tied to $V_{CC} - 1.3$ V and the V_{CS} bias should be tied to $V_{EE} + 1.3$ V.

Table 2. Package Model Values

Package	Pin	CPKG (pF)	LPKG (nH)	RPKG (Ω)
PLCC 20	All Pins	1.5	3.5	0.2
DIP 16	End Pin	1.3	5.5	0.1
	Center Pin	0.7	2.5	0.1
DIL 20	Center Pin	0.8	4.85	0.036
	End Pin	2.76	7.17	0.036
DIP 20	Center Pin	0.68	2.99	0.03
	End Pin	1.26	6.7	0.05

For all of the I/O buffer schematics, the resistors should **NOT** be simulated as simple SPICE resistors. Because these resistors are realized by a diffusion step in wafer processing,

there are parasitic capacitances associated with each. The subcircuit schematic is shown for the resistors in the "Resistor Model" schematic of Figure 7. The value of each subcircuit resistor is one half the value given on the top level schematic and the parasitic capacitance is modelled by a diode back biased to V_{CC} . Also note that the resistor temperature coefficient (TC) values for both the resistor subcircuit and the resistors in the device subcircuits are provided. For modelling at nominal temperatures only, these TCs can be omitted. If however, modelling will be performed at the temperature extremes, the TC information should be included.

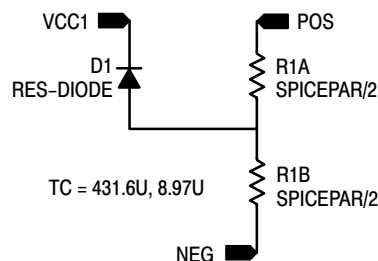


Figure 7. Resistor Model

Handling Power Supplies

It is important to properly apply the power supply voltages to accurately model these circuits. This section will explain the power supply terminology used on the I/O buffer schematics and how to properly apply these supplies with the appropriate package model.

Table 2 lists the voltage supplies referenced on the I/O schematics along with a description of each. The key to properly simulating these power supplies is in the application of the package model. Because the output buffers, to a varying degree, share V_{CC} and ground pins, adjustments need to be made to get a more accurate model if all of the outputs are not simulated at the same time. If for example, a single output is to be simulated, the package model for the V_{CC} and GND supplies should be scaled based on the number of outputs which normally share the supplies. If the simulated output normally shares its supplies with two other outputs, the package inductance would be tripled to simulate the same inductive glitch seen on the power pin in an actual application. The capacitive value for the package model is not as critical and thus can be left alone. This method will allow users to more accurately model an output behavior without resorting to more complicated and lengthy simulations. The internal power and ground pins are all powered through a single pin and are basically static, as a result no adjustments are needed for the package models on these supplies.

Table 3 outlines the internal power distribution for the MECL10KH translators, this information can be used to determine the scaling factors for the package inductance for the output buffers. To use the table, simply identify the output in question and divide the number of outputs in the group by the number of power pins for that group, this will give the multiplication factor for the inductance.

Table 3. Power Pin Descriptions

Power Supply	Description
EVCC	EVCC is the most positive supply for the ECL inputs (+5 V for the H350, H351 and H352, and ground for H124–H125).
VEE	V_{EE} is the most negative supply for an ECL gate. For the H350, it is equal to ground; for the H124–125, it is equal to -5.2 V.
TVCC	Internal V_{CC} for TTL circuitry
GNDI	Internal Ground for TTL circuitry

Table 4. Power Pins vs Outputs

Part Type	No. of Outputs	No. of TVCC	No. of TGND
H124	8	1	1
H125	4	1	1
H350	4	2	1
H351	8	4	1
H352	8	4	1

Summary

The information included in this kit should provide the user with all of the information necessary to do SPICE level system interconnect modelling. The schematic information provided in this document is available in netlist form through EMAIL or an IBM or Macintosh disk (for HSPICE and Berkeley SPICE). If, however, the netlists are designed or questions arise about the contents of this document, the user can contact an ECL applications engineer for assistance.

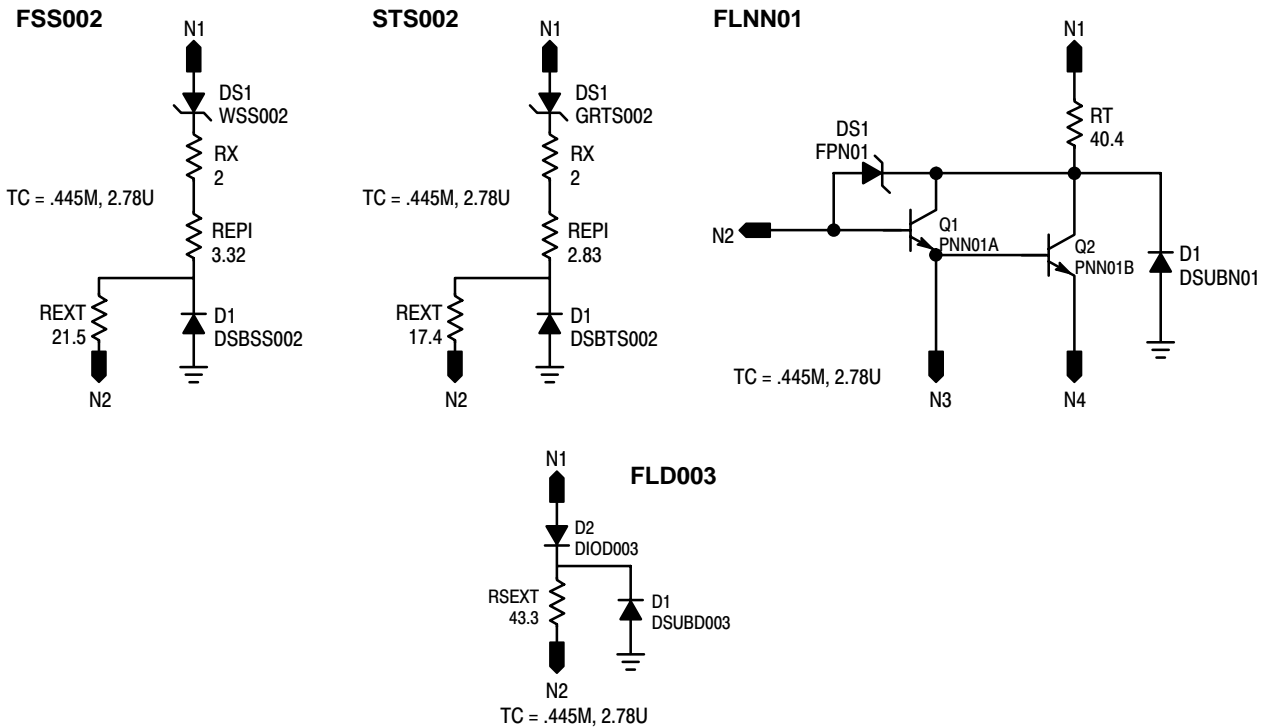


Figure 8. Subcircuits

AN1598/D

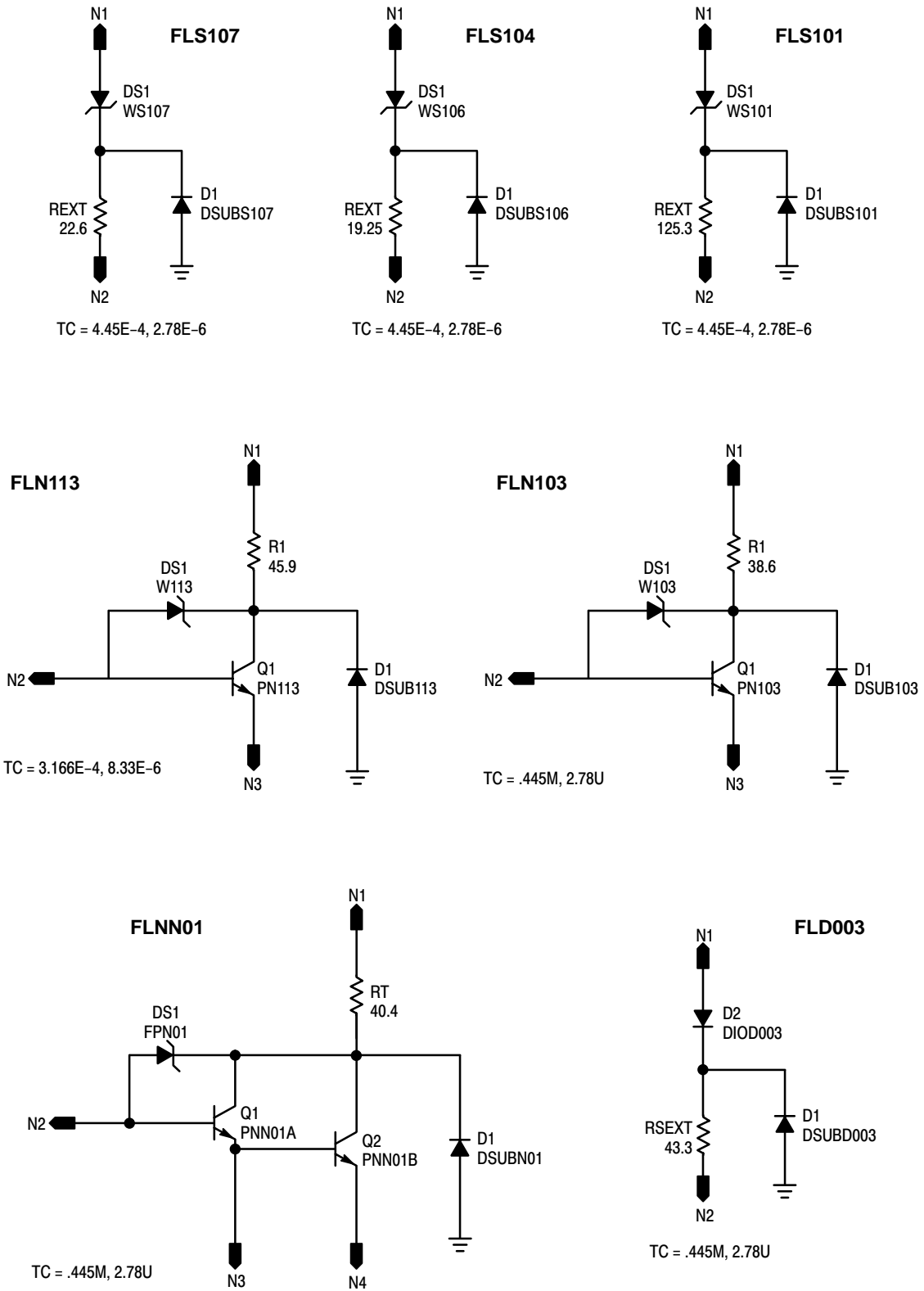


Figure 8. Subcircuits (Continued)

AN1598/D

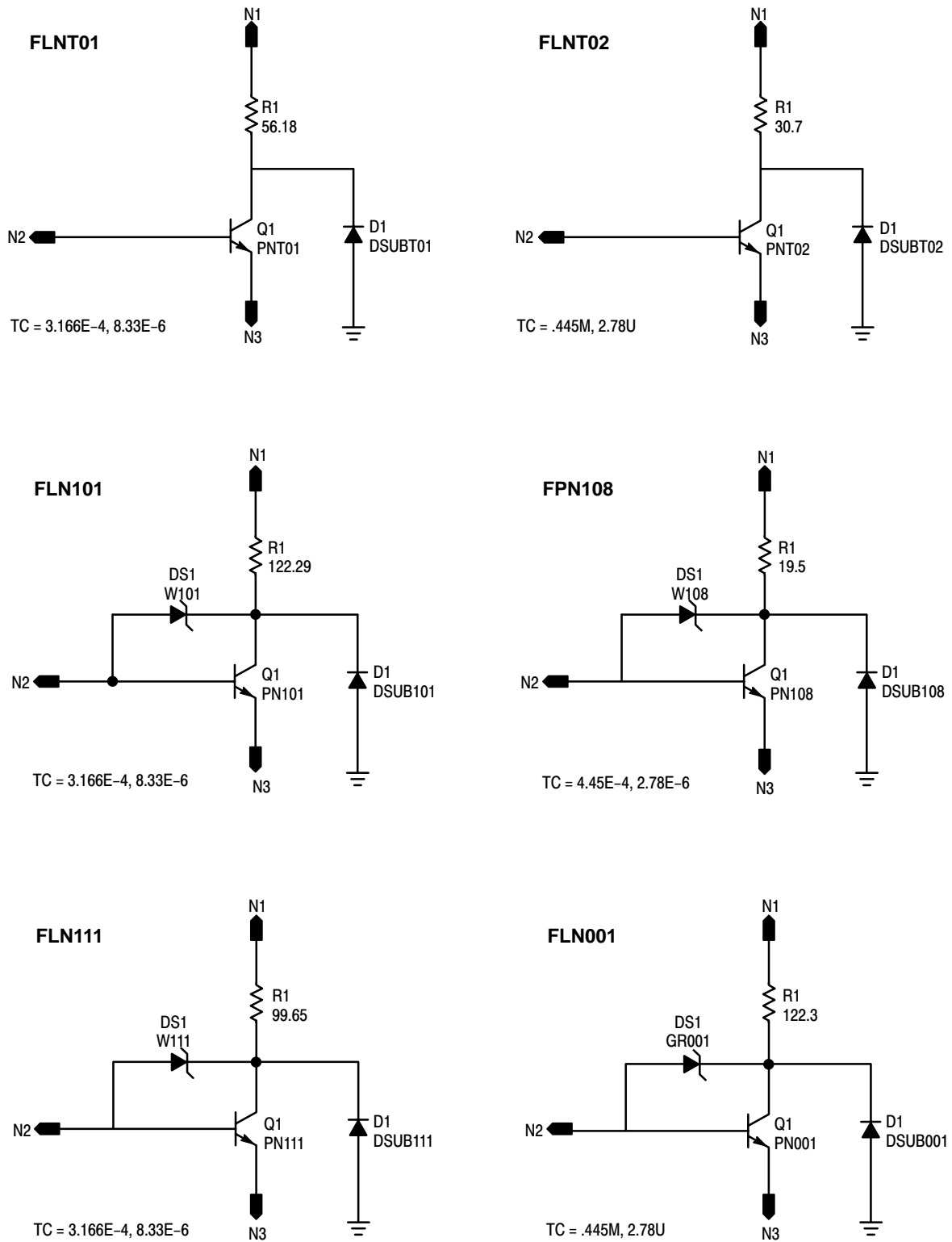


Figure 8. Subcircuits (Continued)

AN1598/D

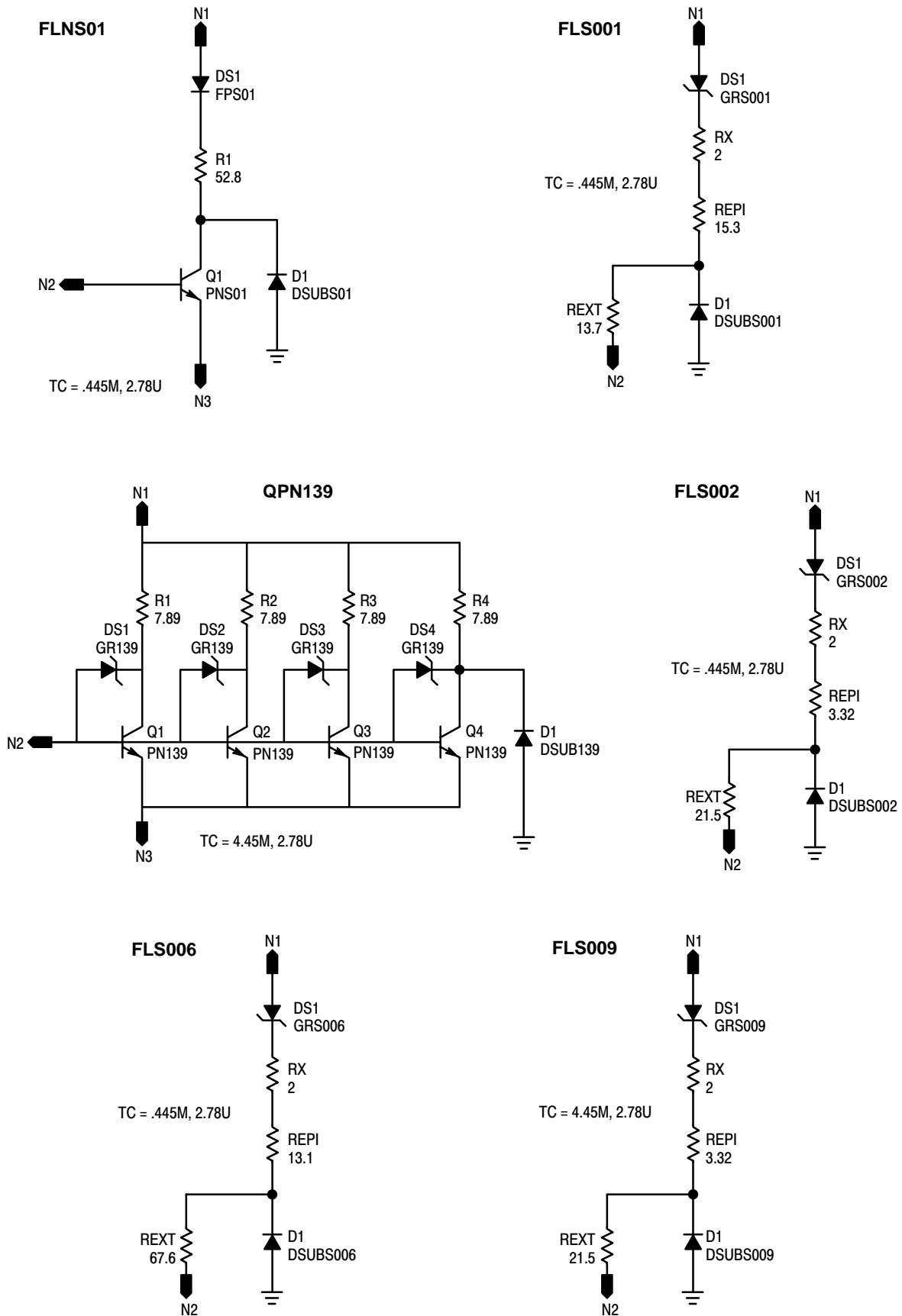


Figure 8. Subcircuits (Continued)

AN1598/D

```
*****
*   PSPICE   *
*****
*   H124,125,350-352 Translator I/O Modelling Kit - Netlist   *
*   Schematics   *
*   *   *
*   The purpose of this document is to provide the netlists *
*   for the various schematics of the H124,125,350-352 Translator *
*   I/O Modelling Kit Application Note. To use these netlists, it *
*   will require a copy of the H124,125,350-352 I/o Spice *
*   Modelling Kit application note. This note is needed to *
*   identify appropriate input and output models for a specific *
*   device. In addition, a copy of this note will help visualize *
*   the netlists and ease the building of the simulation *
*   circuits. *
*   *   *
*           Netlist Organization   *
*   *   *
*   All of the subcircuits are labeled as to what they *
*   represent, (i.e., H124 I/O gate) and are cross referenced *
*   to the figure numbers in the application note. In *
*   addition, all of the subcircuits list the node names for *
*   the specified inputs and outputs for the cell. *
*   The component labels used in the netlists are identical to *
*   those on the schematics in the application note. With the *
*   simplicity of the models, this should allow the user to trace *
*   the netlists back to the schematics. *
*   To ease the task of interconnecting the simulation netlist, *
*   multiple subcircuit models for the different types of *
*   packages are included. The user is expected to call the *
*   subcircuit by the name of the desired translator with an *
*   additional extension that defines the type of used package *
*   (i.e., H124_PLCC20 for a PLCC20 package). These subcircuits *
*   use the pinout as it is printed in the MECL DEVICE DATA Sheet.*
*   The list below provides a summary of the different types of *
*   packages available. *
*   H124,H125,H350 : _DIP16 (16 pin plastic or ceramic *
*                       package), *
*                       _PLCC20 (20 lead PLCC package). *
*   H351,H352 : _DIP20 (20 pin plastic package), *
*               _DIL20 (20 pin ceramic package), *
*               _PLCC20 (20 lead PLCC package). *
*   If all of the outputs are not simulated at the same time, the *
*   unused translator structures may be omitted in the netlist to *
*   shorten simulation time. In that case, the elements in some *
*   of the packages have to be modified according to the hints *
*   that are given in the application note. For that purpose, the *
*   multiplication factor, that is optionally passed to the *
*   package subcircuit as a parameter, might be useful. The *
*   inductance and resistance of the package are multiplied *
*   by the parameter value, whereas the capacitance is to be *
*   divided. This helps to avoid the usage of additional *
*   modified package subcircuits. *
*   *   *
*   The user may notice that there are four terminals on *
*   the transistor models. The fourth terminal represents *
*   the connection to the substrate and is always biased to the *
*   most negative voltage in the schematic. *
*   *   *
*****
```

AN1598/D

```
*****
*
*           Subcircuit Netlists
*
*****
****  H124 16 Pin Plastic or Ceramic Package  (DIP/DIL16)  ****
*
*****
```

```
.SUBCKT H124_DIP16 VCC VEE GND AIN BIN CIN DIN CSTROBE
+
      AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN
V_VCS  VCS      0          -3.9
V_VBB' VBB'     0          -2.1
XP1    BOUT     INT_BOUT  DIP16EP_PKG
XP2    AOUT     INT_AOUT  DIP16EP_PKG
XP3    BOUTN    INT_BOUTN DIP16CP_PKG
XP4    AOUTN    INT_AOUTN DIP16CP_PKG
XP5    AIN      INT_AIN   DIP16CP_PKG
XP6    CSTROBE INT_CSTROBE DIP16CP_PKG
XP7    BIN      INT_BIN   DIP16EP_PKG
XP8    VEE      INT_VEE   DIP16EP_PKG
XP9    VCC      INT_VCC   DIP16EP_PKG
XP10   CIN      INT_CIN   DIP16EP_PKG
XP11   DIN      INT_DIN   DIP16CP_PKG
XP12   COUTN    INT_COUTN DIP16CP_PKG
XP13   DOUTN    INT_DOUTN DIP16CP_PKG
XP14   DOUT     INT_DOUT  DIP16CP_PKG
XP15   COUT     INT_COUT  DIP16EP_PKG
XP16   GND      INT_GND   DIP16EP_PKG
XH124A INT_VCC   INT_GND   INT_VEE VBB' VCS INT_GND INT_AIN
+
      INT_CSTROBE INT_AOUT INT_AOUTN  H124IO
XH124B INT_VCC   INT_GND   INT_VEE VBB' VCS INT_GND INT_BIN
+
      INT_CSTROBE INT_BOUT INT_BOUTN  H124IO
XH124C INT_VCC   INT_GND   INT_VEE VBB' VCS INT_GND INT_CIN
+
      INT_CSTROBE INT_COUT INT_COUTN  H124IO
XH124D INT_VCC   INT_GND   INT_VEE VBB' VCS INT_GND INT_DIN
+
      INT_CSTROBE INT_DOUT INT_DOUTN  H124IO
.ENDS H124_DIP16
```

```
*****           H124 20 lead PLCC Package           *****
*
*****
```

```
.SUBCKT H124_PLCC20 VCC VEE GND AIN BIN CIN DIN CSTROBE
+
      AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN
V_VCS  VCS      0          -3.9
V_VBB' VBB'     0          -2.1
XP2    BOUT     INT_BOUT  PLCC20_PKG
XP3    AOUT     INT_AOUT  PLCC20_PKG
XP4    BOUTN    INT_BOUTN PLCC20_PKG
XP5    AOUTN    INT_AOUTN PLCC20_PKG
XP7    AIN      INT_AIN   PLCC20_PKG
XP8    CSTROBE INT_CSTROBE PLCC20_PKG
XP9    BIN      INT_BIN   PLCC20_PKG
XP10   VEE      INT_VEE   PLCC20_PKG
XP12   VCC      INT_VCC   PLCC20_PKG
XP13   CIN      INT_CIN   PLCC20_PKG
XP14   DIN      INT_DIN   PLCC20_PKG
XP15   COUTN    INT_COUTN PLCC20_PKG
```

AN1598/D

```

XP17  DOUTN   INT_DOUTN  PLCC20_PKG
XP18  DOUT    INT_DOUT   PLCC20_PKG
XP19  COUT    INT_COUT   PLCC20_PKG
XP20  GND     INT_GND    PLCC20_PKG
XH124A INT_VCC  INT_GND  INT_VEE  VBB'  VCS  INT_GND  INT_AIN
+      INT_CSTROBE INT_AOUT INT_AOUTN  H124IO
XH124B INT_VCC  INT_GND  INT_VEE  VBB'  VCS  INT_GND  INT_BIN
+      INT_CSTROBE INT_BOUT INT_BOUTN  H124IO
XH124C INT_VCC  INT_GND  INT_VEE  VBB'  VCS  INT_GND  INT_CIN
+      INT_CSTROBE INT_COUT INT_COUTN  H124IO
XH124D INT_VCC  INT_GND  INT_VEE  VBB'  VCS  INT_GND  INT_DIN
+      INT_CSTROBE INT_DOUT INT_DOUTN  H124IO
.ENDS H124_PLCC20

```

```

*****
*****
****  H125 16 Pin Plastic or Ceramic Package (DIP/DIL16)  ****
*
*****

```

```

.SUBCKT H125_DIP16 VCC VEE GND AIN AINN BIN BINN CIN CINN
+      DIN DINN AOUT BOUT COUT DOUT
V_VCS  VCS      0      -3.9
V_VBB'' VBB''   0      -2.9
XP2    AINN     INT_AINN  DIP16EP_PKG
XP3    AIN      INT_AIN   DIP16CP_PKG
XP4    AOUT     INT_AOUT  DIP16CP_PKG
XP5    BOUT     INT_BOUT  DIP16CP_PKG
XP6    BINN     INT_BINN  DIP16CP_PKG
XP7    BIN      INT_BIN   DIP16EP_PKG
XP8    VEE      INT_VEE   DIP16EP_PKG
XP9    VCC      INT_VCC   DIP16EP_PKG
XP10   CINN     INT_CINN  DIP16EP_PKG
XP11   CIN      INT_CIN   DIP16CP_PKG
XP12   COUT     INT_COUT  DIP16CP_PKG
XP13   DOUT     INT_DOUT  DIP16CP_PKG
XP14   DINN     INT_DINN  DIP16CP_PKG
XP15   DIN      INT_DIN   DIP16EP_PKG
XP16   GND      INT_GND   DIP16EP_PKG
XH125A INT_VCC  INT_GND  INT_VEE  VBB''  VCS  INT_AIN  INT_AINN
+      INT_AOUT      H125IO
XH125B INT_VCC  INT_GND  INT_VEE  VBB''  VCS  INT_BIN  INT_BINN
+      INT_BOUT      H125IO
XH125C INT_VCC  INT_GND  INT_VEE  VBB''  VCS  INT_CIN  INT_CINN
+      INT_COUT      H125IO
XH125D INT_VCC  INT_GND  INT_VEE  VBB''  VCS  INT_DIN  INT_DINN
+      INT_DOUT      H125IO
.ENDS H125_DIP16

```

```

*****          H125 20 lead PLCC Package          *****
*
*****

```

```

.SUBCKT H125_PLCC20 VCC VEE GND AIN AINN BIN BINN CIN CINN
+      DIN DINN AOUT BOUT COUT DOUT
V_VCS  VCS      0      -3.9
V_VBB'' VBB''   0      -2.9
XP3    AINN     INT_AINN  PLCC20_PKG
XP4    AIN      INT_AIN   PLCC20_PKG

```

AN1598/D

```

XP5      AOUT      INT_AOUT    PLCC20_PKG
XP7      BOUT      INT_BOUT    PLCC20_PKG
XP8      BINN      INT_BINN    PLCC20_PKG
XP9      BIN       INT_BIN     PLCC20_PKG
XP10     VEE       INT_VEE     PLCC20_PKG
XP12     VCC       INT_VCC     PLCC20_PKG
XP13     CINN      INT_CINN    PLCC20_PKG
XP14     CIN       INT_CIN     PLCC20_PKG
XP15     COUT      INT_COUT    PLCC20_PKG
XP17     DOUT      INT_DOUT    PLCC20_PKG
XP18     DINN      INT_DINN    PLCC20_PKG
XP19     DIN       INT_DIN     PLCC20_PKG
XP20     GND       INT_GND     PLCC20_PKG
XH125A   INT_VCC INT_GND INT_VEE VBB'' VCS INT_AIN INT_AINN
+        INT_AOUT      H125IO
XH125B   INT_VCC INT_GND INT_VEE VBB'' VCS INT_BIN INT_BINN
+        INT_BOUT      H125IO
XH125C   INT_VCC INT_GND INT_VEE VBB'' VCS INT_CIN INT_CINN
+        INT_COUT      H125IO
XH125D   INT_VCC INT_GND INT_VEE VBB'' VCS INT_DIN INT_DINN
+        INT_DOUT      H125IO
.ENDS H125_PLCC20

```

```

*****
*****
**** H350 16 Pin Plastic or Ceramic Package (DIP/DIL16) ****
*
*****

```

```

.SUBCKT H350_DIP16 TVCC EVCC GND AIN AINN BIN BINN CIN CINN
+        DIN DINN OEN AOUT BOUT COUT DOUT
XP1      EVCC      INT_EVCC    DIP16EP_PKG
XP2      AOUT      INT_AOUT    DIP16EP_PKG
XP3      AIN       INT_AIN     DIP16CP_PKG
XP4      AINN      INT_AINN    DIP16CP_PKG
XP5      BINN      INT_BINN    DIP16CP_PKG
XP6      BIN       INT_BIN     DIP16CP_PKG
XP7      BOUT      INT_BOUT    DIP16EP_PKG
XP8      GND       INT_GND     DIP16EP_PKG
XP9      OEN       INT_OEN     DIP16EP_PKG
XP10     DOUT      INT_DOUT    DIP16EP_PKG
XP11     DIN       INT_DIN     DIP16CP_PKG
XP12     DINN      INT_DINN    DIP16CP_PKG
XP13     CINN      INT_CINN    DIP16CP_PKG
XP14     CIN       INT_CIN     DIP16CP_PKG
XP15     COUT      INT_COUT    DIP16EP_PKG
XP16     TVCC      INT_TVCC    DIP16EP_PKG
XH350A   INT_TVCC INT_EVCC INT_GND INT_AIN INT_AINN INT_OEN
+        INT_AOUT      H350IO
XH350B   INT_TVCC INT_EVCC INT_GND INT_BIN INT_BINN INT_OEN
+        INT_BOUT      H350IO
XH350C   INT_TVCC INT_EVCC INT_GND INT_CIN INT_CINN INT_OEN
+        INT_COUT      H350IO
XH350D   INT_TVCC INT_EVCC INT_GND INT_DIN INT_DINN INT_OEN
+        INT_DOUT      H350IO
.ENDS H350_DIP16

```

AN1598/D

```
*****          H350 20 lead PLCC Package          *****
*                                                                 *
*****
```

```
.SUBCKT H350_PLCC20 TVCC EVCC GND AIN AINN BIN BINN CIN CINN
+          DIN DINN OEN AOUT BOUT COUT DOUT
XP2      EVCC  INT_EVCC  PLCC20_PKG
XP3      AOUT  INT_AOUT  PLCC20_PKG
XP4      AIN   INT_AIN   PLCC20_PKG
XP5      AINN  INT_AINN  PLCC20_PKG
XP7      BINN  INT_BINN  PLCC20_PKG
XP8      BIN   INT_BIN   PLCC20_PKG
XP9      BOUT  INT_BOUT  PLCC20_PKG
XP10     GND   INT_GND   PLCC20_PKG
XP12     OEN   INT_OEN   PLCC20_PKG
XP13     DOUT  INT_DOUT  PLCC20_PKG
XP14     DIN   INT_DIN   PLCC20_PKG
XP15     DINN  INT_DINN  PLCC20_PKG
XP17     CINN  INT_CINN  PLCC20_PKG
XP18     CIN   INT_CIN   PLCC20_PKG
XP19     COUT  INT_COUT  PLCC20_PKG
XP20     TVCC  INT_TVCC  PLCC20_PKG
XH350A   INT_TVCC INT_EVCC INT_GND INT_AIN INT_AINN INT_OEN
+         INT_AOUT      H350IO
XH350B   INT_TVCC INT_EVCC INT_GND INT_BIN INT_BINN INT_OEN
+         INT_BOUT      H350IO
XH350C   INT_TVCC INT_EVCC INT_GND INT_CIN INT_CINN INT_OEN
+         INT_COUT      H350IO
XH350D   INT_TVCC INT_EVCC INT_GND INT_DIN INT_DINN INT_OEN
+         INT_DOUT      H350IO
.ENDS H350_PLCC20
```

```
*****
*****
*****          H351 20 Pin Ceramic Package (DIL20)          *****
*                                                                 *
*                                                                 *
*****
```

```
.SUBCKT H351_DIL20 TVCC EVCC VCC VCC2 GND AIN BIN CIN DIN
+          CSTROBE
+          AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN
V_VCS VCS      0          1.3
XP1    BOUTN   INT_BOUTN   DIL20EP_PKG
XP2    BOUT    INT_BOUT    DIL20EP_PKG
XP4    AOUT    INT_AOUT    DIL20CP_PKG
XP5    AOUTN   INT_AOUTN   DIL20CP_PKG
XP6    VCC     INT_VCC     DIL20CP_PKG
XP7    BIN     INT_BIN     DIL20CP_PKG
XP8    AIN     INT_AIN     DIL20CP_PKG
XP9    CSTROBE INT_CSTROBE DIL20EP_PKG
XP10   GND     INT_GND     DIL20EP_PKG
XP11   TVCC    INT_TVCC    DIL20EP_PKG
XP12   DIN     INT_DIN     DIL20EP_PKG
XP14   CIN     INT_CIN     DIL20CP_PKG
XP15   VCC2    INT_VCC2    DIL20CP_PKG
XP16   DOUTN   INT_DOUTN   DIL20CP_PKG
XP17   DOUT    INT_DOUT    DIL20CP_PKG
XP18   COUT    INT_COUT    DIL20CP_PKG
XP19   COUTN   INT_COUTN   DIL20EP_PKG
```

AN1598/D

```
XP20  EVCC      INT_EVCC   DIL20EP_PKG
XH351A INT_TVCC INT_EVCC VCS INT_VCC INT_GND INT_AIN
+      INT_CSTROBE INT_AOUT INT_AOUTN      H351IO
XH351B INT_TVCC INT_EVCC VCS INT_VCC INT_GND INT_BIN
+      INT_CSTROBE INT_BOUT INT_BOUTN      H351IO
XH351C INT_TVCC INT_EVCC VCS INT_VCC2 INT_GND INT_CIN
+      INT_CSTROBE INT_COUT INT_COUTN      H351IO
XH351D INT_TVCC INT_EVCC VCS INT_VCC2 INT_GND INT_DIN
+      INT_CSTROBE INT_DOUT INT_DOUTN      H351IO
.ENDS H351_DIL20
```

```
*****          H351 20 Pin Plastic Package (DIP20)          *****
*                                                                 *
*                                                                 *
*****
```

```
.SUBCKT H351_DIP20 TVCC EVCC VCC VCC2 GND AIN BIN CIN DIN
+          CSTROBE
+          AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN
V_VCS VCS      0          1.3
XP1   BOUTN    INT_BOUTN  DIP20EP_PKG
XP2   BOUT     INT_BOUT   DIP20EP_PKG
XP4   AOUT     INT_AOUT   DIP20CP_PKG
XP5   AOUTN    INT_AOUTN  DIP20CP_PKG
XP6   VCC      INT_VCC    DIP20CP_PKG
XP7   BIN      INT_BIN    DIP20CP_PKG
XP8   AIN      INT_AIN    DIP20CP_PKG
XP9   CSTROBE INT_CSTROBE DIP20EP_PKG
XP10  GND      INT_GND    DIP20EP_PKG
XP11  TVCC     INT_TVCC   DIP20EP_PKG
XP12  DIN      INT_DIN    DIP20EP_PKG
XP14  CIN      INT_CIN    DIP20CP_PKG
XP15  VCC2     INT_VCC2   DIP20CP_PKG
XP16  DOUTN    INT_DOUTN  DIP20CP_PKG
XP17  DOUT     INT_DOUT   DIP20CP_PKG
XP18  COUT     INT_COUT   DIP20CP_PKG
XP19  COUTN    INT_COUTN  DIP20EP_PKG
XP20  EVCC     INT_EVCC   DIP20EP_PKG
XH351A INT_TVCC INT_EVCC VCS INT_VCC INT_GND INT_AIN
+      INT_CSTROBE INT_AOUT INT_AOUTN      H351IO
XH351B INT_TVCC INT_EVCC VCS INT_VCC INT_GND INT_BIN
+      INT_CSTROBE INT_BOUT INT_BOUTN      H351IO
XH351C INT_TVCC INT_EVCC VCS INT_VCC2 INT_GND INT_CIN
+      INT_CSTROBE INT_COUT INT_COUTN      H351IO
XH351D INT_TVCC INT_EVCC VCS INT_VCC2 INT_GND INT_DIN
+      INT_CSTROBE INT_DOUT INT_DOUTN      H351IO
.ENDS H351_DIP20
```

```
*****          H351 20 lead PLCC Package          *****
*                                                                 *
*                                                                 *
*****
```

```
.SUBCKT H351_PLCC20 TVCC EVCC VCC VCC2 GND AIN BIN CIN DIN
+          CSTROBE
+          AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN
V_VCS VCS      0          1.3
XP1   BOUTN    INT_BOUTN  PLCC20_PKG
```

AN1598/D

```

XP2  BOUT      INT_BOUT      PLCC20_PKG
XP4  AOUT      INT_AOUT      PLCC20_PKG
XP5  AOUTN     INT_AOUTN     PLCC20_PKG
XP6  VCC       INT_VCC       PLCC20_PKG
XP7  BIN       INT_BIN       PLCC20_PKG
XP8  AIN       INT_AIN       PLCC20_PKG
XP9  CSTROBE  INT_CSTROBE  PLCC20_PKG
XP10 GND       INT_GND       PLCC20_PKG
XP11 TVCC      INT_TVCC      PLCC20_PKG
XP12 DIN      INT_DIN      PLCC20_PKG
XP14 CIN      INT_CIN      PLCC20_PKG
XP15 VCC2     INT_VCC2     PLCC20_PKG
XP16 DOUTN    INT_DOUTN    PLCC20_PKG
XP17 DOUT     INT_DOUT     PLCC20_PKG
XP18 COUT     INT_COUT     PLCC20_PKG
XP19 COUTN    INT_COUTN    PLCC20_PKG
XP20 EVCC     INT_EVCC     PLCC20_PKG
XH351A INT_TVCC INT_EVCC VCS INT_VCC INT_GND INT_AIN
+      INT_CSTROBE INT_AOUT INT_AOUTN      H351IO
XH351B INT_TVCC INT_EVCC VCS INT_VCC INT_GND INT_BIN
+      INT_CSTROBE INT_BOUT INT_BOUTN      H351IO
XH351C INT_TVCC INT_EVCC VCS INT_VCC2 INT_GND INT_CIN
+      INT_CSTROBE INT_COUT INT_COUTN      H351IO
XH351D INT_TVCC INT_EVCC VCS INT_VCC2 INT_GND INT_DIN
+      INT_CSTROBE INT_DOUT INT_DOUTN      H351IO
.ENDS H351_PLCC20

```

```

*****
*****
*****      H352 20 Pin Ceramic Package (DIL20)      *****
*
*
*
*****

```

```

.SUBCKT H352_DIL20 CVCC EVCC VCC VCC2 GND AIN BIN CIN DIN
+
+      CSTROBE
+      AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN

```

```

V_VCS VCS      0          1.3
XP1  BOUTN     INT_BOUTN   DIL20EP_PKG
XP2  BOUT      INT_BOUT    DIL20EP_PKG
XP4  AOUT      INT_AOUT    DIL20CP_PKG
XP5  AOUTN     INT_AOUTN   DIL20CP_PKG
XP6  VCC       INT_VCC     DIL20CP_PKG
XP7  BIN       INT_BIN     DIL20CP_PKG
XP8  AIN       INT_AIN     DIL20CP_PKG
XP9  CSTROBE  INT_CSTROBE  DIL20EP_PKG
XP10 GND       INT_GND     DIL20EP_PKG
XP11 CVCC     INT_CVCC     DIL20EP_PKG
XP12 DIN      INT_DIN     DIL20EP_PKG
XP14 CIN      INT_CIN     DIL20CP_PKG
XP15 VCC2     INT_VCC2     DIL20CP_PKG
XP16 DOUTN    INT_DOUTN    DIL20CP_PKG
XP17 DOUT     INT_DOUT     DIL20CP_PKG
XP18 COUT     INT_COUT     DIL20CP_PKG
XP19 COUTN    INT_COUTN    DIL20EP_PKG
XP20 EVCC     INT_EVCC     DIL20EP_PKG
XH352A INT_CVCC INT_EVCC VCS INT_VCC INT_GND INT_AIN
+      INT_CSTROBE INT_AOUT INT_AOUTN      H352IO
XH352B INT_CVCC INT_EVCC VCS INT_VCC INT_GND INT_BIN
+      INT_CSTROBE INT_BOUT INT_BOUTN      H352IO

```


AN1598/D

```
XH352C INT_CVCC INT_EVCC VCS INT_VCC2 INT_GND INT_CIN
+ INT_CSTROBE INT_COUT INT_COUTN H352IO
XH352D INT_CVCC INT_EVCC VCS INT_VCC2 INT_GND INT_DIN
+ INT_CSTROBE INT_DOUT INT_DOUTN H352IO
.ENDS H352_DIL20
```

```
***** H352 20 Pin Plastic Package (DIP20) *****
*
*
*****
```

```
.SUBCKT H352_DIP20 CVCC EVCC VCC VCC2 GND AIN BIN CIN DIN
+ CSTROBE
+ AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN
```

```
V_VCS VCS 0 1.3
XP1 BOUTN INT_BOUTN DIP20EP_PKG
XP2 BOUT INT_BOUT DIP20EP_PKG
XP4 AOUT INT_AOUT DIP20CP_PKG
XP5 AOUTN INT_AOUTN DIP20CP_PKG
XP6 VCC INT_VCC DIP20CP_PKG
XP7 BIN INT_BIN DIP20CP_PKG
XP8 AIN INT_AIN DIP20CP_PKG
XP9 CSTROBE INT_CSTROBE DIP20EP_PKG
XP10 GND INT_GND DIP20EP_PKG
XP11 CVCC INT_CVCC DIP20EP_PKG
XP12 DIN INT_DIN DIP20EP_PKG
XP14 CIN INT_CIN DIP20CP_PKG
XP15 VCC2 INT_VCC2 DIP20CP_PKG
XP16 DOUTN INT_DOUTN DIP20CP_PKG
XP17 DOUT INT_DOUT DIP20CP_PKG
XP18 COUT INT_COUT DIP20CP_PKG
XP19 COUTN INT_COUTN DIP20EP_PKG
XP20 EVCC INT_EVCC DIP20EP_PKG
```

```
XH352A INT_CVCC INT_EVCC VCS INT_VCC INT_GND INT_AIN
+ INT_CSTROBE INT_AOUT INT_AOUTN H352IO
XH352B INT_CVCC INT_EVCC VCS INT_VCC INT_GND INT_BIN
+ INT_CSTROBE INT_BOUT INT_BOUTN H352IO
XH352C INT_CVCC INT_EVCC VCS INT_VCC2 INT_GND INT_CIN
+ INT_CSTROBE INT_COUT INT_COUTN H352IO
XH352D INT_CVCC INT_EVCC VCS INT_VCC2 INT_GND INT_DIN
+ INT_CSTROBE INT_DOUT INT_DOUTN H352IO
.ENDS H352_DIP20
```

```
***** H352 20 lead PLCC Package *****
*
*
*****
```

```
.SUBCKT H352_PLCC20 CVCC EVCC VCC VCC2 GND AIN BIN CIN DIN
+ CSTROBE
+ AOUT AOUTN BOUT BOUTN COUT COUTN DOUT DOUTN
```

```
V_VCS VCS 0 1.3
XP1 BOUTN INT_BOUTN PLCC20_PKG
XP2 BOUT INT_BOUT PLCC20_PKG
XP4 AOUT INT_AOUT PLCC20_PKG
XP5 AOUTN INT_AOUTN PLCC20_PKG
XP6 VCC INT_VCC PLCC20_PKG
```

AN1598/D

```
XP7  BIN      INT_BIN      PLCC20_PKG
XP8  AIN      INT_AIN      PLCC20_PKG
XP9  CSTROBE  INT_CSTROBE PLCC20_PKG
XP10 GND       INT_GND      PLCC20_PKG
XP11 CVCC     INT_CVCC     PLCC20_PKG
XP12 DIN     INT_DIN      PLCC20_PKG
XP14 CIN     INT_CIN      PLCC20_PKG
XP15 VCC2     INT_VCC2     PLCC20_PKG
XP16 DOUTN   INT_DOUTN    PLCC20_PKG
XP17 DOUT     INT_DOUT     PLCC20_PKG
XP18 COUT     INT_COUT     PLCC20_PKG
XP19 COUTN   INT_COUTN    PLCC20_PKG
XP20 EVCC     INT_EVCC     PLCC20_PKG
XH351A INT_CVCC INT_EVCC VCS INT_VCC INT_GND INT_AIN
+ INT_CSTROBE INT_AOUT INT_AOUTN H352IO
XH351B INT_CVCC INT_EVCC VCS INT_VCC INT_GND INT_BIN
+ INT_CSTROBE INT_BOUT INT_BOUTN H352IO
XH351C INT_CVCC INT_EVCC VCS INT_VCC2 INT_GND INT_CIN
+ INT_CSTROBE INT_COUT INT_COUTN H352IO
XH351D INT_CVCC INT_EVCC VCS INT_VCC2 INT_GND INT_DIN
+ INT_CSTROBE INT_DOUT INT_DOUTN H352IO
.ENDS H352_PLCC20
```

```
***** H124 I/O Gate (NO TAG) *****
* *
*****
```

```
.SUBCKT H124IO TVCC EVCC VEE VBB' VCS EVCCO IN CSTROBE OUT OUTB
Q1  2 4 5 VEE      T08I3
Q2  EVCC 9 12 VEE  T08I3
Q3  9 VCS 10 VEE  T06B4
Q4  12 VCS 13 VEE T06B4
Q5  16 12 17 VEE  T08I3
Q6  21 VBB' 17 VEE T08I2
Q7  17 VCS 18 VEE T12B4
Q8  EVCCO 21 OUT VEE T8106
Q9  EVCCO 16 OUTB VEE T8106
XD3  4 IN          FLD003
XD4  4 CSTROBE     FLD003
Q12  5 5 6 VEE     T08I3
Q13  6 6 7 VEE     T08I3
XD7  7 EVCC        FLD003
XR1  TVCC 2 TVCC   RES params: R=216
XR2  2 4 TVCC      RES params: R=809
XR3  7 9 TVCC      RES params: R=426
XR4  10 VEE TVCC   RES params: R=225
XR5  13 VEE TVCC   RES params: R=225
XR6  EVCC 16 EVCC  RES params: R=222
XR7  EVCC 21 EVCC  RES params: R=222
XR8  18 VEE EVCC   RES params: R=111
.ENDS H124IO
```

```
***** H125 I/O Gate (NO TAG) *****
* *
* *
*****
```

```
.SUBCKT H125IO TVCC GNDI VEE VBB'' VCS IN INN OUT
Q1  11 VCS 12 VEE  T12B1
```

AN1598/D

```

Q2      6 11 GNDI VEE      T16I3
Q3      6 4 7 VEE          T16I3
Q4      6 VBB'' 7 VEE      T16I3
Q5      7 VCS 8 VEE        T18B1
Q6      TVCC 15 20 VEE     T16I2
Q7      22 23 7 VEE        T16I3
XQ8     TVCC 6 26 OUT       FLNN01
Q9      OUT 22 GNDI VEE    T025E
Q10     17 17 18 VEE       T12B1
Q11     18 18 GNDI VEE     T12B1
QRXCX2  TVCC IN TVCC VEE   RXCX1
QRXCX1  TVCC INN TVCC VEE  RXCX1
XDS1    26 6               FSS002
XDS2    GNDI OUT           STS002
XRB1    IN 23 TVCC         RES params: R=75
XRB2    INN 4 TVCC         RES params: R=75
XR1     TVCC 6 TVCC        RES params: R=795
XR2     TVCC 11 TVCC       RES params: R=7000
XR3     12 VEE TVCC        RES params: R=475
XR4     8 VEE TVCC         RES params: R=75
XR5     TVCC 15 TVCC       RES params: R=987
XR6     15 17 TVCC         RES params: R=1314
XR7     20 22 TVCC         RES params: R=400
XR8     26 OUT TVCC        RES params: R=20000
.ENDS H125IO

```

```

*****          H350 I/O Gate  (NO TAG)          *****
*
*
*****

```

```

.SUBCKT H350IO TVCC EVCC VEE IN INN OEN OUT
Q1      EVCC 2 9 VEE      T04I3
Q2      EVCC 4 15 VEE     T04I3
Q3      9 9 12 VEE        T04I3
Q4      15 15 19 VEE      T04I3
Q5      14 14 VEE VEE     T04I3
Q6      18 14 VEE VEE     T04I3
Q7      TVCC 21 18 VEE    T04I3
XQ8     21 18 VEE         FLNS01
XQ9     33 31 25          FLN001
XQ10    TVCC 25 57 OUT    FLNN01
XQ11    25 23 26          FLN113
XQ12    26 27 VEE         FLN113
XQ13    37 35 VEE         FLN103
XQ14    39 38 VEE         FLN103
XQ15    OUT 26 VEE        QPN139
Q16     9 10 9 VEE        C90PF
Q17     15 16 15 VEE      C90PF
XQ20    EVCC 47 50        FLNT02
XQ21    EVCC 50 32        FLNT01
XQ22    43 41 44          FLN111
XQ23    47 44 48          FPN108
XQ24    32 48 VEE         QPN139
XQ25    54 53 32          FLN101
XQ26    29 54 VEE         FLN101
QRXCX2  EVCC 4 EVCC VEE  RXCX1
QRXCX1  EVCC 2 EVCC VEE  RXCX1
XD1     38 57             FLD003
XD20    41 OEN            FLS001
XDS1    23 21             FLS107

```

AN1598/D

```

XDS2  31 32          FLS107
XDS3  25 32          FLS107
XDS4  23 32          FLS107
XDS5  57 33          FLS104
XDS6  OUT 33         FLS001
XDS7  26 38          FLS101
XDS8  26 39          FLS101
XDS9  VEE OUT       FLS002
XDS20 44 OEN        FLS001
XDS21 VEE OEN       FLS002
XR1   IN 2 EVCC     RES params: R=75
XR2   INN 4 EVCC    RES params: R=75
XR1   10 14 EVCC    RES params: R=150
XR2   12 14 EVCC    RES params: R=2500
XR3   16 18 EVCC    RES params: R=150
XR4   19 18 EVCC    RES params: R=2500
XR5   27 29 TVCC    RES params: R=500
XR6   TVCC 21 TVCC  RES params: R=30000
XR7   TVCC 23 TVCC  RES params: R=6000
XR8   TVCC 25 TVCC  RES params: R=3000
XR9   TVCC 31 TVCC  RES params: R=5000
XR10  57 VEE TVCC   RES params: R=26260
XR11  26 35 TVCC   RES params: R=1000
XR12  26 37 TVCC   RES params: R=1500
XR20  EVCC 41 EVCC  RES params: R=10000
XR21  EVCC 43 EVCC  RES params: R=4220
XR22  EVCC 47 EVCC  RES params: R=1470
XR23  50 32 EVCC   RES params: R=5000
XR24  44 VEE EVCC   RES params: R=8660
XR25  48 VEE EVCC   RES params: R=2760
XR26  EVCC 53 EVCC  RES params: R=19000
XR27  EVCC 29 EVCC  RES params: R=6160
.ENDS H350IO

```

```

*****          H351 I/O Gate (NO TAG)          *****
*                                                         *
*                                                         *
*****

```

```

.SUBCKT H351IO TVCC EVCC VCS EVCCO GNDI IN STROBE OUT OUTB
Q1  GNDI STROBE 2      TPNP2
Q2  4 4 5 GNDI        T08I3
Q3  5 5 6 GNDI        T08I3
Q4  6 6 7 GNDI        T08I3
Q5  GNDI IN 2         TPNP2
Q6  7 7 GNDI GNDI     T08I3
Q7  9 2 10 GNDI       T08I3
Q8  14 15 10 GNDI     T08I3
Q9  EVCC 9 EVCC GNDI  C15PF
Q10 EVCC 14 EVCC GNDI C15PF
Q11 10 VCS 11 GNDI    T12B1
Q12 EVCCO 14 OUT GNDI T5406
Q13 EVCCO 9 OUTB GNDI T5406
Q14 15 GNDI 15 GNDI   C60PF
Q15 EVCC 17 15 GNDI   T12B1
Q16 17 17 18 GNDI     T12B1
Q17 18 18 19 GNDI     T12B1
Q18 19 19 20 GNDI     T12B1
Q19 20 20 GNDI GNDI   T12B1
Q20 15 20 GNDI GNDI   T12B1
XDS1 GNDI IN          FLS009

```

AN1598/D

```
XDS2 GNDI STROBE      FLS009
XDS3 2 4              FLS006
XR1  TVCC 2 TVCC      RES params: R=2000
XR2  TVCC 4 TVCC      RES params: R=5000
XR3  EVCC 9 EVCC      RES params: R=249
XR4  EVCC 14 EVCC     RES params: R= 249
XR5  11 GNDI EVCC     RES params: R=110
XR6  EVCC 17 EVCC     RES params: R=1500
.ENDS H351IO
```

```
*****          H352 I/O Gate  (NO TAG)          *****
*                                                                 *
*                                                                 *
*****
```

```
.SUBCKT H352IO CVCC EVCC VCS EVCCO GNDI IN STROBE OUT OUTB
Q1  GNDI STROBE 2      TPNP2
Q2  4 4 5 GNDI        T08I3
Q3  5 5 6 GNDI        T08I3
Q4  6 6 7 GNDI        T08I3
Q5  GNDI IN 2         TPNP2
Q6  7 7 GNDI GNDI     T08I3
Q7  9 2 10 GNDI       T08I3
Q8  14 15 10 GNDI     T08I3
Q9  EVCC 9 EVCC GNDI  C15PF
Q10 EVCC 14 EVCC GNDI C15PF
Q11 10 VCS 11 GNDI    T12B1
Q12 EVCCO 14 OUT GNDI T5406
Q13 EVCCO 9 OUTB GNDI T5406
Q14 15 GNDI 15 GNDI   C60PF
Q15 EVCC 17 15 GNDI   T12B1
Q16 17 17 18 GNDI     T12B1
Q17 18 18 19 GNDI     T12B1
Q18 19 19 20 GNDI     T12B1
Q19 20 20 GNDI GNDI   T12B1
Q20 15 20 GNDI GNDI   T12B1
Q21 CVCC 2 21 GNDI    T08I3
XDS2 GNDI IN          FLS009
XDS3 GNDI STROBE      FLS009
XDS1 2 4              FLS006

XR1  CVCC 2 CVCC      RES params: R=2000
XR2  CVCC 4 CVCC      RES params: R=5000
XR3  EVCC 9 EVCC      RES params: R=249
XR4  EVCC 14 EVCC     RES params: R=249
XR5  11 GNDI EVCC     RES params: R=110
XR6  EVCC 17 EVCC     RES params: R=1500
XR7  21 GNDI EVCC     RES params: R=4000
.ENDS H352IO
```

AN1598/D

```
***** SUBCIRCUITS (NO TAG) *****
*****
*****
***** FLS001 *****
*
*****
```

```
.SUBCKT FLS001 N1 N2
RX 3 4 2.0 TC=.445M,2.78U
REPI 4 5 15.3 TC=.445M,2.78U
REXT 5 N2 13.7 TC=.445M,2.78U
DS1 N1 3 GRS001
D1 0 5 DSUBS001
.ENDS FLS001
```

```
***** FLS002 *****
*
*****
```

```
.SUBCKT FLS002 N1 N2
RX 3 4 2.0 TC=.445M,2.78U
REPI 4 5 3.32 TC=.445M,2.78U
REXT 5 N2 21.5 TC=.445M,2.78U
DS1 N1 3 GRS002
D1 0 5 DSUBS002
.ENDS FLS002
```

```
***** FLS006 *****
*
*****
```

```
.SUBCKT FLS006 N1 N2
RX 3 4 2.0 TC=.445M,2.78U
REPI 4 5 13.1 TC=.445M,2.78U
REXT 5 N2 67.6 TC=.445M,2.78U
DS1 N1 3 GRS006
D1 0 5 DSUBS006
.ENDS FLS006
```

```
***** FLS009 *****
*
*****
```

```
.SUBCKT FLS009 N1 N2
RX 3 4 2.0 TC=4.45M,2.78U
REPI 4 5 3.32 TC=4.45M,2.78U
REXT 5 N2 21.5 TC=4.45M,2.78U
DS1 N1 3 GRS009
D1 0 5 DSUBS009
.ENDS FLS009
```

AN1598/D

***** FSS002 *****
* *

.SUBCKT FSS002 N1 N2
RX 3 4 2.0 TC=.445M,2.78U
REPI 4 5 3.32 TC=.445M,2.78U
REXT 5 N2 21.5 TC=.445M,2.78U
DS1 N1 3 WSS002
D1 0 5 DSBSS002
.ENDS FSS002

***** STS002 *****
* *

.SUBCKT STS002 N1 N2
RX 3 4 2.0 TC=.445M,2.78U
REPI 4 5 2.83 TC=.445M,2.78U
REXT 5 N2 17.4 TC=.445M,2.78U
DS1 N1 3 GRYS002
D1 0 5 DSBTS002
.ENDS STS002

***** FLD003 *****
* *

.SUBCKT FLD003 N1 N2
RSEXT 3 N2 43.3 TC=.445M,2.78U
D2 N1 3 DIOD003
D1 0 3 DSUBD003
.ENDS FLD003

***** FLS101 *****
* *

.SUBCKT FLS101 N1 N2
REXT 3 N2 125.3 TC=4.45E-4,2.78E-6
DS1 N1 3 WS101
D1 0 3 DSUBS101
.ENDS FLS101

***** FLS104 *****
* *

.SUBCKT FLS104 N1 N2
REXT 3 N2 19.25 TC=4.45E-4,2.78E-6
DS1 N1 3 WS106
D1 0 3 DSUBS106
.ENDS FLS104

AN1598/D

* FLS107 *

.SUBCKT FLS107 N1 N2
REXT 3 N2 22.6 TC=4.45E-4,2.78E-6
DS1 N1 3 WS107
D1 0 3 DSUBS107
.ENDS FLS107

* FLNN01 *

.SUBCKT FLNN01 N1 N2 N3 N4
Q1 5 N2 N3 0 PNN01A
Q2 5 N3 N4 0 PNN01B
RT N1 5 40.4 TC=.445M,2.78U
D1 0 5 DSUBN01
DS1 N2 5 FPN01
.ENDS FLNN01

* QPN139 *

.SUBCKT QPN139 N1 N2 N3
Q1 4 N2 N3 0 PN139
Q2 5 N2 N3 0 PN139
Q3 6 N2 N3 0 PN139
Q4 7 N2 N3 0 PN139
R1 N1 4 7.89 TC=4.45M,2.78U
R2 N1 5 7.89 TC=4.45M,2.78U
R3 N1 6 7.89 TC=4.45M,2.78U
R4 N1 7 7.89 TC=4.45M,2.78U
DS1 N2 4 GR139
DS2 N2 5 GR139
DS3 N2 6 GR139
DS4 N2 7 GR139
D1 0 7 DSUB139
.ENDS QPN139

* FLN113 *

.SUBCKT FLN113 N1 N2 N3
Q1 4 N2 N3 0 PN113
R1 N1 4 45.9 TC=3.166E-4,8.33E-6
D1 0 4 DSUB113
DS1 N2 4 W113
.ENDS FLN113

AN1598/D

```
*****
                                FLN103
                                *****
*
*****
*****

.SUBCKT FLN103 N1 N2 N3
Q1  4 N2 N3 0  PN103
R1  N1 4      38.6 TC=.445M,2.78U
D1  0 4      DSUB103
DS1 N2 4      W103
.ENDS FLN103
```

```
*****
                                FLN101
                                *****
*
*****
*****

.SUBCKT FLN101 N1 N2 N3
Q1  4 N2 N3 0  PN101
R1  N1 4      122.29 TC=3.166E-4,8.33E-6
D1  0 4      DSUB101
DS1 N2 4      W101
.ENDS FLN101
```

```
*****
                                FLNT01
                                *****
*
*****
*****

.SUBCKT FLNT01 N1 N2 N3
Q1  4 N2 N3 0  PNT01
R1  N1 4      56.18 TC=3.166E-4,8.33E-6
D1  0 4      DSUBT01
.ENDS FLNT01
```

```
*****
                                FLNT02
                                *****
*
*****
*****

.SUBCKT FLNT02 N1 N2 N3
Q1  4 N2 N3 0  PNT02
R1  N1 4      30.7 TC=.445M,2.78U
D1  0 4      DSUBT02
.ENDS FLNT02
```

```
*****
                                FLN001
                                *****
*
*****
*****

.SUBCKT FLN001 N1 N2 N3
Q1  4 N2 N3 0  PN001
R1  N1 4      122.3 TC=.445M,2.78U
D1  0 4      DSUB001
DS1 N2 4      GR001
.ENDS FLN001
```

AN1598/D

```
*****
                                FLN111
                                *****
*
*
*****

.SUBCKT FLN111 N1 N2 N3
Q1  4 N2 N3 0  PN111
R1  N1 4      99.65 TC=3.166E-4,8.33E-6
D1  0 4      DSUB111
DS1 N2 4      W111
.ENDS FLN111
```

```
*****
                                FPN108
                                *****
*
*
*****

.SUBCKT FPN108 N1 N2 N3
Q1  4 N2 N3 0  PN108
R1  N1 4      19.5
D1  0 4      DSUB108
DS1 N2 4      W108
.ENDS FPN108
```

```
*****
                                FLNS01
                                *****
*
*
*****

.SUBCKT FLNS01 N1 N2 N3
Q1  5 N2 N3 0  PNS01
R1  4 5      52.8 TC=4.45E-4,2.78E-6
D1  0 5      DSUBS01
DS1 N1 4      FPS01
.ENDS FLNS01
```

AN1598/D

```
***** Package Models (NO TAG) *****
*
*
* Package Model (20-lead PLCC)
*****
```

```
.SUBCKT PLCC20_PKG EXT INT params: MULT=1.0
CPKG 1 0 {1.5PF/MULT}
RPKG1 EXT 1 {MULT*750}
RPKG2 1 2 {MULT*750}
RPKG3 2 INT {MULT*0.2}
LPKG1 EXT 1 {MULT*3.5NH}
LPKG2 1 2 {MULT*3.5NH}
.ENDS PLCC20_PKG
```

```
*****
*
* Package Model (16-Pin DIP/DIL Center Pin)
*****
```

```
.SUBCKT DIP16CP_PKG EXT INT params: MULT=1.0
CPKG 1 0 {0.7PF/MULT}
RPKG1 EXT 1 {MULT*750}
RPKG2 1 2 {MULT*750}
RPKG3 2 INT {MULT*0.1}
LPKG1 EXT 1 {MULT*2.5NH}
LPKG2 1 2 {MULT*2.5NH}
.ENDS DIP16CP_PKG
```

```
*****
*
* Package Model (16-Pin DIP/DIL End Pin)
*****
```

```
.SUBCKT DIP16EP_PKG EXT INT params: MULT=1.0
CPKG 1 0 {1.3PF/MULT}
RPKG1 EXT 1 {MULT*750}
RPKG2 1 2 {MULT*750}
RPKG3 2 INT {MULT*0.1}
LPKG1 EXT 1 {MULT*5.5NH}
LPKG2 1 2 {MULT*5.5NH}
.ENDS DIP16EP_PKG
```

```
*****
*
* Package Model (20-Pin DIL Center Pin)
*****
```

```
.SUBCKT DIL20CP_PKG EXT INT params: MULT=1.0
CPKG 1 0 {0.81PF/MULT}
RPKG1 EXT 1 {MULT*750}
RPKG2 1 2 {MULT*750}
RPKG3 2 INT {MULT*0.036}
LPKG1 EXT 1 {MULT*4.85NH}
LPKG2 1 2 {MULT*4.85NH}
.ENDS DIL20CP_PKG
```

AN1598/D

```
*****
*
* Package Model (20-Pin DIL End Pin)
*****
```

```
.SUBCKT DIL20EP_PKG EXT INT params: MULT=1.0
CPKG 1 0 {2.76PF/MULT}
RPKG1 EXT 1 {MULT*750}
RPKG2 1 2 {MULT*750}
RPKG3 2 INT {MULT*0.063}
LPKG1 EXT 1 {MULT*7.17NH}
LPKG2 1 2 {MULT*7.17NH}
.ENDS DIL20EP_PKG
```

```
*****
*
* Package Model (20-Pin DIP Center Pin)
*****
```

```
.SUBCKT DIP20CP_PKG EXT INT params: MULT=1.0
CPKG 1 0 {0.68PF/MULT}
RPKG1 EXT 1 {MULT*750}
RPKG2 1 2 {MULT*750}
RPKG3 2 INT {MULT*0.03}
LPKG1 EXT 1 {MULT*2.99NH}
LPKG2 1 2 {MULT*2.99NH}
.ENDS DIP20CP_PKG
```

```
*****
*
* Package Model (20-Pin DIP End Pin)
*****
```

```
.SUBCKT DIP20EP_PKG EXT INT params: MULT=1.0
CPKG 1 0 {1.26PF/MULT}
RPKG1 EXT 1 {MULT*750}
RPKG2 1 2 {MULT*750}
RPKG3 2 INT {MULT*0.05}
LPKG1 EXT 1 {MULT*6.7NH}
LPKG2 1 2 {MULT*6.7NH}
.ENDS DIP20EP_PKG
```

AN1598/D

```
***** Resistor Model (NO TAG) *****
*
*
* Resistor with parasitic capacitance
*****
```

```
.SUBCKT RES POS NEG VCC1 params: R=50
R1A POS 1 {R/2} TC=431.6U,8.97U
R1B NEG 1 {R/2} TC=431.6U,8.97U
DR 1 VCC1 RES-DIODE
.ENDS RES
```

```
***** SPICE Parameter List *****
*
* TTL Subcircuit Models
*
*****
```

```
.MODEL DSUB101 D (CJO=104FF VJ=.51 M=.24)
.MODEL PN101 NPN (IS=7E-18 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=0.1 NR=1 XCJC=0.1 VAR=100
+ IKR=.3MA ISC=7.59E-17 NC=1 RB=1441 RBM=400
+ RE=0 RC=217.6
+ CJE=41.3FF VJE=.9 MJE=.4
+ CJC=32.2FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=1.64MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL W101 D (IS=2.15E-13 RS=123.4 N=1.044 TT=10PS
+ CJO=28.8FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB103 D (CJO=309.7FF VJ=.51 M=.24)
.MODEL PN103 NPN (IS=1.89E-16 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=.1 NR=1 XCJC=0.1 VAR=100
+ IKR=8.1MA ISC=2.24E-16 NC=1 RB=715.6 RBM=98.4
+ RE=0 RC=8.06
+ CJE=646.4FF VJE=.9 MJE=.4
+ CJC=171.9FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=10A PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=.5)
.MODEL W103 D (IS=5.39E-13 RS=49.2 N=1.044 TT=10PS
+ CJO=72.2FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB111 D (CJO=122FF VJ=.51 M=.24)
.MODEL PN111 NPN (IS=1.05E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=0.1 NR=1 XCJC=0.1 VAR=100
+ IKR=.45MA ISC=1.14E-16 NC=1 RB=1010 RBM=315.7
+ RE=0 RC=145
+ CJE=57.8FF VJE=.9 MJE=.4
+ CJC=39FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=2.46MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL W111 D (IS=4.8E-13 RS=68.2 N=1.044 TT=10PS
+ CJO=64.3FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
**** FLN113 ****
.MODEL DSUB113 D (CJO=182FF VJ=.51 M=.24)
.MODEL PN113 NPN (IS=2.45E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=0.1 NR=1 XCJC=0.1 VAR=100
+ IKR=1MA ISC=2.66E-16 NC=1 RB=469 RBM=171
+ RE=0 RC=62.2
```

AN1598/D

```
+ CJE=123FF VJE=.9 MJE=.4
+ CJC=69FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=5.74MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL W113 D (IS=7.41E-13 RS=43 N=1.044 TT=10PS
+ CJO=99FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS01 D (CJO=164.4FF VJ=.51 M=.24)
.MODEL PNS01 NPN (IS=2.1E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=.1 NR=1 XCJC=0.1 VAR=100
+ IKR=.9MA ISC=2.48E-17 NC=1 RB=573 RBM=225.8
+ RE=0 RC=72.5
+ CJE=107FF VJE=.9 MJE=.4
+ CJC=67.5FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=10A PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=.5)
.MODEL FPS01 D (IS=1.8E-13 RS=0 N=1.044 TT=10PS
+ CJO=151.1FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBN01 D (CJO=1.785PF VJ=.51 M=.24)
.MODEL PNN01A NPN (IS=1.68E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=.1 NR=1 XCJC=0.1 VAR=100
+ IKR=.72MA ISC=1.99E-17 NC=1 RB=982.1 RBM=357.1
+ RE=0 RC=90.7
+ CJE=83.6FF VJE=.9 MJE=.4
+ CJC=57FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=10A PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=.5)
.MODEL PNN01B NPN (IS=3.64E-16 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=.1 NR=1 XCJC=0.1 VAR=100
+ IKR=7.8MA ISC=2.15E-16 NC=1 RB=374.5 RBM=54.1
+ RE=0 RC=4.18
+ CJE=606.8FF VJE=.9 MJE=.4
+ CJC=160.4FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=10A PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=.5)
.MODEL FPN01 D (IS=8.63E-14 RS=39.4 N=1.044 TT=10PS
+ CJO=72.3FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL WS107 D (IS=1.49E-12 RS=14 N=1.044 TT=10PS
+ CJO=200FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS107 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=221FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL GRS001 D (IS=4.27E-14 RS=52.8 N=1.044 TT=10PS
+ CJO=54FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS001 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=87.7FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL GRS002 D (IS=5.43E-13 RS=4.15 N=1.044 TT=10PS
+ CJO=54FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS002 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=593FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL GRTS002 D (IS=6.84E-13 RS=3.3 N=1.044 TT=10PS
+ CJO=865FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSBTS002 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=673FF VJ=.51 M=.24
```

AN1598/D

```
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL WSS002 D (IS=7.52E-13 RS=28.3 N=1.044 TT=10PS
+ CJO=100.8FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=35)
.MODEL DSBSS002 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=97.8FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DIOD003 D (IS=5.73E-17 RS=2.98 N=1 TT=500PS
+ CJO=199.1FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DSUBD003 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=276.8FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DSUB001 D (CJO=105FF VJ=.51 M=.24)
.MODEL PN001 NPN (IS=7E-18 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=0.1 NR=1 XCJC=0.1 VAR=100
+ IKR=.3MA ISC=7.59E-17 NC=1 RB=1341 RBM=300
+ RE=0 RC=217.6
+ CJE=41FF VJE=.9 MJE=.4
+ CJC=59FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=1.64MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL GR001 D (IS=3.8E-14 RS=88 N=1.044 TT=10PS
+ CJO=48FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS009 D (CJO=106FF VJ=.51 M=.24)
.MODEL PN009E NPN (IS=3.92E-16 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+ IKR=.3MA ISC=4.25E-15 NC=1 RB=185 RBM=39
+ RE=0 RC=3.9
+ CJE=1.37PF VJE=.9 MJE=.4
+ CJC=609FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=1.64MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL GRS009 D (IS=5.4E-13 RS=9.57 N=1.044 TT=10PS
+ CJO=683FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBT01 D (CJO=155FF VJ=.51 M=.24)
.MODEL PNT01 NPN (IS=2.73E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=0.1 NR=1 XCJC=0.1 VAR=100
+ IKR=1.17MA ISC=2.96E-16 NC=1 RB=566.4 RBM=181.8
+ RE=0 RC=55.79
+ CJE=129.5FF VJE=.9 MJE=.4
+ CJC=73.4FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=6.4MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL DSUBT02 D (CJO=97.8FF VJ=.51 M=.24)
.MODEL PNT02 NPN (IS=7.0E-18 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=.1 NR=1 XCJC=0.1 VAR=100
+ IKR=.3MA ISC=8.28E-18 NC=1 RB=1475 RBM=433
+ RE=0 RC=217.6
+ CJE=41.3FF VJE=.9 MJE=.4
+ CJC=35.4FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=10A PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=.5)
.MODEL DSUBS106 D (CJO=149.4FF VJ=.51 M=.24)
.MODEL WS106 D (IS=3.91E-13 RS=98.9 N=1.044 TT=10PS
+ CJO=52.4FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB139 D (CJO=2.12PF VJ=.51 M=.24)
.MODEL PN139 NPN (IS=1.03E-16 BF=113 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
```

AN1598/D

```
+ IKR=4.4MA ISC=1.22E-16 NC=1 RB=117 RBM=47
+ RE=0 RC=8.41
+ CJE=493FF VJE=.9 MJE=.4
+ CJC=244FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=96.7MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL GR139 D (IS=7E-14 RS=10 N=1.044 TT=10PS
+ CJO=88FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB108 D (CJO=163FF VJ=.51 M=.24)
.MODEL PN108 NPN (IS=1.75E-17 BF=113 NF=1.008 VAF=30 IKF=10a
+ ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+ IKR=.75MA ISC=1.9E-16 NC=1 RB=638.8 RBM=222
+ RE=0 RC=87
+ CJE=90.6FF VJE=.9 MJE=.4
+ CJC=50.3FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=4.1MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5)
.MODEL W108 D (IS=5.1E-13 RS=58.8 N=1.044 TT=10PS
+ CJO=68.3FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL GRS006 D (IS=6.39E-14 RS=35 N=1.044 TT=10PS
+ CJO=81FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS006 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=149FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL WS101 D (IS=1.9E-13 RS=111 N=1.044 TT=10PS
+ CJO=25.6FF VJ=.4 M=.33
+ EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS101 D (IS=1E-16 RS=0 N=1 TT=500PS
+ CJO=63.2FF VJ=.51 M=.24
+ EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL FSS002 D IS=7.56E-13
*
```

```
*****
* MECL10KH Transistor Models *
* *
*****
```

```
.MODEL T04I3 NPN
+ IS=2.78E-17 BF=85 RB=707 RC=180 RE=12 BR=5
+ CJE=.04E-12 CJC=.13E-12 CJS=.18E-12
.MODEL T06B4 NPN
+ IS=4.048E-17 BF=85 RB=1330 BR=5 RE=7.5
+ RC=121.2 CJE=.06E-12 CJC=.1E-12 CJS=.161E-12
.MODEL T08I2 NPN
+ IS=2.6E-17 BF=85 RB=470 BR=5
+ RC=163 RE=7.5 CJE=6.53E-14 CJC=1.235E-13 CJS=1.338E-13
.MODEL T025E NPN
+ IS=1.3E-15 BF=85 RB=64.5 BR=5
+ RC=5.68 RE=.2
.MODEL T08I3 NPN
+ IS=4.189E-17 BF=85 RB=450 BR=5
+ RC=118.9 RE=7.5 CJE=6.5E-14 CJC=1.72E-13 CJS=2.08E-13
.MODEL T12B1 NPN
+ IS=7.53E-17 BF=85 RB=707 BR=5
+ RC=87.8 RE=3.75 CJE=.11E-12 CJC=.14E-12 CJS=.14E-12
.MODEL T12B4 NPN
+ IS=17E-17 BF=85 RB=750 BR=5
```


AN1598/D

```
+ RC=25.27 CJE=1.14E-13 CJC=1.3E-13 CJS=1.477E-13
.MODEL T16I3 NPN
+ IS=7.96E-17 BF=85 RB=240 BR=5
+ RC=63.1 RE=3.75 CJE=.12E-12 CJC=.27E-12 CJS=.25E-12
.MODEL T16I2 NPN
+ IS=7.96E-17 BF=85 RB=240 BR=5
+ RC=88.6 RE=3.75 CJE=.12E-12 CJC=.25E-12 CJS=.18E-12
.MODEL T18B1 NPN
+ IS=1.10E-16 BF=85 RB=456 BR=5
+ RC=61.3 RE=2.5 CJE=.17E-12 CJC=.19E-12 CJS=.19E-12
.MODEL T5406 NPN
+ IS=3.3E-16 BF=85 RB=86.6 BR=5
+ RC=23.6 RE=.833 CJE=.495E-12 CJC=.722E-12 CJS=.576E-12
.MODEL T8106 NPN
+ IS=1.6E-16 BF=85 RB=61.1 BR=5
+ RC=16 RE=.57 CJE=.726E-12 CJC=.556E-12 CJS=.724E-12
.MODEL TPNP2 PNP
+ IS=7.69E-17 BF=5 BR=1 RB=164 RC=56 CJE=.086E-12
+ CJC=1.4E-12
.MODEL C15PF NPN
+ IS=8.9426E-16 BF=85 BR=5 RB=1016.2 RC=27 RE=.2
+ CJE=1.2E-12 CJC=.64E-12 CJS=.4E-12
.MODEL RXCX1 NPN
+ IS=4.6077E-16 BF=85 BR=5 RB=7084 RC=24 RE=.5
+ CJE=.647E-12 CJC=3.855E-12 CJS=.786E-12
.MODEL C60PF NPN
+ IS=8.8224E-16 BF=85 BR=5 RB=141 RC=16 RE=.3
+ CJE=3.657E-12 CJC=2.927E-12 CJS=1.029E-12
.MODEL C90PF NPN
+ IS=1.419E-15 BF=85 BR=5 RB=16 RC=9 RE=.4
+ CJE=5.325E-12 CJC=4.452E-12 CJS=1.448E-12

*****
*                               Resistor Diode Model                               *
*                                                                                       *
*****

.MODEL RES-DIODE D
+ IS=3.7E-16 CJO=4.14E-13
```

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada

Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.