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AN-9740
Bi-Directional Translator Architectures

Introduction

Voltage translators, or "level shifters" as they are sometimes called, allow the coupling of signals that do not share common V_{CC} domains. For example, a signal generated from a 1.0 V device may need to connect to a 3.3 V device. In Figure 1, the FXLP34 voltage translator can be used to level shift 1.0 V signals from device A to 3.3 V signals at device B.

Uni-Directional Voltage Translation

The voltage translation of Figure 1 is simple to implement in a design. As long as the VCCA pin of the translator agrees with the V_{CC} of device A, the VCCB pin of the translator agrees with the V_{CC} of device B, and VCCA and VCCB are within their respective specified operating voltage ranges; device B automatically receive a valid 3.3V signal from device A, even though device A generates only a 1.0 V signal. The FXLP34 translator delivers 2.6 mA of DC drive when VCCB equals 3 V.

The Figure 1 translator is limited to level shifting from device A to device B. This translator is considered uni-directional. Some level shifting applications require bi-directional functionality, as seen in Figure 2.

Bi-Directional Voltage Translation

The FXLH1T45 translator of Figure 2 provides bi-directional level shifting, where the direction is determined by the DIR pin. If DIR is LOW, device B transmits to device A (receiver). If DIR is HIGH, device A transmits to device B (receiver). To minimize bus contention, device A and device B should disable (3-state) their respective I/O pins during direction change. The FXLH1T45 delivers 18 mA of DC drive when the output V_{CC} equals 3 V.

The bi-directional translator of Figure 2 is somewhat limited because the burden of direction control is on either device A or device B. This limitation led to the innovation of the "auto-direction" translator of Figure 3.

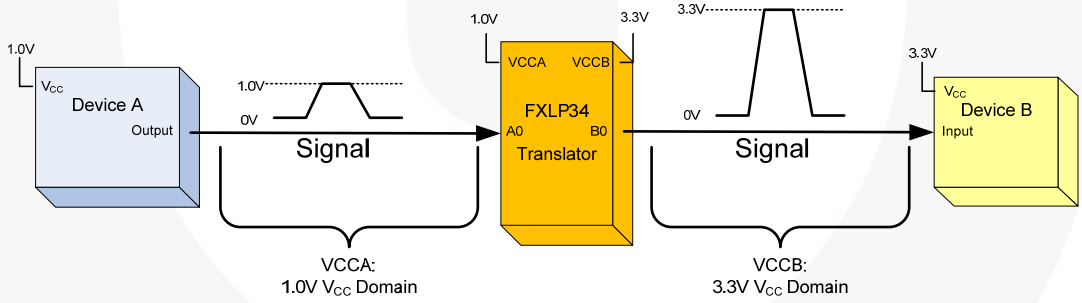

Figure 1. FXLP34 Uni-Directional Translator

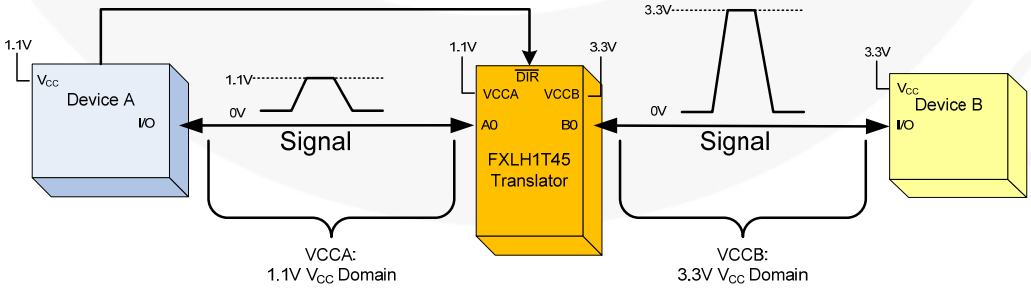

Figure 2. FXLH1T45 Bi-Directional Translator

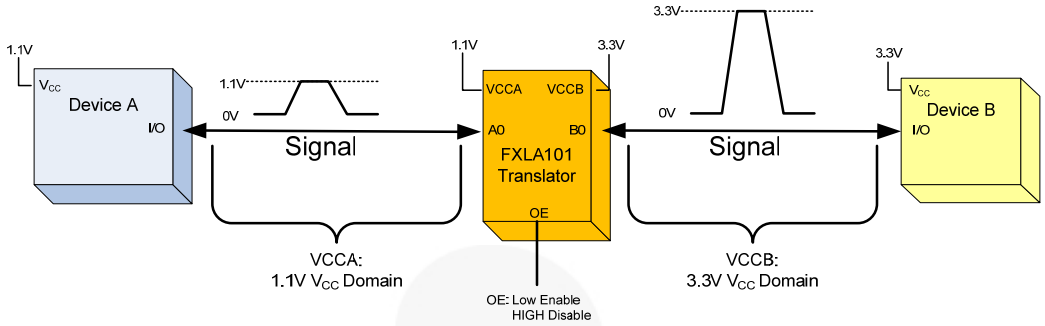

Figure 3. FXLA101 Auto-Direction Bus Hold Translator

The auto-direction translator of Figure 3 does not require a direction pin. It performs automatic bi-directional level shifting between device A and device B with a proprietary circuit called Bus Hold.

Bus Hold

Figure 4 illustrates the basic functionality of the bus hold circuit. Essentially, the dynamic driver is a strong driver, on the order of 20 mA - 30 mA (depending on the V_{CC}), that temporarily turns on for approximately 10 - 40 ns after detecting a LOW-to-HIGH or HIGH-to-LOW edge on either the A or B side. After the dynamic driver has turned off (timed out), a weaker driver holds the state previously delivered by the dynamic driver. This weaker bus hold driver is on until the next external A or B side LOW-to-HIGH or HIGH-to-LOW transition is sensed. Typically, 500 µA of external sourcing or sinking is required to override the bus hold by an external device.

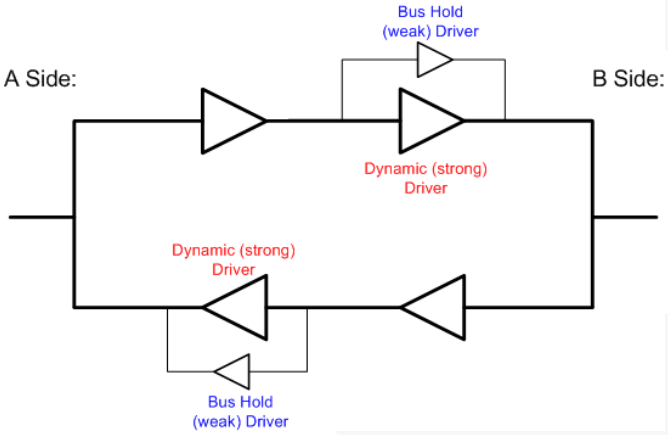

Figure 4. Bus Hold Block Diagram, One Channel

The strong driver quickly charges and discharges capacitive transmission lines. The bus hold dynamic driver is designed to drive a minimum of 50 pF. During bus hold, power consumption is minimized, where I_{CC} is typically under 5 µA.

Figure 5 illustrates a more detailed view of the bus hold auto-direction architecture. The edge detectors on the A and B ports are responsible, for sensing edges on either port that are meant to override a currently held state. Any time one edge detector senses an edge, it automatically turns off the opposite edge detector. Then the edge detector that sensed an edge sets the appropriate direction control to trigger the appropriate dynamic driver for that direction. The dynamic driver is turned on for approximately 10 ns – 40 ns until the time out expires. The opposite edge detector is disabled during this 10 ns – 40 ns time. After the timeout has elapsed, the "holder" driver continues holding the current state with a weak drive strength from 100 µA - 500 µA, depending on the referenced V_{CC}, and both edge detectors are enabled.

In summary, the "holders" on the A and B ports are the weak drivers responsible for holding the current voltage state. The A and B port dynamic drivers (with timeout) are the strong drivers responsible for temporarily hard driving a new state sensed by the edge detector circuit. The MUX is responsible for changing ownership of the bus hold. If OE is enabled, A holds the B port and B holds the A port. If OE is disabled, A holds the A port and B holds the B port.

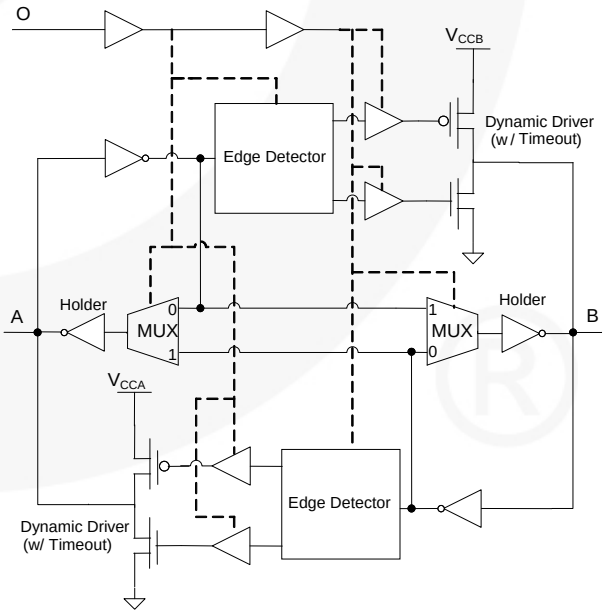

Figure 5. Bus Hold Block Detailed Diagram, One Channel

Bus Hold AC Parameters

The strength of the strong output driver during LH / HL transitions is captured by the dynamic output current HIGH / LOW (I_{OLH}, I_{OHD}) plot in Figure 6. Because the strong output driver is turned on only during LH/HL transitions, the actual drive current is difficult to measure directly. Approximate the drive current with the following formulas:

$$I_{OHD} \approx (C_L + C_{IO}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{IO}) \times \frac{(20\% - 80\%) * V_{CC0}}{t_{RISE}} \quad (1)$$

$$I_{OLD} \approx (C_L + C_{IO}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{IO}) \times \frac{(80\% - 20\%) * V_{CC0}}{t_{FALL}} \quad (2)$$

where $C_{I/O}$ = the typical lumped capacitance and V_{CCO} is the supply voltage of the output driver.

Figure 6 depicts typical dynamic output current of the auto-direction bus hold Architecture with a lumped load capacitance of 4 pF. The bus hold dynamic driver is designed to drive a minimum of 50 pF.

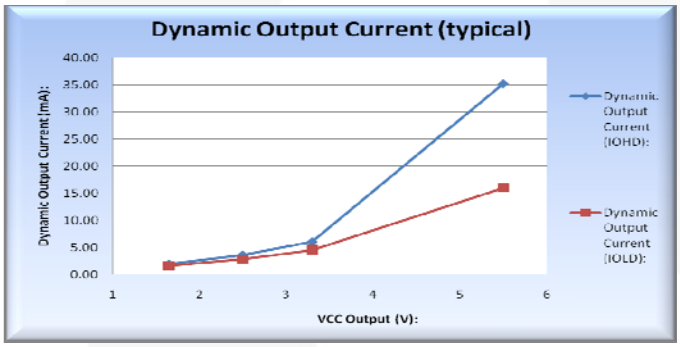

Figure 6. Dynamic Output Current of Auto-Direction Bus Hold

Bus Hold DC Parameters

In addition to the above AC parameters (I_{OHD} and I_{OLD}), there are three fundamental DC parameters pertaining to the Bus Hold Circuitry:

1. $I_{I(HOLD)}$: Bus-Hold Input Minimum Drive Current
2. $I_{I(ODH)}$: Bus-Hold Input Overdrive High Current
3. $I_{I(ODL)}$: Bus-Hold Input Overdrive Low Current

Bus Hold Minimum Drive Current

Specifies the minimum amount of current the bus hold driver can source/sink. The BUS hold minimum drive current (I_{IHOLD}) is V_{CC} dependent and guaranteed in the DC electrical tables of the datasheet. The intent is to maintain a valid state after the dynamic driver has timed out, but can be overridden when a data transition is required.

Bus Hold Input Overdrive Drive Current

Specifies the minimum amount of current required (by an external device) to overdrive the bus hold in the event of a direction change. The bus hold overdrive (I_{IODH}, I_{IODL}) is V_{CC} dependent and guaranteed in the DC electrical tables of the datasheet.

Auto-Direction Hybrid Driver Architecture

The auto-direction bus hold architecture is well suited for push / pull driver environments and should not be used in open-drain environments where pull-up resistors are used. Pull-up resistors conflict with the bus hold circuitry, resulting in unwanted behavior.

To provide the auto-direction feature for open-drain environments using pull-up resistors, the hybrid driver architecture like Figure 7 is required.

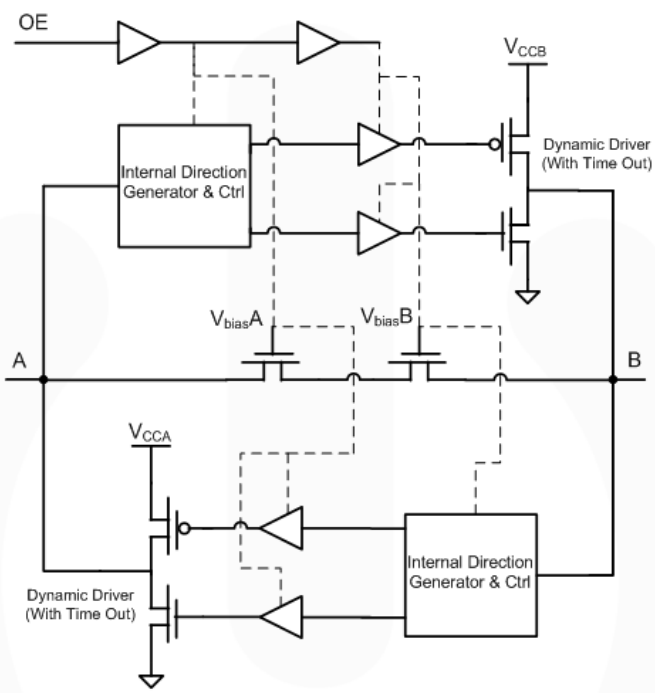

Figure 7. Hybrid Driver Block Diagram, One Channel

I^2C is a very common application for open-drain level shifting and is a driving force behind the hybrid driver architecture design. The FXMA2102 I^2C / SMBUS translator (Figure 8) uses the hybrid driver of Figure 7.

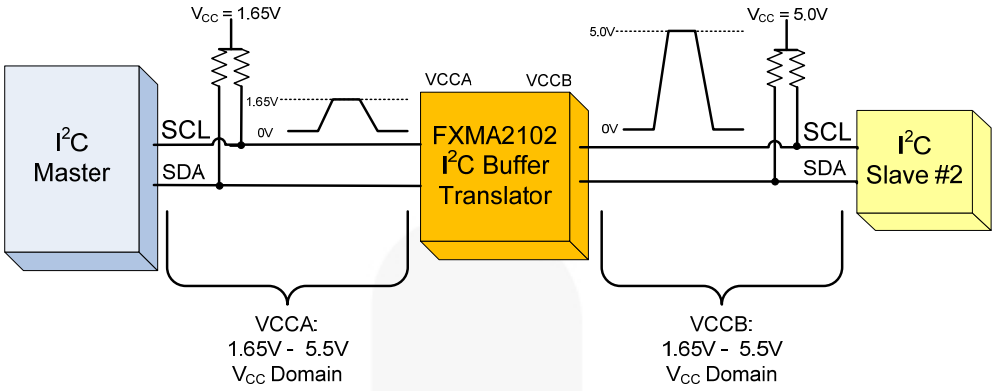

Figure 8. FXMA2102 I²C/SMBUS Translator Application

Hybrid Architecture Theory of Operation and I²C

The FXMA2102 is designed for high-performance level shifting and buffer / repeating in an I²C application. Figure 7 shows that each bi-directional channel contains two series Npassgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I²C application where auto-direction is a necessity.

For example, during the following three I2C protocol events, the bus direction needs to change from master to slave or from slave to master without the occurrence of an edge:

- Clock Stretching
- Slave's ACK Bit (9^{th} bit = 0) Following a Master's Write Bit (8^{th} bit = 0)
- Clock Synchronization and Multi Master Arbitration

If there is an I²C translator between the master and slave in these examples, the I²C translator must change direction when both A and B ports are LOW. The Npassgates can accomplish this task very efficiently because, when both A and B ports are LOW, the Npassgates act as a low resistive short between the two (A and B) ports.

Due to I²C's open-drain topology, I²C masters and slaves are not push/pull drivers. Logic LOWs are "pulled down" (I_{sink}), while logic HIGHs are "let go" (3-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant, where R = R_{PU} and C = the bus capacitance. If the FXMA2102 is attached to the master [on the A port] in this example, and there is a slave on the B port, the Npassgates act as a low resistive short between both ports until either of the port's V_{CC}/2 thresholds are reached. After the RC time constant has reached the V_{CC}/2 threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot in Figure 9. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports because both the Npassgates are turned off. If a master or slave device decides to pull SCL or SDA LOW, that device's driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or B port V_{CC}/2 threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

The auto-direction hybrid driver architecture is designed to drive a minimum of 400 pF. 400 pF is the maximum capacitance of an I²C segment. The FXMA2102 scope shot of Figure 9 reflects a (30% - 70%) rise time of 112ns, with a 600 pF lumped load and a 2.2 kΩ external pull-up resistor. According to the I²C specification, the maximum rise time in Fast Mode (400KHz) is 300ns, so the FXMA2102 is a strong choice for the I²C application. *For more information about the FXMA2102 I²C translator, please see application note AN-9718.*

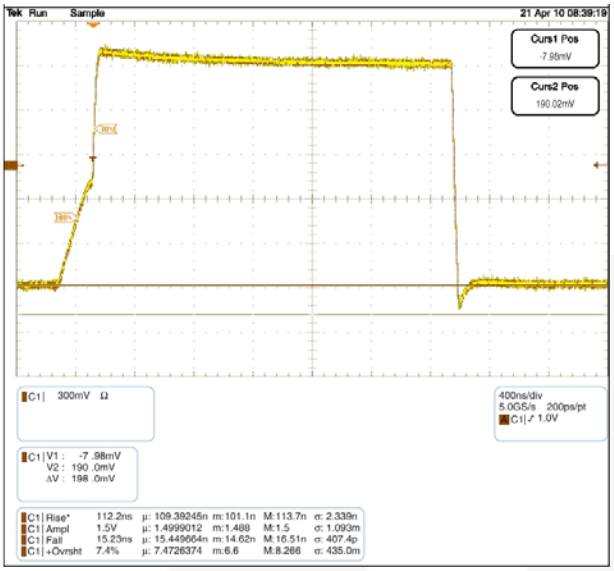

Figure 9. Hybrid Driver Scope Shot 600 pF||2.2 kΩ

Hybrid Architecture and Push-Pull

While the bus hold auto-direction architecture cannot be used for open-drain environments, the hybrid driver architecture can be used for open-drain environments as well as push-pull environments, as long as pull-up resistors are present on the A-side and B-side IOs.

Architecture Bandwidth

This note has discussed three different architectures for bi-directional level shifting:

- Bi-directional with a direction pin
- Auto-direction with BUS hold
- Auto-direction with hybrid driver

Of the three, bi-directional level shifting architectures discussed, auto-direction hybrid in an open-drain environment is the slowest. This is due to the intrinsic bandwidth limiting, LOW-to-HIGH transition RC time constant before the edge rate accelerators trigger. Given a push / pull environment, all three bi-direction architectures exhibit similar bandwidth, mainly limited by their respective V_{CC} translation combinations. Most Fairchild translator datasheets publish maximum data rates vs. V_{CC} combinations. The worst-case data rate is typically when either $V_{CCA/B}$ is at its lowest rated value.

Direction Change Time

There may be instances when an application requires very fast latency for the direction change. Both auto-direction architectures; bus hold and hybrid, offer slower "direction change times" (40ns typical) vs. the bi-directional architecture (4ns typical) requiring the direction pin. If fast direction time is critical, and the system can provide direction pin control, then the bi-directional with direction pin architecture may be a better choice over the auto-direction architectures.

For example, the application in Figure 10 illustrates a proprietary chip-to-chip interface where the clock requires uni-directional level shifting from 1.2 V to 3.3 V at 60 MHz. Meanwhile, the data signal needs to be translated from 1.2 V to 3.3 V at 60 Mbps (30 MHz) in both directions. The direction change needs to occur within one clock cycle or 16.7 ns. The FXL2TD245 is a better choice for this application vs. a BUS hold type auto-direction translator (like the FXLA102) because the FXL2TD245 direction change is much faster.

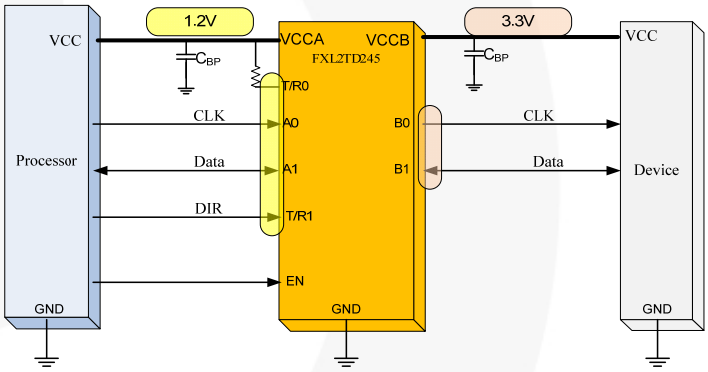

Figure 10. Proprietary Chip-to-Chip 60 MHz Three-Wire Interface

The simulation (worst-case slow process and -40°C temperature) excerpt shown in Figure 11, assuming a load of 5 pF||10 kΩ, reveals that the FXL2TD245 successfully changes direction within one 16.7 ns clock cycle.

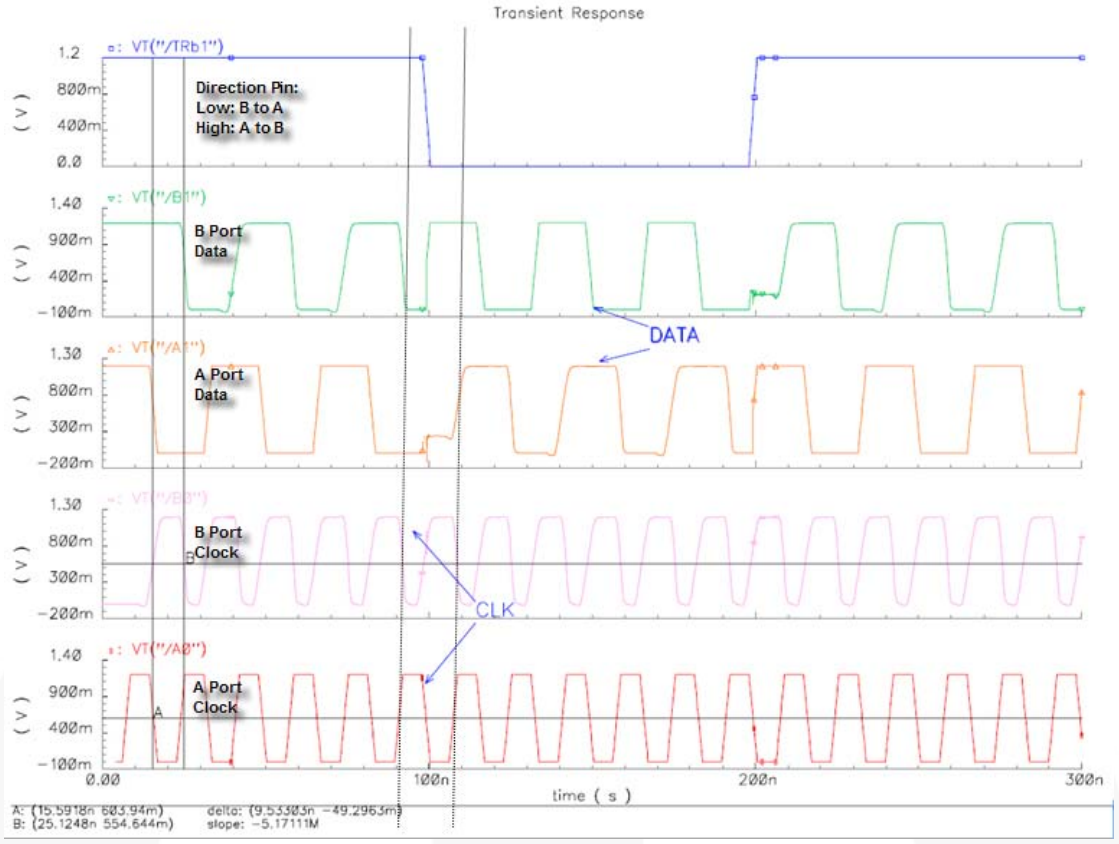

Figure 11.Proprietary Chip-to-Chip Interface Direction Change Timing

Table 1 illustrates the relationship between direction change time and V_{CC} translation range. 0 reflects the worst-case direction change times with respect to process and temperature variation. FXM devices level shift from 1.65 V to 5.5 V in either direction. FXL devices level shift from 1.1 V to 3.6 V in either direction. The direction change delays of 0 are dominated by the Dynamic Driver timeouts of Figure 5 (BUS hold) and Figure 7 (hybrid). While the dynamic driver accelerates the edge in one direction, the opposite edge detection is disabled. By definition, direction change is inhibited until the dynamic driver edge rate accelerator has elapsed

Hybrid Driver Applications

Aside from the I^2C and SMBUS applications, the hybrid driver is a great fit for level shifting the I/O pin of the SIM card interface.

Table 1. Direction Change Time and V_{CC} Translation Range

Family	Architecture:	V_{CCA} (V)	V_{CCB} (V)	Direction Change	Direction Change Time	Units
FXM	Auto-Hybrid	5.50	5.50	Either direction	25	ns
FXM	Auto-Hybrid	1.65	3.30	A to B → B to A	40	ns
FXM	Auto-Hybrid	3.30	1.65	A to B → B to A	80	ns
FXM	Auto-Hybrid	1.65	5.5	A to B → B to A	25	ns
FXM	Auto-Hybrid	5.50	1.65	A to B → B to A	80	ns
FXM	Auto-Hybrid	1.65	1.65	A to B → B to A	80	ns
FXL	Auto-Bus Hold	3.60	3.60	Either direction	4	ns
FXL	Auto-Bus Hold	1.20	3.60	A to B → B to A	15	ns
FXL	Auto-Bus Hold	3.60	1.20	A to B → B to A	25	ns
FXL	Auto-Bus Hold	1.20	1.20	Either direction	40	ns

SIM Card Applications

Figure 12 is a block diagram of the FXL4555 SIM card controller/translator with integrated LDO. The VSEL pin controls the card port voltage to be 1.8 V or 3 V, depending on the inserted SIM card. Per the ISO7816-3 SIM card specification, the I/O channel is bi-directional open drain, while the CLK and RST channels are uni-directional push / pull. Therefore, the FXLP4555 is designed with two uni-directional translators for CLK and RST and one hybrid auto-directional translator (with internal pull-up resistors) for the I/O channel.

Figure 13 is a block diagram of the FXLA2203 dual-host dual-SIM card translator. The FXLA2203 contains very low R_{ON} power switches for routing existing PMIC LDOs to either SIM card slot. The FXLA2203 allows simultaneous level shifted communication between any two hosts and any two SIM Card Slots. This simultaneous communication is critical for dual standby, dual-mode smart phone applications. Per the ISO7816-3 SIM card specification, the I/O channel is bi-directional open drain, while the CLK and RST channels are uni-directional push/pull. Therefore, the FXLA2203 is designed with uni-directional translation for CLK and RST and hybrid auto-direction channel translation (with internal pull-up resistors) for the I/O channel.

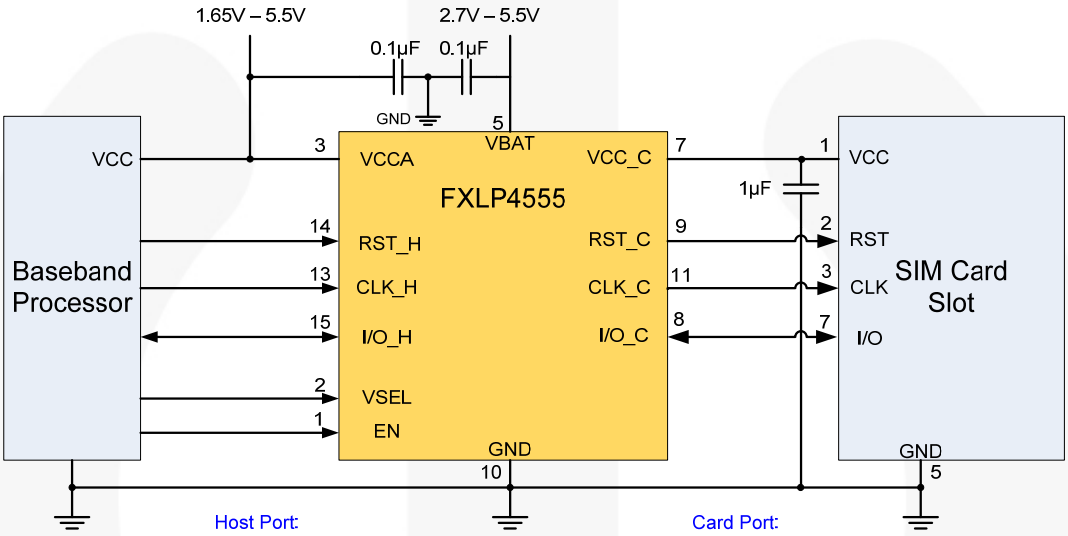

Figure 12. FXLP4555 SIM Card Controller / Translator

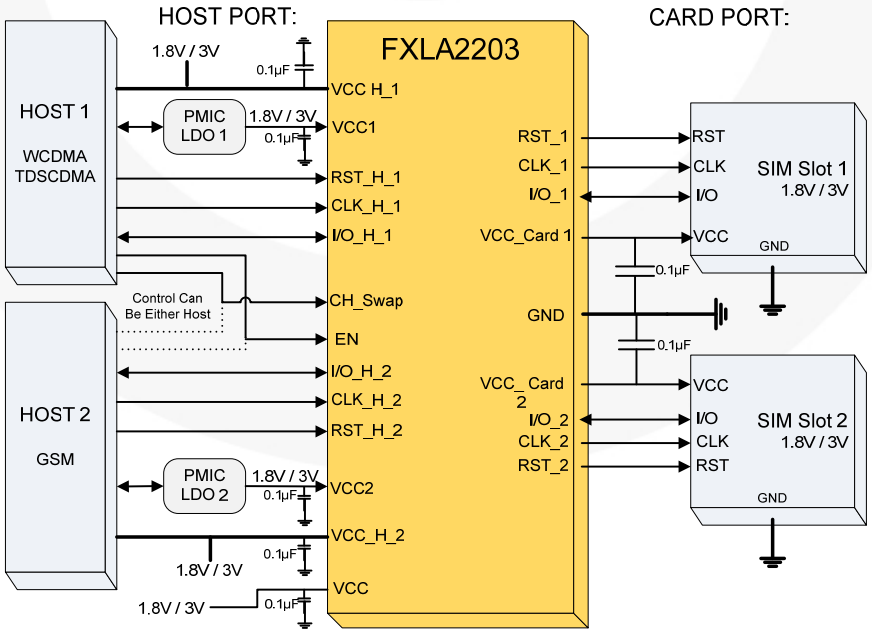

Figure 13. FXLA2203 Dual-Host Dual SIM Card Translator

Auto-Direction BUS Hold Applications

The auto-direction BUS hold architecture is applicable to push-pull applications, such as SPI. The auto-direction bus hold architecture is not recommended for open-drain environments using pull-up resistors.

SPI Application

Figure 14 is a block diagram of the FXLA104 SPI translator. SPI is a 4-bit, non-open-drain, chip-to-chip communication protocol, typically running 5 MHz – 20 MHz. In comparison to I^2C and SMUS, SPI goes much faster, but uses more pins and requires dedicated slave select (SS) pins for each slave. I^2C and SMBUS run much slower (400 KHz), but use only two pins and can daisy-chain multiple slaves as well as multiple masters.

Depending on the V_{CC} combination, the FXLA104 level shifts SPI applications (1.1 V – 3.6 V) from 20 MHz up to 70 MHz.

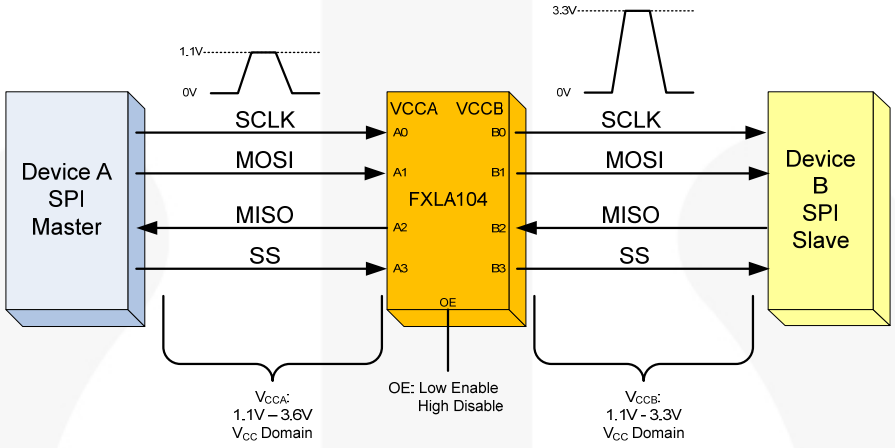

Figure 14. FXLA104 SPI Translator

Table 2. Summary of Fairchild Mobile Translator Architectures

Item	Feature	Uni-Directional	Bi-Direction Direction Pin	Auto-Direction Bus Hold	Auto-Direction Hybrid
1	Direction Pin	N/A	Yes	No	No
2	Open Drain	Yes	Yes	No	Yes
3	Push/Pull	Yes	Yes	Yes	Yes
4	Static Drive	Strong (10s mA)	Strong (10 s mA)	Weak (100 µA)	Weak (100 µA)
5	Dynamic Drive	Strong (10s mA)	Strong (10 s mA)	Strong (10 s mA)	Strong (10 s mA)
6	Direction Change Time	N/A	Fast (4 ns Typ.)	Slow (40 ns Typ.)	Slow (40 ns Typ.)

Table 3. Fairchild Mobile Translator Portfolio Listed by Architecture

Family	Part Number	Application	# of Bits / Channels	Architectures	Static Drive	Package	Pin Count	Smallest Package Dimentions (mm)	Voltage Range (V)
FX-A Auto Direction Translators	FXLA101	Mobile	1	Auto	100 µA	MicroPak™, SC70	6	1.00 x 1.45	1.1 to 3.6
	FXLA102	Mobile	2	Auto	100 µA	MicroPak	8	1.6 x 1.6	1.1 to 3.6
	FXLA104	Mobile, SPI	4	Auto	100 µA	UMLP	16	1.8 x 2.6	1.1 to 3.6
	FXLA018	Mobile	8	Auto	100 µA	DQFN	20	2.5 x 4.5	1.1 to 3.6
	FXMA108	Mobile	8	Auto	100 µA	DQFN	20	2.5 x 4.5	1.65 to 5.50
FXL Translators	FLXH1T45	Mobile	1	B	18 mA	MircoPak	6	1.0 0x 1.45	1.1 to 3.6
	FXLP34	Mobile	1	U	2.6 mA	MicroPak, SC70	6	1.00 x 1.45	0.9 to 3.6
	FXL2T245	Mobile	2	B	24 mA	MicroPak	10	1.6 x 2.1	1.1 to 3.6
	FXL2TD245	Mobile	2	B	24 mA	MicroPak	10	1.6 x 2.1	1.1 to 3.6
	FXL4T245	Mobile	4	B	24 mA	DQFN	14	2.5 x 3.0	1.1 to 3.6
	FXL4TD245	Mobile	4	B	24 mA	UMLP	16	1.8 x 2.6	1.1 to 3.6
	FXL5T244	Mobile	5	U	24 mA	DQFN	14	2.5 x 3.0	1.1 to 3.6
	FXL4245	Mobile	8	B	24 mA	MLP	24	3.5 x 4.5	1.1 to 3.6
	FXLH42245	Mobile	8	B	24 mA	MLP	24	3.5 x 4.5	1.1 to 3.6
Specialty	FXMA2102	I^2C, SMBUS	2	H	NA	MicroPak, UMLP	8	1.2 x 1.4	1.65 to 5.50
	FXLA2203	Dual SIM Card	8	H, U, PS	H, U, PS	UMLP	24	2.5 x 3.4	1.65 to 3.6
	FXLP4555	SIM Card	3	H, U, L	H, U, L	MLP	16	3.0 x 3.0	1.65 to 3.6

Table 4. Architecture Key

Auto	Auto Direction with Bus Hold
B	Bi-Directional with Direction Pin
U	Uni-Directional
H	Hybrid Auto Direction for Open-Drain
PS	Power Switch
L	LDO

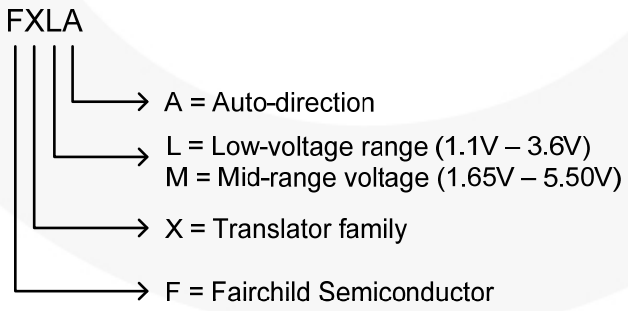

Figure 15. Nomenclature

Related Datasheets

FXLA101 – Low-Voltage Dual-Supply 1-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

FXLA102 – Low-Voltage Dual-Supply 2-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

FXLA104 – Low-Voltage Dual-Supply 4-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

FXLA018 – Low-Voltage Dual-Supply 8-Bit Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

FXMA108 – Dual-Supply, 8-Bit Signal Translator with Configurable Voltage Supplies and Signals Levels, 3-State Outputs and Auto Direction Sensing

FXLP34 –Single Bit Uni-Directional Translator

FXL2T245 – Low Voltage Dual Supply 2-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs

FXL2TD245 – Low Voltage Dual Supply 2-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs and Independent Direction Controls

FXL4T245 – Low Voltage Dual Supply 4-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs

FXL4TD245 – Low Voltage Dual Supply 4-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs and Independent Direction Controls

FXL5T244 – Low Voltage Dual Supply 5-Bit Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs

FXL4245 – Low-Voltage, Dual-Supply, 8-Bit, Signal Translator with Configurable Voltage Supplies, Signal Levels, and 3-State Outputs

FXLH42245 – Low-Voltage, Dual-Supply, 8-Bit, Signal Translator with Configurable Voltage Supplies, Bushold Data Inputs, 3-State Outputs and 26Ω Series Resistors in the B-Port Outputs

FXMA2102 – Dual Supply, 2-Bit Voltage Translator / Buffer / Repeater / Isolator for I^2C Applications

FXLA2203 – Dual-Mode, Dual-SIM-Card Level Translator

FXLP4555 – 1.8V / 3.0V SIM Card Power Supply and Level Shifter

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